24 bit, 96 kHz Stereo A/D Converter

Features

- 24-bit I^2S audio data format output
- Single power supply 3.3 V for analog and digital
- Single-ended analog input with internal anti-alias filter
- SNR: 98 dB (A-weighted)
- DR: 99 dB (A-weighted)
- THD: -91 dB
- Master/slave mode selection
- Multiple sampling frequencies (F_S): 8~96 kHz
- System clock: 128 F_S, 256 F_S, 384 F_S, 512 F_S
- Power down function
- Internal PLL
- 16-pin TSSOP package

Applications

- DVD recorders
- CD recorders
- MD players
- HDD players
- A/V receivers
- Personal Video recorders
- Musical Instrument
- Automotive audio applications

Description

The AD12250A converts stereo single-ended analog input signals into 24-bit I^2S digital audio data through on-chip anti-aliasing filter, multi-bit Σ-Δ modulator, decimation filter and high-pass filter which removes dc offsets. The AD12250A supports sampling frequencies from 8 kHz to 96 kHz and offers 128 F_S, 256 F_S, 384 F_S or 512 F_S system clock operation modes depending on sampling frequency and master/slave mode selection. The AD12250A is suitable for digital audio media applications which require high performance A/D conversion and low system cost.

Ordering Information

Product Number	Package	Packing	Comments
AD12250A-SG	16L TSSOP 4.4mm	Tube	Green
AD12250A-SG/TR	16L TSSOP 4.4mm	2.5k Tape & Reel	Green

AD12250A

- Marking Information

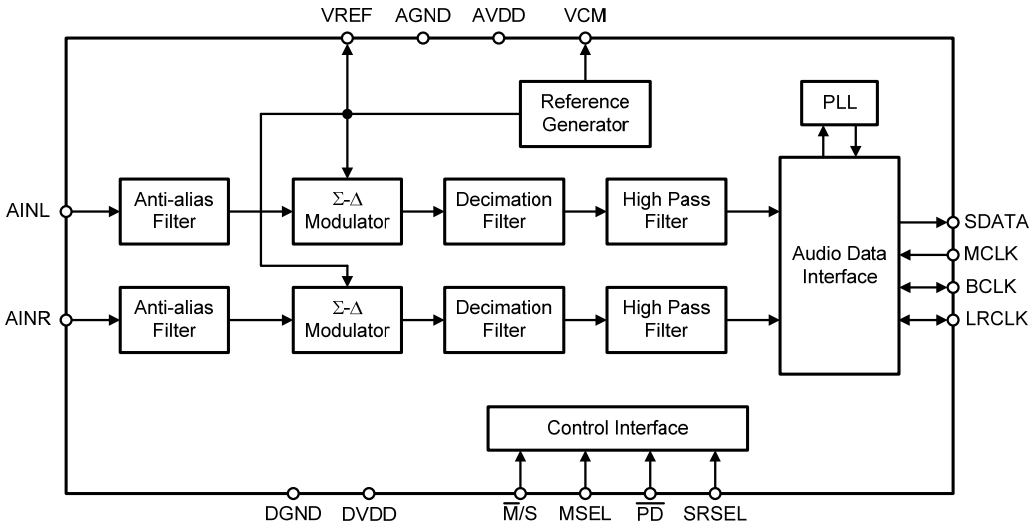
Line 1：LOGO

Line 2：Product No

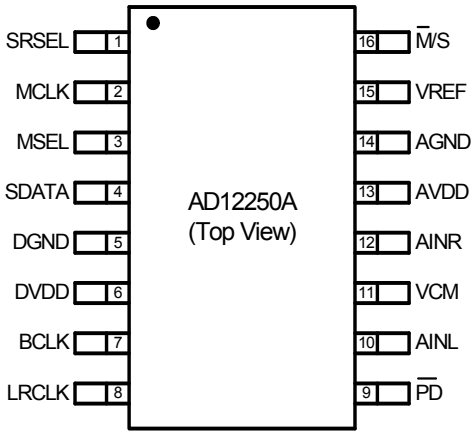
Line 3：Tracking Code

Line 4：Date Code

Functional Block Diagram



Pin Assignment



Pin Description

Pin	Name	Type	Description	Characteristics
1	SRSEL	I	48kHz/96kHz sample rate selection	Schmitt trigger input buffer
2	MCLK	I	Master clock input	Schmitt trigger input buffer
3	MSEL	I	MCLK divided-by-2 selection in master mode	Schmitt trigger input buffer
4	SDATA	O	Serial audio data output	
5	DGND	P	Digital ground	
6	DVDD	P	Digital supply	
7	BCLK	I/O	Bit clock input/output (64Fs)	Schmitt trigger input buffer
8	LRCLK	I/O	Left/Right clock input/output (Fs)	Schmitt trigger input buffer
9	$\overline{PD}$	I	Power down, low active	Schmitt trigger input buffer
10	AINL	I	Left channel analog input	
11	VCM	O	Common-mode voltage	
12	AINR	I	Right channel analog input	
13	AVDD	P	Analog supply	
14	AGND	P	Analog ground	
15	VREF	O	Positive reference voltage	
16	$\overline{M}$/S	I	Master/Slave mode selection	Schmitt trigger input buffer

Package Options

Package Type	Part Number	Thermal Information
16L TSSOP 4.4mm	AD12250A-SG	$\theta_{JA} \cong 60$ °C/W (Condition: still air)
16L TSSOP 4.4mm	AD12250A-SG/TR	$\theta_{JA} \cong 60$ °C/W (Condition: still air)

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	0	3.6	V
AVDD	Supply for Analog Circuit	0	3.6	V
	Analog Input Voltage	AGND	AVDD	V
	Digital Input Voltage	DGND	DVDD	V
T_{stg}	Storage Temperature	-65	150	°C
T_a	Ambient Operating Temperature	-40	85	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
DVDD	Supply for Digital Circuit	3.0	3.3	3.6	V
AVDD	Supply for Analog Circuit	3.0	3.3	3.6	V
T_a	Ambient Operating Temperature	0		70	°C

Digital Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	2.0			V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{OH}	High-Level Output Voltage	2.4			V
V_{OL}	Low-Level Output Voltage			0.4	V
C_I	Input Capacitance		6.4		pF

Power Supply Characteristics

● Condition: T_A = 25 °C, F_S = 48 kHz, MCLK = 256 F_S, slave mode, full-scale 1 kHz input signal

Symbol	Parameter	Condition	Min	Typ	Max	Units
AVDD	Supply for Analog Circuit		3.0	3.3	3.6	V
DVDD	Supply for Digital Circuit		3.0	3.3	3.6	V
I_A	Analog Power Supply Current	AVDD = 3.3 V		18		mA
I_D	Digital Power Supply Current	DVDD = 3.3 V		12		mA
P_C	Power Consumption	Normal Operation, AVDD, DVDD = 3.3 V		99		mW
		Power Down		<0.5		μW
PSRR	Power Supply Rejection Ratio (Note1)	1 kHz signal at AVDD		56		dB

Note1: PSRR = 56dB for 1μF capacitor on VCM pin and 36dB for 0.1μF capacitor on VCM pin.

Analog Characteristics and Specifications

● Condition: T_A = 25 °C, AVDD = DVDD = 3.3 V, F_S = 48 kHz, MCLK = 256 F_S, master mode, 1 kHz input signal, without using external reference voltage (unless otherwise stated)

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
	Full Scale Input Range				0.85·AVDD		Vpp
	Input Common Mode Voltage				1/2·AVDD		V
	Positive Reference Voltage				9/14·AVDD		V
	Input Resistance				107		kΩ
THD	Total Harmonic Distortion	F_S = 48 kHz	-1 dB		-84 (-91*)		dB
		F_S = 96 kHz	-1 dB		-84 (-91*)		dB
SNR	Signal to Noise Ratio (A-weighted)	F_S = 48 kHz	-1 dB		95 (98*)		dB
		F_S = 96 kHz	-1 dB		94 (97*)		dB
DR	Dynamic Range (A-weighted)	F_S = 48 kHz	-60 dB		98 (99*)		dB
		F_S = 96 kHz	-60 dB		97 (98*)		dB
	Channel Separation		0 dB		-90		dB
	Interchannel Gain Mismatch				0.1		dB

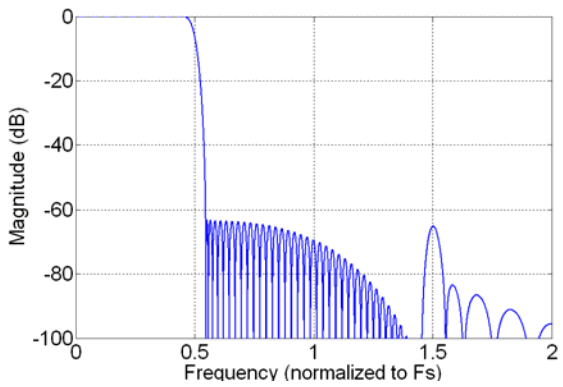
* Performance can be further improved by using clean external reference voltage as shown in circuit connection diagram.

Digital Filter Characteristics and Specifications

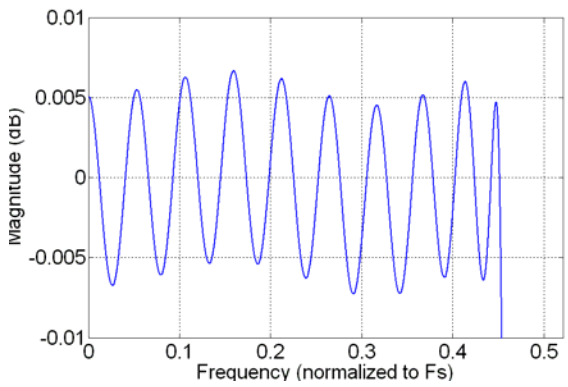
Parameter	Min	Typ	Max	Units
SRSEL = 0 (F_S = 48 kHz)				
Passband	0		0.4535	F_S
Passband Ripple			±0.008	dB
Stopband	0.5465			F_S
Stopband Attenuation	63.24			dB
Group Delay		21/F_S		s
SRSEL = 1 (F_S = 96 kHz)				
Passband	0		0.4535	F_S
Passband Ripple			±0.008	dB
Stopband	0.5465			F_S
Stopband Attenuation	63.24			dB
Group Delay		21/F_S		s
High pass filter (SRSEL = 0)				
Cutoff frequency (-3 dB)		2		Hz
High pass filter (SRSEL = 1)				
Cutoff frequency (-3 dB)		4		Hz

Digital Filter Response

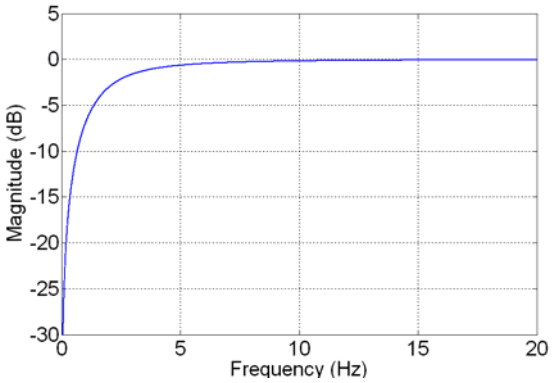
- Frequency response when SRSEL = 0 (F_S = 48 kHz)



Total frequency response

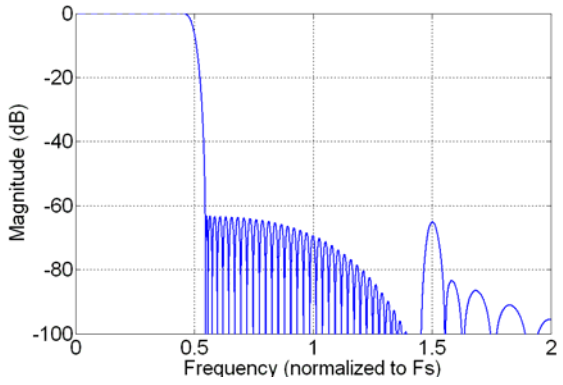


Inband ripple

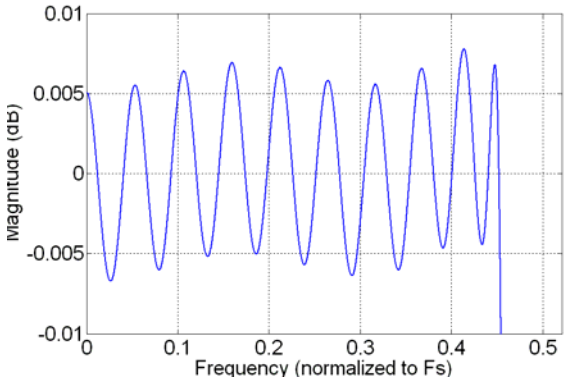


Highpass filter response (F_S = 48 kHz)

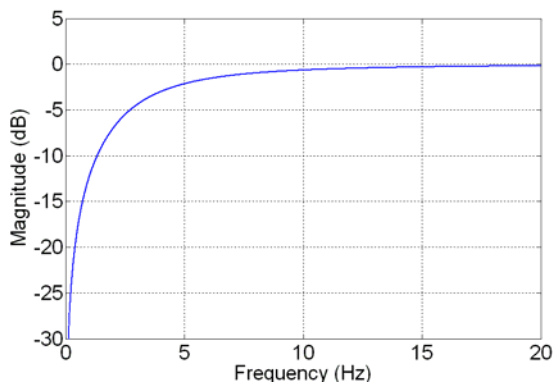
- Frequency response when SRSEL = 1 (F_S = 96 kHz)



Total frequency response



Inband ripple



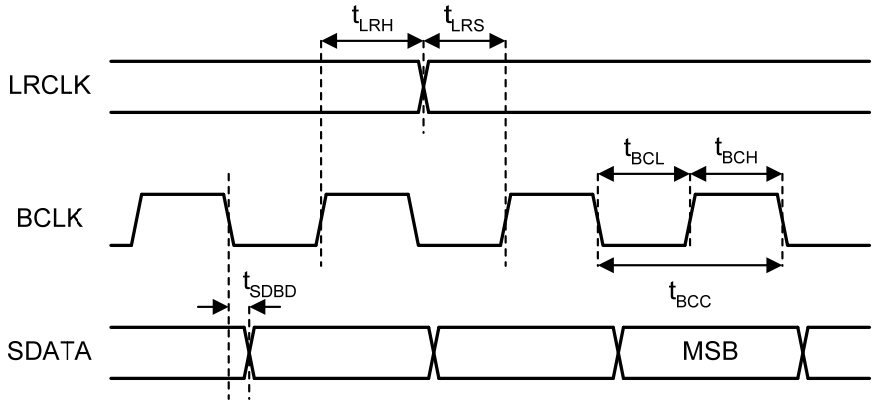
Highpass filter response (F_S = 96 kHz)

Interface Configuration

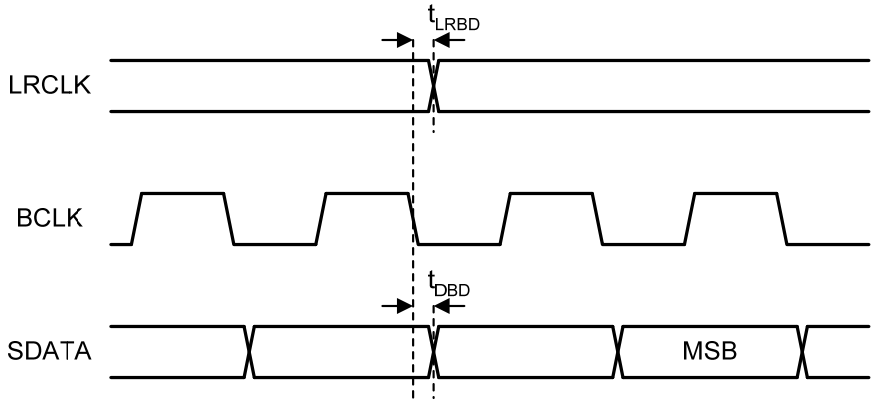
- I^2S

  AD12250A will output serial audio data in I^2S format.

  1. Slave mode



  2. Master mode

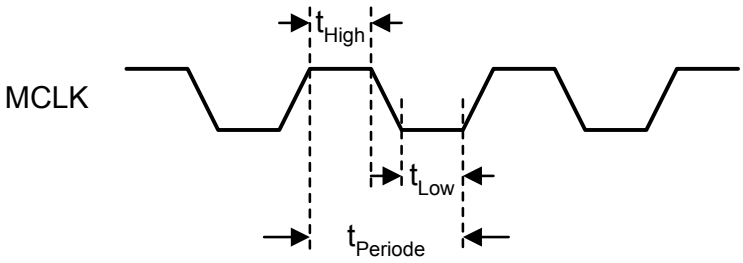


Symbol	Parameter	Min	Typ	Max	Units
Slave Mode					
t_{LRH}	LRCLK Hold Time to BCLK Rising Edge	10			ns
t_{LRS}	LRCLK Set-Up Time to BCLK Rising Edge	10			ns
t_{BCL}	BCLK Pulse Width Low	20			ns
t_{BCH}	BCLK Pulse Width High	20			ns
t_{BCC}	BCLK Period	40			ns
t_{SDBD}	SDATA Delay from BCLK Falling Edge	0		15	ns
Master Mode					
t_{LRBD}	LRCLK Delay from BCLK Falling Edge	0		10	ns
t_{DBD}	SDATA Delay from BCLK Falling Edge	0		10	ns

- System Clock Timing

AD12250A has only one central clock (MCLK) to drive the sigma delta circuit and digital filter. The following table contains supported clock frequencies. MCLK timing requirements are shown in the following figure.

LRCLK (kHz)	MCLK (MHz)			
	$128F_S$	$256F_S$	$384F_S$	$512F_S$
8	1.024	2.048	3.072	4.096
32	4.096	8.192	12.288	16.384
44.1	5.6448	11.2896	16.9340	22.5792
48	6.144	12.288	18.432	24.576
64	8.192	16.384	24.576	–
88.2	11.2896	22.5792	33.8688	–
96	12.288	24.576	36.864	–



$t_{High} \geq 13.56ns$, $t_{Low} \geq 13.56ns$ and $t_{Periode} \geq 27.13ns$

Typical MCLK duty cycle = 50%

Operation Descriptions

AD12250A uses multi-bit sigma-delta modulators and digital decimation filters to covert analog audio signal to high precision digital form.

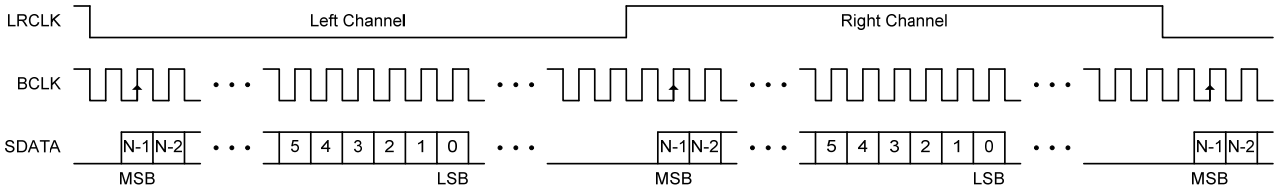
- Serial data interface

  In the master mode, AD12250A outputs data with I^2S format through 3 pins, LRCLK, BCLK and SDATA. There are 64 BCLK cycles in each LRCLK cycle. 24-bit I^2S serial data are outputted through the SDATA.

  LRCLK: Left-right clock which indicates which-channel output is currently on SDATA pin. (Bi-directional)

  BCLK: Bit sampling clock which indicates the individual serial bits on SDATA pin. (Bi-directional)

  SDATA: Serial audio data output which is 2's complement and MSB first.



  In the slave mode, both BCLK and LRCLK are input pins. AD12250A can support up to 64 BCLK clock cycles in one LRCLK clock cycle. It must be an even number of BCLK clock cycles in one LRCLK clock cycle. AD12250A will output up to 24 bits I^2S serial audio output data to SDATA pin.

- High pass filter

  AD12250A has digital high pass filters which will remove the DC component in input audio signals.

- Power down mode

  AD12250A will enter power down mode when $\overline{PD}$ pin is pulled low. In the power down mode, clock will be stopped from feeding into digital circuits and analog circuits will be turned off. After the power down mode is de-asserted, SDATA will be hold to zero in the next 400 ms (for F_S = 48 kHz & 96 kHz) then a fade-in procedure will be executed. After the fade-in procedure is finished, AD12250A will enter normal operation.

- Master mode

  When $\overline{M}$/S pin is pulled low, AD12250A will enter the master mode. LRCLK and BCLK will become output pins. BCLK frequency will be fixed at 64 F_S. SRSEL and MSEL will determine the ratio of LRCLK and MCLK frequency (see the following table). AD12250A has an internal PLL which will transfer input master clock frequency to 256 F_S for internal circuits.

LRCLK (F_S)	MCLK	
	MSEL = 1	MSEL = 0
SRSEL=0 (8kHz≦F_S≦48KHz)	256F_S	512F_S
SRSEL=1 (48kHz＜F_S≦96KHz)	128F_S	256F_S

- Slave Mode

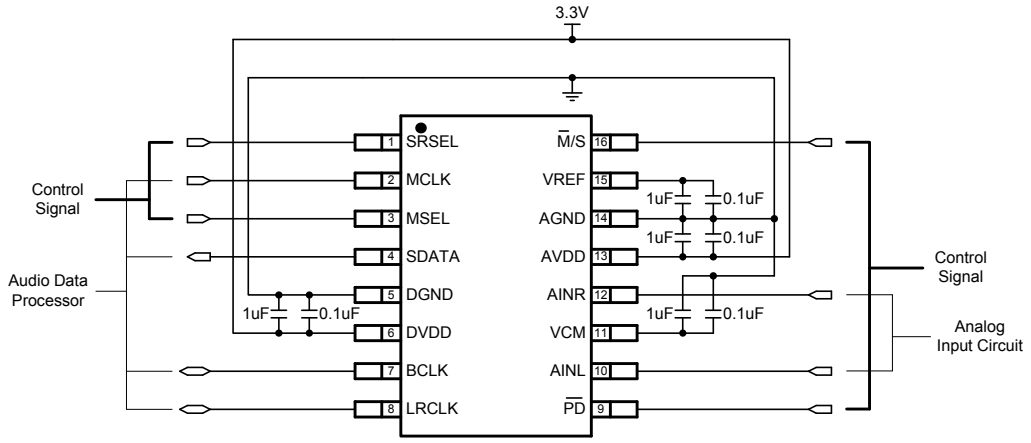
  When $\overline{M}$/S pin is pulled high, AD12250A will enter the slave mode. LRCLK and BCLK will become input pins. Supported MCLK & LRCLK ratios are listed below. AD12250A will automatically detect the cycle number of MCLK within a LRCLK period in slave mode and then transfer input master clock frequencies in the following table to 256F_S by the internal PLL. When clock error is greater than 8 MCLK cycles in the following table, AD12250A will force the output to be zero till the clock error is within 8 MCLK cycles. It is suggested to use the exact MCLK/LRCLK ratio in the following table to get maximum performance.

LRCLK (F_S)	MCLK
SRSEL=0 (8kHz≦F_S≦48KHz)	256F_S, 384F_S, 512F_S
SRSEL=1 (48kHz＜F_S≦96KHz)	128F_S, 256F_S , 384F_S

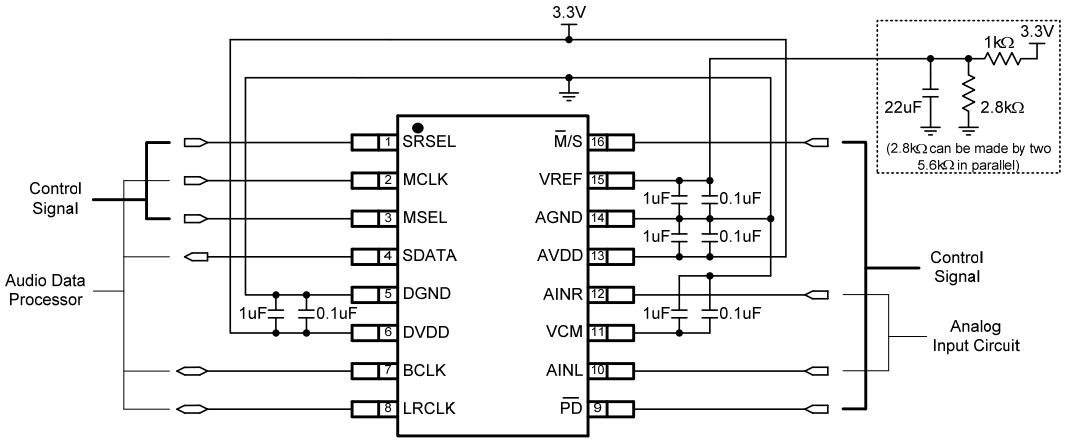
Application Circuit Example

- Circuit connection diagram

  1. Without external reference voltage



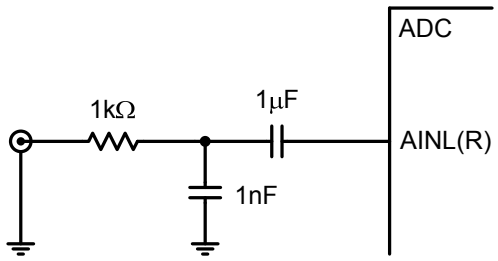
2. With external reference voltage



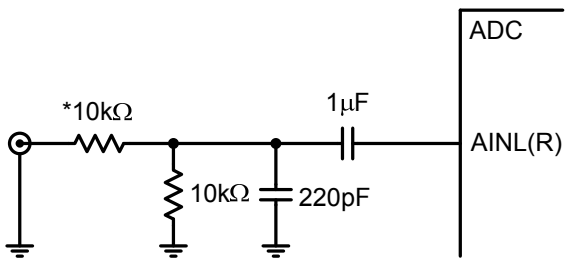
- Analog Input circuit example

  1. AINL(R) dc bias provided by ADC (Note2)

     a. Without signal attenuation (for 1 Vrms full scale input)



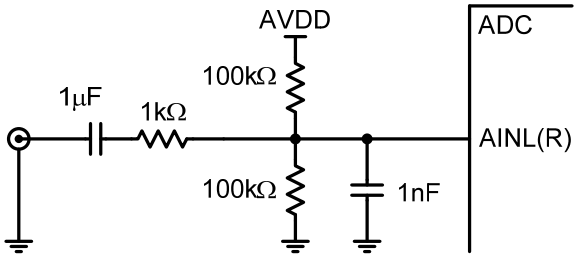
     b. With 6dB signal attenuation (for 2 Vrms full scale input)



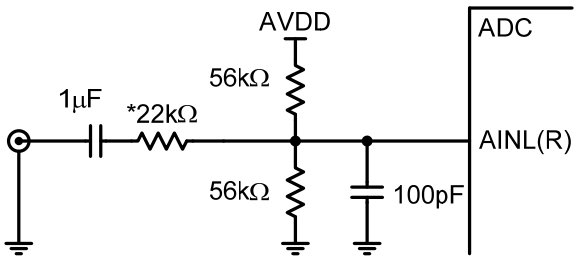
*Other gain setting can be made by adjusting this resistance (Note3)

2. AINL(R) dc bias provided by external potential divider

a. Without signal attenuation (for 1 Vrms full scale input)



b. With 6dB signal attenuation (for 2 Vrms full scale input)



*Other gain setting can be made by adjusting this resistance (Note4)

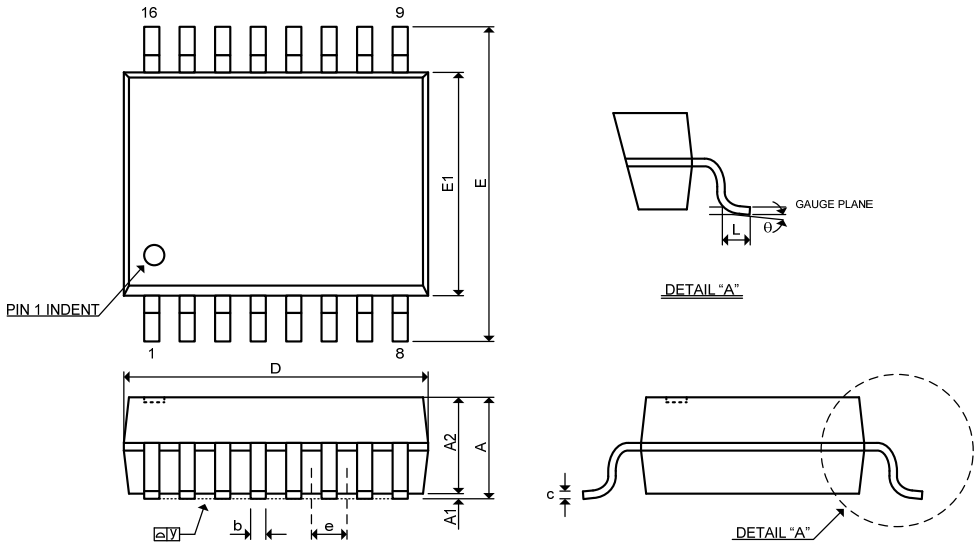
Note2: Typically, AINL(R) dc bias has about 70 mV level up shift from AVDD/2 at AVDD = 3.3 V.

Note3: If the resistance becomes $\alpha\ \Omega$, gain $\cong \frac{10k}{\alpha+10k}$ and low-pass 3-dB frequency $\cong \frac{1}{2\cdot\pi\cdot(\alpha\|10k)\cdot220p}$ Hz.

Note4: If the resistance becomes $\alpha\ \Omega$, gain $\cong \frac{22k}{\alpha+22k}$ and low-pass 3-dB frequency $\cong \frac{1}{2\cdot\pi\cdot(\alpha\|22k)\cdot100p}$ Hz.

Package Dimensions – AD12250A

- 16L TSSOP (4.4 mm) Package



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	1.20	–	–	0.0472
A1	0.00	–	0.15	0.000	–	0.0059
A2	0.80	1.00	1.05	0.0315	0.0394	0.0413
b	0.19	–	0.30	0.0075	–	0.0118
D	4.90	5.00	5.10	0.1929	0.1969	0.2008
E	6.40 BSC			0.2520 BSC		
E1	4.30	4.40	4.50	0.1693	0.1732	0.1772
e	0.65 BSC			0.0256 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
y	0.05			0.0020		
θ	0°	–	8°	0°	–	8°

Revision History

Revision	Date	Description
1.0	2005.11.03	Original
1.1	2007.04.27	Modify characteristics pin1-3、7-9、16 to Schmitt trigger TTL input buffer
1.2	2008.11.27	1. Describe in detail about the support of Fs 2. Document no. rename
1.3	2009.03.24	1. Add AD12250A-SG/TR 2. Modify ordering information Comments from Pb-free to Green 3. Add marking

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