



Anomaly Sheet for All Revisions

AD1940/AD1941

This anomaly list represents the known bugs, anomalies, and workarounds for the AD1940 and AD1941 SigmaDSP products. The anomalies listed apply to all AD1940/AD1941 packaged material branded as follows:

First Line AD1940 or AD1941

Analog Devices, Inc. is committed, through future silicon revisions, to continuously improving silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems implementing the recommended workarounds outlined here.

AD1940/AD1941 SILICON REVISION HISTORY

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
		All silicon branded AD1940YST AD1941YST	Release	Rev. 0	2

Rev. 0

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AD1940/AD1941

ANOMALIES

1. Incorrect Polarity of Serial Input Port Left-Justified Mode [er001]

Background: The input data format is set in the serial input control register.

Issue: When the AD1940/AD1941 serial input port is set to left-justified mode with left-justified formatted data being input to the part, the channels will be swapped. This means that in the SigmaDSP core the left channel data is present when LRCLK is low, and the right channel data shows on the high half of the LRCLK frame.

Workarounds:

1. The easiest solution for this problem is to simply flip the channels from the serial input block in SigmaStudio™. In this case, the serial input control register should be set up properly for left-justified mode, as described in the Data Format Configurations table in the AD1940/AD1941 data sheet. Figure 1 shows how this can be done in SigmaStudio. If SDATA_IN0 is used in left-justified mode, then SigmaStudio Input 1 is the right channel data, and SigmaStudio Input 2 is the left channel data. This is the reverse of what is expected in left-justified mode.

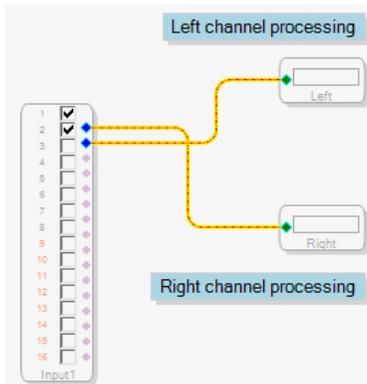


Figure 1. Swapping Channels in SigmaStudio

2. In the serial input control register (Address 2646), set Bit 4 to 1 for "Frame begins on rising edge." Normally, a left-justified frame begins on the falling edge. If this solution is used, there is a one-sample offset between the left and right channels in a frame.

Related Issues: None.

2. Data Capture Readback [er002]

Background:	Internal signals can be read back from any point in the signal flow with the data capture registers.
Issue:	A read from the data capture registers using the control port readback (Addresses 2634 to 2639) may read back portions of multiple data-words from the SigmaDSP. In most cases, this is not a problem for slowly changing signals (such as from a level detector), but may cause unexpected jumps in read data. The data capture registers are each updated at the rate of f_s (usually 44.1 kHz or 48 kHz). The control port (SPI or I ² C) reads back the data from the DSP core byte by byte. If the control port is running slower than f_s or is not synchronized with f_s , then bytes from two or three different 24-bit words may be read back as one word. The worst case of where this problem will manifest itself is when a bit transition occurs at the byte crossing. The example below shows a slowly decreasing value from subsequent data capture reads, as might be read from a level detector. First word: 00000001 01010101 01010101 Second word: 00000001 00100000 00000000 Third word: 00000001 00000010 00000000 Fourth word: 00000000 11111111 01010101 Fifth word: 00000000 11100101 01010101 Between the third and fourth words that are read, there is a bit transition between the 8 th and 9 th MSBs, which results in a significant change in level if individual bytes are taken from subsequent reads to create the complete read word. In this example, if the first byte of the third word is read back, along with the second byte of the fourth word and the third byte of the fifth word, then the resultant read word is 00000001 11111111 01010101, which has a value much higher than any of the individual words from which it was read. This example shows the worst possible error that could be encountered because of this anomaly.
Workarounds:	<ol style="list-style-type: none"> 1. In the SigmaDSP program, scale the data to be captured so it fits in a single byte. Then, when the data is read back, use only one of the three bytes. If this is done, then just the first byte can be read and the control port transaction can be ended without reading the last two bytes. 2. Before reading back from the data capture registers, disable these registers by writing an illegal program count value. This illegal count should be written after the desired data capture address has been written to the data capture register. The address portion of the data capture control register is 11 bits long. The program has a maximum length of 1535, so any address values from 1536 to 2048 (2¹¹) disables the register. The proper sequence of events is to first write an address >1535 to the data capture program count field. Second, read all three bytes from the data capture register. In this setup, it is okay to read three bytes because the data in the register is static and is not updated at the rate of f_s. These three bytes will be the last word that was saved into the data capture register before the illegal count was written. Lastly, write the correct desired program count back to the data capture registers to re-enable the data capture. Solution two takes more control port bandwidth, but is cleaner and allows all 24 bits of the data to be read.
Related Issues:	None.

AD1940/AD1941 SILICON ANOMALIES

Anomaly No.	Description	Status
er001	Incorrect Polarity of Serial Input Port Left-Justified Mode	Pending
er002	Data Capture Readback	Pending

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