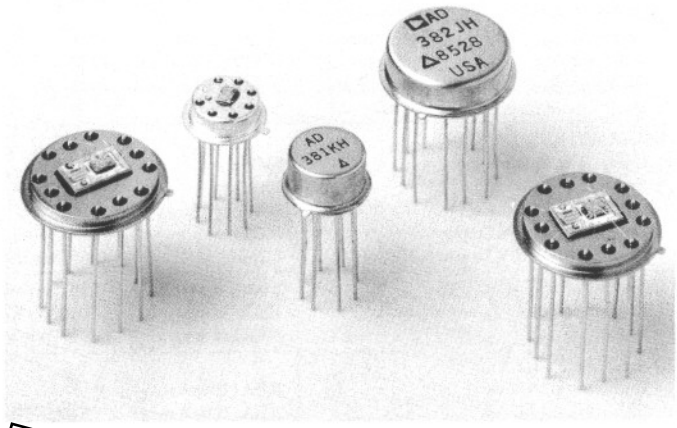
High Speed, Low Drift FET Operational Amplifier

AD381/AD382

FEATURES
- High Slew Rate 30V/μs
- Fast Settling to 0.1%: 700ns
- High Output Current: 50mA for AD382 (10mA for AD381)
- Low Drift (5μV/°C–L Grades)
- Low Offset Voltage (250μV–L Grades)
- Low Input Bias Currents
- Low Noise (2μV p-p)



PRODUCT DESCRIPTION

The AD381/AD382 are hybrid operational amplifiers combining the very low input bias current advantages of a FET input stage with high slew rate and line driving capability of a high power output stage.

The offset voltage (0.25mV maximum for the L grades) and offset voltage drift (5μV/°C maximum for the L grades) are exceptionally low for high speed operational amplifiers.

In addition to superior low drift performance, the AD381 and AD382 offer the lowest guaranteed input bias currents of any wideband FET amplifier with 100pA max for the J grades of each and 50pA max for the AD382 K, L and S grades. Since Analog Devices, unlike most other manufacturers, specifies input bias current with the amplifiers warmed-up, our FET amplifiers are specified under actual operating conditions.

The AD381 and AD382 are especially designed for use in applications, such as precision high speed data acquisition systems and signal conditioning circuits, that require excellent input parameters and a fast, high power output.

The AD381 and AD382 are offered in three commercial versions, J, K and L specified from 0 to +70°C, and one extended temperature version, the S specified from −55°C to +125°C. All grades are packaged in hermetically sealed metal cans.

PRODUCT HIGHLIGHTS

1. Laser trimming techniques reduce offset voltage drift to 5μV/°C max and reduce offset voltage to only 250μV max on the L grade versions.
2. Analog Devices FET processing provides 100pA max (20pA typical) bias currents specified after 5 minutes of warm-up.
3. Internal frequency compensation, low offset voltage, and full device protection eliminate the need for external components and adjustments. This reduces circuit size and complexity and increases reliability.
4. The fast settling output (700ns to 0.1%) makes the AD381 and AD382 ideal for D/A and A/D converter amplifier applications.
5. The AD382's high output current (50mA minimum at ±10 volts) makes it suitable for driving terminated (200Ω) twisted pair cables over the commercial temperature ranges.
6. The high slew rate (30V/μs) and high gain bandwidth product (5MHz) make the AD381 and AD382 an ideal choice for sample and holds and for high speed integrator circuits.

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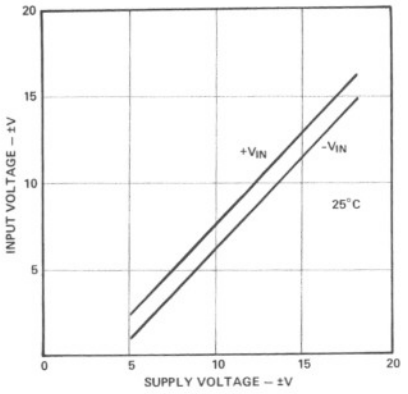


Figure 1. Input Voltage Range vs. Supply Voltage

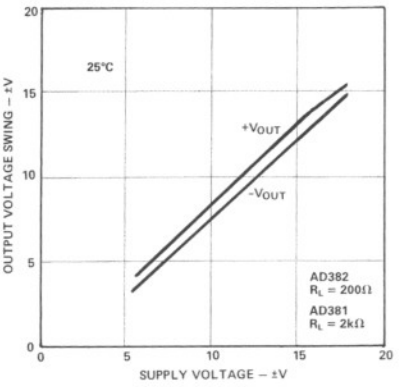


Figure 2. Output Voltage Swing vs. Supply Voltage

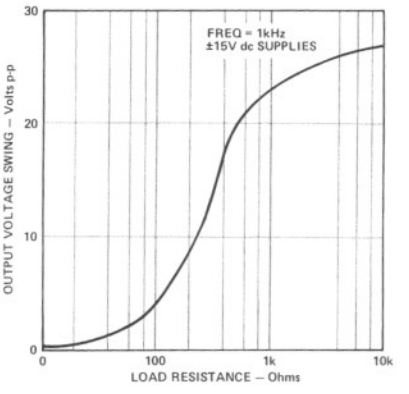


Figure 3a. Output Voltage Swing vs. Load Resistor for AD381

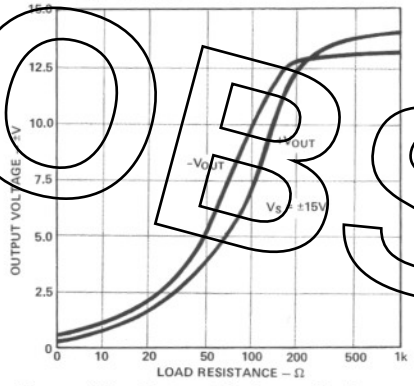


Figure 3b. Output Voltage Swing vs. Load Resistor for AD382

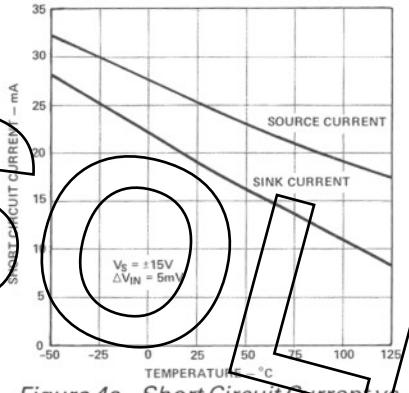


Figure 4a. Short Circuit Current vs. Temperature for AD381

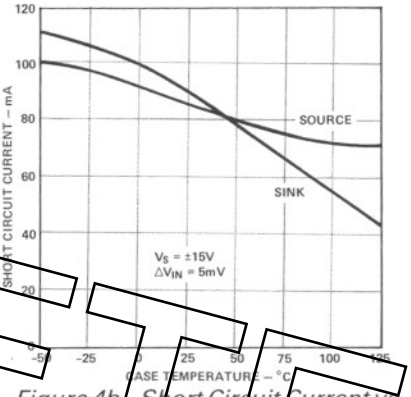


Figure 4b. Short Circuit Current vs. Temperature for AD382

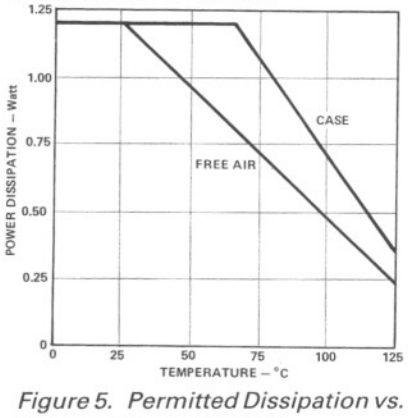


Figure 5. Permitted Dissipation vs. Temperature for AD382

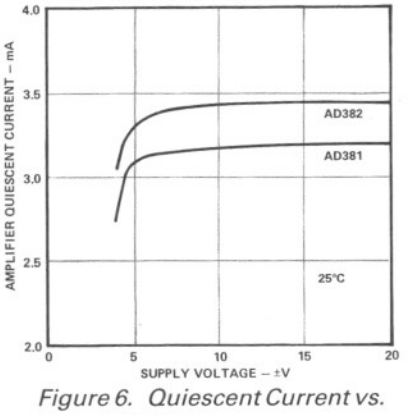


Figure 6. Quiescent Current vs. Supply Voltage

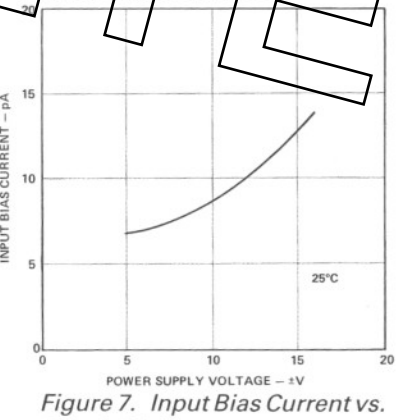


Figure 7. Input Bias Current vs. Supply Voltage

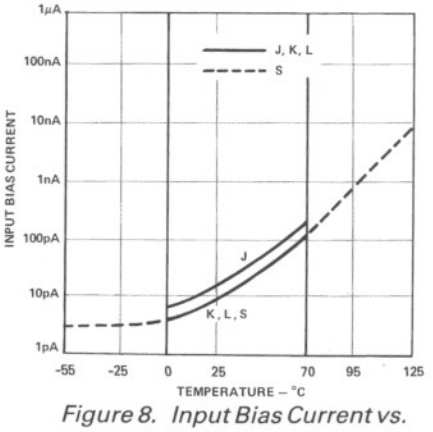


Figure 8. Input Bias Current vs. Temperature

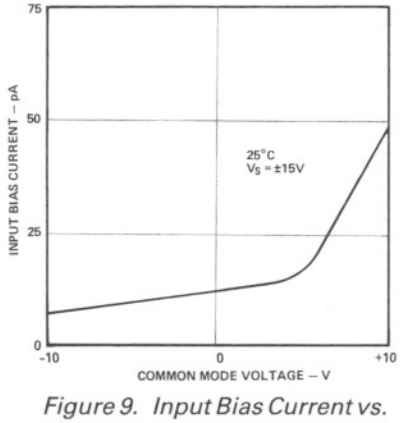


Figure 9. Input Bias Current vs. CMV

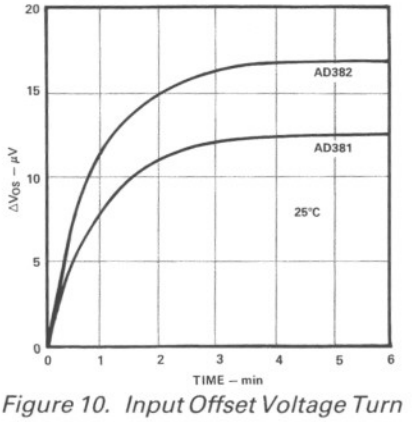


Figure 10. Input Offset Voltage Turn On Drift vs. Time

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD381JH AD382JH	AD381KH AD382KH	AD381LH AD382LH	AD381SH AD382SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$ (AD381)	60,000 min	100,000 min	**	**
V_{OUT} = ±10V, R_L = 200Ω (AD382)	25,000 min	35,000 min	**	**
R_L = 10kΩ (AD382)	100,000 min	150,000 min	**	**
OUTPUT CHARACTERISTICS (AD382)				
Voltage @ R_L = 200Ω	±12V (±10V min)	*	*	Note 1
Voltage @ R_L = 10kΩ	±13V (±12V min)	*	*	*
Short Circuit Current, Continuous	80mA	*	*	*
OUTPUT CHARACTERISTICS (AD381)				
Voltage @ R_L = 1kΩ, T_A = min to max	±12V (±10V min)	*	*	Note 2
Voltage @ R_L = 2kΩ, T_A = min to max	±12V (±10V min)	*	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±13V (±12V min)	*	*	*
Short Circuit Current, Continuous	20mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	5MHz	*	*	*
Full Power Response	500kHz	*	*	*
Slew Rate, Unity Gain	30V/μs (20V/μs min)	*	*	*
Settling Time: 10V Step to 0.1%	700ns	*	*	*
10V Step to 0.01%	1.2μs	1.2μs (2.0μs max)	**	**
INPUT OFFSET VOLTAGE	1.0mV max	0.5mV max	0.25mV max	*
vs. Temperature, T_A = min to max[3]	25μV/°C max	10μV/°C max	5μV/°C max	10μV/°C max
vs. Supply	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT[4]				
Either Input (AD381)	20pA (100pA max)	*	*	*
Either Input (AD382)	20pA (100pA max)	10pA (50pA max)	**	**
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{12}\Omega \| 7pF$	*	*	*
Common Mode	$10^{12}\Omega \| 7pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common-Mode Rejection, V_{IN} = ±10V	76dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	
Quiescent Current AD382	3.4mA (6mA max)	*	*	*
AD381	3.2mA (5mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz–10Hz	2μV p-p	*	*	*
10Hz	35nV/√Hz	*	*	*
100Hz	22nV/√Hz	*	*	*
1kHz	18nV/√Hz	*	*	*
10kHz	16nV/√Hz	*	*	*
TEMPERATURE RANGE[6]				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance – θJA (AD382)	100°C/W	*	*	*
Thermal Resistance – θJC (AD382)	70°C/W	*	*	*

NOTES

[1]The AD382SH has an output voltage of ±12V (±10V min) for a 200Ω load from T_{min} to +100°C. To +125°C the output current is 35mA.

[2]The AD381SH has an output voltage of ±12V (±10V min) for a 1kΩ load from T_{min} to +70°C. From +70°C to +125°C the output current is 7mA.

[3]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C for every mV of offset nulled.

[4]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[6]The S-grade is available in full compliance with MIL-STD-883 Rev C. Ask for the MIL-data sheet.

*Specifications same as J grade.

**Specifications same as K grade.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Initial Offset	Offset T.C.	Output	Price (100's)
AD381JH	1mV	15μV/°C	10mA	$ 8.30
AD381KH	0.5mV	10μV/°C	10mA	$10.25
AD381LH	0.25mV	5μV/°C	10mA	$12.90
AD381SH	1mV	10μV/°C	10mA	$16.25
AD382JH	1mV	15μV/°C	50mA	$19.00
AD382KH	0.5mV	10μV/°C	50mA	$23.00
AD382LH	0.25mV	5μV/°C	50mA	$30.00
AD382SH	1mV	10μV/°C	50mA	$31.00

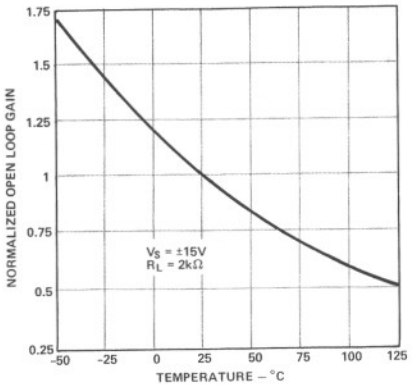


Figure 11a. Open Loop Gain vs. Temperature for AD381

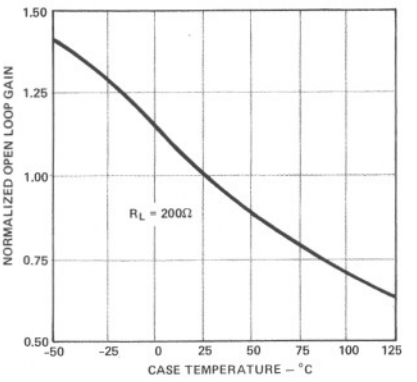


Figure 11b. Open Loop Gain vs. Temperature for AD382

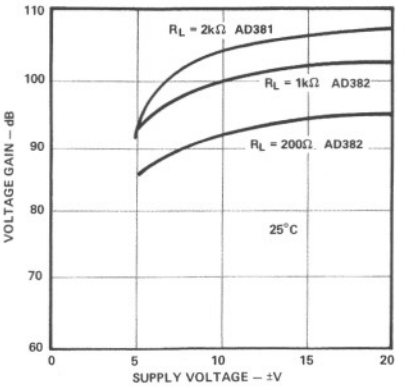


Figure 12. Open Loop Voltage Gain vs. Supply Voltage

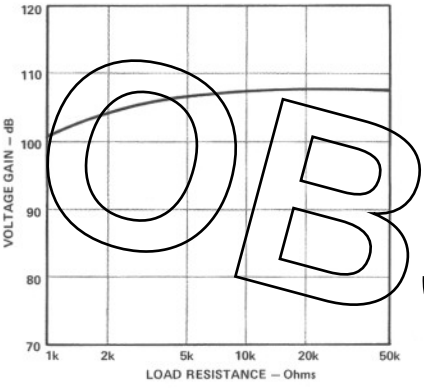


Figure 13a. Voltage Gain vs. Load Resistance for AD381

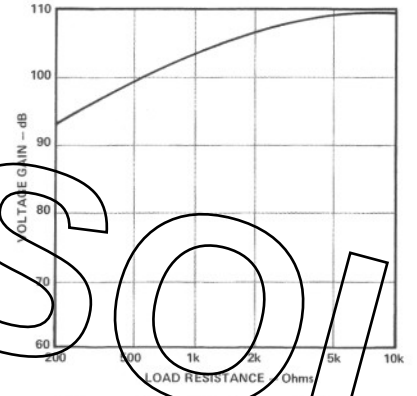


Figure 13b. Voltage Gain vs. Load Resistance for AD382

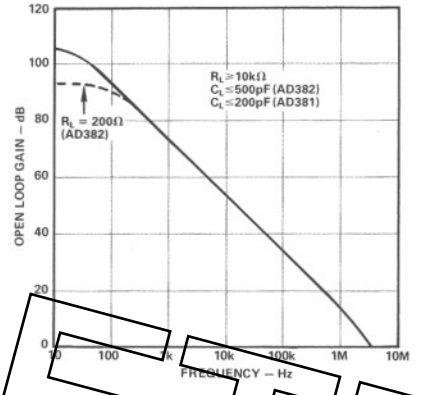


Figure 14. Open Loop Gain vs. Frequency

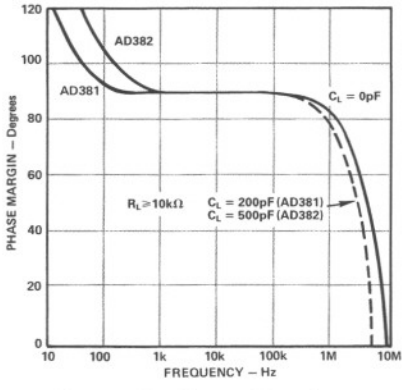


Figure 15. Phase Margin vs. Frequency

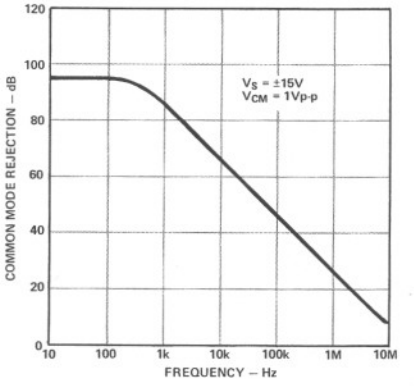


Figure 16. Common-Mode Rejection vs. Frequency

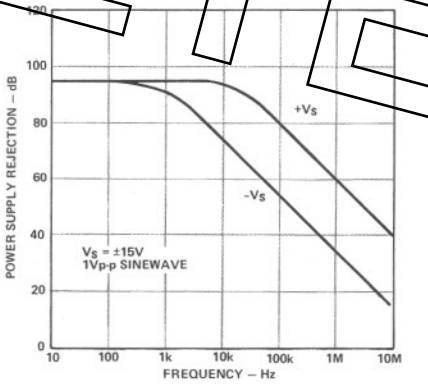


Figure 17. Power Supply Rejection vs. Frequency

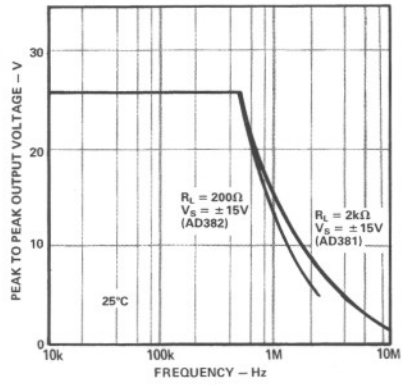


Figure 18. Large Signal Frequency Response

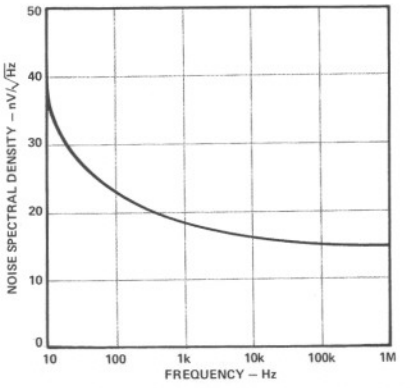


Figure 19. Noise vs. Frequency

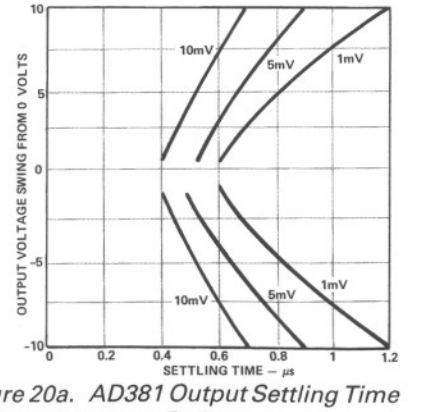


Figure 20a. AD381 Output Settling Time vs. Output Voltage Swing and Error (Circuit of Figure 22a)

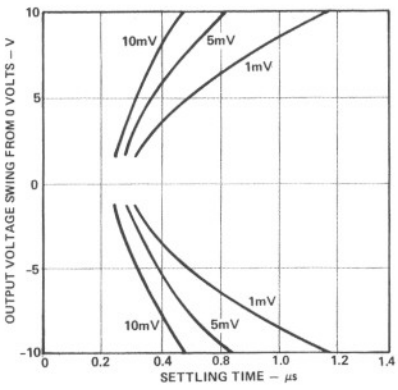


Figure 20b. AD382 Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

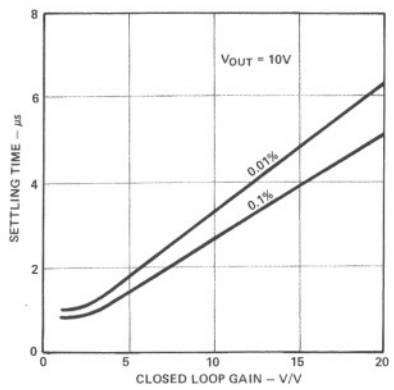


Figure 21. Settling Time vs. Closed Loop Gain (Circuits of Figures 22a & 23a)

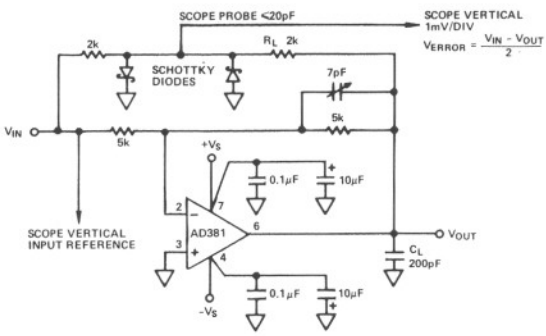


Figure 22a. AD381 Unity Gain Inverter Settling Time Test Circuit

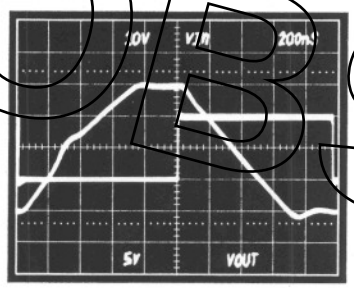


Figure 22b. AD381 Unity Gain Inverter Pulse Response (Large Signal)

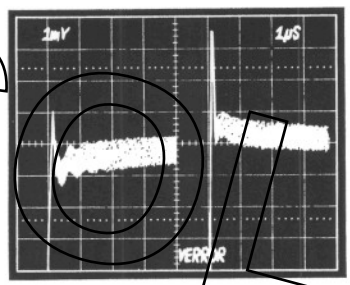


Figure 22c. AD381 Unity Gain Inverter Pulse Response (Large Signal Error Voltage)

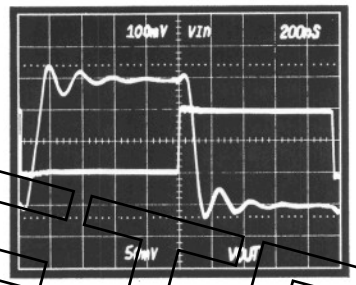


Figure 22d. AD381 Unity Gain Inverter Pulse Response (Small Signal)

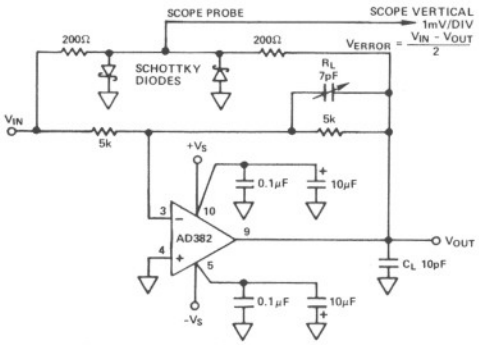


Figure 23a. AD382 Unity Gain Inverter Settling Time Test Circuit

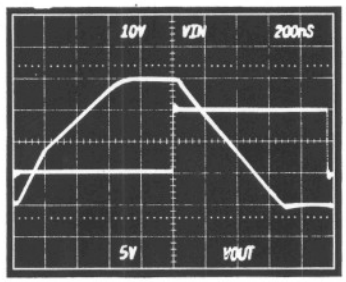


Figure 23b. AD382 Unity Gain Inverter Pulse Response (Large Signal)

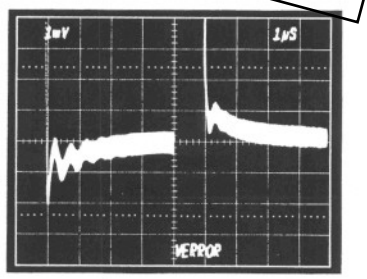


Figure 23c. AD382 Unity Gain Inverter Pulse Response (Large Signal Error Voltage)

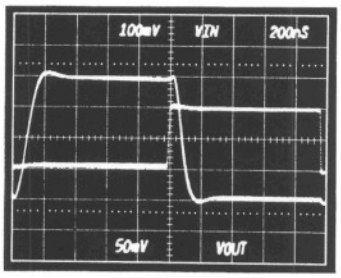


Figure 23d. AD382 Unity Gain Inverter Pulse Response (Small Signal)

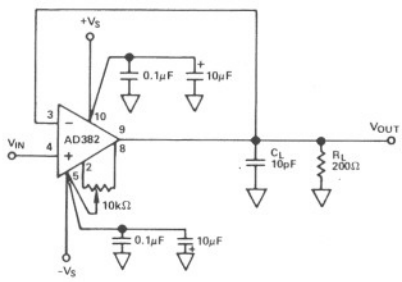


Figure 24a. AD382 Unity Gain Follower

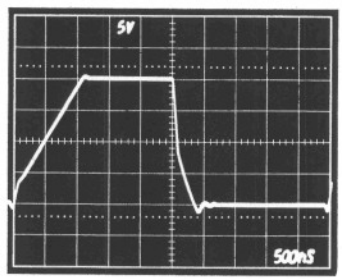


Figure 24b. AD382 Unity Gain Follower Pulse Response (Large Signal)

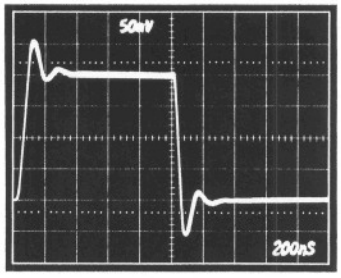


Figure 24c. AD382 Unity Gain Follower Pulse Response (Small Signal)

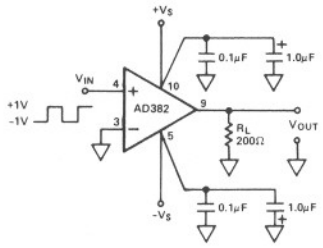


Figure 25a. AD382 Overdrive Recovery Test Circuit

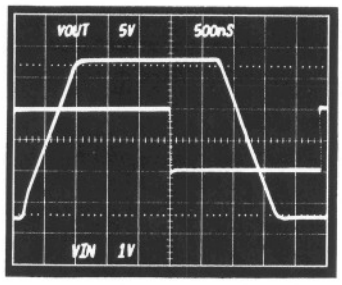


Figure 25b. AD382 Overdrive Recovery Response

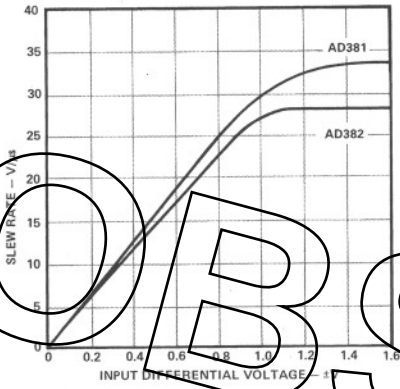


Figure 26. Slew Rate vs. Input Voltage

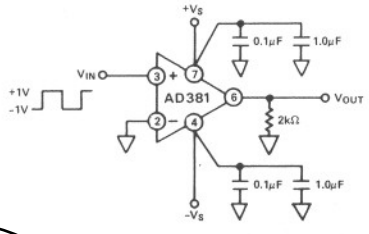


Figure 27a. AD381 Overdrive Recovery Test Circuit

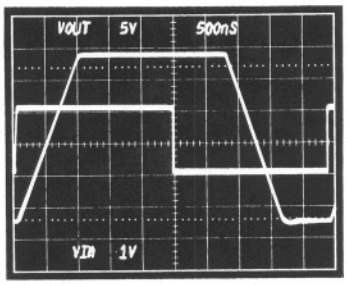


Figure 27b. AD381 Overdrive Recovery Response

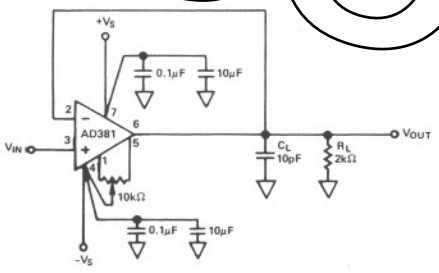


Figure 28a. AD381 Unity Gain Follower

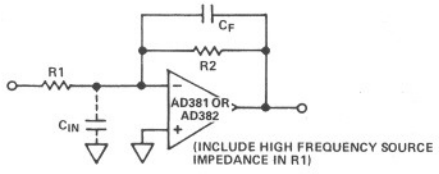
Figure 28b. AD381 Unity Gain Follower Large Signal Pulse Response

Compensation Capacitor

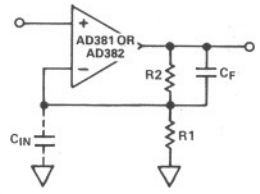
The AD381 and AD382 have sufficient phase margin to insure stability in most applications without compensation. However, in applications with capacitive load, very high speed, low gain or high resistor values ($R_{IN} \geq 5k\Omega$) the high frequency noise rejection will be improved by adding a compensation capacitor. The AD381 and AD382 have an input capacitance of 7pF. When soldered on a printed circuit board or inserted in a socket the total input capacitance could be 10pF. This input capacitance can lower the 0° phase margin crossover point from 8MHz, as shown in Figure 15, to around 1MHz.

By adding a small compensation capacitor in the feedback loop we can cancel the effects of the input capacitance and reduce high frequency noise gain. 5 to 10pF will suffice in most applications. In some current output, digital-to-analog converter applications the output capacitance of the DAC may be 200pF which would require a large compensation capacitor in the amplifier feedback loop.

A scheme for compensating inverting and noninverting circuits is shown in Figure 29. Choose $C_F = C_{IN} \frac{R1}{R2}$.



a. Inverting Amplifier



b. Noninverting Amplifier

Figure 29.

Offset Null

The AD381/AD382 should not have to be offset nulled for most applications because of its low initial offset voltage. If nulling is required for very high precision applications, such as an output amplifier for 13-bit or better digital-to-analog converters, connect a 10kΩ potentiometer between the offset null pins (pins 1 and 5 for the AD381 and pins 2 and 8 for the AD382). The wiper of the potentiometer is tied to the negative supply. With the analog input signal to the circuit grounded, adjust the potentiometer for zero output.

AD382 Heat Sinking

A heat sink for convection cooling is required if operating at full power and at ambient temperatures greater than 70°C. As shown in Figure 5 the free air power dissipation curve for the AD382 crosses the full power dissipation point (0.75W) at 70°C. The power dissipation can be improved by using a heat sink up to the case power dissipation curve (also referred to as the infinite heat sink power dissipation curve). We recommend connecting the heat sink to the AD382 case and keeping the combination ungrounded. The case of the AD382 is not connected to any pin and should be allowed to "float".

TYPICAL CIRCUITS

In many digital-to-analog converter applications, including automatic test equipment, the load may be large enough to require a buffer amplifier. The AD382 can supply ±10V into a 200Ω load. The AD381 can supply up to ±10V into a 1kΩ load.

The AD381 and AD382 are also well suited for CMOS DAC output amplifier applications due to their low initial offset voltage.

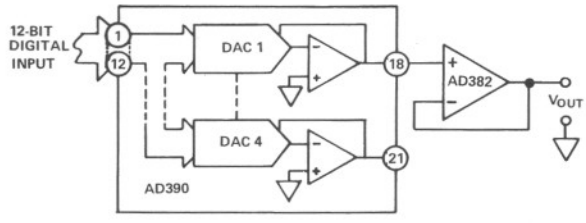


Figure 30. Buffer Amplifier to a 12-Bit Voltage Output DAC

No external trims are required with 12-bit CMOS DACs. Since the output impedance of CMOS DACs varies with input code, the output voltage could appear nonmonotonic if the offset voltage is greater than 1/2LSB. An LSB for a 12-bit DAC such as the AD7545 is 2.44mV (10 volts full scale/4096). Thus the AD381 and AD382, with only 1mV of offset maximum, assure monotonic performance without external trims.

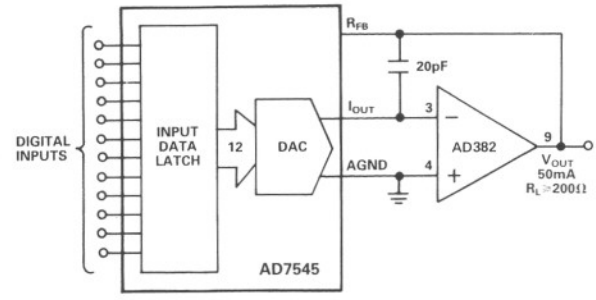


Figure 31. CMOS DAC Output Amplifier

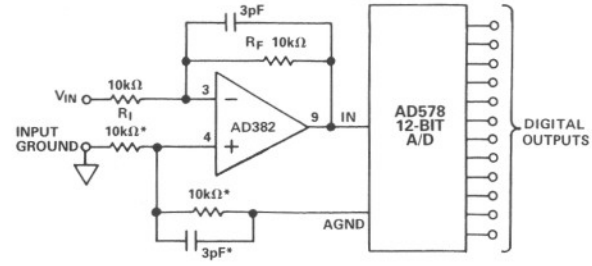


Figure 32. Fast-Settling Buffer

Many high speed A/D converters require a wideband buffer that can hold a constant output voltage under dynamically-changing load conditions that fluctuate at the bit decision rate.

Its quick recovery from load variations makes the AD382 an excellent buffer for fast successive approximation A/D converters.

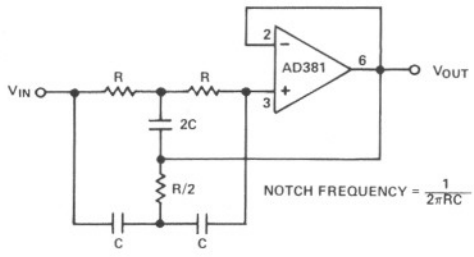


Figure 33. High Q Notch Filter

The above notch filter will have a notch of −55dB. To obtain a Q of 100 the capacitors should be well matched. Polystyrene, Teflon or NPO ceramic capacitors and metal-film resistors are recommended. For low frequency filter applications resistor values will be large. The AD381 is well suited for this application due to its low input bias current. It is also good for high frequency filtering because of its wide gain bandwidth product. This filter is capable of driving 1kΩ loads over a ±10V output range.

Figure 34 shows a fast sample and hold circuit that can acquire a sample to 0.01% in 2μs (20 volt swing). The AD381 is well suited for fast 12-bit sample/hold amplifier circuits. R1 and R2 set the circuit gain. R3 is adjusted for minimum ac feedthrough. Potentiometer R4 is set for minimum sample/hold offset voltage. R6 improves the settling time and circuit stability by adding phase margin. Bias resistors R7 and R8 insure complete shut-off of the D-MOS FET switches at TTL logic zero. Pull up resistors R9 and R10 lower the on resistance of the D-MOS switches. The SD5000 D-MOS switch is recommended for its fast transition speed and low on resistance.

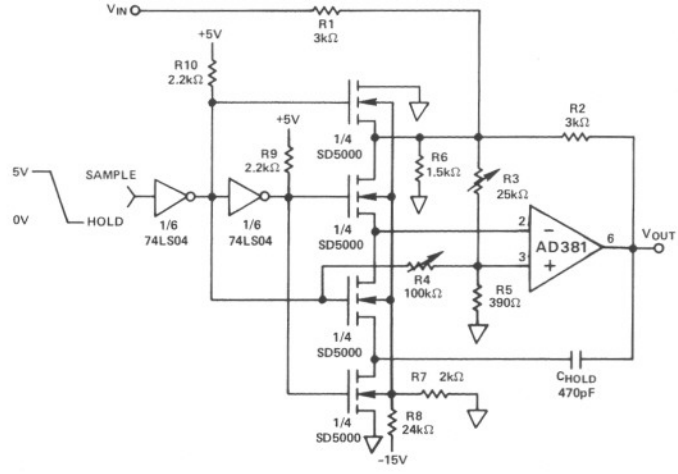
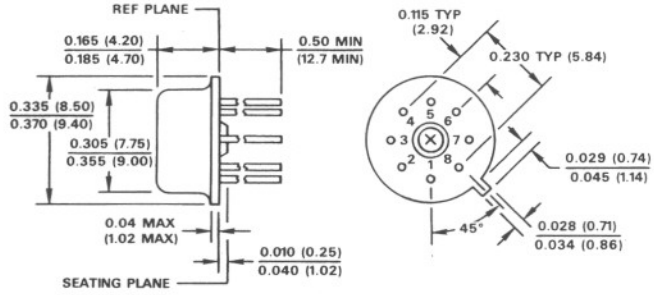


Figure 34. Fast Sample/Hold Amplifier

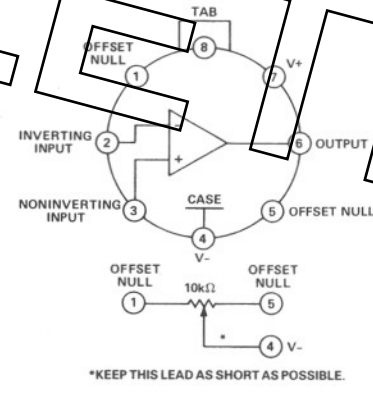
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

TO-99 PACKAGE (AD381)



AD381 PIN CONFIGURATION TOP VIEW

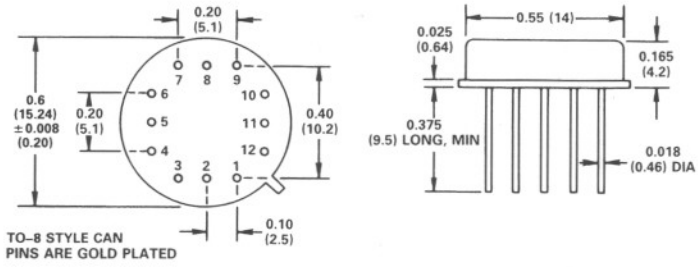


*KEEP THIS LEAD AS SHORT AS POSSIBLE.

OUTLINE DIMENSIONS

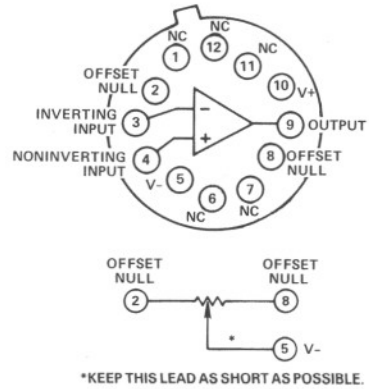
Dimensions shown in inches and (mm).

TO-8 STYLE PACKAGE (AD382)



BOTTOM VIEW

AD382 PIN CONFIGURATION TOP VIEW



*KEEP THIS LEAD AS SHORT AS POSSIBLE.

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