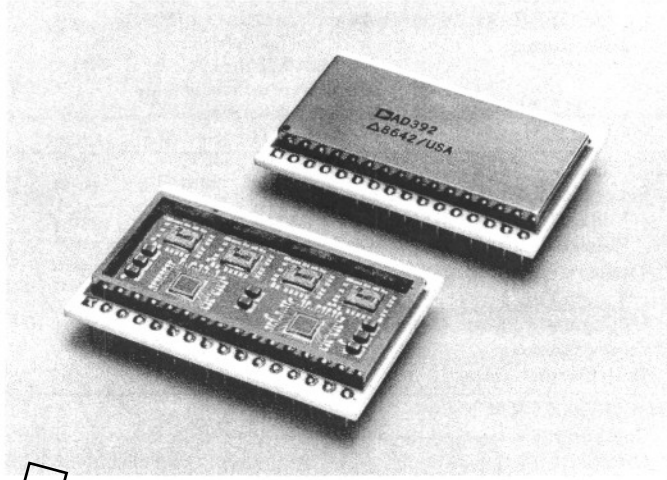
Complete Quad 12-Bit D/A Converter with Readback

AD392

FEATURES
- Data Readback Capability
- Four Complete, Voltage Output, 12-Bit DACs in One 32-Pin Hermetic Package
- Fast Bus Access: 40ns max, T_{min}-T_{max}
- Asynchronous Reset to Zero Volts
- Minimum of Two TTL Load Drive (Readback Mode)
- Double-Buffered Data Latches
- Monotonicity Guaranteed T_{min}-T_{max}
- Linearity Error ±1/2LSB
- Low Digital-to-Analog Feedthrough, 2nV sec typ
- Factory Trimmed Gain and Offset
- Low Cost



PRODUCT DESCRIPTION

The AD392 is a quad 12-bit, high-speed, voltage output digital-to-analog converter with readback in a 32-pin hermetically sealed package. The design is based on a custom IC interface to complete 12-bit DAC chips which reduces chip count and provides high reliability. The AD392 is ideal for systems requiring digital control of many analog voltages and for the monitoring of these analog voltages especially where board space is a premium. Such applications include ATE, robotics, process controllers and precision filters.

Featuring maximum access time of 40ns, the AD392 is capable of interfacing to the fastest of microprocessors. The readback capability provides a diagnostic check between the data sent from the microprocessor and the actual data received and transferred to the DAC. When $\overline{\text{RESET}}$ is low, all four DACs are simultaneously set to (bipolar) zero providing a known starting point.

The AD392 is laser-trimmed to ±1/2LSB integral linearity and ±1LSB max differential linearity at +25°C. Monotonicity is guaranteed over the full operating temperature range. The high initial accuracy and stability over temperature are made possible by the use of precision thin-film resistors.

The individual DAC registers are accessed by the address lines A0 and A1 and control lines $\overline{\text{CS}}$ and 2ND UP. These control signals permit the registers of the four DACs to be loaded sequentially and the outputs to be simultaneously updated.

The AD392 outputs are calibrated for a ±10V output range with positive true offset binary input coding.

The AD392 is packaged in a 32-lead ceramic package and is hermetically sealed. The AD392 is specified for operation over the 0 to +70°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD392 is packaged in a 32-pin DIP and is a complete solution to space constraint multiple DAC applications.
2. Readback capability provides system monitor of DAC output useful in ATE, robotics or any closed-loop system.
3. Fast bus access time of 40ns maximum allows for fast system updating compatible with high-speed microprocessing.
4. Simultaneous reset to zero volts output is extremely useful for system calibration or simply when all DAC outputs must initially start at zero volts.
5. Readback drive capability of two TTL loads virtually eliminates the need to buffer.
6. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors.
7. Monolithic DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
8. Low digital-to-analog feedthrough (2nV sec typ) is maintained to assure DAC accuracy.
9. New pin stake package provides a low-cost solution to cost constraint applications.

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SPECIFICATIONS (V_{CC} = +15V, V_{EE} = −15V, V_{DD} = +5V, T_A +25°C, unless otherwise specified)

Parameter	AD392 Min	Typ	Max	Units	Comments
DATA INPUTS (Pins 1-13, 16-18, 30-32)					
TTL Compatible					
Input Voltage					
Bit ON (Logic "1")	+2.0		$+V_{DD}$	V	V_{DD} = 5.25V
Bit OFF (Logic "0")	DGND		+0.8	V	V_{DD} = 4.75V
Input Current					
+25°C	−2		+2	μA	V_{IN} = V_{DD} or GND
T_{min} to T_{max}	−20		+20	μA	V_{IN} = V_{DD} or GND
RESOLUTION			12	Bits	
OUTPUT					
Bidirectional Outputs (Pins 2-13)					
Voltage Output Low (I_{OL} = +4.0mA)	0		+0.4	V	
Voltage Output High (I_{OH} = −4.0mA)	+2.4		V_{DD}	V	
Tristate Output Leakage					
T_{min} to T_{max}	−20		+20	μA	See Note 1
DAC Output Voltage Range		±10		V	
Current Range	−5		+5	mA	
Short Circuit Current			+40	mA	
STATIC ACCURACY					
Gain Error	−0.1	±0.05	+0.1	% of FSR	
Offset	−0.05	±0.025	+0.05	% of FSR	
Bipolar Zero		±0.025		% of FSR	
Integral Linearity Error	−0.5	±0.25	+0.5	LSB	
Differential Linearity Error	−1	±0.5	+1	LSB	
TEMPERATURE PERFORMANCE					
Gain Drift	−25	±20	+25	ppm FSR/°C	
Offset Drift	−25	±20	+25	ppm FSR/°C	
Integral Linearity Error					
T_{min} to T_{max}	−1		+1	LSB	
Differential Linearity Error	– Monotonicity Guaranteed Over Full Temperature Range –				
AC ANALOG PERFORMANCE					
Settling Time (to ± 1/2LSB)					
Change All Register Inputs					
From +5V to 0V/0V to +5V			4	μs	See Note 2
For LSB Change		1	2	μs	
Slew		10		V/μs	
Digital-to-Analog Glitch Impulse		2		nV sec	See Note 3
Crosstalk		0.1		LSB	See Note 4
POWER REQUIREMENTS					
$+V_{CC}$, $-V_{EE}$	±13.5		±16.5	V	
$+V_{DD}$	+4.5		+5.5	V	
Current (All Digital Inputs DGND or $+V_{DD}$ ONLY, No Load)					
I_{CC}		26	44	mA	
I_{EE}		62	82	mA	
I_{DD}		7.2	13	mA	
Power Dissipation		1356	1955	mW	See Note 5
POWER SUPPLY GAIN SENSITIVITY					
$+V_{CC}$, V_{DD}, $-V_{EE}$			0.002	%FS/%V_S	See Note 6
TEMPERATURE RANGE					
Operating (Full Specifications)	0		+70	°C	
Storage	−65		+150	°C	

NOTES
[1] V_{OUT} = V_{DD} or DGND.
[2] Referenced to trailing rising edge of $\overline{WR}$.
[3] Digital-to-Analog Glitch Impulse: This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. Specified as the area of the glitch in nV secs.
[4] Crosstalk is defined as the change in any one output as a result of any other output being driven from −10V to +10V into a 2kΩ load.
[5] θ_{jc} approximately 10°C/W.
[6] $+V_{CC}$, $+V_{DD}$, $-V_{EE}$ are ±10%.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_{CC}$ to AGND (Any DAC) . . . . . 0 to +18V
$-V_{EE}$ to AGND (Any DAC) . . . . . 0 to −18V
$+V_{DD}$ to DGND . . . . . −0.3V to +7V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stess rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

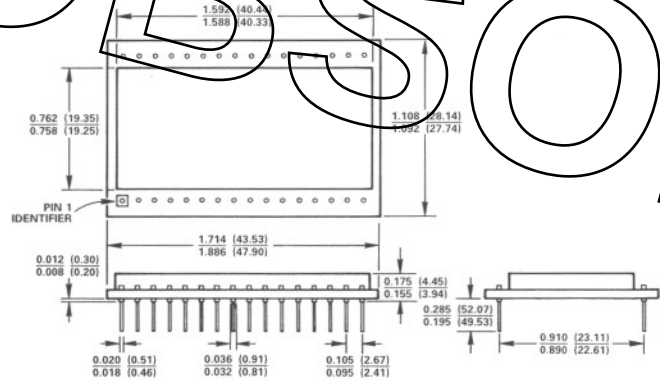
Digital Inputs to DGND
(Pins 1-13, 16-18, 30-32) . . . . . −0.3V to +7V
Analog Outputs (Pins 20, 22, 26, 28)
Short Circuit Duration . . . . . Indefinite
($+V_{CC}$, $-V_{EE}$ or AGND)
Storage Temperature . . . . . −65°C to +150°C

CAUTION:

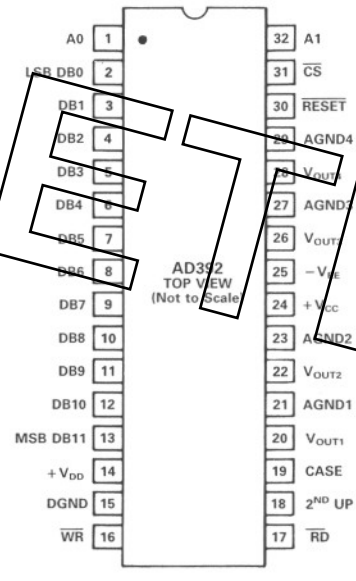
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PACKAGE OUTLINE

Dimensions shown in inches and (mm).



PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Gain Error	Linearity Error T_{min}-T_{max}	Quantity	Price
AD392JV	0 to +70°C	±4LSB	±1LSB	1-24	$151.00
				25-99	$132.00
				100+	$ 99.00

Theory of Operation

The AD392 is a quad 12-bit digital-to-analog converter with readback capability. The analog portion of the AD392 includes four bipolar process digital-to-analog converters. Each DAC contains current steering switches and a resistor ladder network which is laser-wafer trimmed for 12-bit accuracy. A precision output amplifier for voltage out operation and an internal highly stable voltage reference are all integrated on a single chip. The DAC is fixed to run in bipolar, 20V span analog output mode as shown in Table I.

Data Input			Analog Output	Analog Output Voltage	
1111	1111	1111	$+1 \cdot (V_{REFIN}) \left\{\frac{2047}{2048}\right\}$	+9.9951V	+Full Scale − 1LSB
1100	0000	0000	$+1 \cdot (V_{REFIN}) \left\{\frac{1024}{2048}\right\}$	+5.000V	+1/2 Scale
1000	0000	0001	$+1 \cdot (V_{REFIN}) \left\{\frac{1}{2048}\right\}$	+4.88mV	+1LSB
1000	0000	0000	$+1 \cdot (V_{REFIN}) \left\{\frac{0}{2048}\right\}$	+0.000V	Zero
0111	1111	1111	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{2048}\right\}$	−4.88mV	−1LSB
0100	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{1024}{2048}\right\}$	−5.000V	−1/2 Scale
0000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{2048}{2048}\right\}$	−10.000V	−Full Scale

Table I. AD392 Bipolar Code Table.

The digital portion of the AD392 includes the readback function, control logic and registers all integrated on a custom IC. Data can be latched into any one of the first rank registers by selecting the correct combination of address lines (A0 and A1) and $\overline{CS}$. The second rank registers are controlled by the 2ND UP control line. Use of the 2ND UP line enables the DACs to be updated simultaneously. The digital word can be readback from the second rank registers by asserting the correct address lines, 2ND UP and $\overline{RD}$ command. The $\overline{RD}$ and $\overline{WR}$ commands control the bidirectional I/O port. The AD392 features a $\overline{RESET}$ command for simultaneous update of all DACs to 0 volts out. This is useful for easy system calibration.

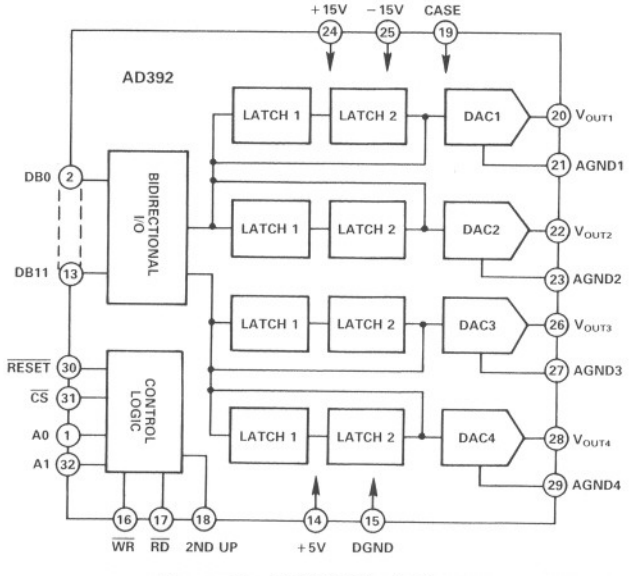


Figure 1. AD392 Block Diagram

DATA AND CONTROL SIGNAL FORMAT

The double buffered registers of the AD392 are addressed by the $\overline{CS}$, A1 and A0 lines. Each rank of registers is 12 bits wide and is presented in a straight offset binary notation. The first rank of registers are loaded sequentially, with valid $\overline{CS}$, A1, A0 on the trailing rising edge of $\overline{WR}$. The second rank of registers, on the other hand, are loaded simultaneously with the data which is in their corresponding first rank registers, with a valid $\overline{CS}$ and positive pulse of the 2ND UP command. (Note: All second rank registers can be made transparent by tieing the 2ND UP line to a Logic "1".) The data loaded into the second rank registers represents the actual digital code which is on the input of the individual DACs. This data can be read back through the data port, with valid $\overline{CS}$, A1 and A0, by taking the $\overline{RD}$ line to a Logic "0". The AD392 also features an asyncronous reset to zero volts for all four DACs by applying a negative pulse to the $\overline{RESET}$ line. Executing a reset replaces the contents of both ranks of registers with the bipolar zero code (MSB equals Logic "1", all other bits equal Logic "0".)

$\overline{CS}$	A1	A0	$\overline{WR}$	$\overline{RD}$	$\overline{RESET}$	2ND Up	Output
1	X	X	X	X	1	X	Chip Read/Write Disable
X	X	X	X	X	0	X	MSBs Go to 1, All Others Go to 0
0	X	X	X	X	1	1	All 2ND Rank Latches Transparent
0	X	X	X	X	1	0	All 2ND Rank Latches Latched
0	0	0	1	0	1	X	Read Back DAC1 2ND Rank
0	0	0	↓	1	1	X	Write to 1ST Rank DAC1
0	0	1	1	0	1	X	Read Back DAC2 2ND Rank
0	0	1	↓	1	1	X	Write to 1ST Rank DAC2
0	1	0	1	0	1	X	Read Back DAC3 2ND Rank
0	1	0	↓	1	1	X	Write to 1ST Rank DAC3
0	1	1	1	0	1	X	Read Back DAC4 2ND Rank
0	1	1	↓	1	1	X	Write to 1ST Rank DAC4

Symbols: X = Don't Care
1 = Logic High
0 = Logic Low
↓ = Positive Trailing Edge Triggered

Table II. AD392 Truth Table

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TIMING

The timing diagrams (Figures 2 and 3) illustrate the precise relationship between control signals, address signals and the data. The address lines ($\overline{CS}$, A1, A0) as well as the data (D0-D11) must be valid a minimum of 15ns before a $\overline{WR}$ is executed, and the data must remain valid a minimum of 15ns after the $\overline{WR}$ has been executed. Minimum pulse width for the $\overline{WR}$, 2ND UP and $\overline{RESET}$ commands is 15ns. Similarly, the address lines ($\overline{CS}$, A1, A0) must be valid a minimum of 15ns before a $\overline{RD}$ is executed. Data will be valid a maximum of 40ns after $\overline{RD}$ goes low. (Note: This is a MAXIMUM and, therefore, data should be off the bus just before $\overline{RD}$ goes low to avoid bus contention problems, i.e., damage to the device, data bus oscillations which may result in latching erroneous data in the registers.) Data will be off the bus a maximum of 30ns after $\overline{RD}$ goes high. (Note: This is a MAXIMUM and, therefore, the data read should be completed just before $\overline{RD}$ goes high to avoid reading erroneous data.) DAC settling time is measured from the trailing rising edge of the $\overline{WR}$ signal.

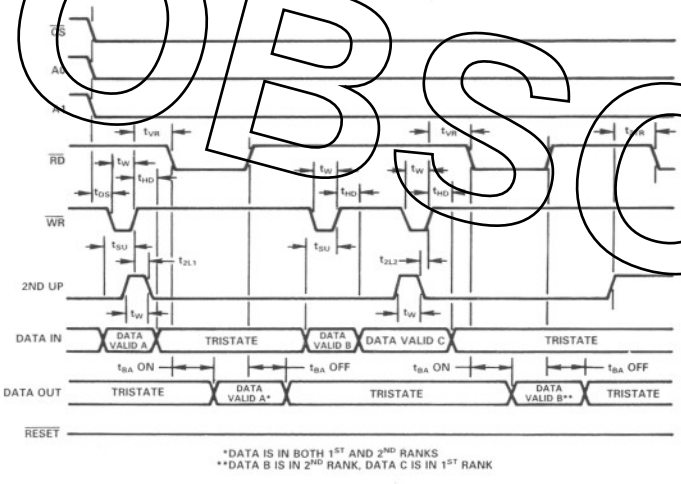

Figure 2. AD392 Write/Read Cycle Timing Diagram

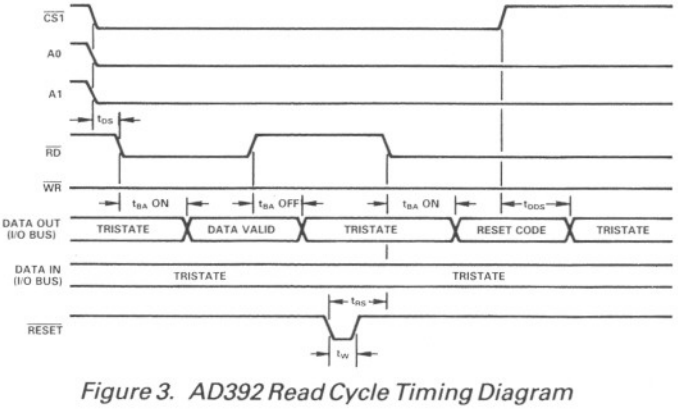

Figure 3. AD392 Read Cycle Timing Diagram

Symbol	Parameter	Min	Max	Unit
t_{DS}	Device Select	15		ns
t_W	Write/Update/Reset Pulse Width	15		ns
t_{SU}	Data Setup Time	15		ns
t_{HD}	Data Hold Time	15		ns
t_{RS}	Reset Valid for Read		35	ns
t_{VR}	Read Valid After Write	30		ns
t_{DDS}	Device De-Select (from Read Data to Tristate		40	ns
t_{BA} On	Bus Access On Time		40	ns
t_{BA} Off	Bus Access Off Time		30	ns
t_{2L1}	Minimum Latch Delay after Write/	10		ns
t_{2L2}	Minimum Latch Delay after Next Write/	5		ns
t_{2TR}	2ND Rank Transparent for Valid Read	25		ns
t_{2TD}	2ND Rank Transparent to DAC Port Outputs		40	ns
t_R,, t_F	Data Rise, Fall Times	0	5	ns

NOTES
Timing between pulses measured at 50% points.

Bus access on time measured from 50% point of read going low to active high (2.4) or active low (0.4) (see Figures 4 and 5).

Bus access off time measured from 50% point of read going high to point at which voltage trails away from active high or low under standard tristate load conditions (see Figure 6).

Table III. AC Charactertics: V_{DD} = 5.0V ± 10%; $0 \le T_A \le +70°C$; $V_{IN} = V_{DD}$ or DGND

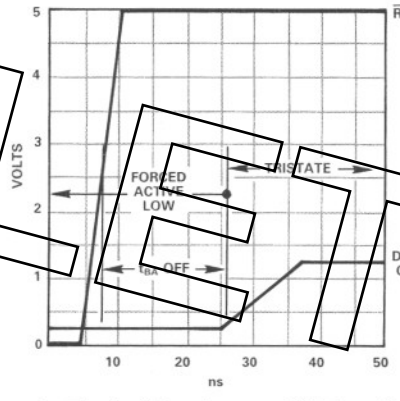

Figure 4. Typical Bus Access Off Time (t_{BA} Off)

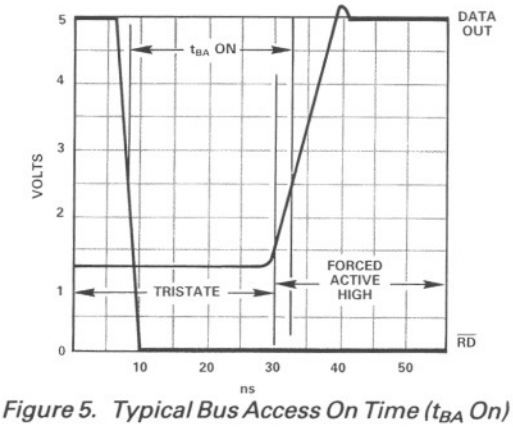

Figure 5. Typical Bus Access On Time (t_{BA} On)

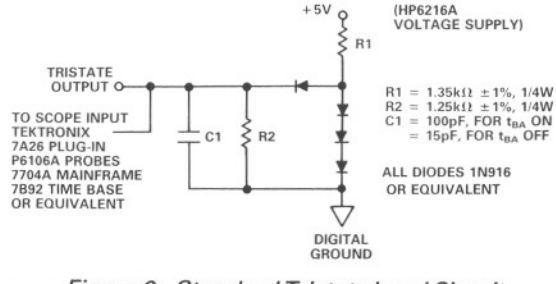

Figure 6. Standard Tristate Load Circuit

SETTLING TIME

The output amplifiers used in the AD392 are capable of supplying a ±10 volt swing into a resistive load of 2kΩ or greater. The settling characteristics of the output amplifier is shown in Figure 7. The test setup used to determine settling time is shown in Figure 8.

POWER SUPPLY DECOUPLING

The power supplies used with the AD392 should be well filtered and regulated. Internally the $+V_{CC}$ and $-V_{EE}$ supplies are independently decoupled about each DAC with 0.039μF chip capacitors to their corresponding AGND. Therefore, if the grounding scheme of Figure 9 is used, it should be sufficient to place a 4.7μF tantalum electrolytic capacitor across the $+V_{CC}$ and $-V_{EE}$ supplies. Decoupling the $+V_{DD}$ supply to DGND should be done in the same manner, however, using a parallel combination of 0.047μF ceramic and a 4.7μF tantalum electrolytic capacitor.

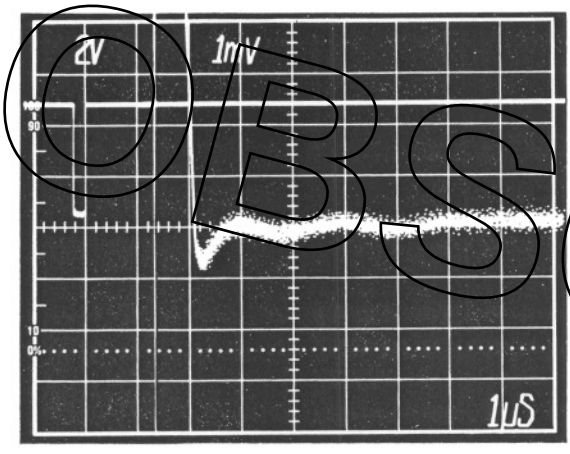

Figure 7. AD392 V_O Settling 20V Step

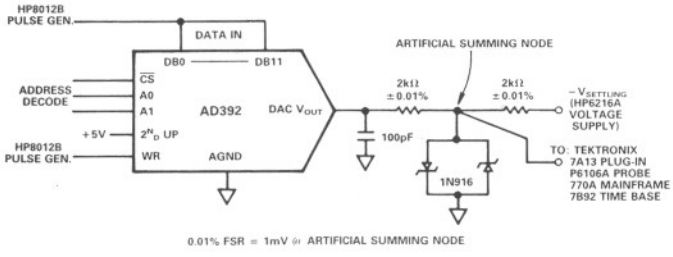

Figure 8. AD392 V_O Settling Time Circuit

GROUNDING RULES

The AD392 has been designed with four independent DAC analog grounds and a separate digital ground return pin. The analog ground pins are not only the reference points for the individual voltage outputs, they also serve as the return path for the switched DAC bit input currents. These rapidly switching currents may be as large as several milliamps for each DAC and, therefore, should be returned to a low impedance node to avoid code dependent linearity errors, digital-to-analog feed-through and crosstalk between DAC outputs. It is recommended that all four DAC analog grounds and the digital ground be tied together at the package for optimal performance. $+V_{CC}$ and $-V_{EE}$ grounds can be tied together back at the system supply and brought up to the AD392 together, whereas the $+V_{DD}$ ground is tied to the other grounds at the package and not back at the system supply. This configuration is recommended because the DAC bit input currents are sourced from the $+V_{DD}$ supply and should return by the shortest possible path and not down the analog return (see Figure 9 for details.).

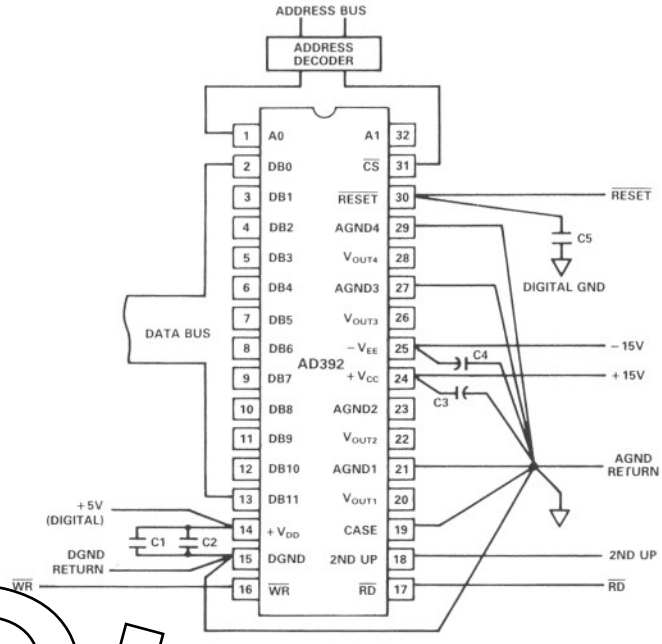

Figure 9. AD392 Recommended Circuit Schematic

CIRCUIT DETAILS

The following two suggestions are intended to aid the user in the normal operation of the AD392:

1. *Bus Termination*: The bidirectional tristateable port of the AD392 (as well as the digital inputs) should not be allowed to "float". These functions are provided by a custom CMOS integrated circuit having an input control circuit which is essentially the common gate contact of a pair of P and N channel MOS devices connected in series between the $+V_{DD}$ and DGND supply lines. An unterminated bus allows the gate potential to float to a point where both channels are partially "on" creating an ohmic path across the supply. Therefore, to avoid excessive supply current drain and possible reflections of the digital signal the bus should be terminated in its characteristic impedance to DGND.
2. *Digital Signal Integrity and the $\overline{RESET}$ line*: The AD392 has been designed to respond to extremely fast data rates and as a result must operate with a "clean" bus to ensure that valid data is being transmitted (i.e., transients on the bus that cross thresholds with sufficient duration, 5ns-10ns, may cause data to become invalid just before a $\overline{WR}$ command). If the $\overline{RESET}$ line is not connected to this "clean" bus (i.e., connected to some sort of power on reset circuitry), then it is recommended that this line be decoupled with a minimum of 1000pf capacitor to avoid an unwanted asynchronous zero volt reset on all four DACs. If this signal is not used, it should be tied to $+V_{DD}$ at the package.

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