INTERSIL

AD503
High Accuracy
Low Offset Op Amp

FEATURES

- **Low I_{BIAS}: 15pA MAX**
- **Low Drift: 25μV°C MAX**

GENERAL DESCRIPTION

The AD503 is an IC FET input op amp which provides the user with input currents of a few pA, high overall performance, low cost, and accurately specified, predictable operation. The device achieves maximum bias currents as low as 5pA, minimum gain of 75,000, CMRR of 80dB, and a minimum slew rate of 3V/μs. It is free from latch-up and is short circuit protected, and no external compensation is required, as the internal 6dB/octave rolloff provides stability in closed loop applications.

The AD503 is suggested for all general purpose FET input amplifier requirements where low cost is of prime importance.

The circuits are supplied in the TO-99 package; the AD503J, K are specified for 0 to +70°C temperature range operation; the AD503S for operation from -55°C to +125°C.

It provides performance comparable to modular FET op amps, but because of its monolithic construction, however, its cost is significantly below that of modules, and becomes even lower in large quantities.

The AD503 is especially designed for applications involving the measurement of low level currents or small voltages from high impedance sources, in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations, the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the noninverting "buffer" connection is used). The AD503, therefore, is of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

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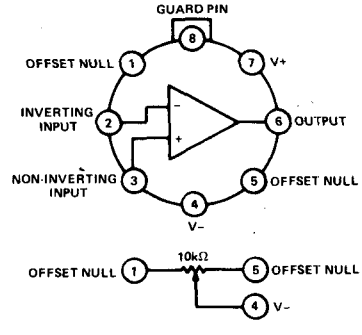
ORDERING INFORMATION

AD503 J H

- H — Package: H — TO-99 metal can
- Electrical option: See Specification Table, next page.
- Basic Part number

PIN CONFIGURATION



(outline dwg TO-99)

SPECIFICATIONS (Typical @ +25°C and ±15Vdc, unless otherwise noted)

PARAMETER	AD503J	AD503K	AD503S
OPEN LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000 min (50,000 typ)	50,000 min (120,000 typ)	**
T_A = min to max	15,000 min	40,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Load Capacitance[2]	750pF	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	3.0V/μs min (6.0V/μs typ)	*	*
Settling Time, Unity Gain (to 0.1%)	10μs	*	*
INPUT OFSET VOLTAGE[3]	50mV max (20mV typ)	20mV max (8mV typ)	**
vs Temperature, T_A = min to max	75μV/°C max (30μV/°C typ)	25μV/°C max (10μV/°C typ)	50μV°C max (20μV/°C typ)
vs Supply, T_A = min to max	400μV/V max (200μV/V typ)	200μV/V max (100μV/V typ)	**
INPUT BIAS CURRENT			
Either Input[4]	15pA max (5pA typ)	10pA max (2.5pA typ)	**
INPUT IMPEDANCE			
Differential	10^{11} Ω||2pF	*	*
Common Mode	10^{12} Ω||2pF	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	15μV (p-p)	*	*
5Hz to 50kHz	5.0μV (rms)	*	*
f = 1kHz (spot noise)	30.0nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±3.0V	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{IN} = ±10V	70dB min (90dB typ)	80dB min (90dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	±(5 to 22)V
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

Note 1. Open Loop Gain is specified with V_{OS} both nulled and unnulled.

Note 2. A conservative design would not exceed 500pF of load capacitance.

Note 3. Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

Note 4. Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

Note 5. See comments in Input Considerations section.

*Specifications same as for AD503J.
**Specifications same as for AD503K.
Specifications subject to change without notice.

APPLICATIONS CONSIDERATIONS

Bias Current

Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the "maximum" bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed up operating unit.

The AD503 specifies maximum bias currents at either input after warmup, thus giving the user the values he expected.

Improving Bias Current Beyond Guaranteed Values

Bias currents can be substantially reduced by decreasing the junction temperature of the device. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

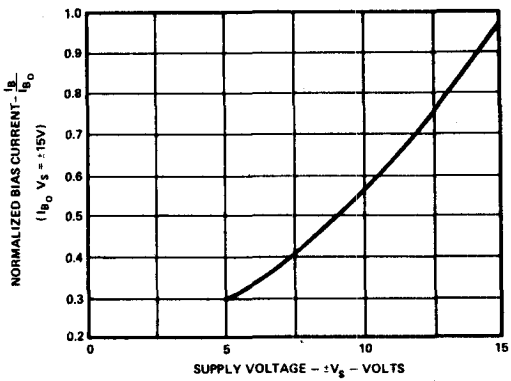


Figure 1. Normalized Bias Current vs Supply Voltage

Operation of the AD503K at ±5V reduces the warmed up bias current by 70% to a typical value of 0.75pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading.

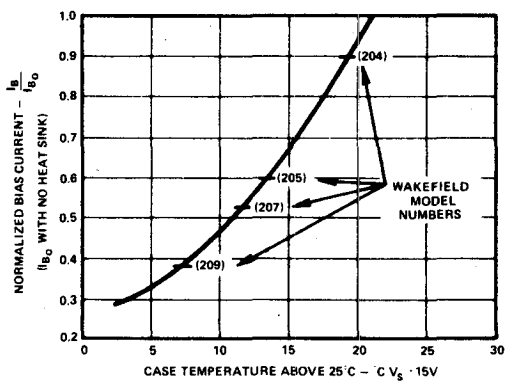


Figure 2. Normalized Bias Current vs Case Temperature

Note that the use of the model 209 heat sink reduces warmed up bias current by 60% to 1.0pA in the AD503K.

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

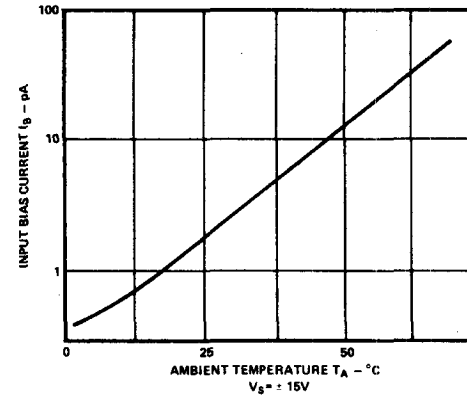


Figure 3. Input Bias Current vs Temperature

Input Considerations

The common mode input characteristic is shown in Figure 4. Note that positive common mode inputs up to +13.5 Volts and negative common mode inputs to –Vs are permissible, without incurring excessive bias currents. To prevent possible damage to the unit, do not exceed V_{CM} = Vs.

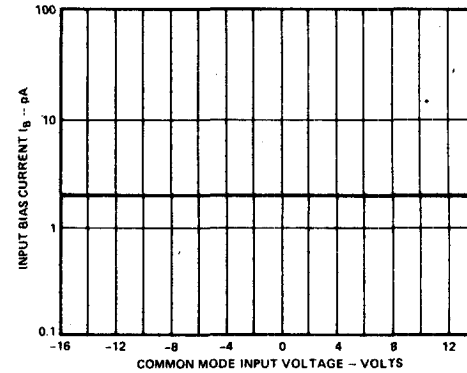


Figure 4. Input Bias Current vs Common Mode Voltage

Like most other FET input op amps, the AD503 displays a degraded bias current specification when operated at moderate differential input voltages. It maintains its specified bias current up to a differential input voltage of ±3V typically. Above ±3V, the bias current will increase to approximately 400μA. This is not a failure mode. Above ±10V differential input voltage, the bias current will increase 100μA/V_{diff} (in volts), and other parameters may suffer degradation.