2x15W Stereo Class-D Audio Amplifier with Power Limit

Features

- Single supply voltage
  4.5V ~ 14.4V for loudspeaker driver
  Built-in LDO output 5V for others
- Loudspeaker power from 12V supply
  BTL Mode: 8W/CH into 8Ω @1% THD+N
  BTL Mode: 10W/CH into 6Ω @<1% THD+N
  BTL Mode: 12W/CH into 4Ω @<1% THD+N
  PBTL Mode: 16W/CH into 4Ω @1% THD+N
- Loudspeaker power from 12V supply
  BTL Mode: 10W/CH into 8Ω @10% THD+N
  BTL Mode: 14W/CH into 6Ω @10% THD+N
  BTL Mode: 15W/CH into 4Ω @10% THD+N
  PBTL Mode: 20W/CH into 4Ω @10% THD+N
- 93% efficient Class-D operation eliminates need for heat sink
- Differential inputs
- Internal oscillator
- Short-Circuit protection
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Superior EMC performance

Applications

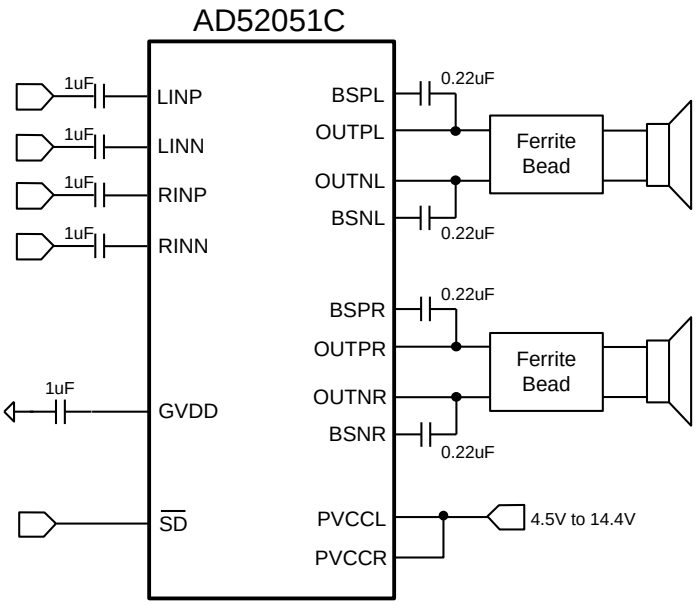
- TV audio
- Boom-Box
- Powered speaker
- Monitors
- Consumer Audio Equipment

Description

The AD52051C is a high efficiency stereo class-D audio amplifier with adjustable power limit function. The loudspeaker driver operates from 4.5V~14.4V supply voltage. It can deliver 15W/CH output power into 4Ω loudspeaker within 10% THD+N at 12V supply voltage and without external heat sink when playing music.

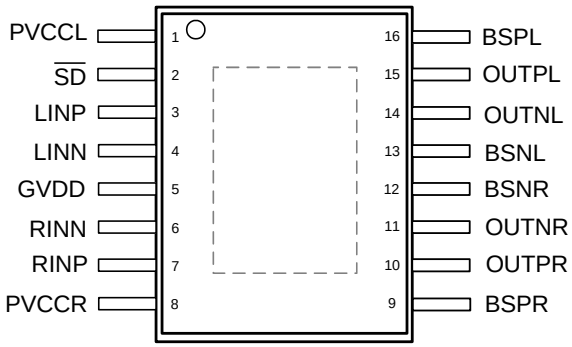
Output DC detection and short circuit protection prevents speaker damage from long-time current stress. AD52051C provides superior EMC performance for filter-free application. The over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments

E-TSSOP-16L
(TOP VIEW)



Pin Description

NAME	E-TSSOP-16L	TYP	DESCRIPTION
PVCCL	1	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
$\overline{SD}$	2	I	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to PVCC.
LINP	3	I	Positive audio input for left channel.
LINN	4	I	Negative audio input for left channel.
GVDD	5	O	5V regulated output.
RINN	6	I	Negative audio input for right channel.
RINP	7	I	Positive audio input for right channel.
PVCCR	8	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
BSPR	9	I	Bootstrap I/O for right channel, positive high side FET.
OUTPR	10	O	Class-D H-bridge positive output for right channel.
OUTNR	11	O	Class-D H-bridge negative output for right channel.
BSNR	12	I	Bootstrap I/O for right channel, negative high side FET.
BSNL	13	I	Bootstrap I/O for left channel, negative high side FET.
OUTNL	14	O	Class-D H-bridge negative output for left channel.
OUTPL	15	O	Class-D H-bridge positive output for left channel.
BSPL	16	I	Bootstrap I/O for left channel, positive high side FET.
Thermal Pad (GND)		P	Must be soldered to PCB's ground plane.

Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD52051C-26QG16NRR	E-TSSOP-16L	Tape & Reel 2.5K pcs	Green

Available Package

Package Type	Device No.	θ_{JA}(℃/W)	θ_{JT}(℃/W)	Ψ_{JT}(℃/W)	Exposed Thermal Pad
E-TSSOP-16L	AD52051C	39.6	24.6	0.7	Yes (Note 1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.

Note 1.2: θ_{JA} is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{JT} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

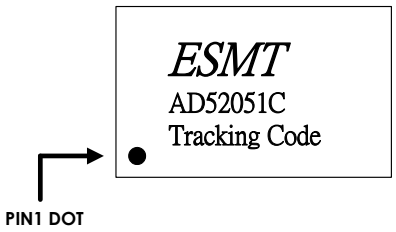
Note 1.4: Ψ_{JT} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{JA}, using a procedure described in JESD51-5.

Marking Information

AD52051C

- Marking Information

Line 1：LOGO
Line 2：Product No
Line 3：Tracking Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCCL, PVCCR	-0.3	20	V
V_I	Interface pin voltage	$\overline{SD}$	-0.3	20	V
T_A	Operating free-air temperature range		-40	85	°C
T_J	Operating junction temperature range		-40	150	°C
T_{stg}	Storage temperature range		-65	150	°C
R_L	Minimum Load Resistance		3.2		Ω
ESD	Human Body Model			±2K	V
	Charged Device Model			±500	

Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCCL, PVCCR	4.5	14.4	V
V_I	Signal input level voltage	LINP, LINN, RINP, RINN		2	Vrms
V_{IH}	High-level input voltage	$\overline{SD}$	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, VI=2V, PVCC=12V		50	uA
I_{IL}	Low-level input current	$\overline{SD}$, V_I=0.8V, PVCC=12V		5	uA
I_{OH}	High-level output current	V_I=2V, PVCC=12V		50	uA
I_{OL}	Low-level output current	V_I=0.8V, PVCC=12V		50	uA
T_A	Operating free-air		-40	85	°C

General Electrical Characteristics

- PVCC=12V, R_L=8Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$I_{CC(q)}$	Quiescent supply current	SD=2V, no load, PVCC=12V		8	12	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SD=0.8V, no load, PVCC=12V		< 12	25	uA
$R_{DS(on)}$	Drain-source on-state resistance-High side NMOS	PVCC=12V, Id=500mA, T_J=25 °C		170		mΩ
	Drain-source on-state resistance-Low side NMOS			170		mΩ
$\|V_{OS}\|$	Class-D output offset voltage (measured differential)	PVCC=12V V_I=0V, Gain=26dB		1.5	10	mV
t_{ON}	Turn-on time	SD=2V		8		ms
t_{OFF}	Turn-off time	SD=0.8V		3		us
GVDD	Regulator output	I_{GVDD}=0.1mA	4.75	5	5.25	V
$PVCC_{UV}$	Under voltage protection of AVCC			4.0		V
	Under voltage hysteresis window of AVCC		0.2			
G	Gain	PVCC=12V, SD=2V	25	26	27	dB
f_{OSC}	Oscillator frequency		250	310	370	kHz
I_{SC}	L(R) Channel Over-Current Protection (Note 2)	PVDD=12V		8		A
	Mono Over-Current Protection (Note 2)	PVDD=12V		15		A
T_{SENSOR}	Thermal trip point			160		°C
	Thermal hysteresis			25		°C

Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Electrical Characteristics and Specifications of Loudspeaker Driver (BTL, Stereo)

- PVCC=12V, R_L=8Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power	THD+N=10%, f=1kHz, 8Ω		10		W
		THD+N=10%, f=1kHz, 6Ω		14		
		THD+N<10%, f=1kHz, 4Ω		15		
THD+N	Total harmonic distortion plus noise	PVCC=12V, R_L=8Ω, f=1kHz, P_O=5W (half-power)		<0.02		%
		PVCC=12V, R_L=6Ω, f=1kHz, P_O=7W (half-power)		<0.02		
		PVCC=12V, R_L=4Ω, f=1kHz, P_O=7.5W (half-power)		<0.02		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=26dB, a-weighted		94		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=26dB, a-weighted filter, R_L=8Ω		110		uV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=26dB, inputs ac-grounded		-70		dB
Crosstalk	Crosstalk	F=1kHz, V_O=1Vrms, Gain=26dB		-95		dB

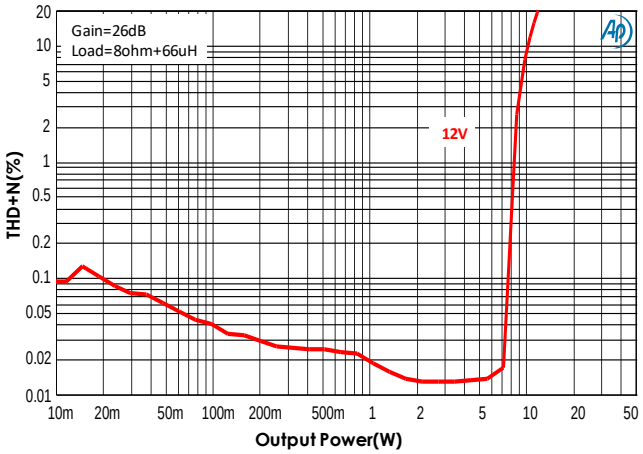
Electrical Characteristics and Specifications of Loudspeaker Driver (PBTL, Mono)

- PVCC=12V, R_L=4Ω, T_A=25°C (unless otherwise noted)

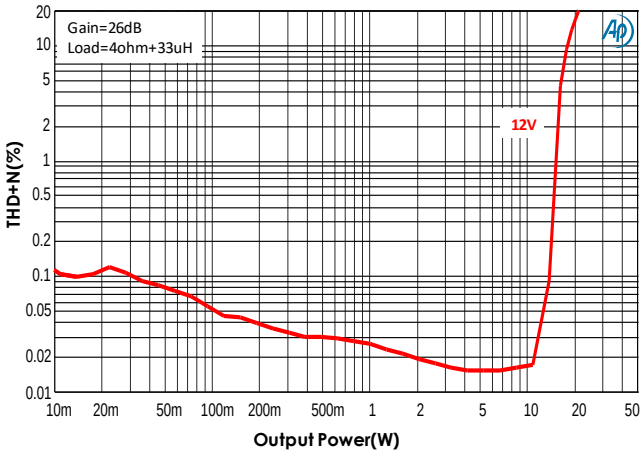
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power	THD+N=1%, f=1kHz, 4Ω		16		W
		THD+N=10%, f=1kHz, 4Ω		20		
THD+N	Total harmonic distortion plus noise	PVCC=12V, R_L=4Ω, f=1kHz, P_O=10W		<0.02		%
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=26dB, a-weighted		95		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=26dB, a-weighted filter, R_L=8Ω		110		uV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=26dB, inputs ac-grounded		-66		dB

Typical Characteristics

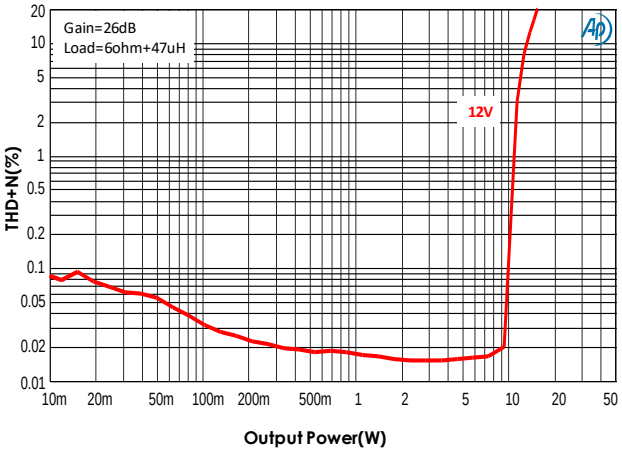
THD+N vs. Output Power, 8Ω load



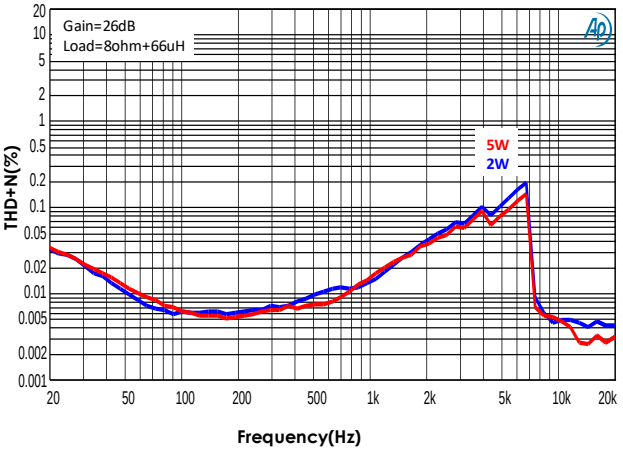
THD+N vs. Output Power, 4Ω load



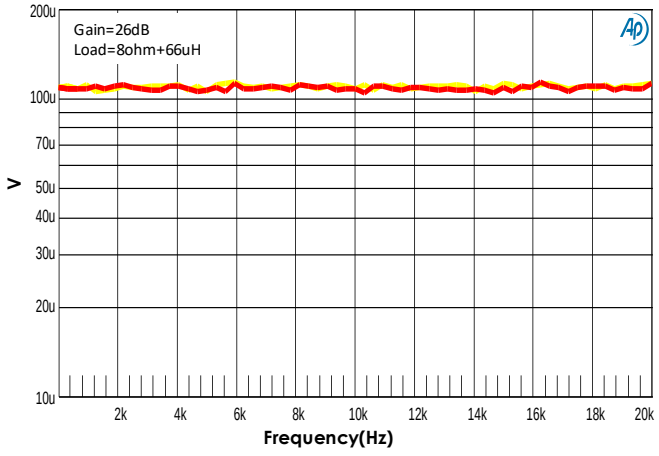
THD+N vs. Output Power, 6Ω load



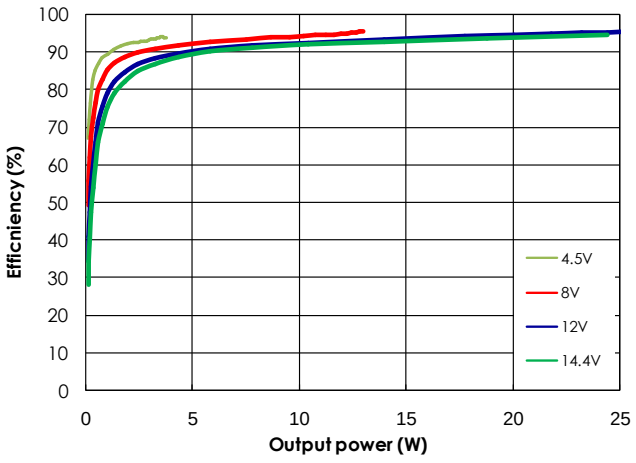
THD + N (%) vs. Frequency, 8Ω load



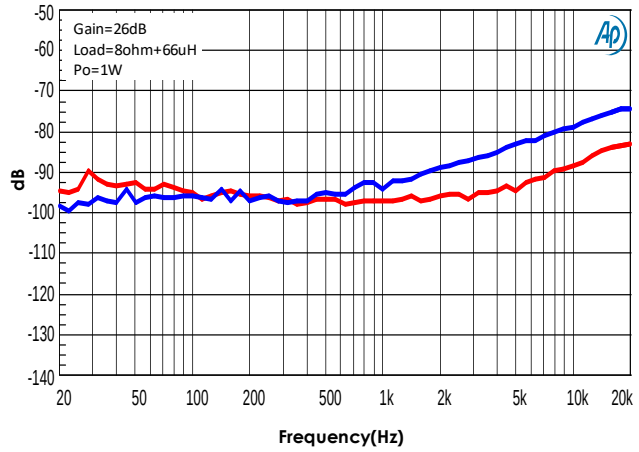
Noise, 8Ω load



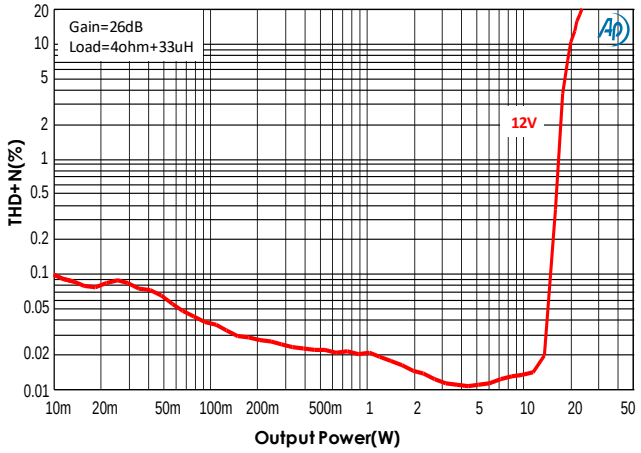
Efficiency (Stereo 8Ω load) / 2ch



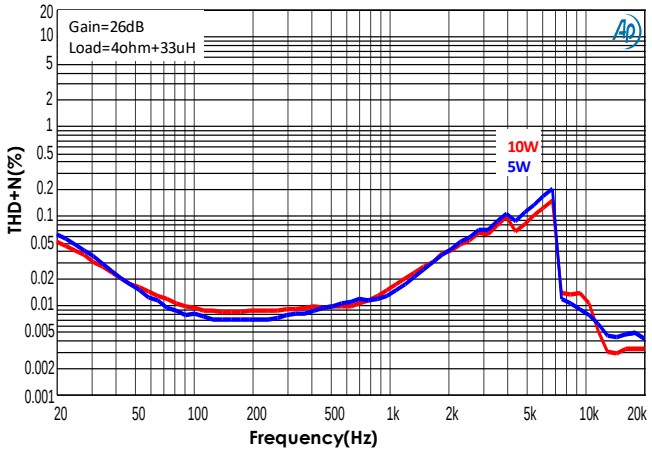
Cross-Talk ,8Ω load (Stereo)



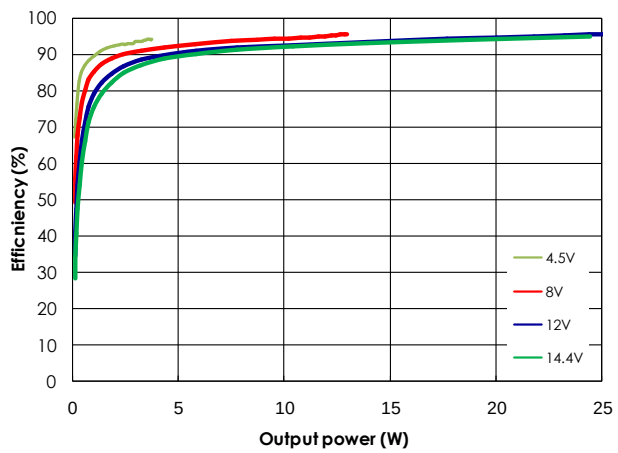
THD+N vs. Output Power, 4Ω load (PBTL)



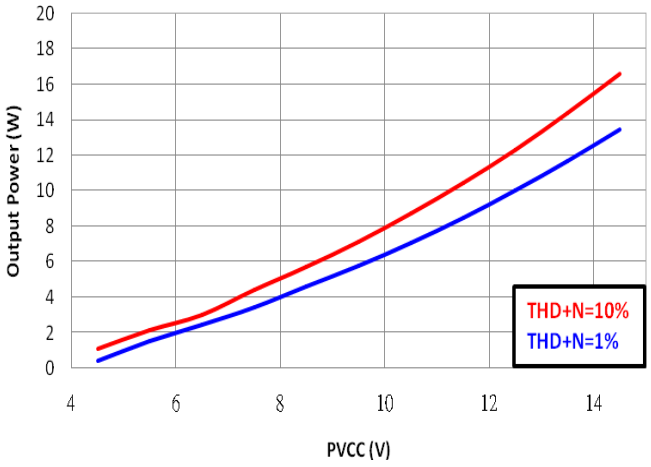
THD + N (%) vs. Frequency, 4Ω load (PBTL)



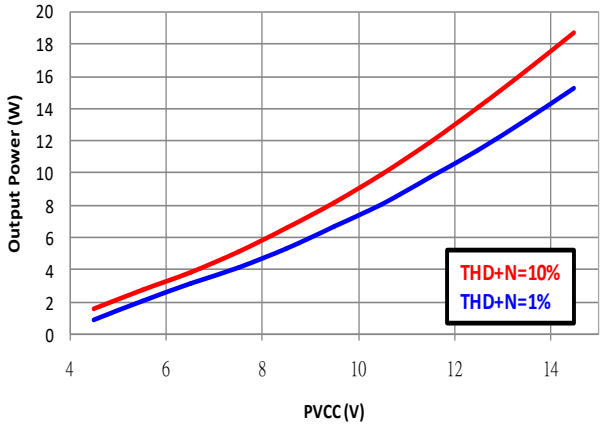
Efficiency (PBTL 4Ω load)



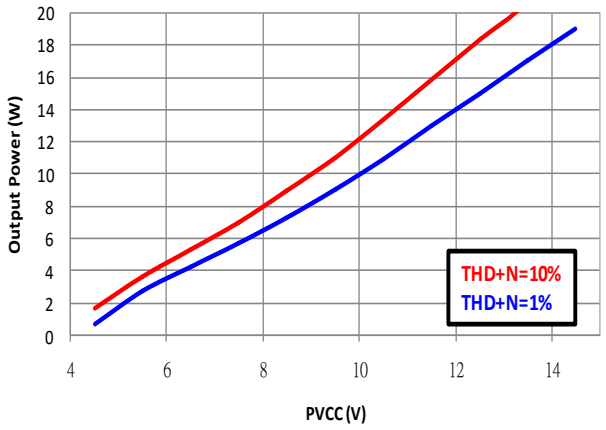
Supply voltage vs. Output Power, 8Ω load (Stereo)



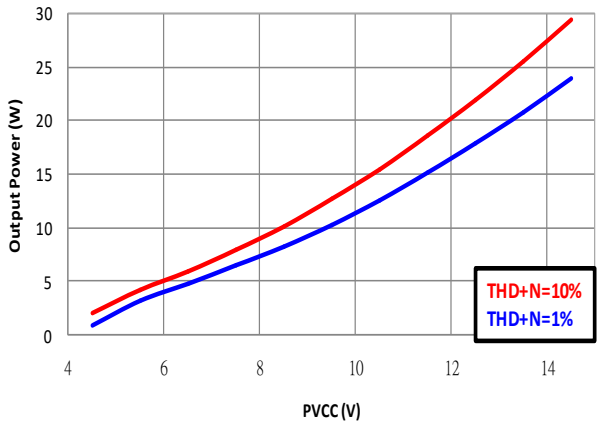
Supply voltage vs. Output Power, 6Ω load (Stereo)



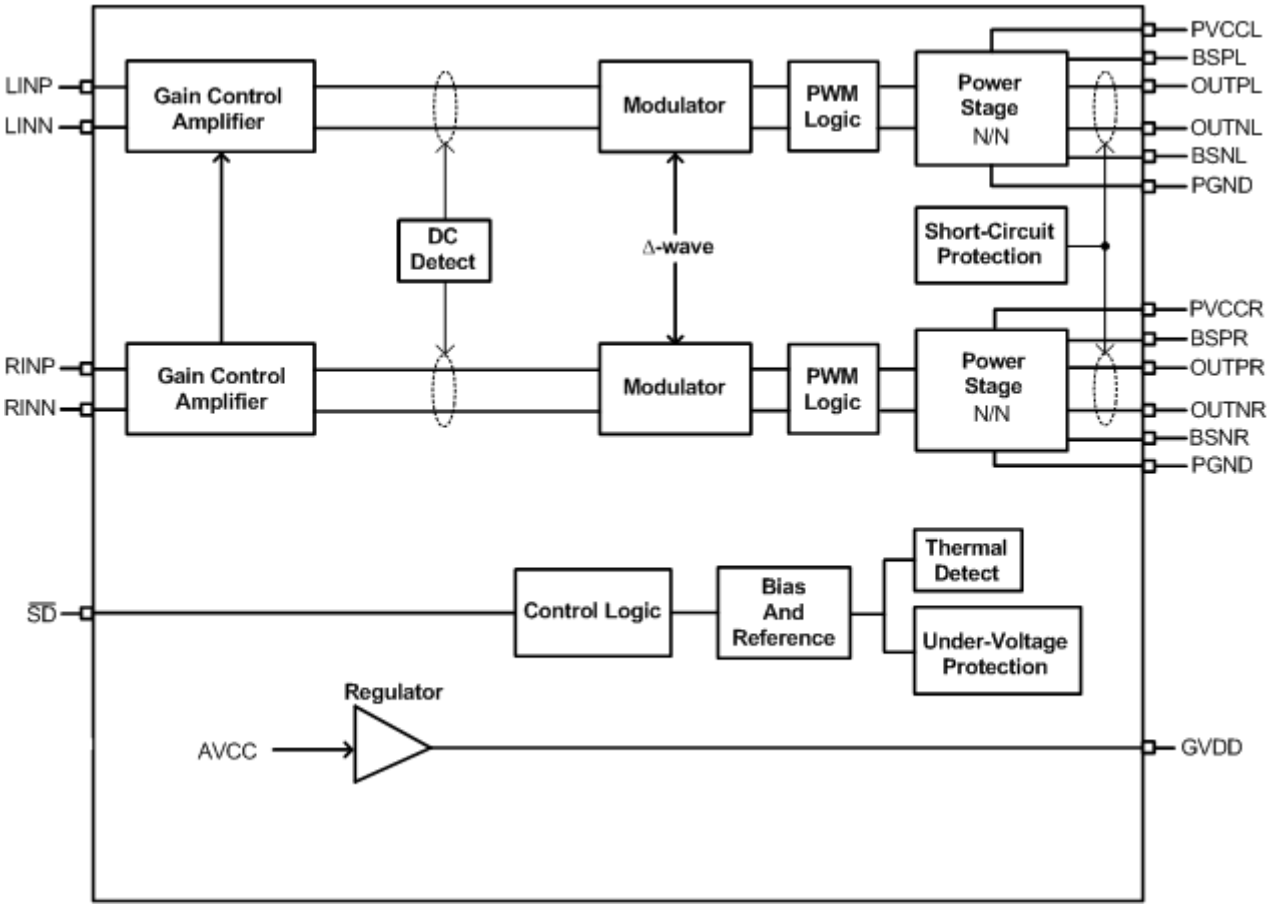
Supply voltage vs. Output Power, 4Ω load (Stereo)



Supply voltage vs. Output Power, 4Ω load (PBTL)



Functional Block Diagram



Operation Descriptions

- **Shutdown ($\overline{SD}$) control**

  Pulling $\overline{SD}$ pin low will let AD52051C operate in low-current state for power conservation. The AD52051C outputs will enter mute once $\overline{SD}$ pin is pulled low, and regulator will also disable to save power. If let $\overline{SD}$ pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

- **DC detection**

  AD52051C has DC detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 340ms, the DC detect error will occur. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. The fault state can not be cleared by cycling $\overline{SD}$, it is necessary to cycle the PVCC supply.

  The minimum differential input voltages required to trigger the DC detect function are shown in table1. The input voltage must keep above the voltage listed in the table for more than 340msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in table 2.

Table 1. DC Detect Threshold

AV (dB)	Vin (mV, differential)
26	125

Table 2. Output DC Detect Duty (for Either Channel)

PVCC (V)	Output Duty Exceeds
8	20.8%
12	20.8%

- **Thermal protection**

  If the internal junction temperature is higher than 160^{o}C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD52051C returning to normal operation is about 135^{o}C. The variation of protected temperature is about 10%.

- **Short-circuit protection**

  To protect loudspeaker drivers from over-current damage, AD52051C has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to VSS or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The latch can be cleared by reset $\overline{SD}$ or power supply cycling.

- **Under-voltage detection**

  When the GVDD voltage is lower than 2.8V or the PVCC voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD52051C return to normal operation.

- **PBTL (Mono) function**

  AD52051C provides the application of parallel BTL operation with two outputs of each channel connected directly. If connect INPL and INNL directly to Ground (without capacitors) this sets the device in Mono mode during power up. Connect OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for the negative pin. Analog input signal is applied to INPR and INNR.

- **Over-voltage protection**

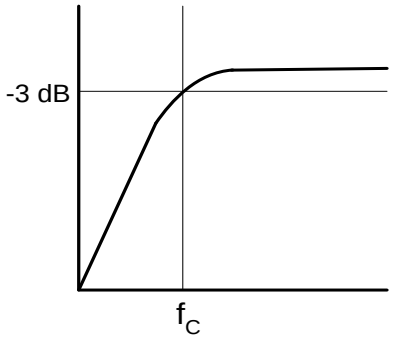
  When the PVCC voltage is higher than 15.5V, loudspeaker will be disabled kept at low state. The protection status will be released as PVCC lower than 15V.

Application information

- **Input capacitors (C_{in})**

  The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{in}.The resistance of input resistors is 30kΩ at gain +26dB setting in AD52051C. However, there is 20% variation in input resistance from production variation.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \ (\text{Hz}) \quad \cdots\cdots\cdots (2)$$



- **Ferrite Bead selection**

  If the traces from the AD52051C to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

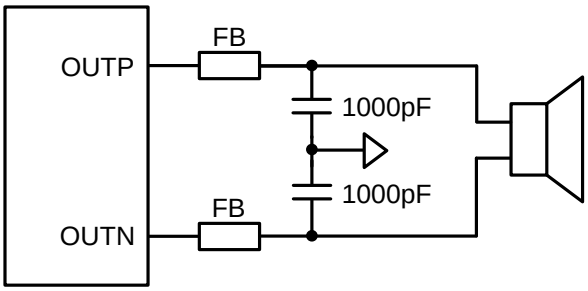


Figure 2. Typical Ferrite Bead Filter

- **Output LC Filter**

  If the traces from the AD52051C to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 3 shows the typical output filter for 8Ω speaker with a cut-off frequency of 27 kHz and Figure 4 shows the typical output filter for 4Ω speaker with a cut-off frequency of 27 kHz.

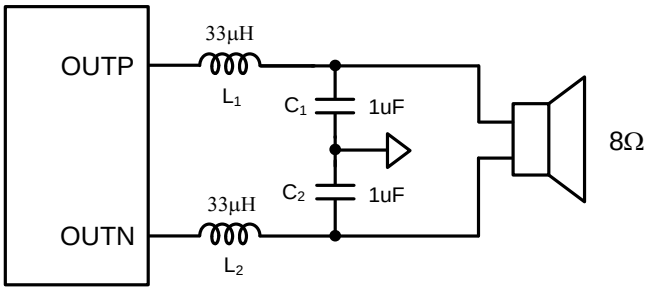


Figure 3. Typical LC Output Filter for 8Ω Speaker

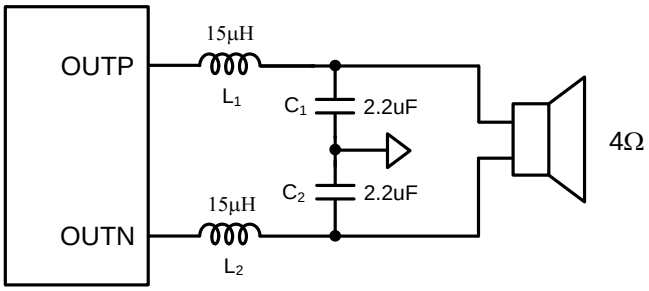


Figure 4. Typical LC Output Filter for 4Ω Speaker

- **Power supply decoupling capacitor (Cs)**

  Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1uF or 1uF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100uF or greater capacitor (tantalum or electrolytic type) is suggested.

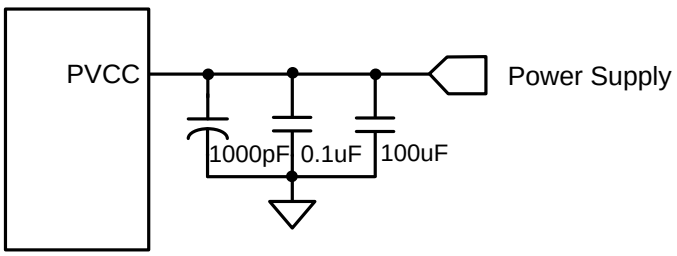
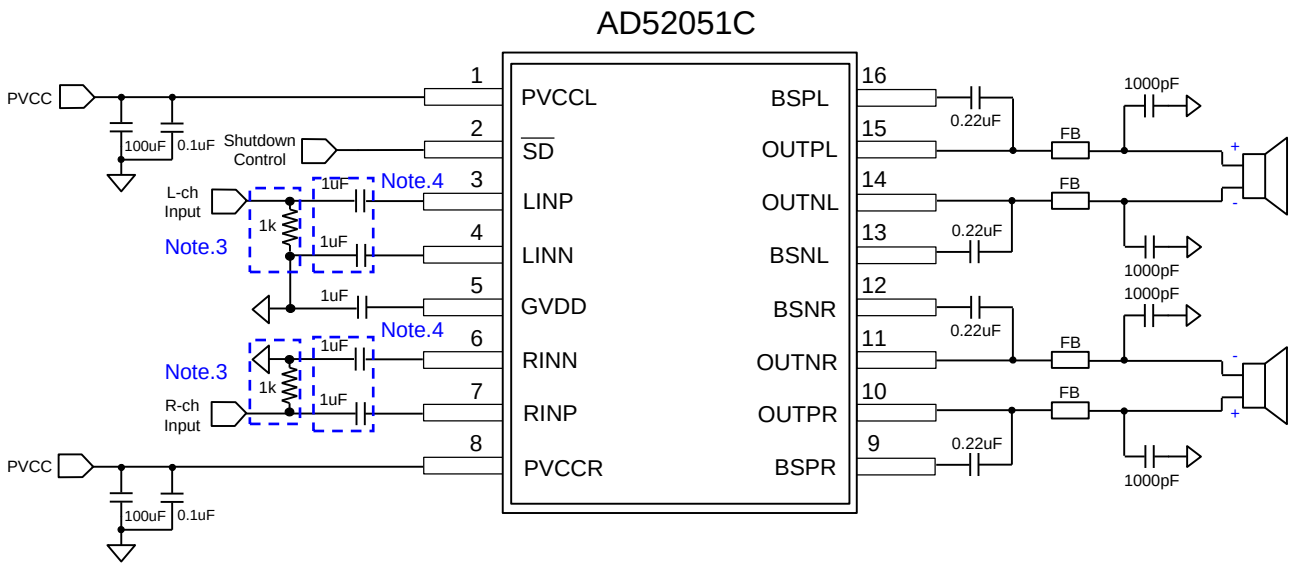


Figure 5. Recommended Power Supply Decoupling Capacitors.

Application Circuit Example

- Application circuit for BTL (Stereo) mode configuration and Single-Ended Input

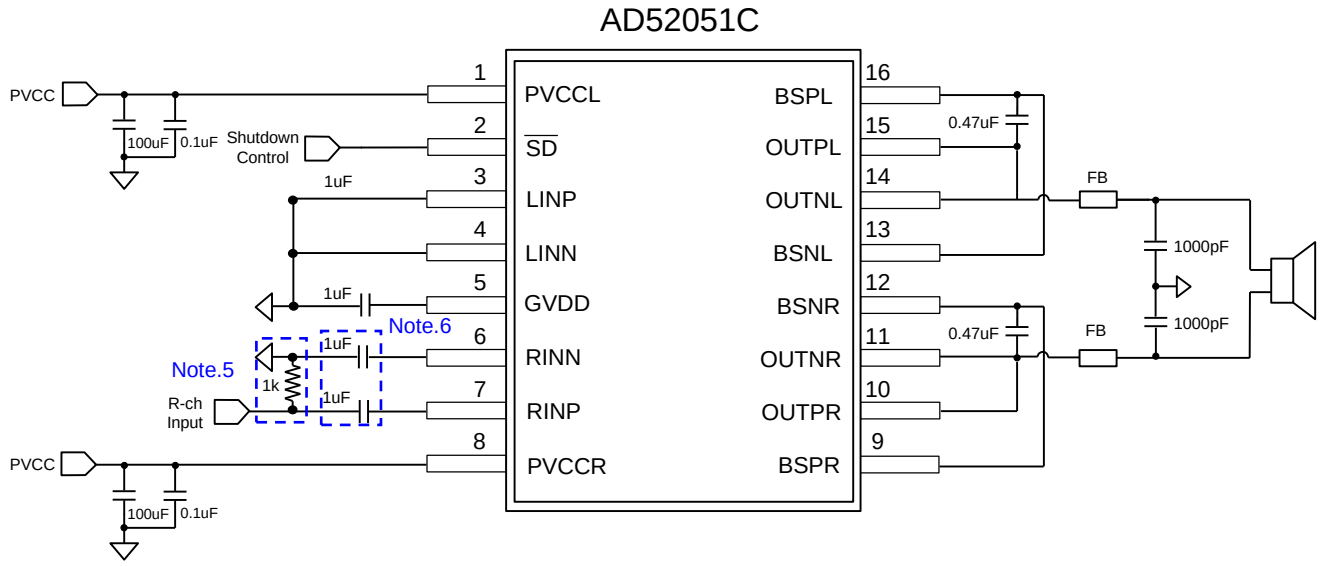


Note 3: These resistances must be connected to ground, resistance=1Kohm

Note 4: The faster turn-on time 8ms is designed for AD52051C, the pop sound shall be take care with the input resistor (Rin) added into for input signal attenuation requirement. The longer shutdown release time is necessary if the input resistor (Rin) is adopted.

Application Circuit Example

- Application circuit for parallel PBTL (Mono) mode configuration and Single-Ended Input



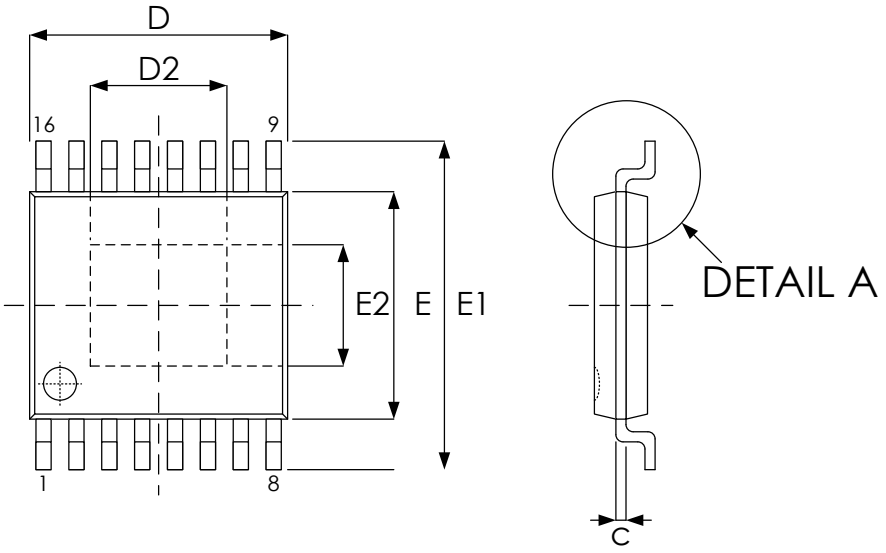
Note 5: These resistances must be connected to ground, resistance=1Kohm

Note 6: The faster turn-on time 8ms is designed for AD52051C, the pop sound shall be take care with the input resistor (Rin) added into for input signal attenuation requirement. The longer shutdown release time is necessary if the input resistor (Rin) is adopted.

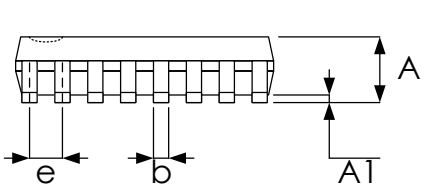
Note 7: Be noted that input should be applied on R-channel only for Mono application.

Package Outline Drawing

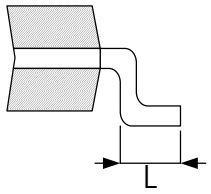
- **E-TSSOP-16L**



TOP VIEW



SIDE VIEW



DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	--	1.20
A1	0.00	0.15
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	4.30	4.50
E1	6.20	6.60
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	2.40	3.00
E2	1.90	3.00

Revision History

Revision	Date	Description
0.1	2023.12.06	Original.
0.2	2024.04.24	1. Update supply voltage 4.5~14.4V. Page 1, 4. 2. Update pin assignments. Page 2. 3. Update ordering Information and available package. Page 3. 4. Update general electrical characteristics. Page 5~6. 5. Update typical characteristics. Page 7~9. 6. Update operation descriptions for under-voltage detection. Page 12. 7. Update package outline drawing. Page 17.

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