

**2x7W Stereo / 1x10W Mono Class-D Audio Amplifier
With Built-in Step-up Converter**

Features

- Input voltage 2.9V~12V
- Adjustable boost converter output up to 14V
- Loudspeaker power @8V boost from 4.2V
Stereo: 7W/CH into 4Ω @ THD+N=10%
- Loudspeaker power @10V boost from 4.2V
Mono (PBTL): 10W/CH into 4Ω @ <10% THD+N
- Loudspeaker power @8V boost from 3.7V
Stereo: 6W/CH into 4Ω @ THD+N=1%
- Mono (PBTL): 8.7W/CH into 4Ω @THD+N=10%
- Differential inputs signal
- Fixed gain setting
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Superior EMC performance

Applications

- Blue-tooth Box
- Portable Media
- Audio Docking System
- Tablet Personal PC
- Consumer Audio Equipment

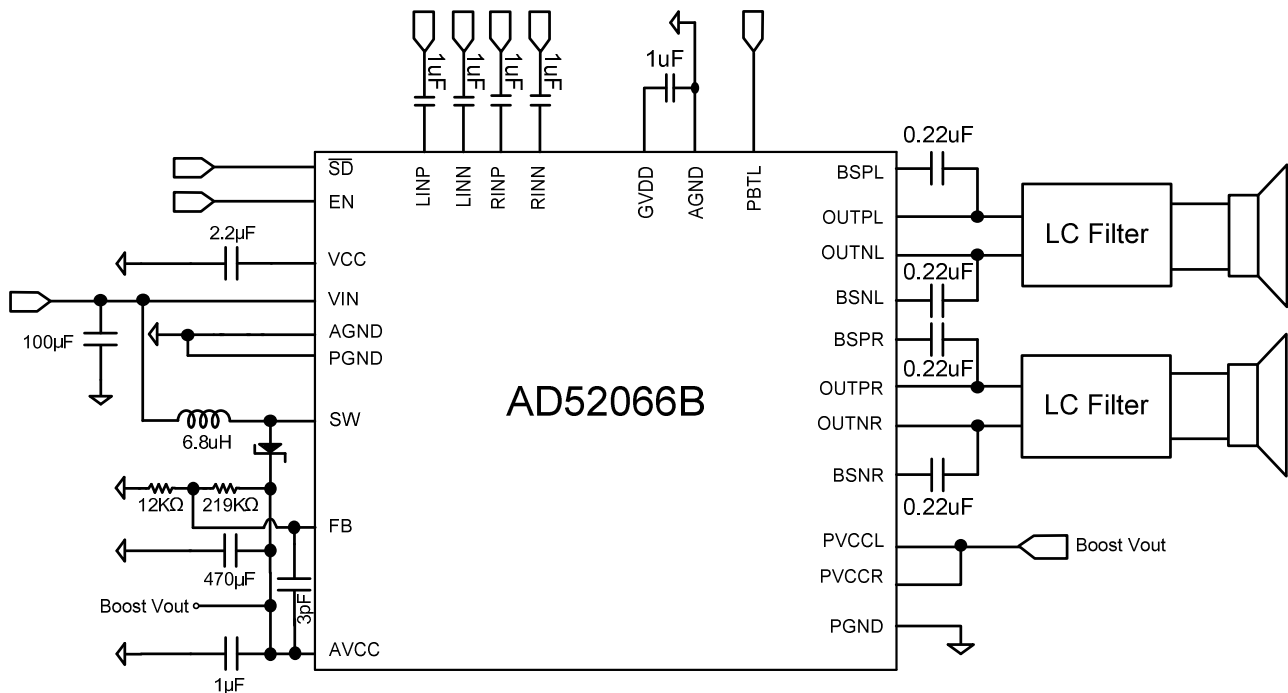
Description

The AD52066B is a high efficiency stereo class-D audio amplifier with built-in boost DC-DC converter. The loudspeaker driver can deliver stereo 7W/CH output power into 4Ω loudspeaker under 10% THD+N at one-cell Li-ion battery (4.2V).

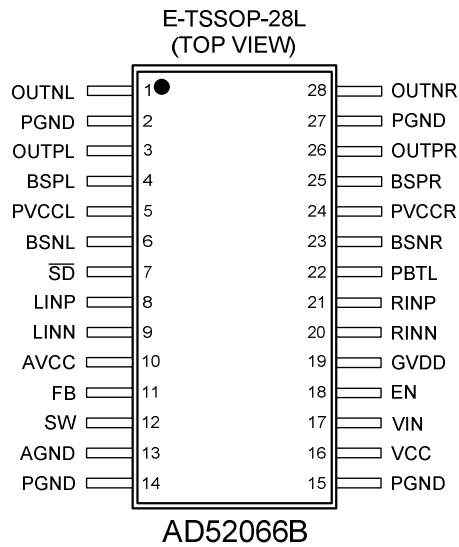
AD52066B provides parallel BTL (Mono) application also, and it can deliver 10W into 4Ω loudspeaker under 10% THD+N at 4.2V supply voltage.

Output DC detection prevents speaker damage from long-time current stress. AD52066B provides superior EMC performance for filter-free application. The output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments



Pin Description

PIN NAME	E-TSSOP-28L	TYP	DESCRIPTION
OUTNL	1	O	Class-D H-bridge negative output for left channel.
OUTPL	3	P	Class-D H-bridge positive output for left channel.
BSPL	4	I	Bootstrap I/O for left channel, positive high side FET.
PVCCCL	5	P	High-voltage power supply for left-channel. Right channel and left channel power supply inputs are connect internal.
BSNL	6	I	Bootstrap I/O for left channel, negative high side FET.
\overline{SD}	7	I	Shutdown signal for IC (low=disabled, high=operational). Voltage compliance to AVCC.
LINP	8	I	Positive audio input for left channel.
LINN	9	I	Negative audio input for left channel.
AVCC	10	P	Analog supply.
FB	11	I	Receives the feedback voltage from an external resistive divider across the output.
SW	12	O	Must be connected an Inductor from VCC pin to SW pin for boost and rectifying switches.
AGND	13	P	Boost ground pin
VCC	16	P	A ceramic capacitor of more than 2.2uF requirement between this pin and GND.
VIN	17	P	Must be closely decoupled to GND pin with 470uF*1or greater ceramic capacitor.
EN	18	I	Boost enable pin (high=Enable; low=Disable).
GVDD	19	P	5V regulated output.

RINN	20	I	Negative audio input for right channel. Biased at 2.5V.
RINP	21	I	Positive audio input for right channel. Biased at 2.5V.
PBTL	22	I	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to AVCC.
BSNR	23	I	Bootstrap I/O for right channel, negative high side FET.
PVCCR	24	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
BSPR	25	I	Bootstrap I/O for right channel, positive high side FET.
OUTPR	26	O	Class-D H-bridge positive output for right channel.
PGND	27	P	Power ground for the H-bridges.
OUTNR	28	O	Class-D H-bridge negative output for right channel.
PGND	2,14,15,27	P	Power ground Pin.
Thermal Pad		P	Must be soldered to PCB's ground plane.

Note:

P: Power or ground pins; I: Input pins; O: Output pins; I/O: The bidirectional pins

Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD52066B-26QG28NRT	E-TSSOP 28L	50Units / Tube 100 Tubes / Small Box	Green

Available Package

Package Type	Device No.	θ_{ja} (°C/W)	θ_{jt} (°C/W)	Ψ_{jt} (°C/W)	Exposed Thermal Pad
E-TSSOP 28L	AD52066B	28	27.1	1.33	Yes (Note 1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{JA} is measured on a room temperature ($T_A=25^\circ\text{C}$), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: $\theta_{JC(top)}$ represents the heat resistance for the heat flow between the chip and the package's top surface. (The junction-to-top thermal resistance is obtained by simulating a cold plate test on the top of the package).

Note 1.4: $\Psi_{JC(bottom)}$ represents the heat resistance for the heat flow between the chip and the exposed pad center. (The junction-to-top characterization parameter is extracted from the simulation data to obtain θ_{ja}).

Marking Information

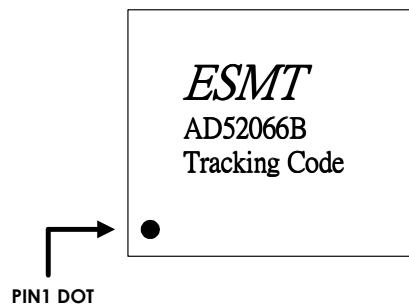
AD52066B

- Marking Information

Line 1 : LOGO

Line 2 : Product No

Line 3 : Tracking Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{IN}	Supply voltage	V _{IN}	-0.3	16	V
V _{I(Boost)}	Interface pin voltage for boost	EN, FB, VCC	-0.3	6	V
	Boost switch pin	LX	-0.3	16	V
PVCC	Class-D supply voltage	PVCCL, PVCCR, AVCC	-0.3	16	V
V _{I(Class-D)}	Interface pin voltage	\overline{SD} , PBTL,	-0.3	16	V
T _J	Operating junction temperature range		-40	150	°C
T _{stg}	Storage temperature range		-65	150	°C
R _L	Minimum Load Resistance	BTL, PBTL	3.2		Ω

Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{IN}	Supply voltage	V _{IN}	2.9	12	V
PVCC	Class-D supply voltage	PVCCL, PVCCR, AVCC	5	14	V
V _{IH}	High-level input voltage	\overline{SD} , PBTL	2		V
		EN	1.2		
V _{IL}	Low-level input voltage	\overline{SD} , PBTL, EN		0.4	V
T _A	Operating free-air		-40	85	°C

Boost General Electrical Characteristics

● T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN_UVLO}	V _{IN} UVLO Threshold	V _{IN} rising	2.55	2.6	2.9	V
	V _{IN} UVLO Threshold	V _{IN} falling	2.35	2.4	2.65	V
F _{OSC}	Operation Frequency	V _{FB} =0.5V	380	500	620	kHz
T _{DUTY}	Maximum Duty Cycle			90		%
V _{REF}	Reference Voltage			0.6		V
I _{LIM}	Current Limit	V _{IN} =6V, V _{EN} =1.2V		5.5		A
	EN Pull down resistor			800		kΩ

Audio General Electrical Characteristics

- PVCC=8V, R_L=4Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
R _{DS(on)}	Drain-source on-state resistance-High side NMOS	PVCC=8V, I _d =250mA, T _J =25 °C		220		mΩ
	Drain-source on-state resistance-Low side NMOS			220		mΩ
V _{OS}	Class-D output offset voltage (measured differential)	PVCC=8V V _I =0V, Gain=36dB		1.5	15	mV
t _{ON}	Turn-on time	SD=2V		90		ms
t _{OFF}	Turn-off time	SD=0.8V		2		μs
GVDD	Regulator output	I _{GVDD} =0.1mA	4.75	5	5.25	V
f _{osc}	Oscillator frequency		250	310	370	kHz
G	Gain	For product ID of AD52066B-32QG28NRT only (E-TSSOP-28L)	24	26	28	dB

Electrical Characteristics and Specifications of Loudspeaker Driver

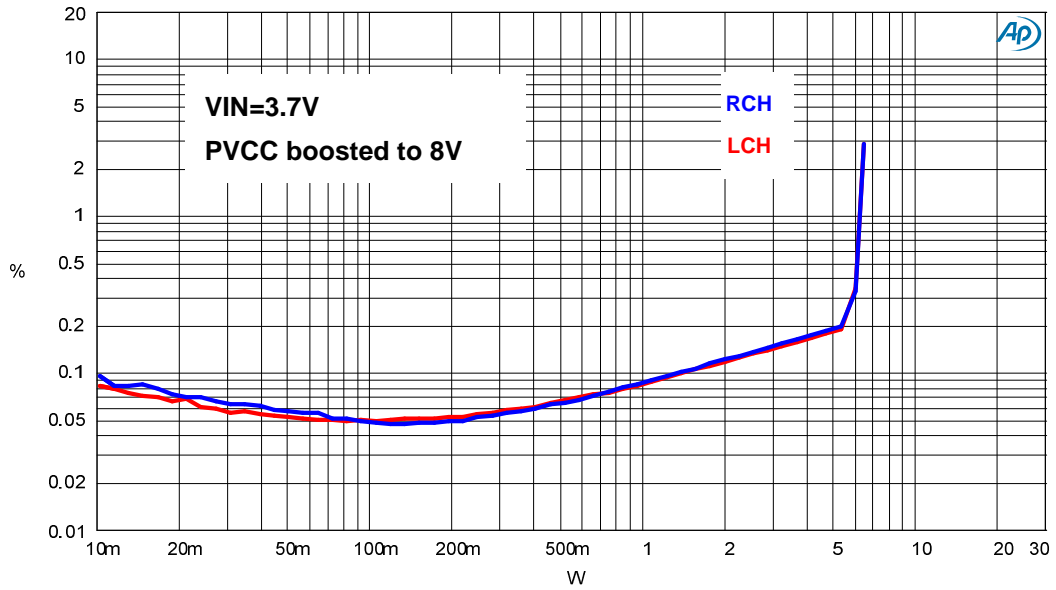
● Stereo Output (BTL Output)

Condition: $V_{IN}=3.7V$, $PVCC$ boosted to 8V, $R_L=4\Omega+33\mu H$, Common mode filter= $15\mu H+2.2\mu F$, $T_A=25^\circ C$ (unless otherwise noted)

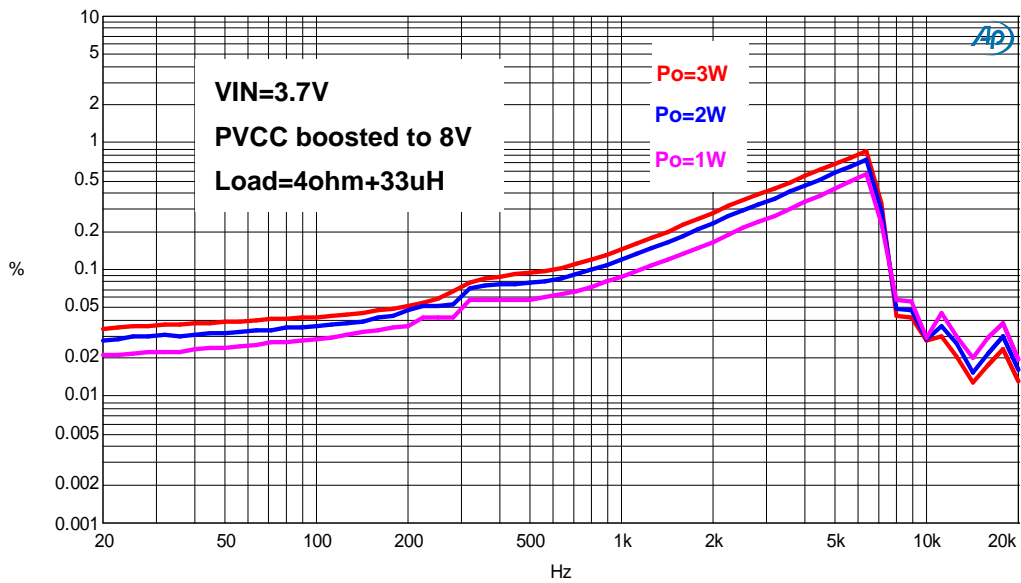
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_o	Output power	THD+N=1%, $f=1kHz$, $PVCC=8V$		6		W
THD+N	Total harmonic distortion plus noise	$PVCC=8V$, $f=1kHz$, $P_o=3W$		0.13		%
SNR	Signal to noise ratio	Maximum output at THD+N<1%, $f=1kHz$, Gain=20dB, a-weighted		91		dB
V_n	Output integrated noise	$F=20Hz \sim 20kHz$, Gain=26dB, a-weighted filter,		125		μV
K_{SVR}	Power Supply Rejection Ratio	$V_{ripple}=200mV_{pp}$ at 1kHz, Gain=26dB, inputs ac-grounded		-70		dB
Crosstalk	Crosstalk	$F=1kHz$, $V_o=1V_{rms}$, Gain=26dB		-90		dB
I_Q	Quiescent Current	$V_{IN}=4.2V$, $PVCC=8V$		30		mA
I_{SD}	Shutdown Current	$V_{IN}=4.2V$, $PVCC=8V$		45		μA

Note: P_o measurement is probed at the terminal on the EVB.

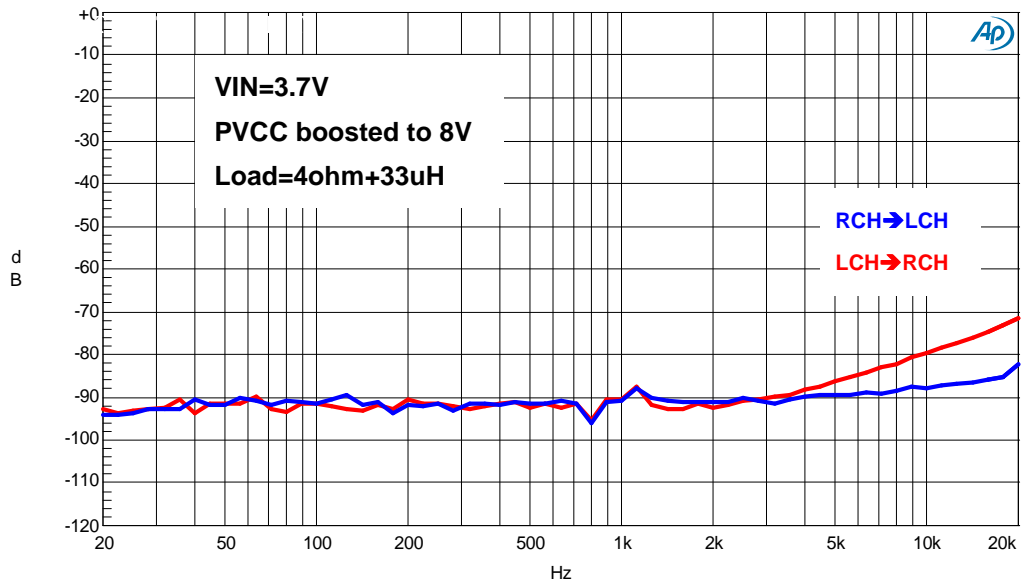
THD + N (%) vs. Output power (4ohm+33uH load)



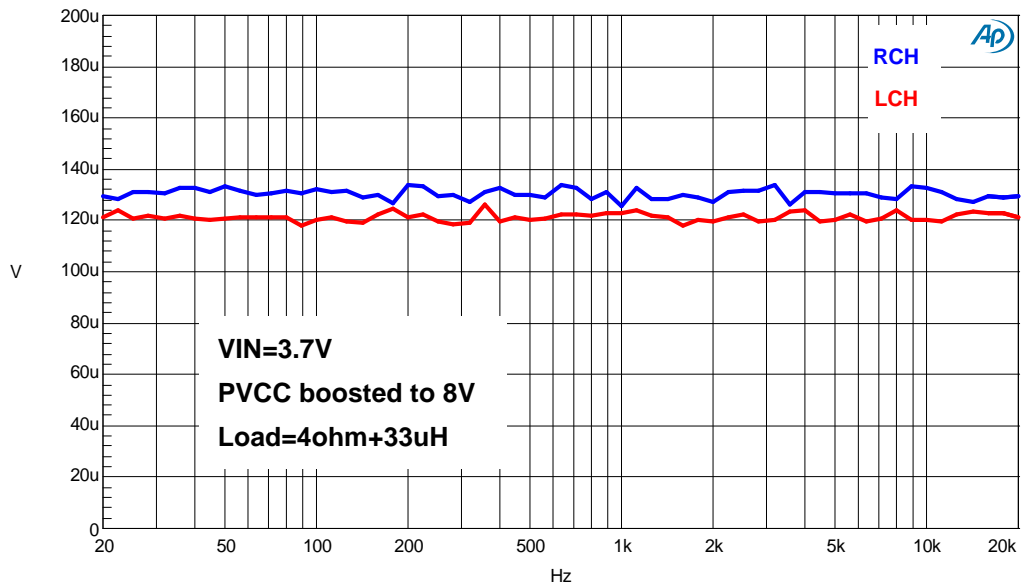
THD + N (%) vs. Frequency



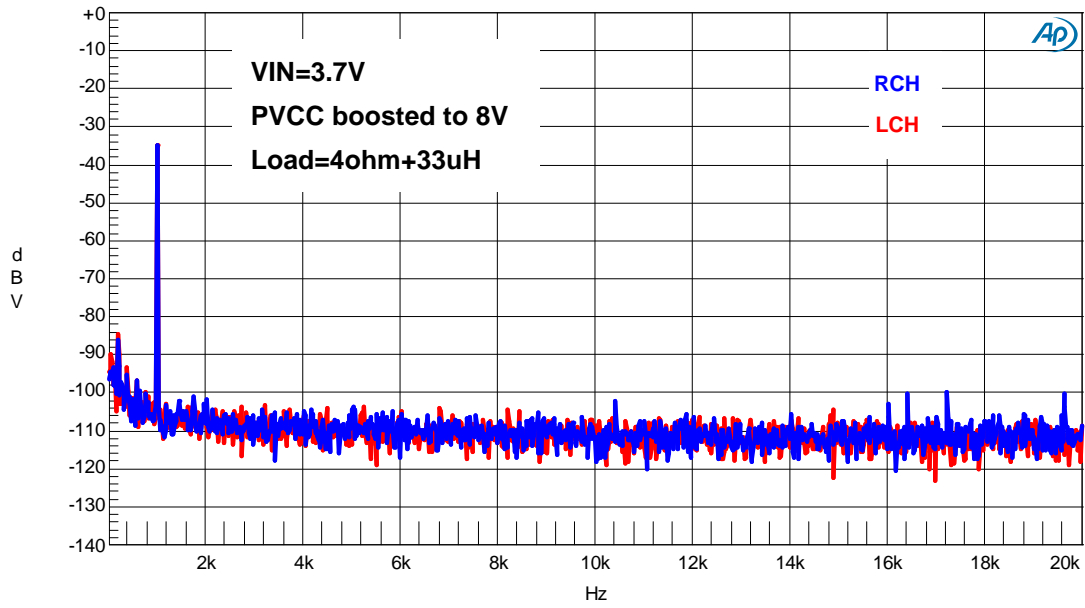
Crosstalk



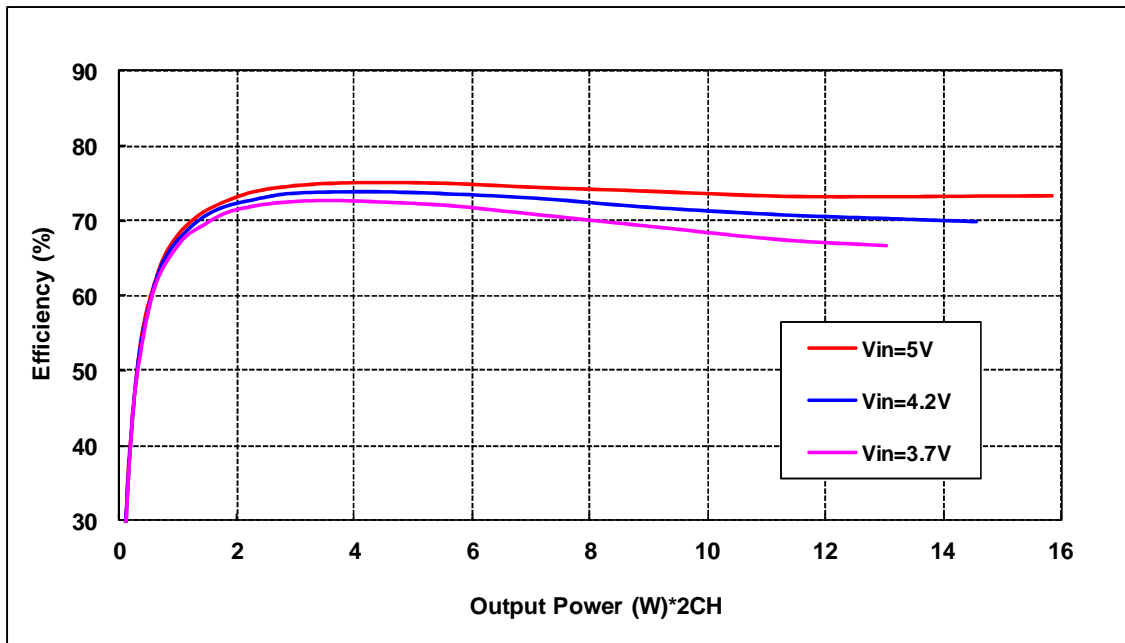
Noise



DR



Efficiency (4ohm+33uH load) / 2ch, PVCC boosted to 8V



Electrical Characteristics and Specifications of Loudspeaker Driver

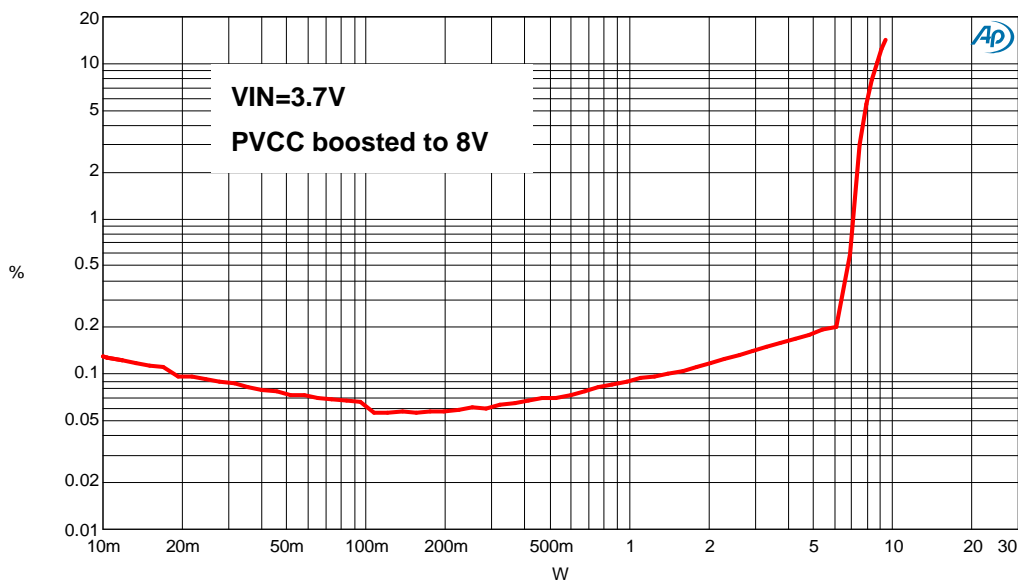
● Mono Output (PBTTL Output)

Condition: $V_{IN}=3.7V$, $PVCC$ boosted to 8V, $R_L=4\Omega+33\mu H$, Common mode filter= $15\mu H+2.2\mu F$, $T_A=25^\circ C$ (unless otherwise noted)

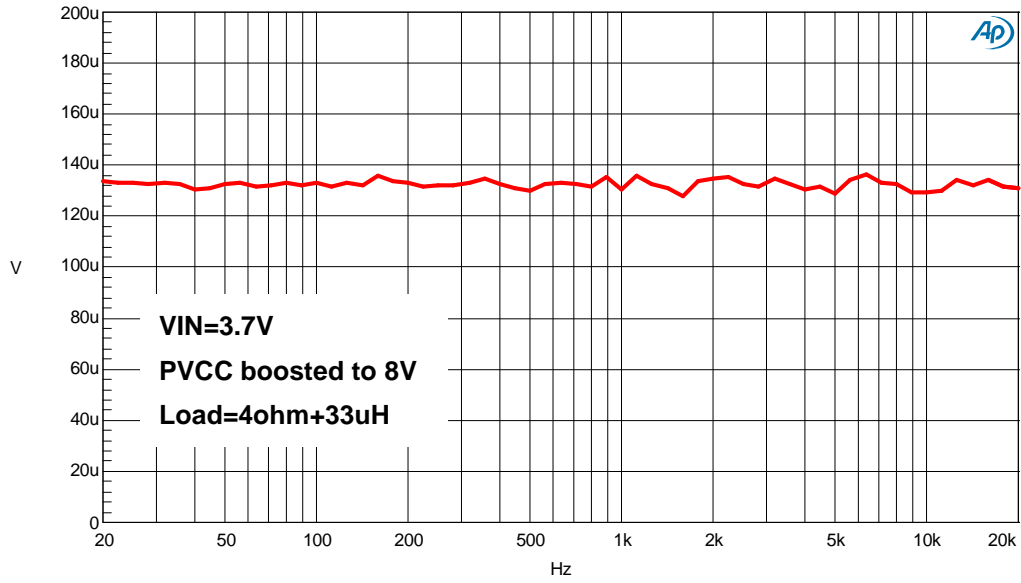
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power	THD+N=1%, f=1kHz, $PVCC=8V$		7		W
		THD+N=10%, f=1kHz, $PVCC=8V$		8.7		
THD+N	Total harmonic distortion plus noise	$PVCC=8V, f=1kHz, P_O=6W$		0.2		%
		$PVCC=8V, f=1kHz, P_O=3W$		0.15		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=20dB, a-weighted		91		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=20dB, a-weighted filter, $R_L=8\Omega$		131		μV
K_{SVR}	Power Supply Rejection Ratio	$V_{ripple}=200mV_{pp}$ at 1kHz, Gain=20dB, inputs ac-grounded		-70		dB
I_Q	Quiescent Current	$V_{IN}=4.2V, PVCC=8V$		30		mA
I_{SD}	Shutdown Current	$V_{IN}=4.2V, PVCC=8V$		45		μA

Note: P_o measurement is probed at the terminal on the EVB.

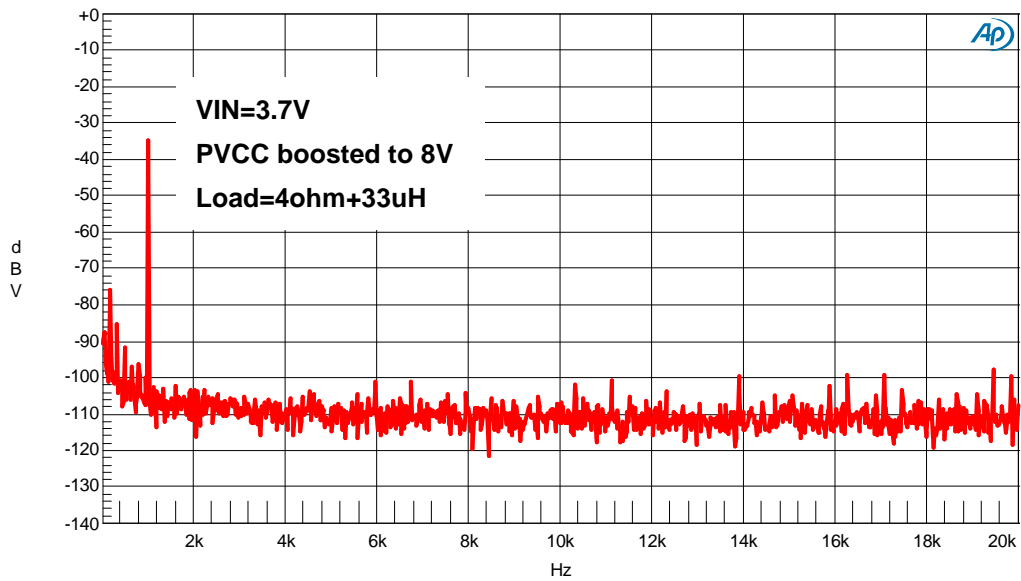
THD + N (%) vs. Output power (4ohm+33uH load)



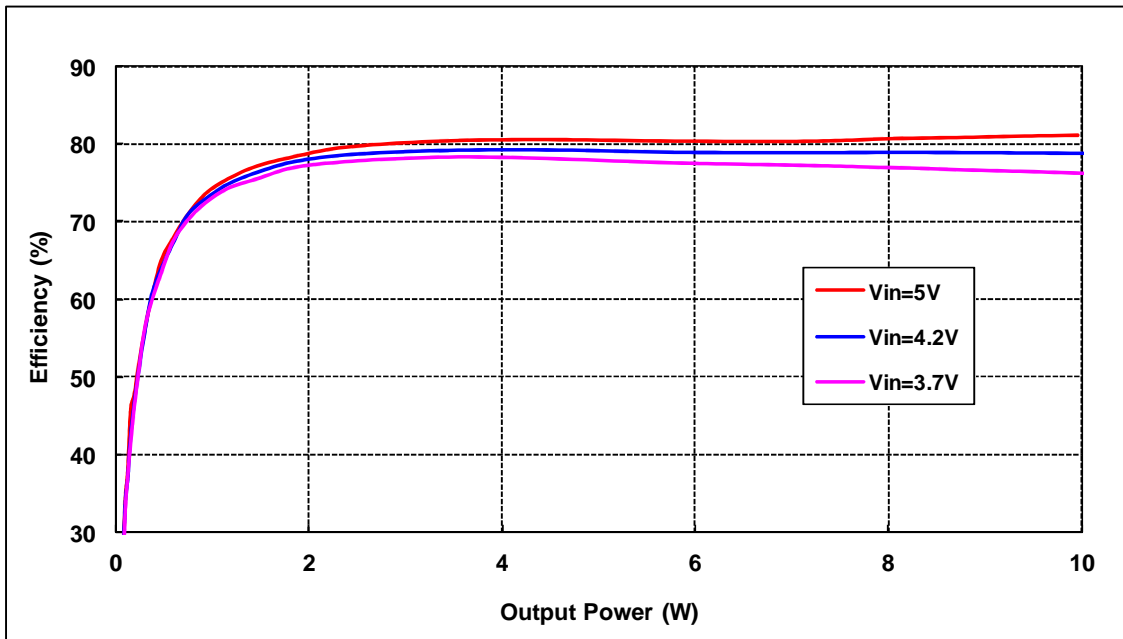
Noise



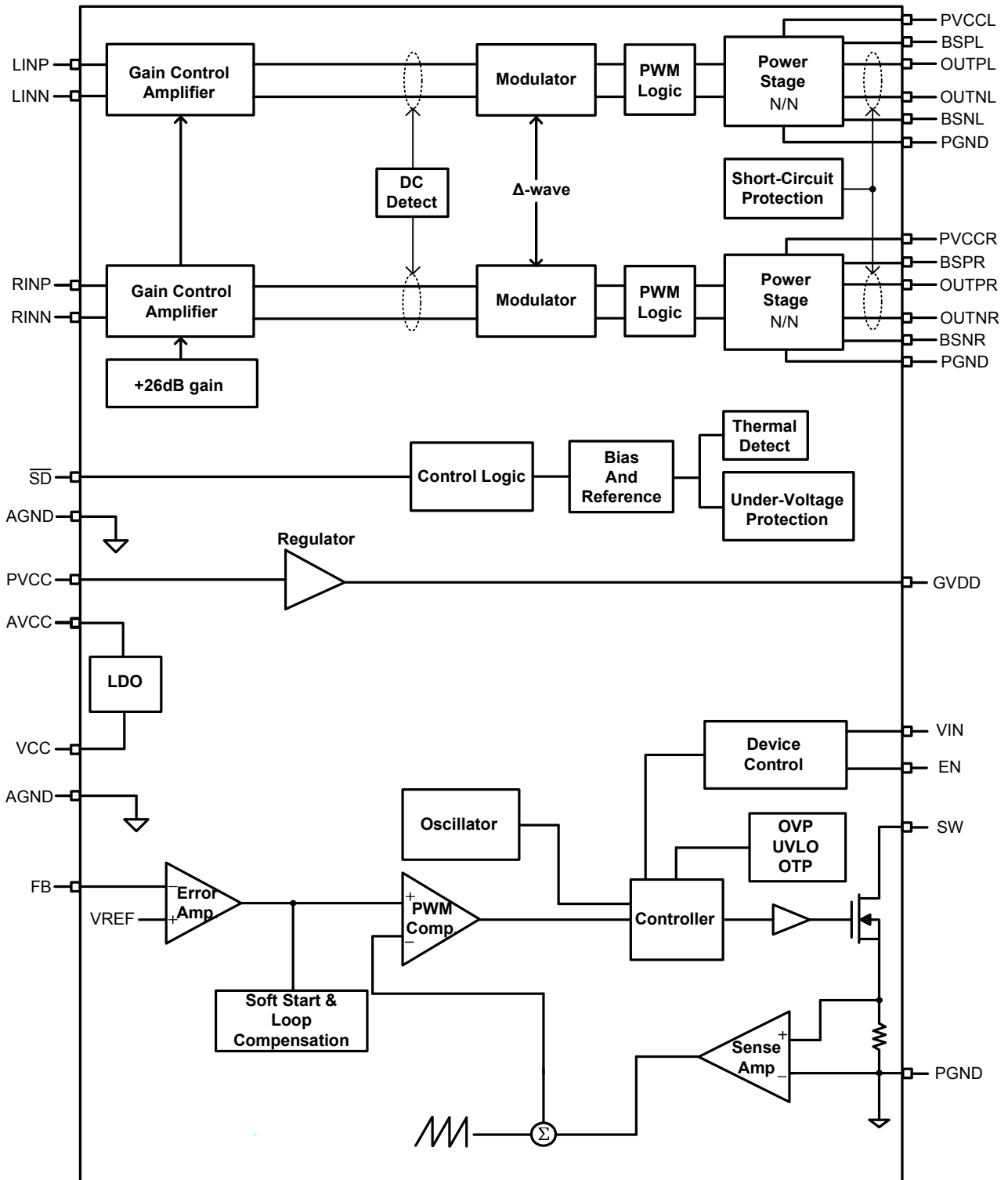
DR



Efficiency (4ohm+33uH load), PVCC boosted to 8V



Functional Block Diagram



Boost Converter Operation Description**● Detailed Description**

The AD52066B with a current mode boost converter. The constant switching frequency is 500kHz and operates with pulse width modulation (PWM). The control loop architecture is peak current mode control; therefore slope compensation circuit is added to the current signal to allow stable operation for duty cycles larger than 50%.

● Soft Start

Soft start circuitry is integrated into AD52066B to avoid inrush current during power on. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current.

● Over Temperature Protection

AD52066B will turn off the power MOSFET automatically when the internal junction temperature is over 160°C. The power MOSFET wake up when the junction temperature drops 30°C under the OTP threshold temperature.

● Over Voltage Protection

The AD52066B has output over-voltage protections. The thresholds output OVP circuit minimum 118% x V_{OUT}, respectively. Once the output voltage is higher than the threshold, the NMOS driver is turned off. When the output voltage drops lower than the threshold, the NMOS will be turned on again.

● Over Current Protection

The AD52066B cycle-by-cycle limits the peak inductor current to protect NMOS driver. The NMOS driver will turn off when switching current reaches OCP level.

Audio Operation Description

● **Gain settings**

The gain of the AD52066B is set by +26dB. The input resistance in AD52066B is listed in Table 1. However, there is 20% variation in input resistance from production variation.

Table 1. Volume gain and input impedance

Volume Gain (dB)	Input Resistance, R_{in} (k Ω)
26	30

● **Shutdown (\overline{SD}) control**

Pulling \overline{SD} pin low will let AD52066B operate in low-current state for power conservation. The AD52066B outputs will enter mute once \overline{SD} pin is pulled low, and regulator will also disable to save power. If let \overline{SD} pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

● **DC detection**

AD52066B has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to \overline{FAULT} pin. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. This fault can not be cleared by cycling \overline{SD} , it is necessary to cycle the PVCC supply.

The minimum differential input voltages required to trigger the DC detect function are shown in table2. The input voltage must keep above the voltage listed in the table for more than 420msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in table3.

Table 2. DC Detect Threshold

AV (dB)	Vin (mV, differential)
26	125

Table 3. Output DC Detect Duty (for Either Channel)

PVCC (V)	Output Duty Exceeds
8	20.8%
12	20.8%

- **Thermal protection**

If the internal junction temperature is higher than 150°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD52066B returning to normal operation is about 125°C. The variation of protected temperature is about 10%.

- **Short-circuit protection**

To protect loudspeaker drivers from over-current damage, AD52066B has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to PGND or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on $\overline{\text{FAULT}}$ pin as a low state. The latch can be cleared by reset $\overline{\text{SD}}$ or power supply cycling.

The short circuit protection latch can have auto-recovery function by connect the $\overline{\text{FAULT}}$ pin directly to $\overline{\text{SD}}$ pin. The latch state will be released after 420msec, and the short protection latch will re-cycle if output overload is detected again.

- **Under-voltage detection**

When the PVCC voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD52066B return to normal operation.

- **PBTL (Mono) function**

AD52066B provides the application of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin is tied high, the positive and negative outputs of left and right channel are synchronized and in phase. Apply the input signal to the RIGHT channel input in PBTL mode and let the LEFT channel input grounded, and place the speaker between the LEFT and RIGHT outputs. The output swing is doubled of that in normal mode. See the application circuit example for PBTL (Mono) mode operation. For normal BTL (Stereo) operation, connect the PBTL pin to ground.

Boost Converter Application information

● Inductor Selection

Inductance value is decided based on different condition. 3.3uH to 6.8uH inductor value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency.

● Capacitor Selection

The output capacitor is required to maintain the DC voltage. Low ESR capacitors are preferred to reduce the output voltage ripple. Ceramic capacitor of X5R and X7R are recommended, which have low equivalent series resistance (ESR) and wider operation temperature range.

● Diode Selection

Schottky diodes with fast recovery times and low forward voltages are recommended. Ensure the diode average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the output voltage.

● Output Voltage Setting

The output voltage of AD52066B can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} * \left(1 + \frac{R_1}{R_2}\right) = 0.6 * \left(1 + \frac{R_1}{R_2}\right)$$

The resistive divider senses the fraction of the output voltage as shown in Figure.1 Using large feedback resistor can increase efficiency, but too large value affects the device's output accuracy because of leakage current going into device's FB pin. The recommended value for R2 is therefore in the range of 10~20KΩ.

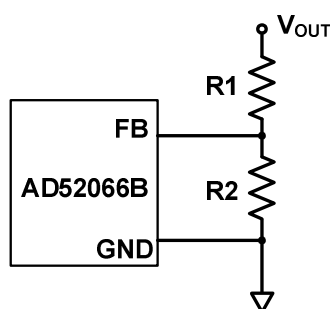


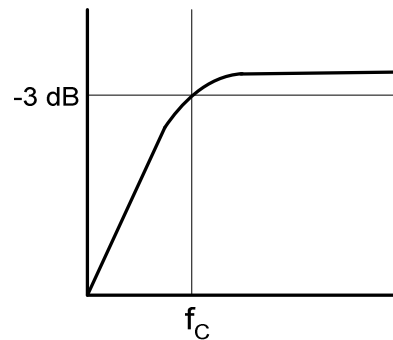
Figure.1 The resistive divider senses the fraction of the output voltage

Audio Application information

● **Input capacitors (C_{in})**

The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{in}. The resistance of input resistors is different at different gain setting. The respective gain and input resistance are listed in Table 1 (shown at GAIN SETTING). However, there is 20% variation in input resistance from production variation.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \text{ (Hz) } \dots\dots\dots (2)$$



● **Ferrite Bead selection**

If the traces from the AD52066B to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

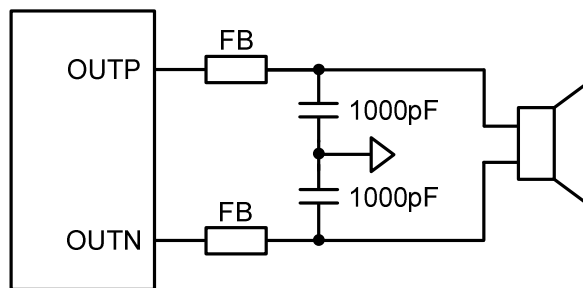


Figure 2. Typical Ferrite Bead Filter

● **Output LC Filter**

If the traces from the AD52066B to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 3 shows the typical output filter for 8Ω speaker with a cut-off frequency of 27 kHz and Figure 4 shows the typical output filter for 4Ω speaker with a cut-off frequency of 27 kHz.

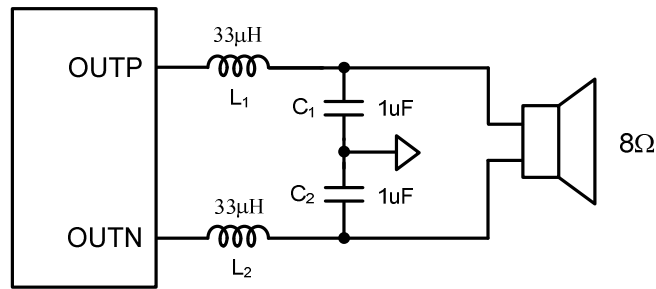


Figure 3. Typical LC Output Filter for 8Ω Speaker

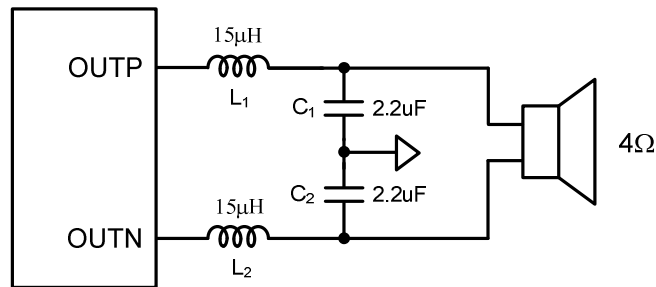


Figure 4. Typical LC Output Filter for 4Ω Speaker

● **Power supply decoupling capacitor (Cs)**

Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1μF or 1μF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100μF or greater capacitor (tantalum or electrolytic type) is suggested.

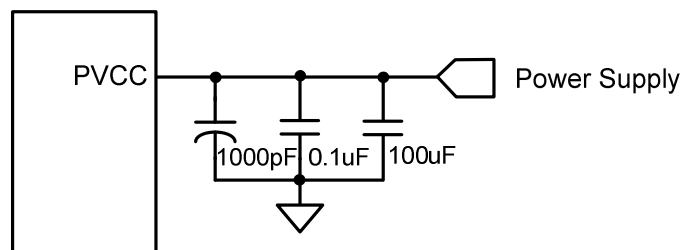
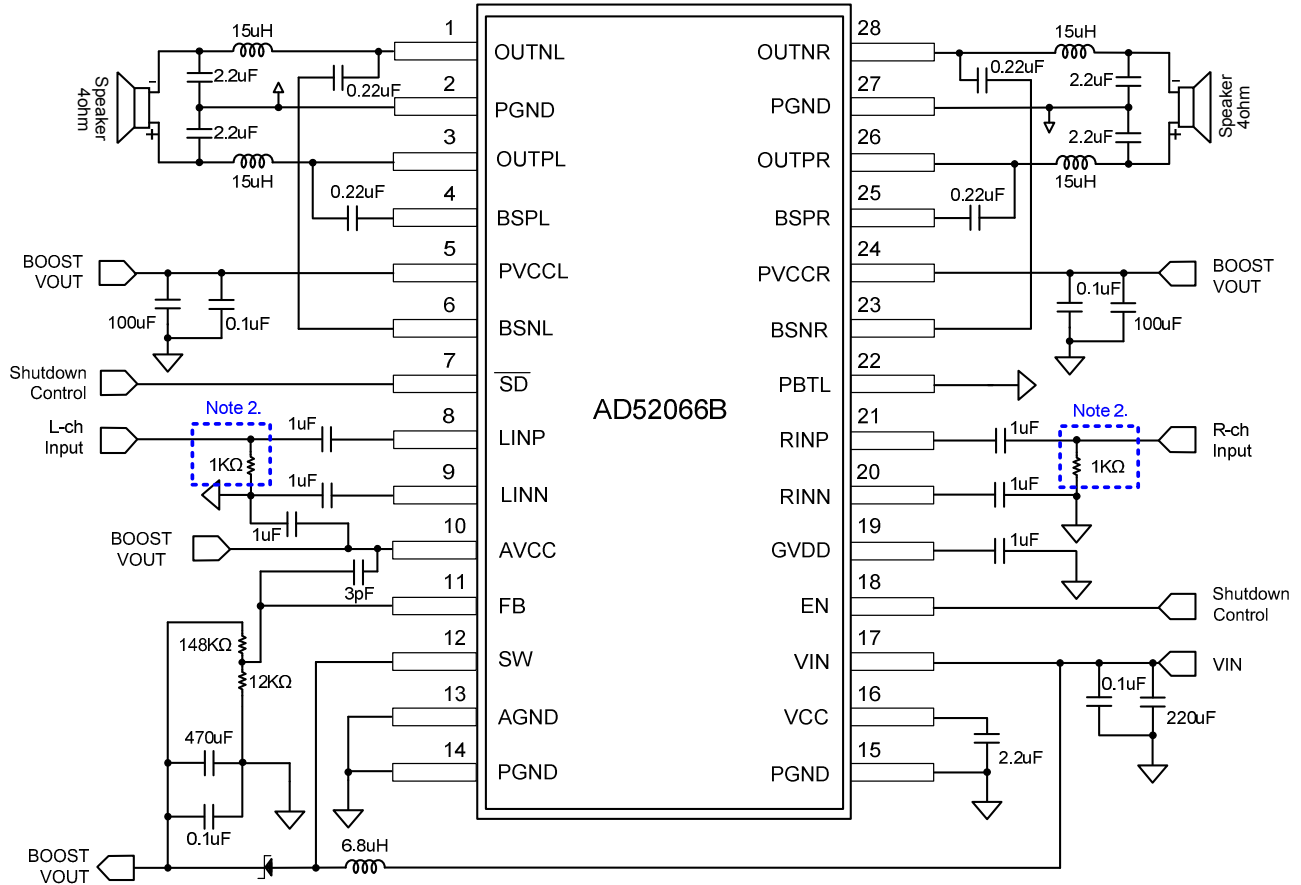


Figure 5. Recommended Power Supply Decoupling Capacitors.

Application Circuit Example

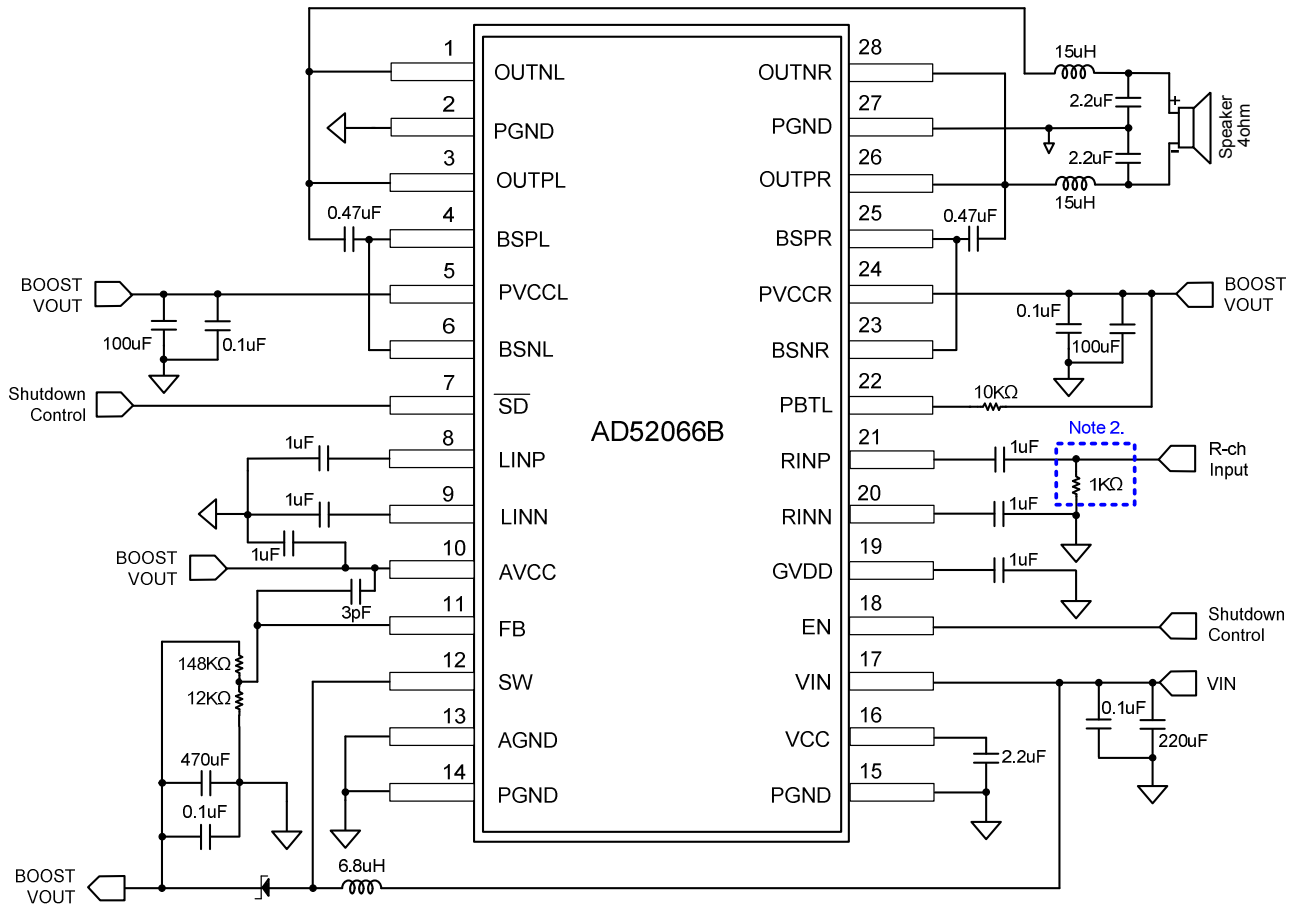
- Application circuit for Stereo (BTL) mode configuration and Single-Ended Input



Note 2: These resistances must be connected to ground, resistance=1Kohm.

Application Circuit Example

- Application circuit for Mono (parallel BTL) mode configuration and Single-Ended Input

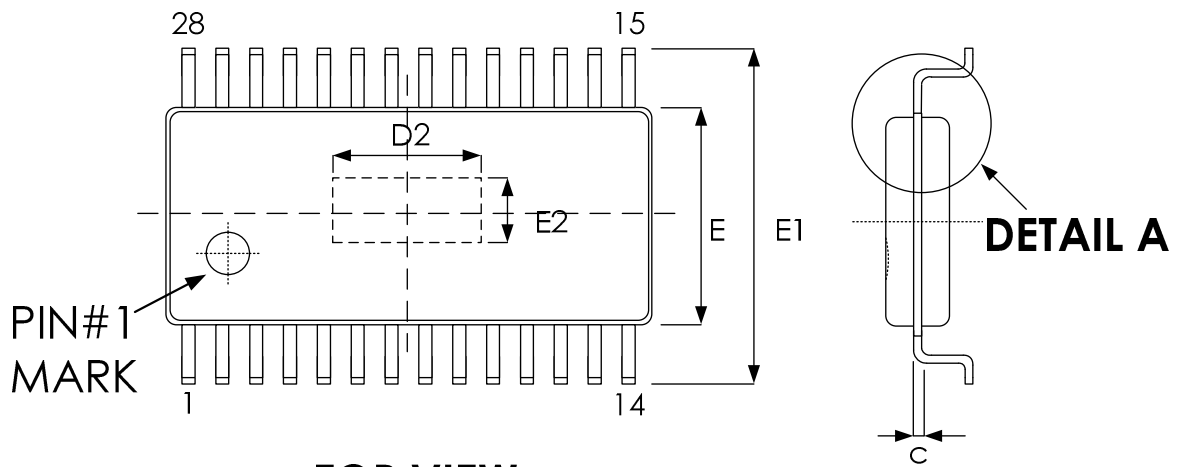


Note 2: These resistances must be connected to ground, resistance=1Kohm.

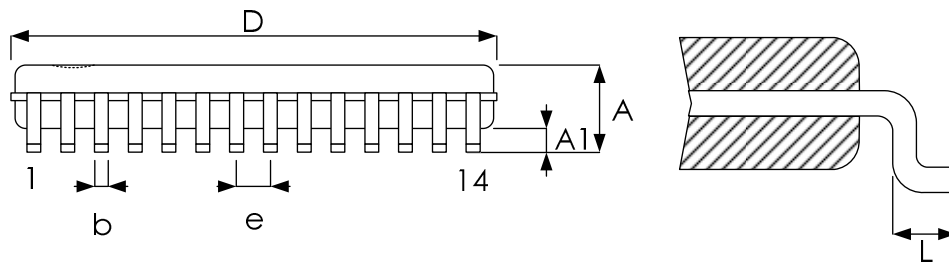
Note 3: Be noted that input should be applied on R-channel only for Mono application.

Package Dimensions

● E-TSSOP 28L



TOP VIEW



SIDE VIEW

Symbol	Dimension in mm	
	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

Option 1	Dimension in mm	
	Min	Max
D2	4.75	5.25
E2	2.56	2.97

Revision History

Revision	Date	Description
0.01	2017.03.14	Draft version.
0.02	2017.03.15	Draft version, electrical characteristic update.
0.03	2017.03.22	Draft version, electrical characteristic update.

Important Notice

All rights reserved.

No part of this document may be reproduced or duplicated in any form or by any means without the prior permission of ESMT.

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.