2x30W Stereo / 1x60W Mono Class-D Audio Amplifier With Low Idle Current and AGC

Features

- Single supply voltage
  4.5V ~ 26V for loudspeaker driver
  Built-in LDO output 5V for others
- Supports Multiple Output Configurations
  BTL Mode: 30W/CH into 8Ω at 24 V
  BTL Mode: 30W/CH into 4Ω at 18 V
  PBTL Mode: 60W/CH into 4Ω at 24 V
  PBTL Mode: 45W/CH into 4Ω at 18 V
  PBTL Mode: 60W/CH into 2Ω at 18 V
- Loudspeaker performance
  BTL Mode: 30W/CH into 8Ω <1% THD+N@24V
  BTL Mode: 30W/CH into 4Ω <1% THD+N@18V
- >90% efficient Class-D operation eliminates need for heat sink
- Energy Saving Class-D Operation
  Low Idle Current <23mA
- Multiple Switching Frequencies
  AM Avoidance
  Master/Slave Synchronization
  300KHz to 1.2MHz Switching Frequency
- Differential inputs
- Four selectable, fixed gain settings
- Internal oscillator
- Short-Circuit protection with auto recovery
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Adjustable Automatic Gain Control or adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Thermal fold-back control
- Over temperature protection with auto recovery

Applications

- TV audio
- Boom-Box
- Powered speaker
- Monitors
- Consumer Audio Equipment

Description

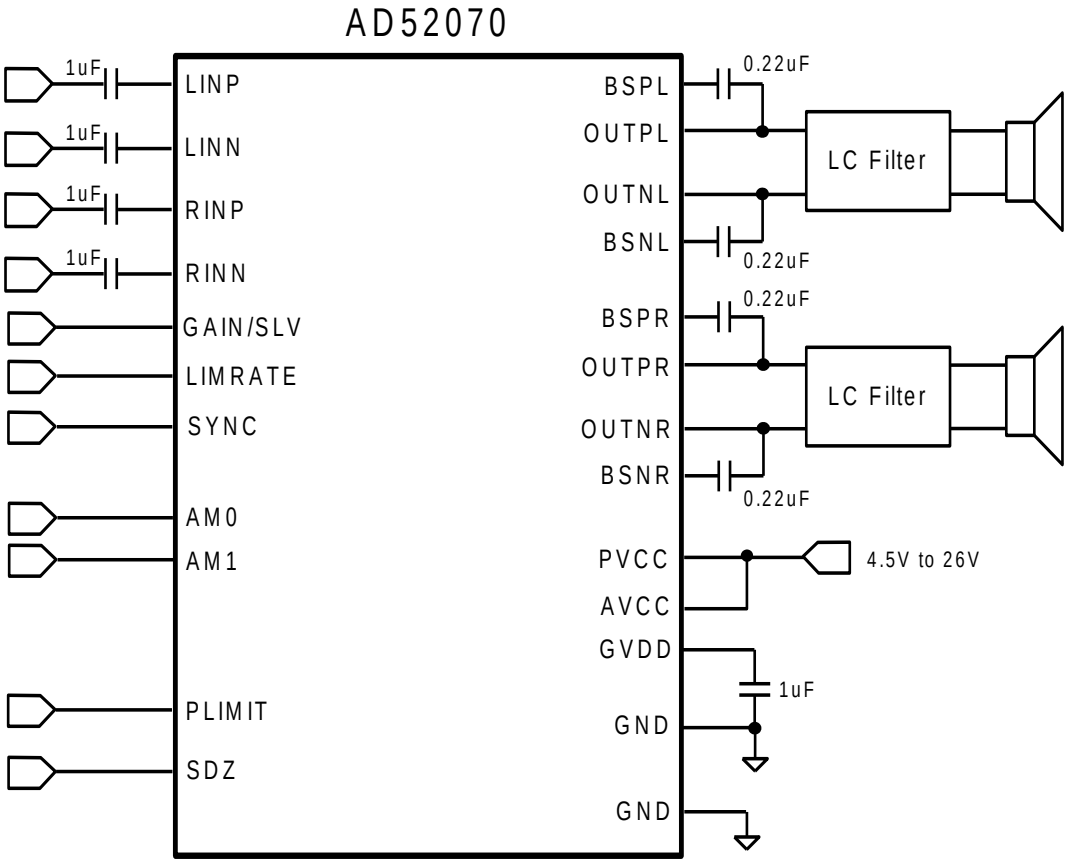
The AD52070 is a high efficiency stereo class-D audio amplifier with adjustable power limit function. It can deliver 30W/CH output power into 4Ω or 8Ω loudspeaker within 1% THD+N at 24V supply voltage. AD52070 also provides parallel BTL (Mono) application, and it can deliver 60W into 4Ω loudspeaker at 24V supply voltage.

The AD52070 has low idle current mode for battery-powered audio system and helps to extend the battery life. The advanced oscillator/PLL circuit employs a multiple switching frequency option to avoid AM interferences. In order to achieve multi-channels application, which the clock slave mode design with, making it possible to synchronize multiple devices.

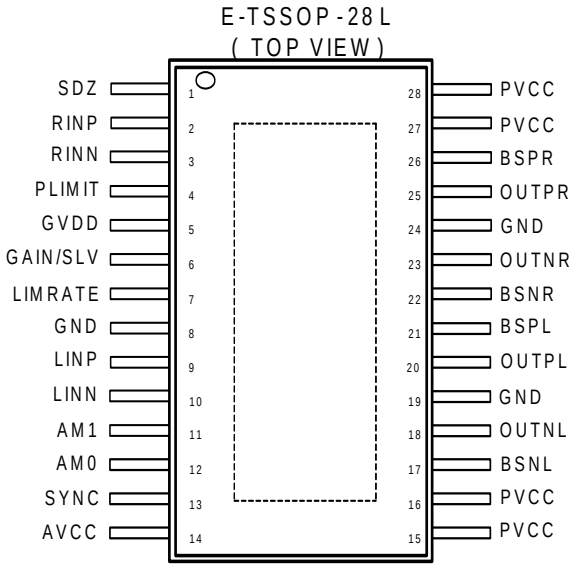
The Automatic Gain Control (AGC) is enabled to prevent output signal from distortion when the input signal exceeds a threshold level. The AGC allows adjustment of maximum output voltage without signal clipping for enhanced speaker protection and audio quality. The power-limit control can provide further limit output power level of amplifier. The adjustable power limit function allows user to set a voltage to limit the amount of current through the speaker. All these functions are performed automatically.

Output DC detection prevents speaker damage from long-time current stress. AD52070 output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments



Pin Description

NAME	E-TSSOP -28L	TYP	DESCRIPTION
SDZ	1	DI	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC. Chip is with internal pull low, 250kohm@normal state, <250ohm@ fault state.
RINP	2	AI	Positive audio input for right channel. Connect to GND for MONO mode.
RINN	3	AI	Negative audio input for right channel. Connect to GND for MONO mode.
PLIMIT	4	AI	Voltage level for AGC or power limiter. Connect a resistor divider from GVDD to GND to set AGC or power limit level. Give $V_{PLIMIT} \leqq 2.1V$ to set AGC or power limit level. Connect to GND to disable AGC or power limit function, and chip will into mute function when connect to GVDD ($\geqq$ 2.4V).
GVDD	5	P	5V regulated output, with a 1uF X7R (or X5R) ceramic decoupling capacitor is necessary. Not to be used as a supply or connected to any components other than the PLIMIT and GAIN/SLV resistor dividers.
GAIN/SLV	6	AI	Selects gain depending on pin voltage divider.
LIMRATE	7	AI	Decay speed for clip free for AGC or power limiter. Connect a resistor divider from GVDD to GND to set decay speed. Connect directly to GND to enable power limit function.
GND	8	P	Power ground. Connect to the thermal pad.
LINP	9	AI	Positive audio input for left channel. Connect to GND for PBTL mode.
LINN	10	AI	Negative audio input for left channel. Connect to GND for PBTL mode.
AM1	11	DI	AM avoidance frequency selection 1. Chip is with internal pull low, 250kohm.

AM0	12	DI	AM avoidance frequency selection 0. Chip is with internal pull low, 250kohm.
SYNC	13	DIO	Clock input/output for synchronizing multiple class-D devices. Direction determined by GAIN/SLV terminal. Chip is at output mode @Master mode; Input mode (HiZ) @Slave mode.
AVCC	14	P	Analog supply.
PVCC	15,16	P	High-voltage power supply.
BSNL	17	BST	Bootstrap I/O for left channel, negative high side FET.
OUTNL	18	O	Class-D H-bridge negative output for left channel.
GND	19	P	Power ground. Connect to the thermal pad.
OUTPL	20	O	Class-D H-bridge positive output for left channel.
BSPL	21	BST	Bootstrap I/O for left channel, positive high side FET.
BSNR	22	BST	Bootstrap I/O for right channel, negative high side FET.
OUTNR	23	O	Class-D H-bridge negative output for right channel.
GND	24	P	Power ground. Connect to the thermal pad.
OUTPR	25	O	Class-D H-bridge positive output for right channel.
BSPR	26	BST	Bootstrap I/O for right channel, positive high side FET.
PVCC	27,28	P	High-voltage power supply.
Thermal Pad		P	Must be soldered to PCB's ground plane.

AI = Analog input; AO = Analog output; AI/O = Analog Bi-directional (input and output); DI = Digital Input; DO = Digital Output; DI/O = Digital Bi-directional (input and output); P = Power or Ground; BST = Boot Strap

Ordering Information

Product ID	Package	Packing	Comments
AD52070-QG28NRR	E-TSSOP 28L	2500 Units / Reel 1 Reels / Small Box	Green

Available Package

Package Type	Device No.	θ_{JA}(℃/W)	θ_{JT}(℃/W)	Ψ_{JT}(℃/W)	Exposed Thermal Pad
E-TSSOP 28L	AD52070	28	27.1	1.33	Yes (Note 1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.

Note 1.2: θ_{JA} is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{JT} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

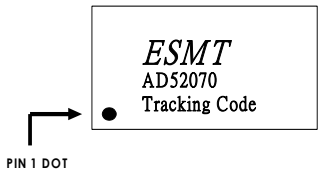
Note 1.4: Ψ_{JT} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{JA}, using a procedure described in JESD51-5.

Marking Information

AD52070

- Marking Information

Line 1：LOGO
Line 2：Product No
Line 3：Tracking Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCC and AVCC	-0.3	30	V
V_I	Interface pin voltage	SDZ, AM0 and AM1	-0.3	30	V
		PLIMIT, GAIN/SLV, SYNC and LIMRATE	-0.3	5.5	
T_A	Operating free-air temperature range		-40	85	°C
T_J	Operating junction temperature range		-40	150	°C
T_{stg}	Storage temperature range		-65	150	°C
R_L	Minimum Load Resistance	BTL (Stereo, Mono)	3.2		Ω
		PBTL ＞ 18V	3.2		Ω
		PBTL ≦ 18V	1.6		Ω
ESD	Human Body Model			±2k	V
	Charged Device Model			±500	

Recommended Operating Conditions

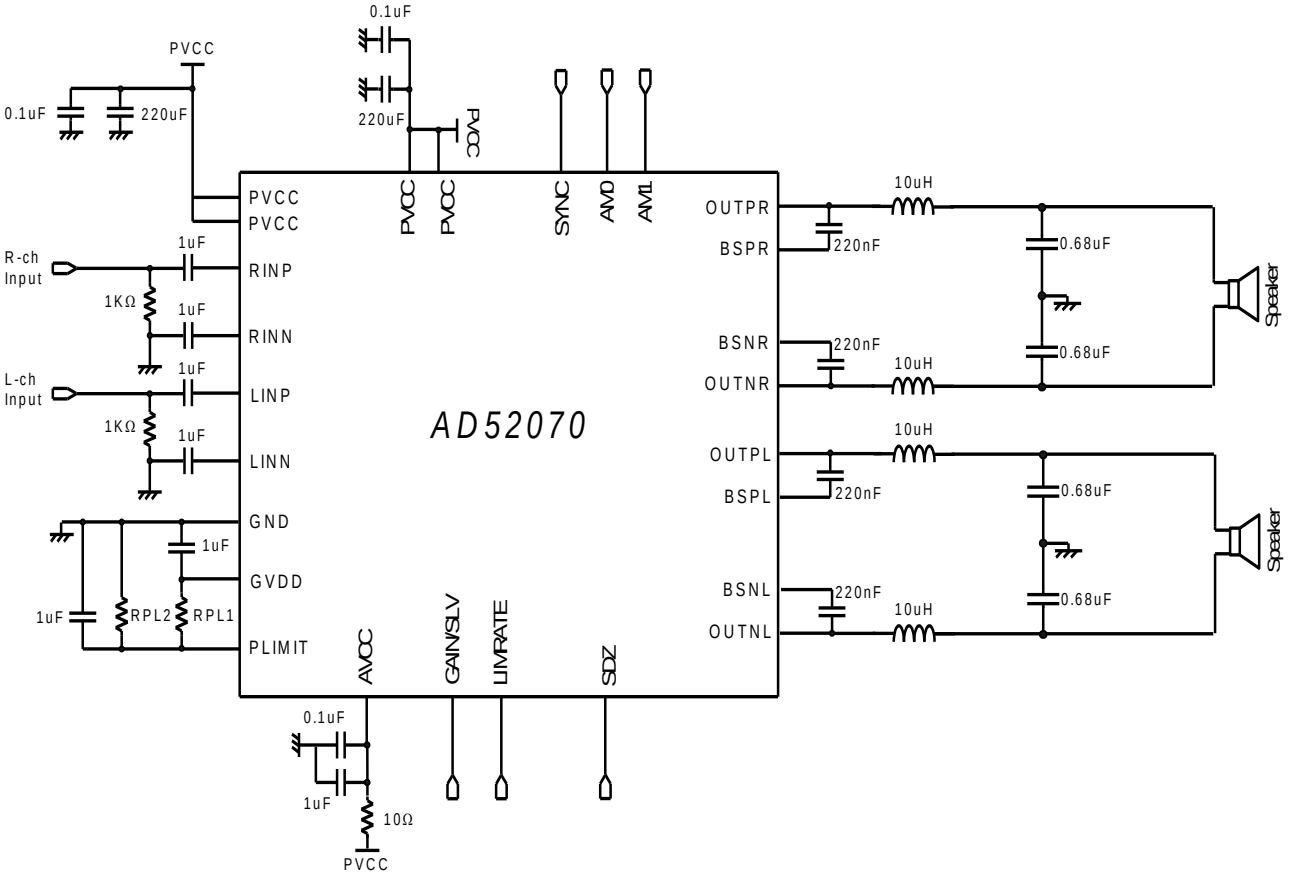
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCC and AVCC	4.5	26	V
V_{IH}	High-level input voltage	SDZ, AM0, AM1 and SYNC	2		V
V_{IL}	Low-level input voltage	SDZ, AM0, AM1 and SYNC		0.8	V
I_{IH}	High-level input current	SDZ, AM0, AM1, SYNC, V_I=2V, PVCC=18V		50	uA
I_{IL}	Low-level input current	SDZ, AM0, AM1, SYNC, V_I=0.8V, PVCC=18V		5	uA
T_A	Operating free-air		-40	85	°C

General Electrical Characteristics

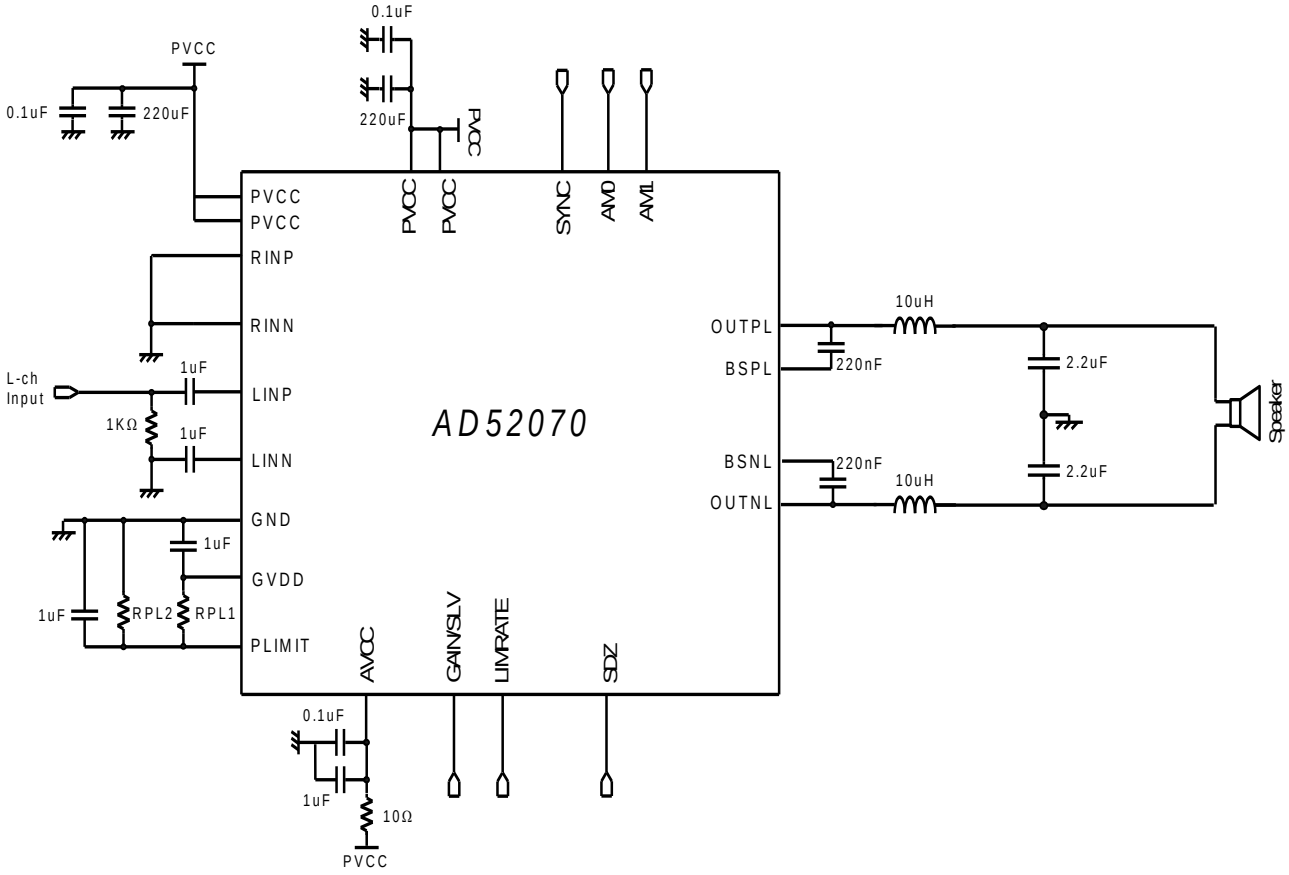
- PVCC=24V, R_L=8Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$I_{CC(q)}$	Quiescent supply current	SDZ=2V, PWM=400KHz, With load and filter, PVCC=12V		17		mA
		SDZ=2V, PWM=400KHz, With load and filter, PVCC=24V		23		
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDZ=0.8V, no load, PVCC=12V		20		uA
		SDZ=0.8V, no load, PVCC=24V		30		
$R_{DS(on)}$	Drain-source on-state resistance-High side NMOS	PVCC=12V, Id=500mA, T_J=25°C		90		mΩ
	Drain-source on-state resistance-Low side NMOS			90		
$\|V_{OS}\|$	Class-D output offset voltage (measured differential)	PVCC=12V VI=0V, Gain=36dB		1.5	15	mV
t_{ON}	Turn-on time	SDZ=2V		10		ms
t_{OFF}	Turn-off time	SDZ=0.8V		10		
GVDD	Regulator output	I_{GVDD}=0.1mA	4.75	5	5.25	V
G	Gain (Master)	R1=5.6kΩ, R2=Open	19	20	21	dB
		R1=20kΩ, R2=100kΩ	25	26	27	
		R1=39kΩ, R2=100kΩ	31	32	33	
		R1=47kΩ, R2=75kΩ	35	36	37	
	Gain (Slave)	R1=51kΩ, R2=51kΩ	19	20	21	dB
		R1=75kΩ, R2=47kΩ	25	26	27	
		R1=100kΩ, R2=39kΩ	31	32	33	
		R1=100kΩ, R2=16kΩ	35	36	37	

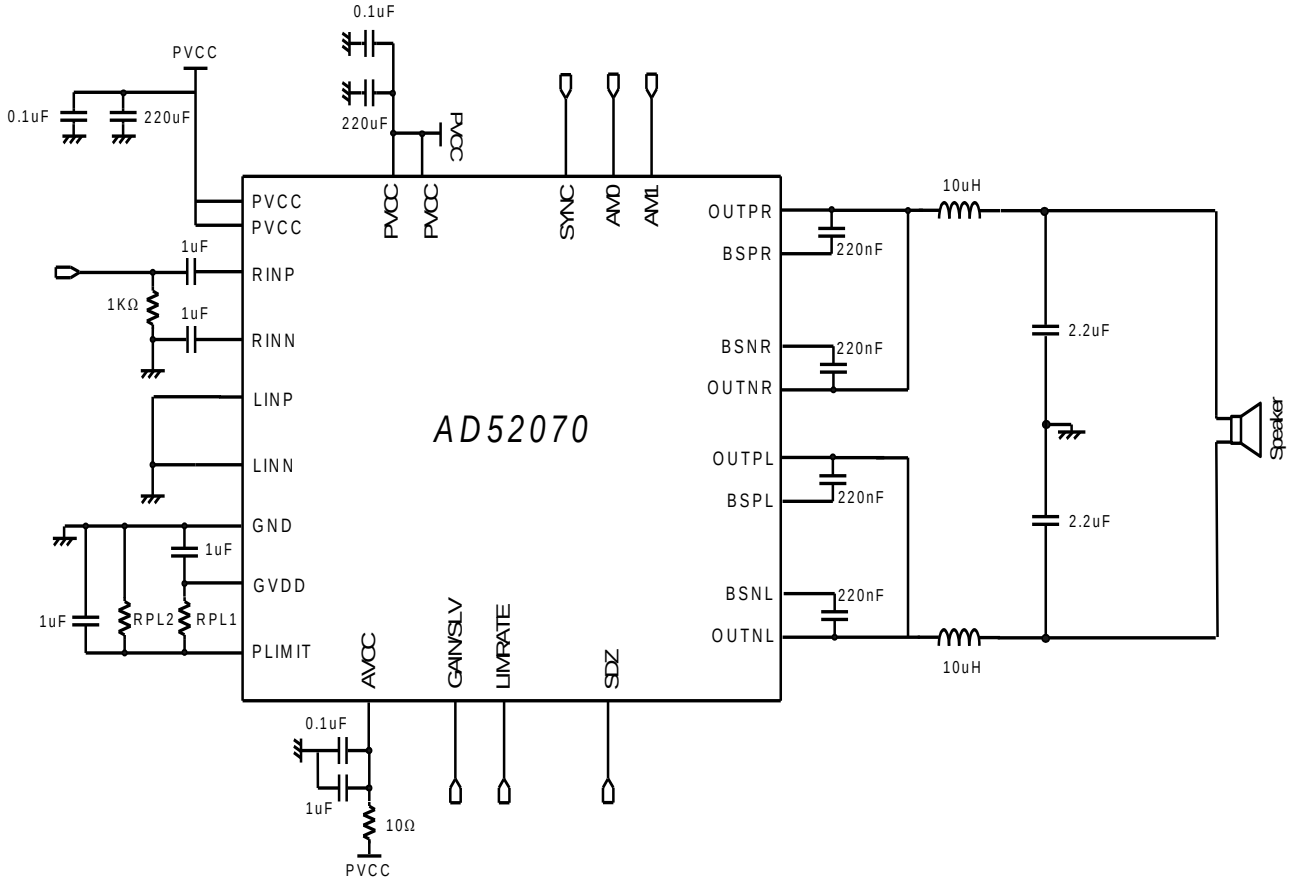
Application Circuit Example for Stereo



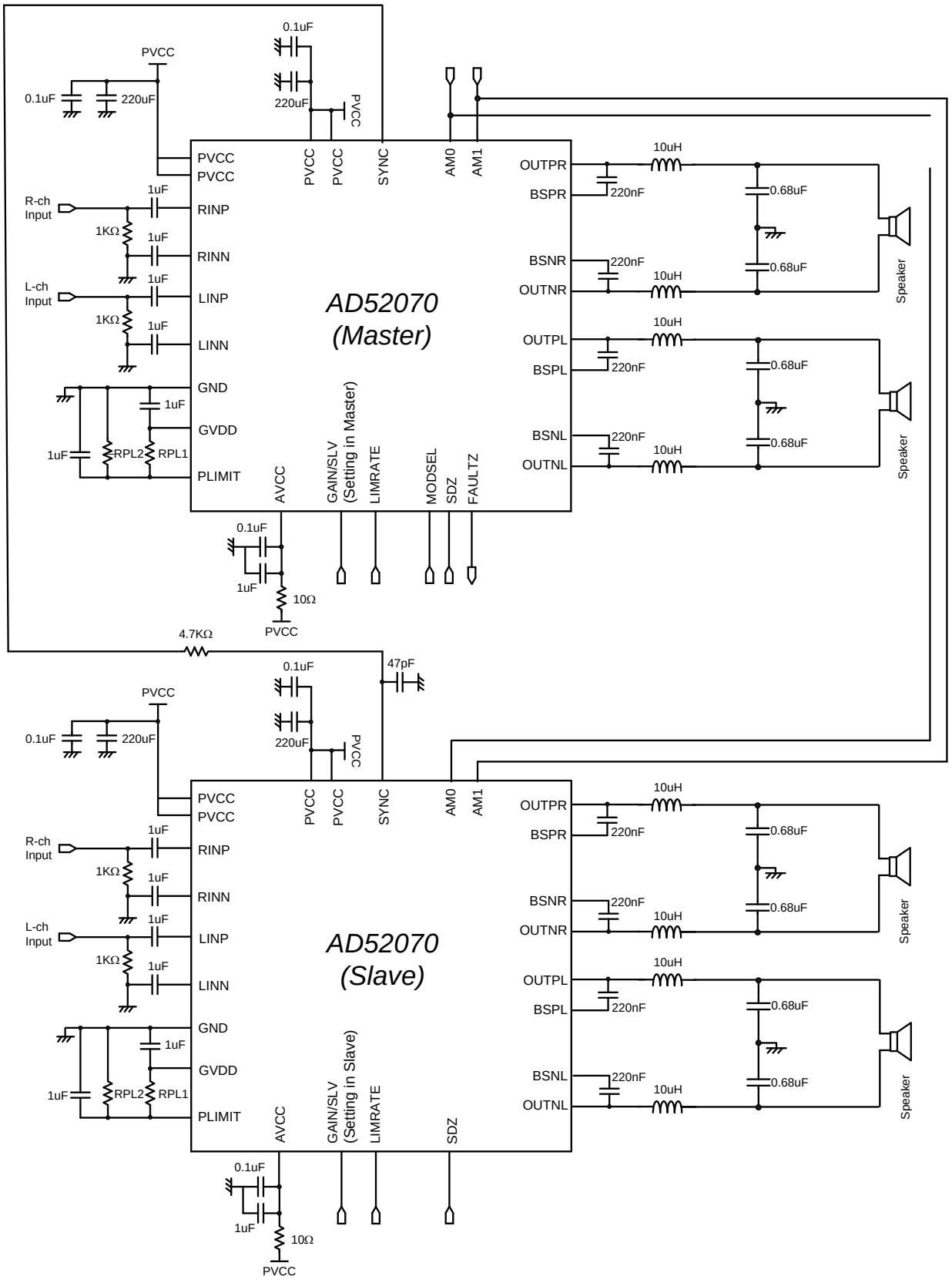
Application Circuit Example for Mono Mode



Application Circuit Example for PBTL Mode



Application Circuit Example for Clock Synchronization (multiple devices)



Electrical Characteristics and Specifications of Loudspeaker Driver

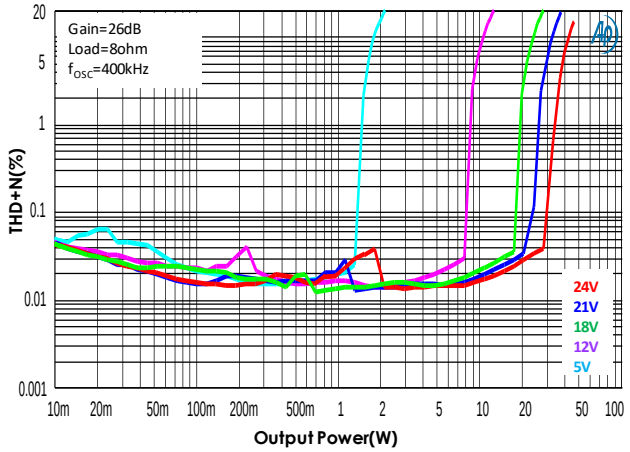
- PVCC=24V, R_L=8Ω with passive LC low-pass filter in ESMT EVB, f_{osc}=400kHz (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power (BTL)	THD+N=0.3%, f=1kHz, PVCC=24V		30		W
		THD+N=10%, f=1kHz, PVCC=12V		10		
		THD+N=0.35%, f=1kHz, VCC=21V, 4ohm		30		
		THD+N=0.95%, f=1kHz, VCC=18V, 4ohm		30		
		THD+N=10%, f=1kHz, PVCC=12V, 4ohm		19		
		THD+N=10%, f=1kHz, PVCC=8V, 4ohm		8.5		
	Output power (PBTL)	THD+N=0.27%, f=1kHz, PVCC=24V, 4ohm		60		
		THD+N=10%, f=1kHz, PVCC=18V, 4ohm		45		
		THD+N=0.5%, f=1kHz, PVCC=18V, 2ohm		60		
THD+N	Total harmonic distortion plus noise	PVCC=24V, R_L=8Ω, f=1kHz, P_O=15W (half-power)		0.02		%
		PVCC=12V, R_L=8Ω, f=1kHz, P_O=5W (half-power)		0.02		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=20dB, a-weighted		103		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=20dB, a-weighted filter, R_L=8Ω		65		uV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=20dB, inputs ac-grounded		-70		dB
X-talk	Crosstalk	F=1kHz, P_O=1W, Gain=20dB		-80		dB
$T_{AGC,AT}$	AGC Attack Time	LIMRATE=GVDD (FAST)		0.32		ms/dB
		LIMRATE=2/3*GVDD (MEDIUM)		2.56		
		LIMRATE=1/3*GVDD (SLOW)		5.12		
$T_{TFB,AT}$	TFB Attack Time	LIMRATE=GVDD (FAST)		164		
		LIMRATE=2/3*GVDD (MEDIUM)		326		
		LIMRATE=1/3*GVDD (SLOW)		655		
T_{RLS}	AGC/TFB Release Time	LIMRATE=GVDD (FAST)		328		
		LIMRATE=2/3*GVDD (MEDIUM)		655		
		LIMRATE=1/3*GVDD (SLOW)		1311		
f_{OSC}	Oscillator frequency	AM1=0, AM0=0 (Low idle current mode)	376	400	424	kHz
		AM1=0, AM0=1 (Low idle current mode)	470	500	530	

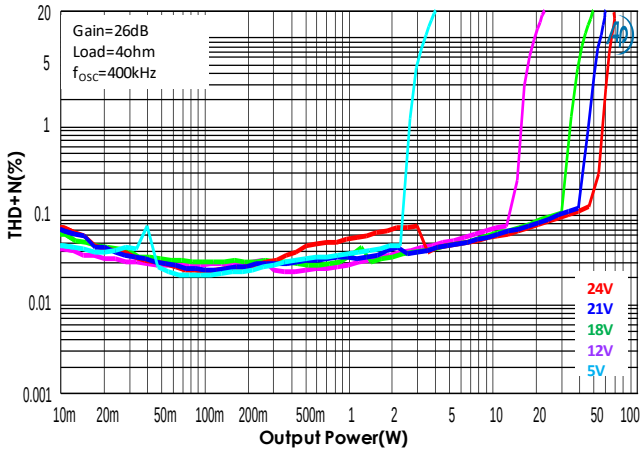
		AM1=1, AM0=0 (Pure quaternary mode)	1128	1200	1272	
		AM1=1, AM0=1 (Pure ternary mode)	282	300	318	
TFB	Thermal Fold-back trip point			150		^{o}C
T_{SENSOR}	Thermal trip point for over temperature			170		^{o}C
	Thermal hysteresis			35		^{o}C

Typical Characteristics

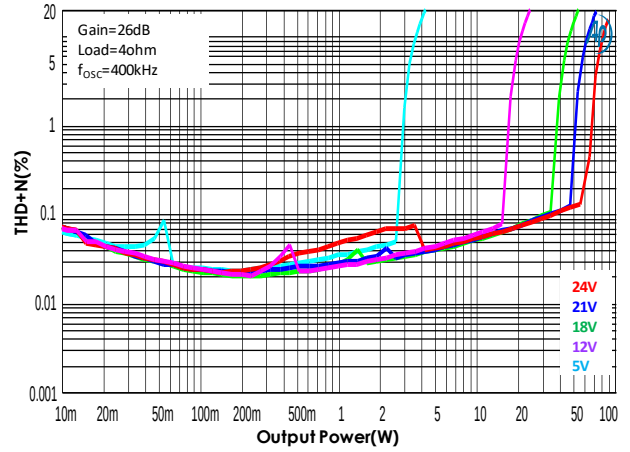
THD+N vs. Output Power, 8Ω load (BTL)



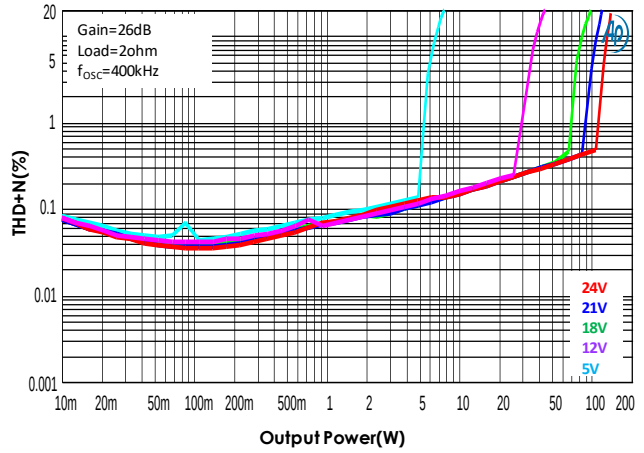
THD+N vs. Output Power, 4Ω load (BTL)



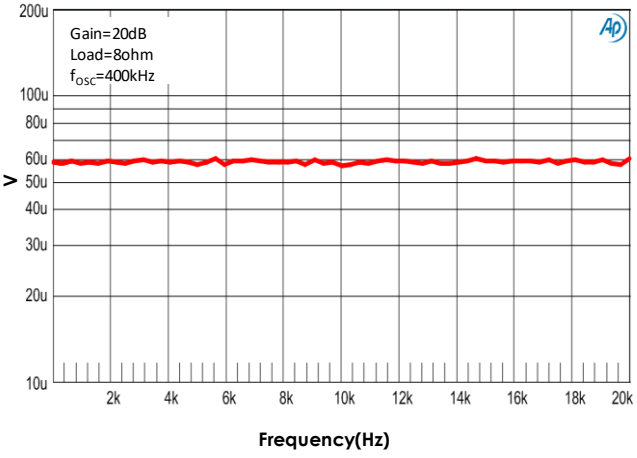
THD+N vs. Output Power, 4Ω load (PBTL)



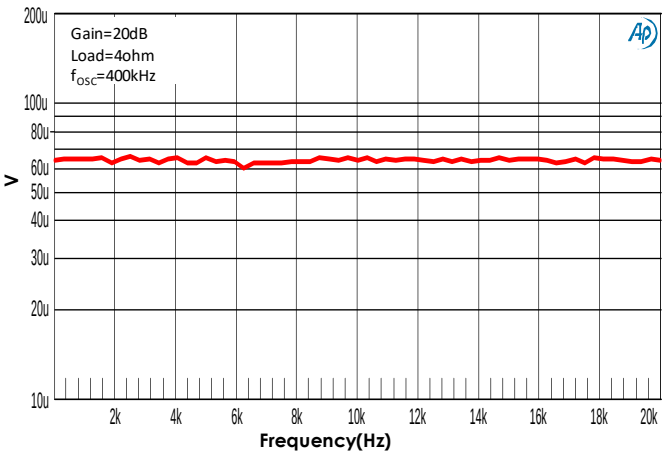
THD+N vs. Output Power, 2Ω load (PBTL)



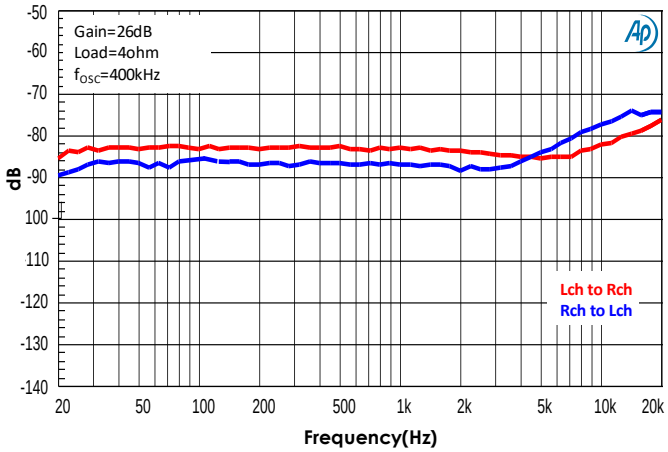
Noise, 24V, 8Ω load (BTL)



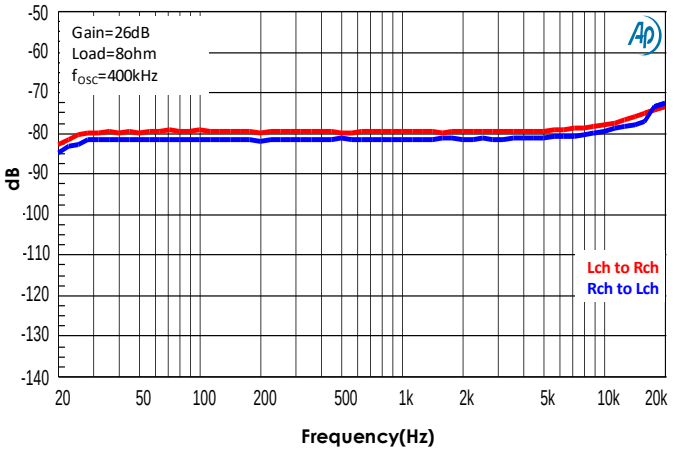
Noise, 24V, 4Ω load (PBTL)



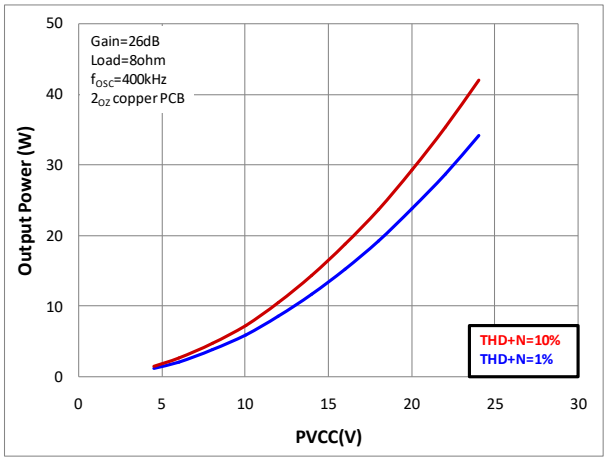
Crosstalk, 24V, 4Ω load (BTL)



Crosstalk, 24V, 8Ω load (BTL)



Maximum Output Power vs Supply Voltage (BTL)



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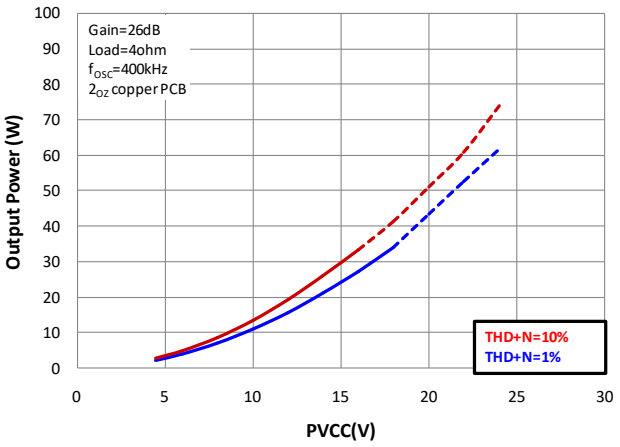
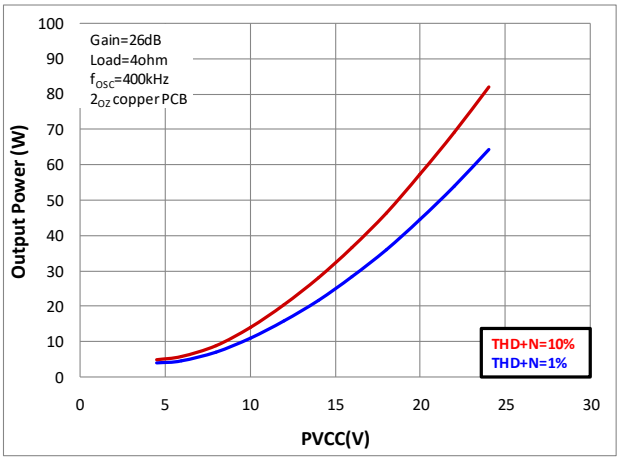
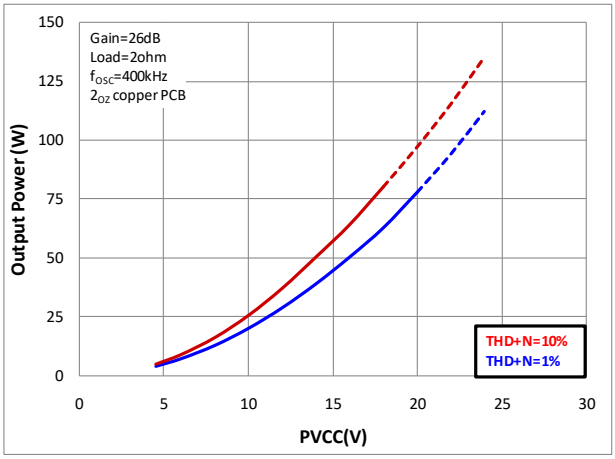


Maximum Output Power vs Supply Voltage (PBTL)

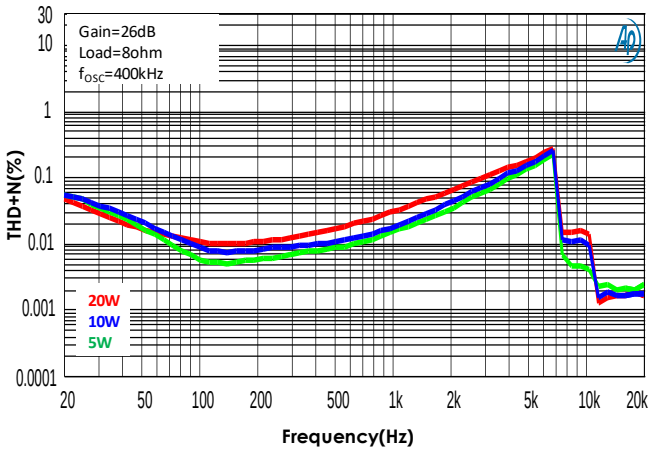


Maximum Output Power vs Supply Voltage (PBTL)

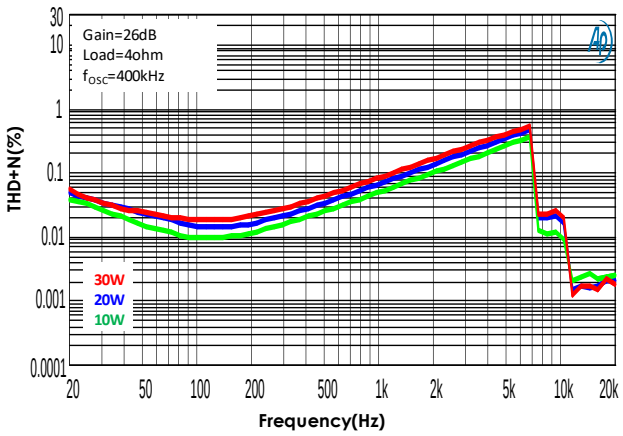


Note: Dashed Line represent thermally limited regions.

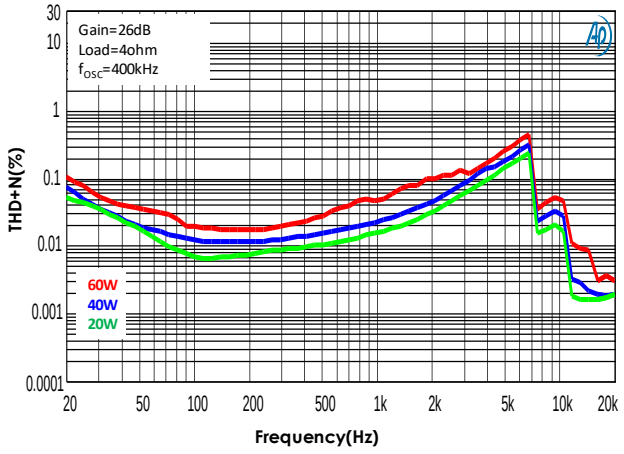
THD + N (%) vs. Frequency, 24V, 8Ω load (BTL)



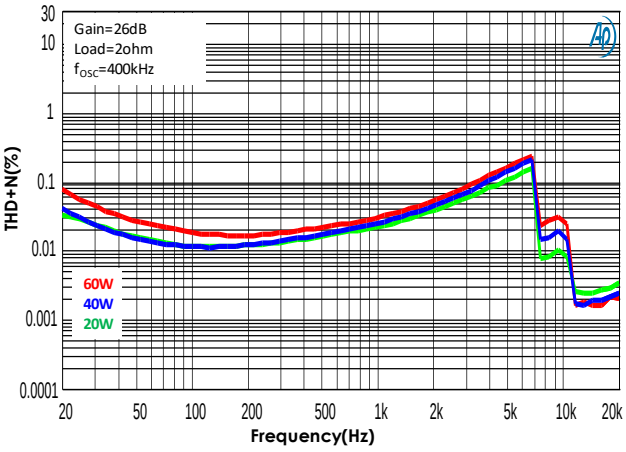
THD + N (%) vs. Frequency, 24V, 4Ω load (BTL)



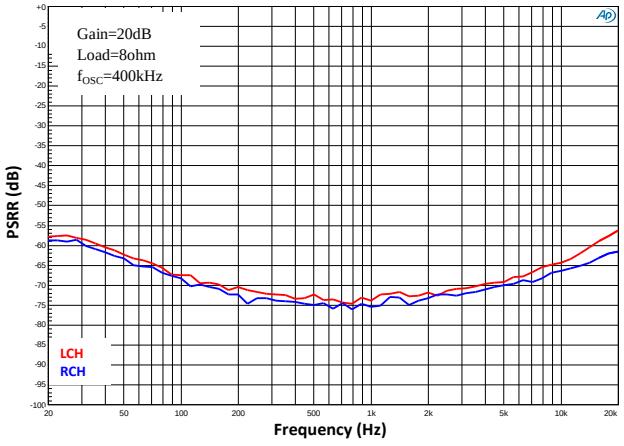
THD + N (%) vs. Frequency, 24V, 4Ω load (PBTL)



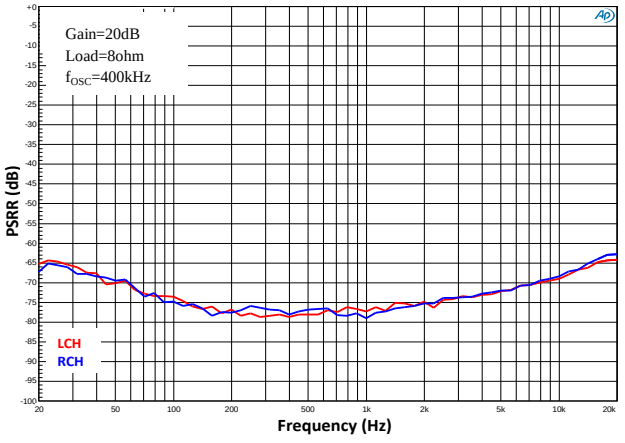
THD + N (%) vs. Frequency, 24V, 2Ω load (PBTL)



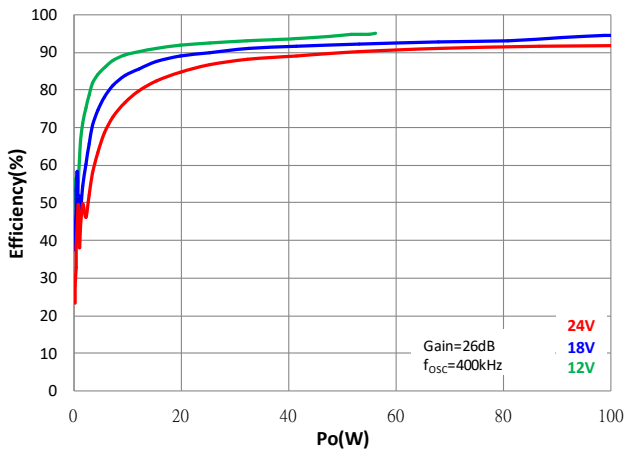
Power Supply Rejection Ratio, 24V, 8Ω load (BTL)



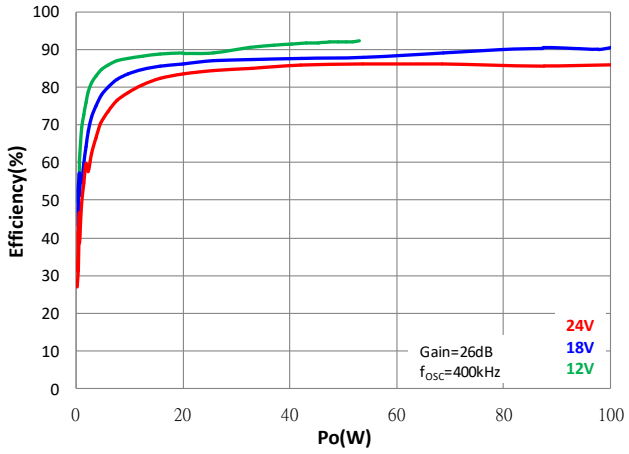
Power Supply Rejection Ratio, 12V, 8Ω load (BTL)



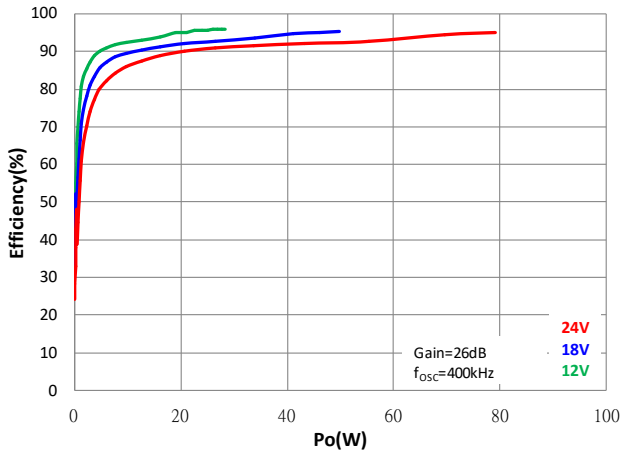
Efficiency, 8Ω load / 2ch (BTL)



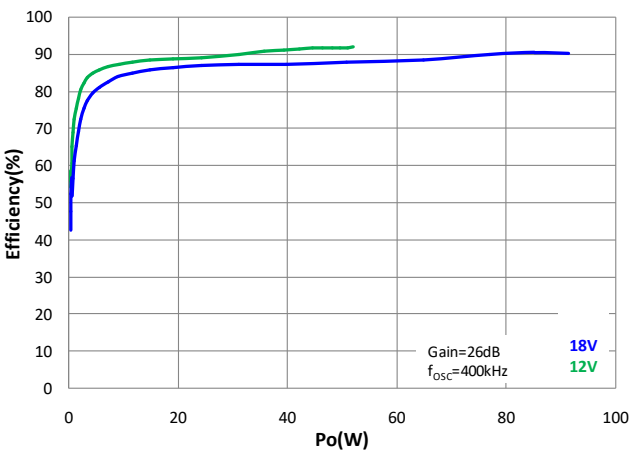
Efficiency, 4Ω load / 2ch (BTL)



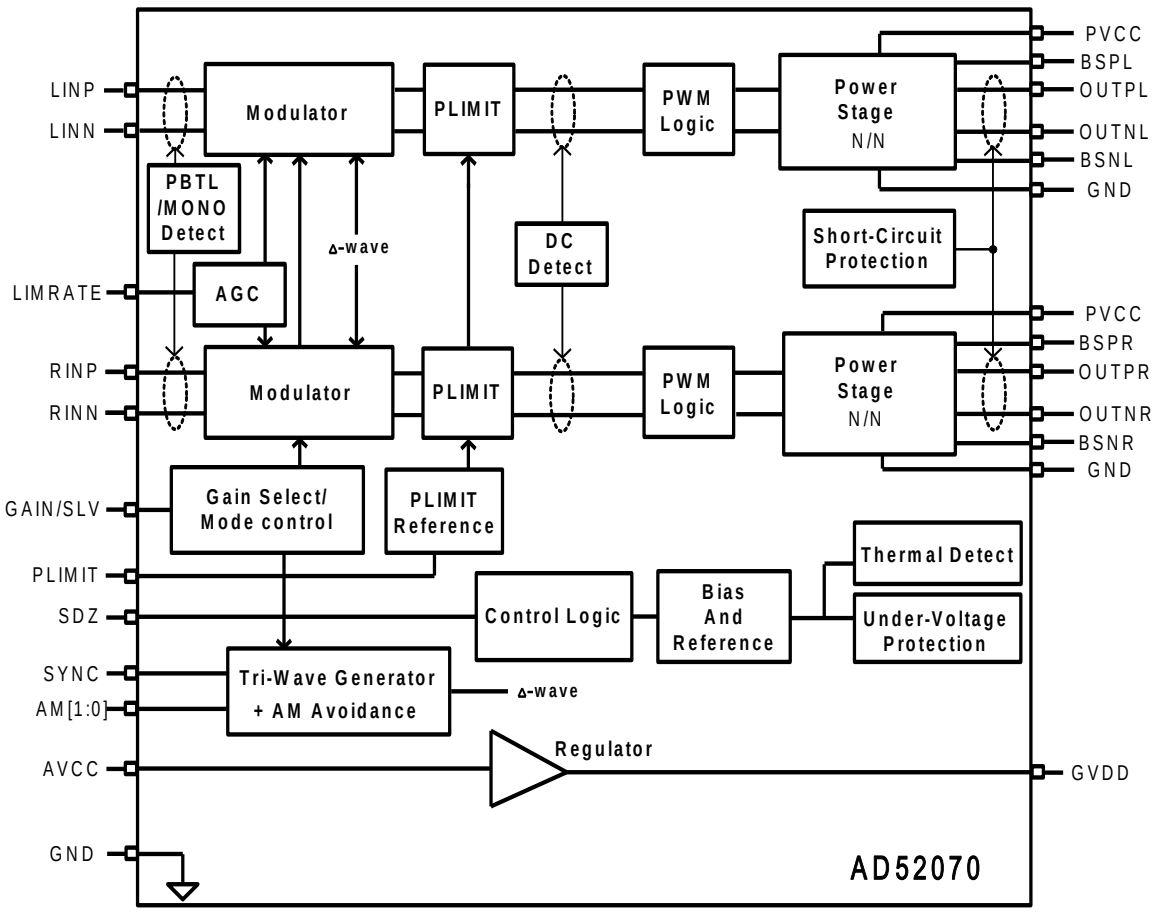
Efficiency, 4Ω load (PBTL)



Efficiency, 2Ω load (PBTL)



Functional Block Diagram



Operation Descriptions

- **Gain settings**

The gain of the AD52070 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four stages sets the GAIN in master mode in gains of 20, 26, 32, 36 dB respectively, while the next four stages sets the GAIN in slave mode in gains of 20, 26, 32, 36 dB respectively. The gain setting is latched during power-up and cannot be changed while device is powered. Table 1 lists the recommended resistor values and the state and gain. However, there is 20% variation in input resistance from production variation.

In Master mode, SYNC terminal is an output, in Slave mode, SYNC terminal is an input for a clock input. TTL logic levels with compliance to GVDD.

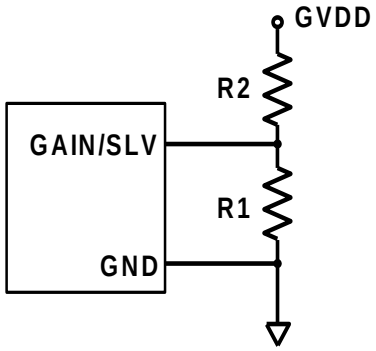


Table 1. Volume gain, master/slave and input impedance

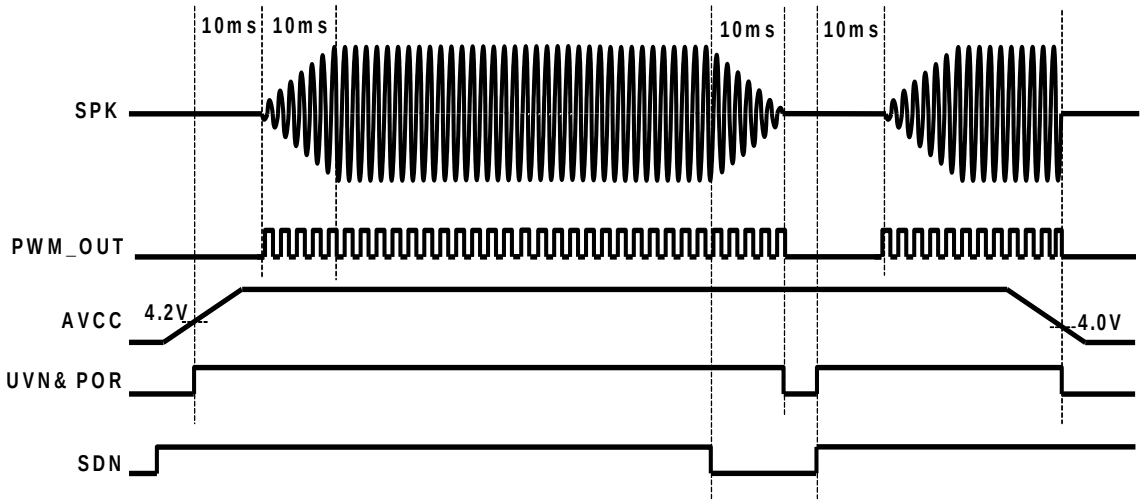
Mode	Gain(dB)	R1(to GND, kΩ)	R2(to GVDD, kΩ)	Input Resistance, R_{in} (kΩ)
Master	20	5.6	open	60
	26	20	100	30
	32	39	100	15
	36	47	75	9
Slave	20	51	51	60
	26	75	47	30
	32	100	39	15
	36	100	16	9

- **Shutdown (SDZ) control**

  Pulling SDZ pin low will let AD52070 operate in low-current state for power conservation. The AD52070 outputs will enter shutdown once SDZ pin is pulled low, and regulator will also disable to save power. SDZ pin with pull low resistor internally, AD52070 will enter shutdown mode still if SDZ pin keep floating. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

- **Fade-in / Fade-out**

  To reduce pop during high-speed on-off switching of audio amp, AD52070 uses slow rate on/off envelopes transition to avoid crack sound and uncomfortable feeling during in every fast turn-on/off.



- **Automatic Gain Control Function**

  Large input signal or lower supply voltage will easily distort output signal. The distorted and crack signal may damage speaker permanently. To provide a better listening experience for user and protect the speaker from overload, AD52070 features an Automatic Gain Control (AGC) function to prevent output signal from distortion. AGC function can automatically adjust system gain to let the output signal remain smooth by detecting the distortion level of output signal and keep the distortion level smaller than adjustable AGC level.

  Figure 1 shows the ideal output waveform without clipping by rail. Figure 2 shows the realistic output signal with clipping by rail. Figure 3 shows the output waveform with AGC function enabled. When output signal is distorted, gain immediately decreases by 0.32ms/dB (2.56ms/dB or 5.12ms/dB) in AGC mode Fast (AGC mode Medium or mode Slow). Once the output signal does not reached predetermined power level, the gain level will remain unchanged until the input signal is lowered. As output is lowered, the attenuated gain step is released incrementally every 328ms/dB in AGC mode-Fast or

655ms/dB in AGC mode-Medium or 1311ms/dB in AGC mode-Slow, which is the predefined release time. The AGC gain adjustment is applied with a ramp speed selectable by the LIMRATE pin setting.

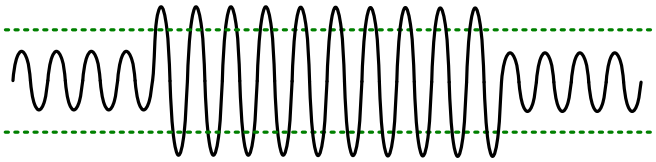


Figure.1 Waveform of output signal without clipping by rail

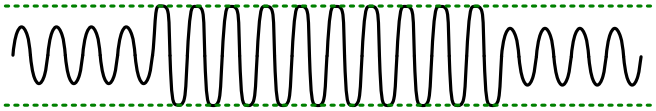


Figure.2 Waveform of output signal with clipping by rail

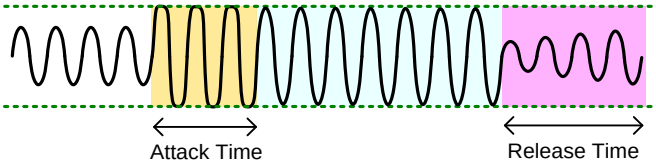


Figure.3 Waveform of output signal with AGC ON

Table 2. AGC and Power limit Setting

LIMRATE Voltage	Mode	AGC attack rate	TFB attack rate	AGC/TFB release rate
GVDD	Fast (AGC)	0.32 ms/dB	164 ms/dB	328 ms/dB
2/3*GVDD	Medium (AGC)	2.56 ms/dB	326 ms/dB	655 ms/dB
1/3*GVDD	Slow (AGC)	5.12 ms/dB	655 ms/dB	1311 ms/dB
GND	PLIMIT	Disable	Disable	Disable

AGC function can not only automatically adjust system gain, but also further limit output power of the amplifier without clipping. Figure 4 shows the output waveform with AGC function. The limiter threshold set by the PLIMT pin voltage.

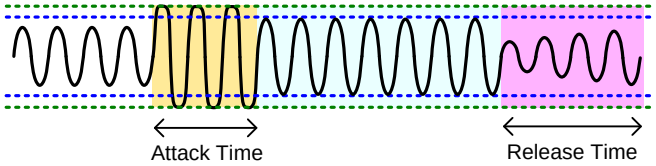


Figure.4 Waveform of output signal with AGC

- **AGC & Power limit level**

The AGC and PLIMIT voltage threshold is set by a voltage at PLIMIT pin. The PLIMIT voltage is set by a voltage divider from GVDD and GND, the limiting is set a limit on the output peak-to-peak voltage. The PLIMIT voltage can be used to calculate the maximum output power for unclipped in AGC mode and clipped in PLIMIT mode. PLIMIT pin is adjustable from 1.33V~2.1V.

For unclipped power,

$$Pout = \frac{2 \times \left[\frac{2.5V - P_{LIMIT}}{2.734V} \times PVCC \times \left(\frac{R_L}{R_L + 90m\Omega} \right) \right]^2}{R_L}$$

Where:

P_{LIMIT}: Adjustable AGC voltage at PLIMIT pin
PVCC: Chip operating voltage
R_L: Load resistance
90mΩ: RDS-on value in AD52070
Pout: Maximum unclipped output power in AGC
Power limit level (Po @1% THD+N): 1.1x Pout (unclipped)

Connect PLIMIT pin to ground to disable AGC/PLIMIT mode. The output variation during AGC/PLIMIT mode may have +-20% variation due to process window.

Table 3.1 AGC or PLIMIT Typical Operation Ⅰ

Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ AGC mode	V_{PLIMIT} (V) @ PLIMIT mode (PO @1%)
PVCC=24V RL=8ohm	5	1.98	1.96
	8	1.85	1.82
	10	1.77	1.74
	12	1.70	1.66
	15	1.61	1.56
	20	1.47	1.42

Table 3.2 AGC or PLIMIT Typical Operation Ⅱ

Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ AGC mode	V_{PLIMIT} (V) @ PLIMIT mode (PO @1%)
PVCC=12V RL=8ohm	3	1.70	1.66
	4	1.58	1.53
	5	1.47	1.42
	6	1.37	-

Table 3.3 AGC or PLIMIT Typical Operation Ⅲ

Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ AGC mode	V_{PLIMIT} (V) @ PLIMIT mode (PO @1%)
PVCC=24V RL=4ohm	10	1.98	1.95
	15	1.86	1.83
	20	1.76	1.73
	30	1.60	1.55

Table 3.4 AGC or PLIMIT Typical Operation Ⅳ

Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ AGC mode	V_{PLIMIT} (V) @ PLIMIT mode (PO @1%)
PVCC=12V RL=4ohm	5	1.76	1.73
	8	1.57	1.52
	10	1.46	1.41
	12	1.36	-

- **DC detection**

  AD52070 has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 320ms, the dc detect error will occur. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z.

  The minimum differential input voltages required to trigger the DC detect function are shown in table4. The input voltage must keep above the voltage listed in the table for more than 320msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in table5.

Table 4. DC Detect Threshold

AV (dB)	Vin (mV, differential)
20	272
26	136
32	64
36	44

Table 5. Output DC Detect Duty (for Either Channel)

PVCC (V)	Output Duty Exceeds
8	40
12	40
16	40

- **Thermal fold-back, TFB**

  The thermal fold-back is designed to protect the AD52070 from excessive die temperature in case of the device being operated beyond the recommended temperature or power limit, or with a weaker thermal system than recommended. The TFB works by reducing the on die power dissipation by reducing the AD52070 gain in steps of 0.5dB if the temperature trigger point is exceeded. Once the die temperature drops below the TFB trigger point, the AD52070 gain is increased by a single or by multiple 0.5dB steps until the TFB trigger point, or a maximum of 12dB attenuation is reached, and the gain will be decreased again, or the gain is at its nominal gain level. The TFB gain adjustment is applied with a ramp speed selectable by the LIMRATE pin setting as shown in Table 2.

- **Thermal protection**

  If the internal junction temperature is higher than 170°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD52070 returning to normal operation is about 135°C. The variation of protected temperature is about 10%.

- **Short-circuit protection**

  To protect loudspeaker drivers from over-current damage, AD52070 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to GND or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The latch can be cleared by reset SDZ or power supply cycling.

- **Under-voltage detection**

  When the GVDD voltage is lower than 2.8V or the AVCC voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD52070 return to normal operation.

- **Over-voltage protection**

  When the AVCC voltage is higher than 29.5V, loudspeaker will be disabled kept at low state. The protection status will be released as AVCC lower than 29V.

- **PBTL function**

  AD52070 provides the application of parallel BTL operation with two outputs of each channel connected directly. If connect LINP and LINN directly to Ground (without capacitors) this sets the device in PBTL mode during power up. Connect OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for the negative pin. Analog input signal is applied to INPR and INNR.

- **Mono function (Single Channel)**

  AD52070 can be connected in MONO mode to cut the idle power-loss nearly by half. If connect RINP and RINN directly to Ground (without capacitors) this sets the device in Mono mode during power up. Connect OUTPL and OUTNL to speaker just like normal BTL mode. Analog input signal is applied to LINP and LINN.

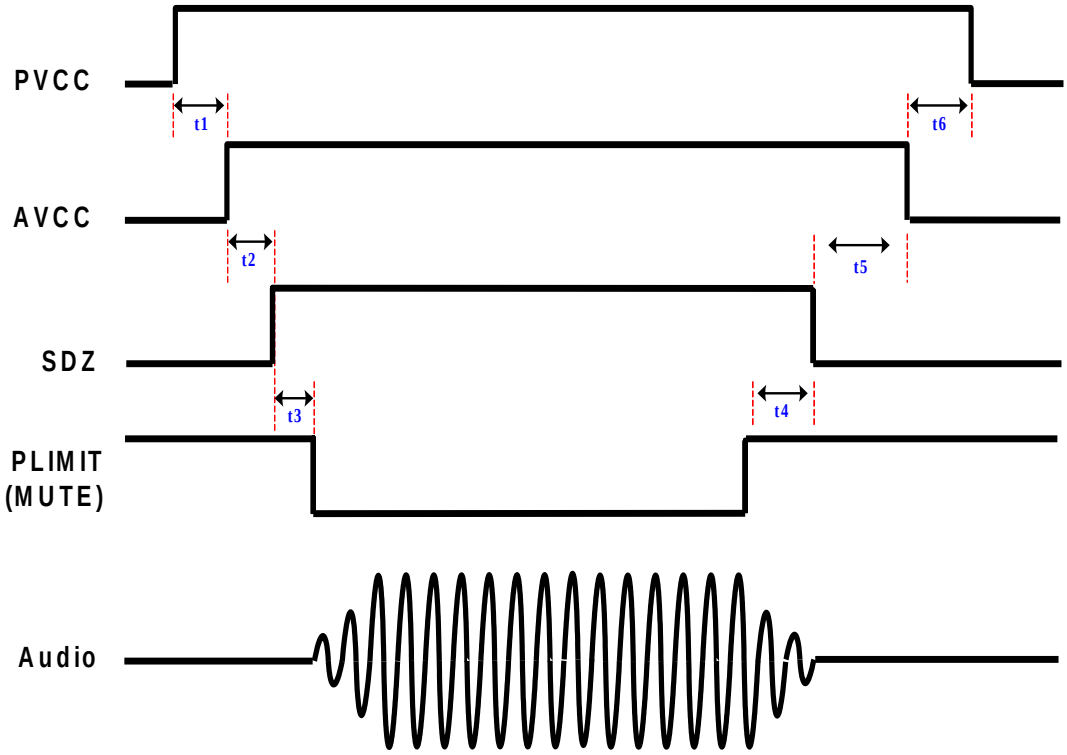
- **Mute control**

  The mute function provides also in AD52070 via PLIMIT pin. To connect PLITMIT pin to GVDD (>2.4V), the outputs will switch at idle PWM duty cycle (Low idle mode). A logic low (<2.3V) on this pin enables the outputs. This function may be used as a quick disable/enable of outputs when transitioning between different audio sources. It's also good with pop suppression via mute control. For power conservation, the SDZ

(shutdown) terminal should be used to reduce the quiescent current to the absolute minimum level.

- **Power On/Off sequence**

  Hereunder is AD52070's power on/off sequence.



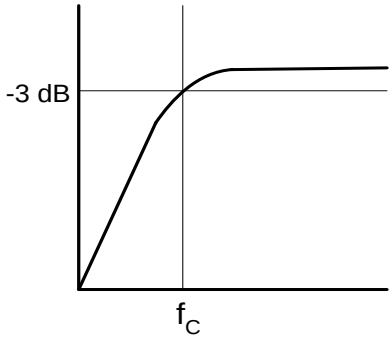
Symbol	Min. (ms)	Typ. (ms)	Max. (ms)
t1	0	-	-
t2	0.1	-	-
t3	10	-	-
t4	10	-	-
t5	10	-	-
t6	0		

Application information

- **Input capacitors (C_{in})**

  The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{in}. The resistance of input resistors is different at different gain setting. The respective gain and input resistance are listed in Table 1 (shown at GAIN SETTING). However, there is 20% variation in input resistance from production variation.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \ (\mathrm{Hz}) \quad \cdots\cdots\cdots (2)$$



- **Boot-strap capacitor**

  The output stage of the AD52070 uses a high-side NMOS driver. To generate the gate driver voltage for the high-side NMOS, a boot-strap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22uF capacitors to connect the appropriate output pin to the boot-strap pin in stereo/mono application.

- **Output LC Filter**

  If the traces from the AD52070 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 3 shows the typical output filter for 8Ω and 4Ω speaker with a cut-off frequency of 61 kHz and Figure 4 shows the typical output filter for 4Ω speaker with a cut-off frequency of 34 kHz.

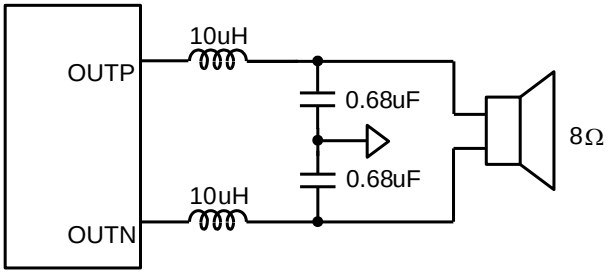


Figure 3. Typical LC Output Filter for 8Ω Speaker

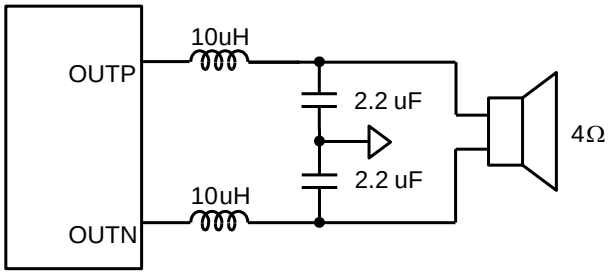


Figure 4. Typical LC Output Filter for 4Ω Speaker

AD52070 switching frequency can be adjusted by 300KHz, 400KHz, 500KHz or 1.2MHz. Higher switching frequency means smaller inductor value needed.

- With 1.2MHz switching frequency, designers can select 6.8uH or 4.7uH as the output filter, this will help to save the inductor size with the same rated current during the inductor selection. With 4.7uH inductor using, make sure PVCC voltage lower enough to avoid the large ripple current to trigger the OC threshold.

PVDD (V)	Speaker Load (Ω)	Recommended Minimum Inductance (uH) for LC filter design
≦21	8	4.7uH
≦16	4	

- **Power supply decoupling capacitor (Cs)**

  Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1μF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 220μF or greater capacitor (tantalum or electrolytic type) is suggested.

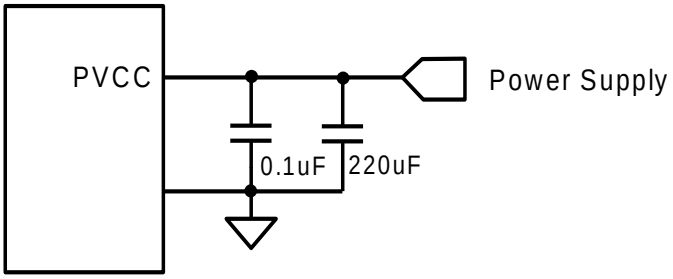


Figure 6. Recommended Power Supply Decoupling Capacitors.

- **GVDD supply**

  The GVDD supply is used to power the gates of the output full bridge transistors. The GVDD supply can also be used to supply the PLIMIT and GAIN/SLV voltage dividers. Decouple GVDD with a X7R (or X5R) ceramic 1μF capacitor to GND. The GVDD supply is not intended to be used for external supply. The current consumption should be limited by using resistor voltage dividers (R to GVDD + R to GND) for GAIN/SLV and PLIMIT of 100 kΩ or more.

- **Inductor selection**

  The inductance vs. current profile for the inductor used in the output LC filter of a class-D amplifier can significantly impact the total harmonic distortion (THD) performance. The inductors always have decreasing inductance with increasing operating current. The inductance falls off severely, which induce inductor distortion is higher during lower-impedance loads. The effective inductance at the peak current is required to be at least 80% of the inductance value

  In addition, it is required that the peak current is smaller than the OCP trigger threshold. Same PVCC and switching frequency, larger inductance means smaller idle current for lower power dissipation. The inductor's saturation current Isat > the amplifier's operating peak current is necessary. To operating safe considering, the inductor's saturation current >1.35 times of the peak current of maximum output power is suggested.

$$Inductor\_Ipeak\_selection \geq \sqrt{2 \times \frac{Maximum\_output\_power}{Rload}} \times 1.35$$

- **AM avoidance**

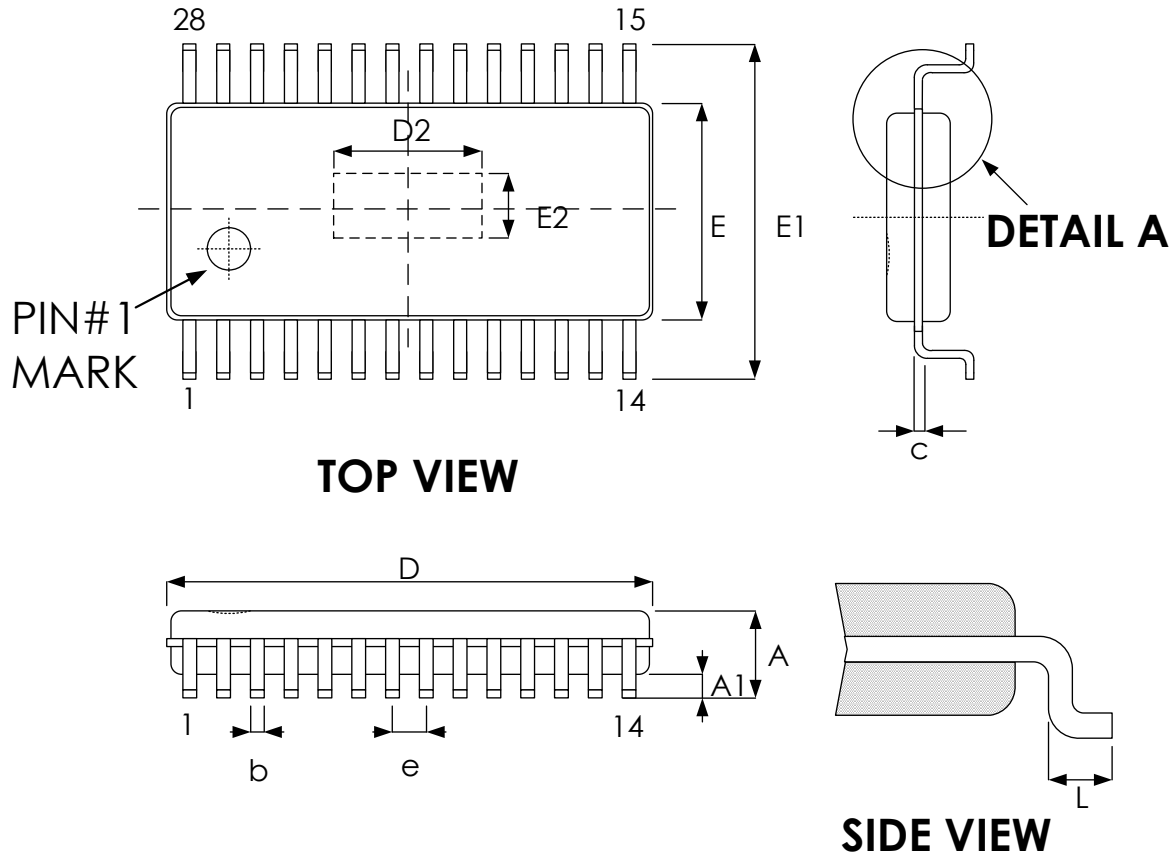
  To reduce interference in the AM radio band, AD52070 has the ability to change the switching frequency by the pins of AM1 and AM0. The recommended frequencies are listed in table 6. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the switching frequency being demodulated by the AM radio.

Table 6. AM Frequencies

US AM Frequency (KHz)	European AM Frequency (KHz)	Switching frequency (KHz)	AM1	AM0
-	522~540	400	0	0
540~917	540~914	500	0	1
917~1125	914~1122	400	0	0
1125~1375	1122~1373	500	0	1
1375~1547	1373~1548	400	0	0
1547~1700	1548~1701	500	0	1

Package Dimensions

- **E-TSSOP 28L (173 mil)**



Symbol	Dimension in mm	
	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	5.00	6.40
E2	2.50	2.90

Revision History

Revision	Date	Description
0.1	2020.12.16	Initial version.
0.2	2021.02.03	Update pin description. Update absolute maximum ratings.
1.0	2021.06.21	Remove “Preliminary” and Revise to 1.0
1.1	2021.10.06	1) Update features and description. 2) Update pin description. 3) Update absolute maximum ratings. 4) Update application circuit example for PBTL. 5) Update electrical characteristics. 6) Update typical characteristics. 7) Update function description.

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