12V STEREO CLASS-D AUDIO POWER AMPLIFIER

Features

- Operate from 8-12V supply voltage
- Class D power
  9.5W/ch into 8Ω from 12V supply @ 10% THD+N for stereo
  11.8W/ch into 6Ω from 12V supply @ 10% THD+N for stereo
- Support single-ended or differential analog input
- Antipop design
- Over-temperature protection
- Over-current protection
- Clock output for synchronization with multiple Class D devices
- Two volume control modes
  - 31 step DC volume control
  - 4 selectable, fixed gain setting
- 48-pin E-LQFP package

Applications

- TV audio
- Boom-Box
- Powered speaker

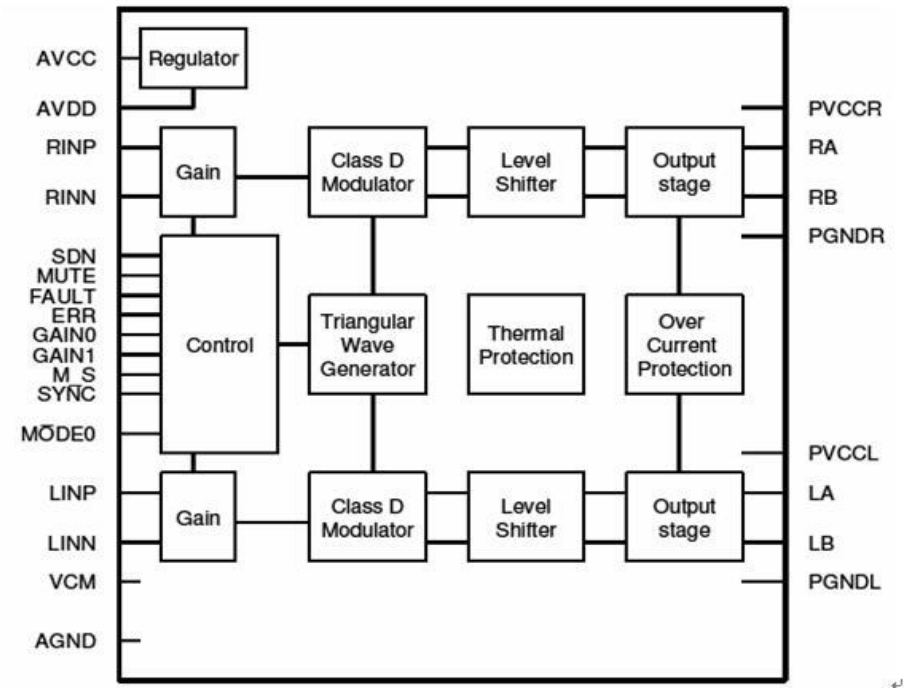
Description

The AD52660A is a high efficiency stereo class-D audio amplifier. Operating with 8 ~ 12V supply, it can deliver 10W/CH output power into 8 Ω loudspeaker within 10% THD+N and without external heat sink.

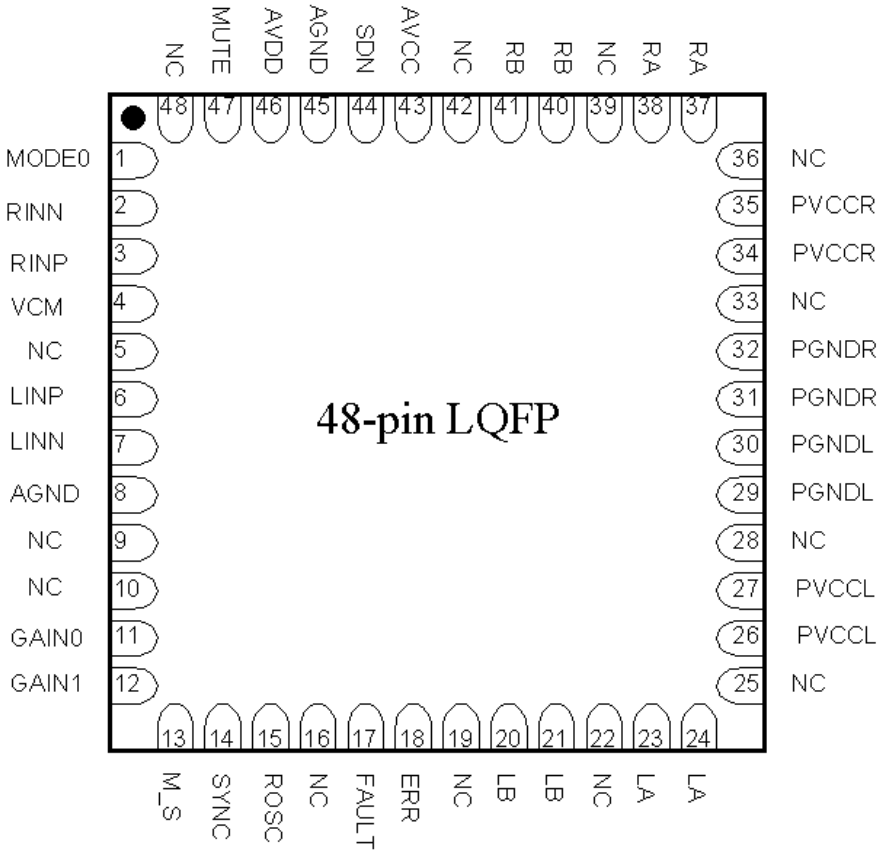
The AD52660A has two volume control modes by setting MODE0 pin. While MODE0 pin is set logic high, AD52660A is in DC volume control mode with 31-step volume gain, adjusted by the DC voltage applied on GAIN0 pin. Otherwise, AD52660A is the 4-step volume gain mode, selected by setting GAIN0 and GAIN1 pins. The two volume adjustment modes are designed to fit the different volume control requirements in various applications.

The AD52660A packaged as E-LQFP 48L is a stereo audio amplifier with high efficiency and low thermal resistance which leads to no external heat sink requirement under 10W/ch output power.

Functional Block Diagram



Pin Assignments



Pin Description

PIN	NAME	TYP	DESCRIPTION
1	MODE0	I	Mode0 control terminal
2	RINN	I	Negative audio input for right channel. Biased at ½ AVDD
3	RINP	I	Positive audio input for right channel. Biased at ½ AVDD
4	VCM	O	Reference for internal amplifiers. Normally equal to ½ AVDD.
5	NC		
6	LINP	I	Positive audio input for left channel. Biased at ½ AVDD
7	LINN	I	Negative audio input for left channel. Biased at ½ AVDD
8	AGND	P	Analog ground
9	NC		
10	NC		
11	GAIN0	I	Gain select bit 0.

12	GAIN1	I	Gain select bit 1.
13	M_S	I	Master/Slave select. HIGH=master mode. LOW=slave mode.
14	SYNC	I/O	Clock input/output for multiple chip synchronization.
15	ROSC	I/O	I/O for current setting resistor of triangular wave generator.
16	NC		
17	FAULT	O	Over-current fault report signal. Active high.
18	ERR	O	Error report signal. Active high.
19	NC		
20	LB	O	Half-bridge output B for left channel
21	LB	O	Half-bridge output B for left channel
22	NC		
23	LA	O	Half-bridge output A for left channel
24	LA	O	Half-bridge output A for left channel
25	NC		
26	PVCCL	P	Power supply for left channel H-bridge
27	PVCCL	P	Power supply for left channel H-bridge
28	NC		
29	PGNDL	P	Power ground for left channel H-bridge
30	PGNDL	P	Power ground for left channel H-bridge
31	PGNDR	P	Power ground for right channel H-bridge
32	PGNDR	P	Power ground for right channel H-bridge
33	NC		
34	PVCCR	P	Power supply for right channel H-bridge
35	PVCCR	P	Power supply for right channel H-bridge
36	NC		
37	RA	O	Half-bridge output B for right channel
38	RA	O	Half-bridge output A for right channel
39	NC		
40	RB	O	Half-bridge output B for right channel
41	RB	O	Half-bridge output B for right channel
42	NC		
43	AVCC	P	High voltage analog power supply.
44	SDN	I	Shutdown signal. Active low.
45	AGND	P	Analog ground
46	AVDD	O	Regulated output for use by internal cells.
47	MUTE	I	Mute signal. Active high.
48	NC		
-	Thermal Pad	-	Must be soldered to PCB's ground plane