

### FEATURES

- 250 MHz operation
- Driver/comparator and active load included
- On-chip Schottky diode bridge
- 52-lead LQFP\_EP package

### APPLICATIONS

- Automatic test equipment (ATE)
- Semiconductor test systems
- Board test systems
- Instrumentation and characterization equipment

### GENERAL DESCRIPTION

The AD53509 is a single chip that performs the pin electronics functions of driver, comparator, and active load in ATE VLSI and memory testers. In addition, a Schottky diode bridge for the active load and a VCOM buffer are included internally.

The driver is a proprietary design that features three active states: data high mode, data low mode, and term mode as well as an inhibit state. The output voltage range is  $-2\text{ V}$  to  $+7\text{ V}$  to accommodate a wide variety of test devices. The output leakage is typically  $<250\text{ nA}$  over the signal range.

The dual comparator, with an input range equal to the driver output range, features built-in latches and ECL-compatible outputs. The outputs are capable of driving  $50\ \Omega$  signal lines terminated to  $-2\text{ V}$ . Signal tracking capability is  $>5\text{ V/ns}$ .

The active load can be set up to  $40\text{ mA}$  load current with less than a  $10\ \mu\text{A}$  linearity error through the set range.  $I_{OH}$ ,  $I_{OL}$ , and the buffered VCOM are independently adjustable. On-board Schottky diodes provide high speed switching and low capacitance.

Also included on the chip is an on-board temperature sensor whose purpose is to give an indication of the surface temperature of the DCL. This information can be used to measure  $\theta_{JC}$  and  $\theta_{JA}$  or flag an alarm if proper cooling is lost. Output from the sensor is a current sink that is proportional to absolute temperature. The gain is trimmed to a nominal value of  $1.0\ \mu\text{A/K}$ . For example, the output current can be sensed by using a  $10\text{ k}\Omega$  resistor connected from  $10\text{ V}$  to the THERM pin. A voltage drop across the resistor then develops that equals

$$10\text{ K} \times 1\ \mu\text{A/K} = 10\text{ mV/K} = 2.98\text{ V (at room temperature)}$$

### FUNCTIONAL BLOCK DIAGRAM

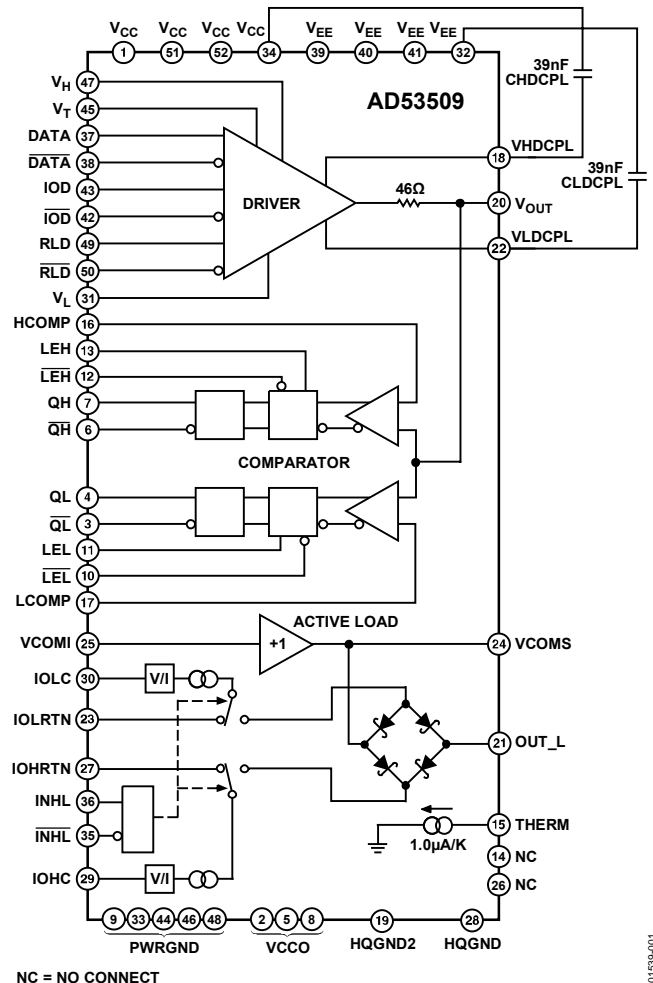


Figure 1.

### Rev. B

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**REVISION HISTORY**

**3/08—Rev. A to Rev. B**

Updated Format .....	Universal
Changes to Features and General Description .....	1
Changes to Table 1.....	3
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**12/00—Rev. 0 to Rev. A**

# SPECIFICATIONS

## DRIVER SPECIFICATIONS

All specifications are at  $T_J = 85^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC} = 11\text{ V} \pm 3\%$ ,  $V_{EE} = -6\text{ V} \pm 3\%$ , unless otherwise noted. All temperature coefficients are measured at  $T_J = 75^\circ\text{C}$  to  $95^\circ\text{C}$ .

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
<b>DIFFERENTIAL INPUT CHARACTERISTICS, DATA to <math>\overline{\text{DATA}}</math>, IOD to <math>\overline{\text{IOD}}</math>, RLD to <math>\overline{\text{RLD}}</math></b>					
Input Voltage	-2		+3	V	All digital inputs within a 2 V range $V_{IN} = -2\text{ V}, +3\text{ V}$
Differential Input Range			2	V	
Bias Current	-250		+250	$\mu\text{A}$	
<b>REFERENCE INPUTS</b>					
Bias Currents	-50		+50	$\mu\text{A}$	$V_L, V_H, V_T = 5\text{ V}$
<b>OUTPUT CHARACTERISTICS</b>					
Logic High Range	-2		+7	V	Data = H, $V_H = -2\text{ V to } +7\text{ V}, V_L = -2\text{ V}, V_T = 0\text{ V}$
Logic Low Range	-2		+6	V	Data = L, $V_L = -2\text{ V to } +6\text{ V}, V_H = 7\text{ V}, V_T = 0\text{ V}$
Amplitude, $V_H$ and $V_L$	0.1		9	V	$V_L = 0\text{ V}, V_H = 0.1\text{ V}, V_T = 0\text{ V}$
Absolute Accuracy					$V_L = -2\text{ V}, V_H = 7\text{ V}, V_T = 0\text{ V}$
$V_H$ Offset	-50		+50	mV	Data = H, $V_H = 0\text{ V}, V_L = -2\text{ V}, V_T = -1\text{ V}$
$V_H$ Gain + Linearity Error	0.3 - 5		0.3 + 5	% of $V_H$ + mV	Data = H, $V_H = -1\text{ V to } +7\text{ V}, V_L = -2\text{ V}, V_T = -2\text{ V}$
$V_L$ Offset	-50		+50	mV	Data = L, $V_L = 0\text{ V}, V_H = 5\text{ V}, V_T = 3\text{ V}$
$V_L$ Gain + Linearity Error	-0.3 - 5		+0.3 + 5	% of $V_L$ + mV	Data = L, $V_L = -2\text{ V to } +6\text{ V}, V_H = 7\text{ V}, V_T = 7\text{ V}$
Offset Temperature Coefficient		0.5		mV/ $^\circ\text{C}$	$V_L = -2\text{ V}, V_H = 0\text{ V}, V_T = -1\text{ V}$ ( $V_H$ offset), $V_L = 0\text{ V}, V_H = 5\text{ V}, V_T = 3\text{ V}$ ( $V_L$ offset)
Output Resistance					
$V_H = -2\text{ V}$	44	46	48	$\Omega$	$V_L = -2\text{ V}, V_T = 0\text{ V}, I_{OUT} = 0\text{ mA}, 1\text{ mA}, 30\text{ mA}$
$V_H = +7\text{ V}$	44	46	48	$\Omega$	$V_L = -1\text{ V}, V_T = 0\text{ V}, I_{OUT} = 0\text{ mA}, -1\text{ mA}, -30\text{ mA}$
$V_L = -2\text{ V}$	44	46	48	$\Omega$	$V_H = 6\text{ V}, V_T = 0\text{ V}, I_{OUT} = 0\text{ mA}, 1\text{ mA}, 30\text{ mA}$
$V_L = +6\text{ V}$	44	46	48	$\Omega$	$V_H = 7\text{ V}, V_T = 0\text{ V}, I_{OUT} = 0\text{ mA}, -1\text{ mA}, -30\text{ mA}$
$V_H = +3\text{ V}$		46		$\Omega$	$V_L = 0\text{ V}, V_T = 0\text{ V}, I_{OUT} = -30\text{ mA}$ (trim point)
Dynamic Current Limit		>100		mA	$C_{BYP} = 39\text{ nF}, V_H = 6\text{ V}, V_L = -2\text{ V}, V_T = 0\text{ V}$
Static Current Limit	-85		+85	mA	Output to $-2\text{ V}, V_H = 7\text{ V}, V_L = -1\text{ V}, V_T = 0\text{ V}$ , data = H and output to $7\text{ V}, V_H = 6\text{ V}$ , $V_L = -2\text{ V}, V_T = 0\text{ V}, \text{data} = \text{L}$
<b><math>V_T</math></b>					
Voltage Range	-2		+7	V	Term mode, $V_T = -2\text{ V to } +7\text{ V}, V_L = 0\text{ V}, V_H = 3\text{ V}$
$V_T$ Offset	-50		+50	mV	Term mode, $V_T = 0\text{ V}, V_L = 0\text{ V}, V_H = 3\text{ V}$
$V_T$ Gain + Linearity Error	-0.3 + 10		+0.3 + 10	% of $V_{SET}$ + mV	Term mode, $V_T = -2\text{ V to } +7\text{ V}, V_L = 0\text{ V}, V_H = 3\text{ V}$
Offset Temperature Coefficient		0.5		mV/ $^\circ\text{C}$	$V_T = 0\text{ V}, V_L = 0\text{ V}, V_H = 3\text{ V}$
Output Resistance	44	46	49	$\Omega$	$I_{OUT} = 30\text{ mA}, 1.0\text{ mA}, V_T = -2.0\text{ V}, V_H = 3\text{ V}$ , $V_L = 0\text{ V}, I_{OUT} = -30\text{ mA}, -1.0\text{ mA}, V_T = 7.0\text{ V}$ , $V_H = 3\text{ V}, V_L = 0\text{ V}, I_{OUT} = \pm 30\text{ mA}, \pm 1.0\text{ mA}$ , $V_T = 0\text{ V}, V_H = 3\text{ V}, V_L = 0\text{ V}$
<b>DYNAMIC PERFORMANCE, <math>V_H</math> AND <math>V_L</math></b>					
Propagation Delay Time		1.5		ns	Measured at 50%, $V_H = 400\text{ mV}$ , $V_L = -400\text{ mV}, V_T = 0\text{ V}$
Propagation Delay Temperature Coefficient		2		ps/ $^\circ\text{C}$	Measured at 50%, $V_H = 400\text{ mV}$ , $V_L = -400\text{ mV}, V_T = 0\text{ V}$
Delay Matching, Edge to Edge		<100		ps	Measured at 50%, $V_H = 400\text{ mV}$ , $V_L = -400\text{ mV}, V_T = 0\text{ V}$

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Parameter	Min	Typ	Max	Unit	Test Conditions
Rise and Fall Times					
1 V Swing		0.42		ns	Measured 20% to 80%, $V_L = 0\text{ V}$ , $V_H = 1\text{ V}$ , $V_T = 0\text{ V}$
3 V Swing		0.75		ns	Measured 20% to 80%, $V_L = 0\text{ V}$ , $V_H = 3\text{ V}$ , $V_T = 0\text{ V}$
5 V Swing		1.65		ns	Measured 10% to 90%, $V_L = 0\text{ V}$ , $V_H = 5\text{ V}$ , $V_T = 0\text{ V}$
9 V Swing		3.0		ns	Measured 10% to 90%, $V_L = -2\text{ V}$ , $V_H = 7\text{ V}$ , $V_T = 0\text{ V}$
Rise/Fall Time Temperature Coefficient					
1 V Swing		$\pm 1$		ps/ $^{\circ}\text{C}$	Measured 20% to 80%, $V_L = 0\text{ V}$ , $V_H = 1\text{ V}$
3 V Swing		$\pm 2$		ps/ $^{\circ}\text{C}$	Measured 20% to 80%, $V_L = 0\text{ V}$ , $V_H = 3\text{ V}$
5 V Swing		$\pm 4$		ps/ $^{\circ}\text{C}$	Measured 10% to 90%, $V_L = 0\text{ V}$ , $V_H = 5\text{ V}$
Overshoot and Preshoot		<3 + 50		% of Step + mV	$V_L, V_H = -0.1\text{ V}, +0.1\text{ V}$ , $V_L, V_H = 0\text{ V}, +1.0\text{ V}$ $V_L, V_H = 0\text{ V}, 3.0\text{ V}$ , $V_L, V_H = 0\text{ V}, 5.0\text{ V}$ $V_L, V_H = -2.0\text{ V}, +7.0\text{ V}$
Settling Time					
to 15 mV		<50		ns	$V_L = 0\text{ V}$ , $V_H = 0.5\text{ V}$ , $V_T = -2\text{ V}$
to 4 mV		<10		$\mu\text{s}$	$V_L = 0\text{ V}$ , $V_H = 0.5\text{ V}$ , $V_T = -2\text{ V}$
Delay Change vs. Pulse Width		50		ps	$V_L = 0\text{ V}$ , $V_H = 2\text{ V}$ , pulse width = 2.5 ns/7.5 ns, 30 ns/90 ns
Minimum Pulse Width					
3 V Swing		1.4		ns	$V_L = 0\text{ V}$ , $V_H = 3\text{ V}$ , 90% (2.7 V) reached, measure @ 50%
5 V Swing		2.0		ns	$V_L = 0\text{ V}$ , $V_H = 5\text{ V}$ , 90% (4.5 V) reached, measure @ 50%
Toggle Rate		250		MHz	$V_L = 0\text{ V}$ , $V_H = 5\text{ V}$ , VDUT > 3.0 V p-p
DYNAMIC PERFORMANCE, INHIBIT					
Delay Time, Active to Inhibit		3.3		ns	Measured at 50%, $V_H = 2\text{ V}$ , $V_L = -2\text{ V}$ , $V_T = 0\text{ V}$
Delay Time, Inhibit to Active		2.9		ns	Measured at 50%, $V_H = 2\text{ V}$ , $V_L = -2\text{ V}$ , $V_T = 0\text{ V}$
Delay Time Matching, Z		<2		ns	Z = delay time, active to inhibit – delay time, inhibit to active (of worst two edges)
Input/Output Spike		150		mV p-p	$V_H = 0\text{ V}$ , $V_L = 0\text{ V}$ , $V_T = 0\text{ V}$
Rise/Fall Time, Active to Inhibit		1.6		ns	$V_H = 2\text{ V}$ , $V_L = -2\text{ V}$ (measured 20%/80% of 1 V output)
Rise/Fall Time, Inhibit to Active		1.4		ns	$V_H = 2\text{ V}$ , $V_L = -2\text{ V}$ (measured 20%/80% of 1 V output)
DYNAMIC PERFORMANCE, $V_T$					
Delay Time, $V_H$ to $V_T$ and $V_L$ to $V_T$		2.5		ns	Measured at 50%, $V_L = -1\text{ V}$ , $V_H = 1\text{ V}$ , $V_T = 0\text{ V}$
Delay Time, $V_T$ to $V_H$ and $V_T$ to $V_L$		2.5		ns	Measured at 50%, $V_L = V_H = 0.4\text{ V}$ , $V_T = -0.4\text{ V}$
Overshoot and Preshoot		<3.0 + 75		% of Step + mV	$V_H/V_L, V_T = (0\text{ V}, -1\text{ V}), (0\text{ V}, -2.0\text{ V}), (0\text{ V}, +6.0\text{ V})$
$V_T$ Mode Rise Time		2.2		ns	$V_L = -2\text{ V}$ , $V_H = 2\text{ V}$ , $V_T = 0\text{ V}$ , 20% to 80%
$V_T$ Mode Fall Time		2.2		ns	$V_L = -2\text{ V}$ , $V_H = 2\text{ V}$ , $V_T = 0\text{ V}$ , 20% to 80%
PSRR, Drive, or Term Mode		35		dB	$V_S = V_S \pm 3\%$

**COMPARATOR SPECIFICATIONS**

All specifications are at  $T_J = 85^\circ\text{C} \pm 5^\circ\text{C}$ . Outputs terminated in  $150\ \Omega$  to GND,  $V_{CC} = 11\ \text{V} \pm 3\%$ ,  $V_{EE} = 6\ \text{V} \pm 3\%$ ,  $V_{CCO} = 3.3\ \text{V}$ , unless otherwise specified. All temperatures coefficients are measured at  $T_J = 75^\circ\text{C}$  to  $95^\circ\text{C}$ .

**Table 2.**

Parameter	Min	Typ	Max	Unit	Test Conditions
<b>DC INPUT CHARACTERISTICS</b>					
Offset Voltage, $V_{OS}$	-25		+25	mV	$CMV = 0\ \text{V}$
Offset Voltage, Drift		50		$\mu\text{V}/^\circ\text{C}$	$CMV = 0\ \text{V}$
HCOMP, LCOMP Bias Current	-50		+50	$\mu\text{A}$	$V_{IN} = 0\ \text{V}$
Voltage Range, $V_{CM}$	-2		+7.0	V	
Differential Voltage, $V_{DIFF}$			9.0	V	
Gain and Linearity	-0.05		+0.05	% FSR	$V_{IN} = -2\ \text{V}$ to $+7\ \text{V}$ (9 V FSR)
<b>LATCH ENABLE INPUTS</b>					
Logic 1 Current, $I_{IH}$			250	$\mu\text{A}$	$LEA, \overline{LEA}, LEB, \overline{LEB} = 3\ \text{V}$
Logic 0 Current, $I_{IL}$	-250			$\mu\text{A}$	$LEA, \overline{LEA}, LEB, \overline{LEB} = -2\ \text{V}$
Logic Input Range	-2		+3	V	
<b>DIGITAL OUTPUTS</b>					
Logic 1 Voltage, $V_{OH}$	$V_{CCO} - 0.98$			V	$Qx$ or $\overline{Qx}$ , 16.7 mA load
Logic 0 Voltage, $V_{OL}$			$V_{CCO} - 1.5$	V	$Qx$ or $\overline{Qx}$ , 10 mA load
Slew Rate		1		V/ns	
VCCO Range	0		8	V	
<b>SWITCHING PERFORMANCE</b>					
Propagation Delay					
Input to Output		1.8		ns	$V_{IN} = 2\ \text{V}$ p-p
Latch Enable to Output		2		ns	HCOMP = 1 V, LCOMP = 1 V
Propagation Delay Temperature Coefficient		2		$\text{ps}/^\circ\text{C}$	
Propagation Delay Change with Respect to					
Slew Rate: 0.5 V/ns, 1.0 V/ns, 3.0 V/ns		< $\pm 100$		ps	$V_{IN} = 0\ \text{V}$ to 5 V
Slew Rate: 5.0 V/ns		< $\pm 350$		ps	$V_{IN} = 0\ \text{V}$ to 5 V
Amplitude: 1.0 V, 3.0 V, 5.0 V		< $\pm 200$		ps	$V_{IN} = 1.0\ \text{V}/\text{ns}$
Equivalent Input Rise Time		450		ps	$V_{IN} = 0\ \text{V}$ to 3 V, 3 V/ns
Pulse Width Linearity		< $\pm 200$		ps	$V_{IN} = 0\ \text{V}$ to 3 V, 3 V/ns, PW = 3 ns to 8 ns
Settling Time		25		ns	Settling to $\pm 8\ \text{mV}$ , $V_{IN} = 1\ \text{V}$ to 0 V
Latch Timing					
Input Pulse Width		1.68		ns	
Setup Time		1.0		ns	
Hold Time		1.1		ns	
Hysteresis		6		mV	Latch inputs programmed for hysteresis

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## ACTIVE LOAD SPECIFICATIONS

All specifications are at  $T_J = 85^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC} = 11\text{ V} \pm 3\%$ ,  $V_{EE} = -6\text{ V} = \pm 3\%$ , unless otherwise noted. All temperature coefficients are measured at  $T_J = 75^\circ\text{C}$  to  $95^\circ\text{C}$ .

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions
<b>INPUT CHARACTERISTICS</b>					
INHL, $\overline{\text{INHL}}$					
Input Voltage	-2		+3	V	IOHC = 1 V, IOLC = 1 V, VCOM = 2 V, OUT_L = 0 V
Bias Current	-250		+250	$\mu\text{A}$	INHL, $\overline{\text{INHL}} = -2\text{ V}, +3\text{ V}$
IOHC Current Program Range					
IOH = 0 mA to -40 mA	0		4	V	OUT_L = -0.7 V, +7 V
IOLC Current Program Range					
IOL = 0 mA to 40 mA	0		4	V	OUT_L = -2 V, +5.7 V
IOHC, IOLC Input Bias Current	-300		+300	$\mu\text{A}$	IOLC = 0 V, 4.0 V and IOHC = 0 V, 4.0 V
IOLRTN, IOHRTN Range	-2		+7	V	IOL = 40 mA, IOH = -40 mA, OUT_L = -2 V, +7 V
VDUT Range	-2		+7	V	IOL = 40 mA, IOH = -40 mA, OUT_L - VCOMI > 1.3 V
VDUT Range, IOH = 0 mA to -40 mA	-0.7		+7	V	OUT_L - VCOM > 1.3 V
VDUT Range, IOL = 0 mA to 40 mA	-2		+5.7	V	VCOM - VDUT > 1.3 V
VCOMI Input Range	-2		+7	V	IOL = 40 mA, IOH = -40 mA
<b>OUTPUT CHARACTERISTICS</b>					
Accuracy					
Absolute Accuracy Error, Load Current	-0.3 - 100		+0.3 + 100	% $I_{SET} + \mu\text{A}$	IOL, IOH = 25 $\mu\text{A}$ to 40 mA, VCOM = 0 V, OUT_L = $\pm 2\text{ V}$ and IOL = 25 $\mu\text{A}$ to 40 mA, VCOM = 7 V, OUT_L = 5.7 V and IOH = 25 $\mu\text{A}$ to 40 mA, VCOM = -2 V, OUT_L = -0.7 V
VCOM Buffer					
Offset Error	-50		+50	mV	IOL, IOH = 40 mA, VCOMI = 0 V, OUT_L = VCOM
Bias Current	-10	+1	+10	$\mu\text{A}$	VCOMI = 0 V, OUT_L = VCOM
Gain Error	-0.2		+0.2	%	IOL, IOH = 40 mA, VCOMI = -1 V to +6 V, $V_{OUT} = VCOM$
Linearity Error	-10		+10	mV	IOL, IOH = 40 mA, VCOMI = -1 V to +6 V, $V_{OUT} = VCOM$
Output Current Temperature Coefficient		< $\pm 2$		$\mu\text{A}/^\circ\text{C}$	Measured at IOH, IOL = 200 $\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>					
Propagation Delay					
$\pm I_{OUT}$ to Inhibit		1.9		ns	VCOM = $\pm 2\text{ V}$ , IOL = 20 mA, IOH = -20 mA
Inhibit to $\pm I_{OUT}$		2.8		ns	VCOM = $\pm 2\text{ V}$ , IOL = 20 mA, IOH = 20 mA
Propagation Delay Matching		<1.8		ns	
Input/Output Spike		240		mV	VCOM = 0 V, IOL = 20 mA, IOH = -20 mA
Settling Time to 15 mV		<50		ns	IOL = 20 mA, IOH = -20 mA, 50 $\Omega$ load to $\pm 15\text{ mV}$
Settling Time to 4 mV		<10		$\mu\text{s}$	IOL = 20 mA, IOH = -20 mA, 50 $\Omega$ load to $\pm 4\text{ mV}$

## TOTAL FUNCTION SPECIFICATIONS

All specifications are at  $T_J = 85^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC} = 11\text{ V} \pm 3\%$ ,  $V_{EE} = -6\text{ V} \pm 3\%$  unless otherwise noted. All temperature coefficients are measured at  $T_J = 75^\circ\text{C}$  to  $95^\circ\text{C}$ .

Table 4.

Parameter <sup>1</sup>	Min	Typ	Max	Unit	Test Conditions
OUTPUT CHARACTERISTICS					
Output Leakage Current, $V_{OUT} = -1\text{ V to }+5\text{ V}$	-250		+250	nA	Driver and load inhibited
Output Leakage Current, $V_{OUT} = -2\text{ V to }+7\text{ V}$	-500		+500	$\mu\text{A}$	
Output Capacitance		8		pF	
POWER SUPPLIES					
Total Supply Range		17		V	Driver = $I_{NH}$ , $I_{LOAD}$ program = 40 mA, load = active Driver = $I_{NH}$ , $I_{LOAD}$ program = 40 mA, load = active VCCO = 3.3 V, comparator output 150 $\Omega$ to GND Driver = $I_{NH}$ , $I_{LOAD}$ program = 40 mA, load = active $R_{LOAD} = 10\text{ k}\Omega$ , $V_{SOURCE} = 11\text{ V}$
Positive Supply, $V_{CC}$		11		V	
Negative Supply, $V_{EE}$		-6		V	
Positive Supply Current			280	mA	
Negative Supply Current			290	mA	
VCCO Current		65		mA	
Total Power Dissipation			4.8	W	
Temperature Sensor Gain Factor		1		$\mu\text{A/K}$	

<sup>1</sup> Connecting or shorting the decoupling pins to ground results in the destruction of the device.

Table 5. Driver Truth Table

DATA	DATA	IOD	IOD	RLD	RLD	Output State
0	1	1	0	X	X	$V_L$
1	0	1	0	X	X	$V_H$
X	X	0	1	0	1	Inhibit
X	X	0	1	1	0	$V_T$

Table 6. Comparator Truth Table

$V_{OUT}$		LEH	$\overline{\text{LEH}}$	LEL	$\overline{\text{LEL}}$	Output States			
						QH	$\overline{\text{QH}}$	QL	$\overline{\text{QL}}$
>HCOMP	>LCOMP	1	0	1	0	1	0	1	0
>HCOMP	<LCOMP	1	0	1	0	1	0	0	1
<HCOMP	>LCOMP	1	0	1	0	0	1	1	0
<HCOMP	<LCOMP	1	0	1	0	0	1	0	1
X	X	0	1	0	1	QH (t - 1)	$\overline{\text{QH}}$ (t - 1)	QL (t - 1)	$\overline{\text{QL}}$ (t - 1)

Table 7. Active Load Truth Table

OUT_L	INHL	$\overline{\text{INHL}}$	Output States (Including Diode Bridge)		
			IOH	IOL	I(OUT_L)
<VCOM	0	1	$V(\text{IOHC}) \times 10\text{ mA}$	$V(\text{IOLC}) \times 10\text{ mA}$	IOL
>VCOM	0	1	$V(\text{IOHC}) \times 10\text{ mA}$	$V(\text{IOLC}) \times 10\text{ mA}$	IOH
X	1	0	0	0	0

## ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Power Supply Voltage	
$V_{CC}$ to GND	13 V
$V_{EE}$ to GND	-8 V
$V_{CC}$ to $V_{EE}$	20 V
VCCO to GND	10 V
PWRGND, HQGND, HQGND2	$\pm 0.4$ V
Inputs	
DATA, $\overline{\text{DATA}}$ , IOD, $\overline{\text{IOD}}$ , RLD, $\overline{\text{RLD}}$	-2 V to +5 V
DATA to $\overline{\text{DATA}}$ , IOD to $\overline{\text{IOD}}$ , RLD to $\overline{\text{RLD}}$	$\pm 3$ V
LEL, $\overline{\text{LEL}}$ , LEH, $\overline{\text{LEH}}$	-2 V to +5 V
LEL to $\overline{\text{LEL}}$ , LEH to $\overline{\text{LEH}}$	$\pm 3$ V
INH $\overline{\text{L}}$ , $\overline{\text{INH}}$	-2 V to +5 V
INH $\overline{\text{L}}$ to $\overline{\text{INH}}$	$\pm 3$ V
$V_H$ , $V_L$ , $V_T$ , VCOMI to GND	-3 V to +8 V
$V_H$ to $V_L$	$\pm 10$ V
$(V_H - V_T)$ and $(V_T - V_L)$	$\pm 10$ V
IOHC	$\pm 6$ V
IOLC	$\pm 6$ V
HCOMP	-3 V to +8 V
LCOMP	-3 V to +8 V
HCOMP, LCOMP to $V_{OUT}$	$\pm 10$ V
Outputs	
$V_{OUT}$ Short-Circuit Duration	Indefinite <sup>1</sup>
$V_{OUT}$ Inhibit Mode	-3 V to +8 V
VHDCPL	Do not connect except for capacitor to $V_{CC}$
VLDCPL	Do not connect except for capacitor to $V_{EE}$
QH, $\overline{\text{QH}}$ , QL, $\overline{\text{QL}}$ Maximum $I_{OUT}$	
Continuous	50 mA
Surge	100 mA
THERM	0 V to 13 V
IOHRTN, IOLRTN	-3.5 V to +8.5 V
VCOMS Short-Circuit Duration	3 sec <sup>1</sup>
Environmental	
Operating Temperature (Junction)	175°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec) <sup>2</sup>	260°C

<sup>1</sup> Output short-circuit protection is guaranteed as long as proper heat sinking is employed to ensure compliance with the operating temperature limits.

<sup>2</sup> To ensure lead coplanarity ( $\pm 0.002$  inches) and solderability, handling with bare hands should be avoided and the device should be stored in environments at 24°C  $\pm$  5°C (75°F  $\pm$  10°F) with relative humidity not to exceed 65%.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Package Thermal Resistance

Airflow (m/s)	$\theta_{JA}$ (°C/W)
0	42.7
1	37.8
2	36.4

For liquid-cooled applications,  $\theta_{JC} = 3.0^\circ\text{C/W}$ .

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

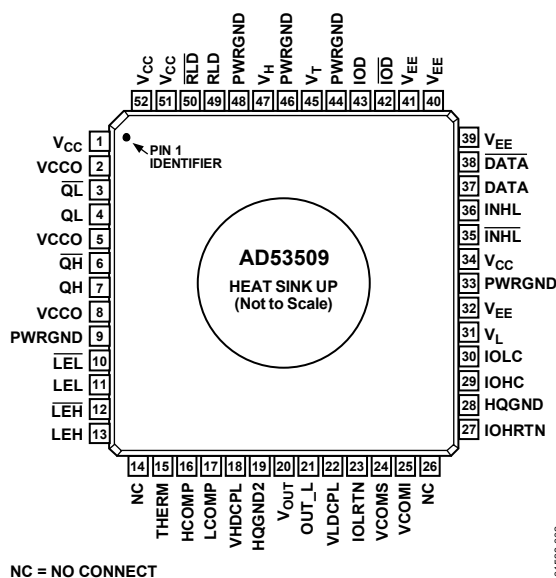


Figure 2. Pin Configuration

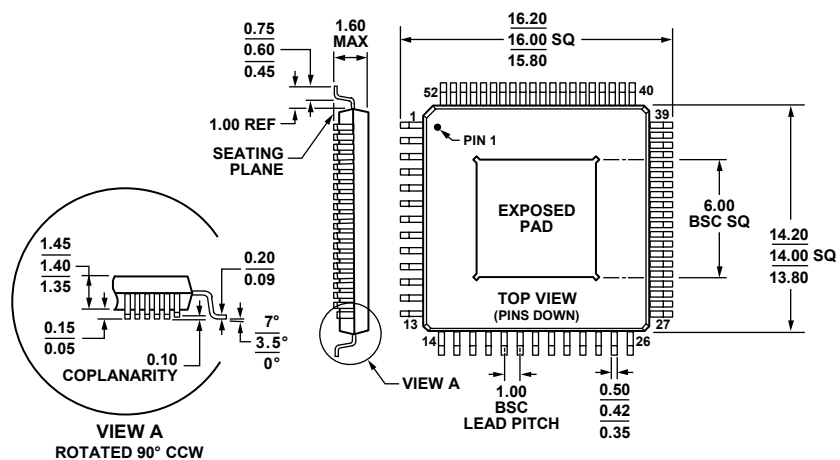
Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 34, 51, 52	V <sub>CC</sub>	Positive Power Supply.
2, 5, 8	V <sub>CCO</sub>	Comparator Output Power Supply.
3	$\overline{QL}$	Comparator Low Output, Inverting.
4	QL	Comparator Low Output, Noninverting.
6	$\overline{QH}$	Comparator High Output, Inverting.
7	QH	Comparator High Output, Noninverting.
9, 33, 44, 46, 48	PWRGND	Ground.
10	$\overline{LEL}$	Latch Enable Low Input, Inverting.
11	LEL	Latch Enable Low Input, Noninverting.
12	$\overline{LEH}$	Latch Enable High Input, Inverting.
13	LEH	Latch Enable High Input, Noninverting.
14, 26	NC	Do not connect.
15	THERM	Temperature Sensor Output.
16	HCOMP	High Comparator Threshold.
17	LCOMP	Low Comparator Threshold.
18	VHDCPL	Connect 39 nF compensation capacitor to V <sub>EE</sub> .
19	HQGND2	Ground.
20	V <sub>OUT</sub>	DUT Connection.
21	OUT_L	Active Load Output.
22	VLDCPL	Connect 39 nF compensation capacitor to V <sub>EE</sub> .
23	IOLRTN	Active Load Low Inhibit Control.
24	VCOMS	VCOM Buffer Sense Output.
25	VCOMI	VCOM Input Voltage.
27	IOHRTN	Active Load High Inhibit Control.
28	HQGND	Ground.
29	IOHC	Active Load High Current Control Input.
30	IOLC	Active Load Low Current Control Input.

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Pin No.	Mnemonic	Description
31	$V_L$	Low Driver Level.
32, 39, 40, 41	$V_{EE}$	Negative Power Supply.
35	$\overline{INHL}$	Inhibit Load Input, Inverting.
36	INHL	Inhibit Load Input, Noninverting.
37	$\overline{DATA}$	Drive Data Input, Noninverting.
38	DATA	Drive Data Input, Inverting.
42	$\overline{IOD}$	IO Data Input, Inverting.
43	IOD	IO Data Input, Noninverting.
45	$V_T$	Term Driver Level.
47	$V_H$	High Driver Level.
49	$\overline{RLD}$	$V_T$ /Inhibit Selection Input, Noninverting.
50	RLD	$V_T$ /Inhibit Selection Input, Inverting.

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BEA-HU

Figure 3. 52-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP\_EP] (SW-52-1)

Dimensions shown in millimeters

022708-A

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
AD53509JSW	0°C to 70°C	52-Lead LQFP_EP	SW-52-1	90
AD53509JSWZ <sup>1</sup>	0°C to 70°C	52-Lead LQFP_EP	SW-52-1	90

<sup>1</sup> Z = RoHS Compliant Part.

**AD53509**

**NOTES**