Quad Ultrahigh-Speed Pin Driver with High-Z and V_{TERM} Modes

AD53513

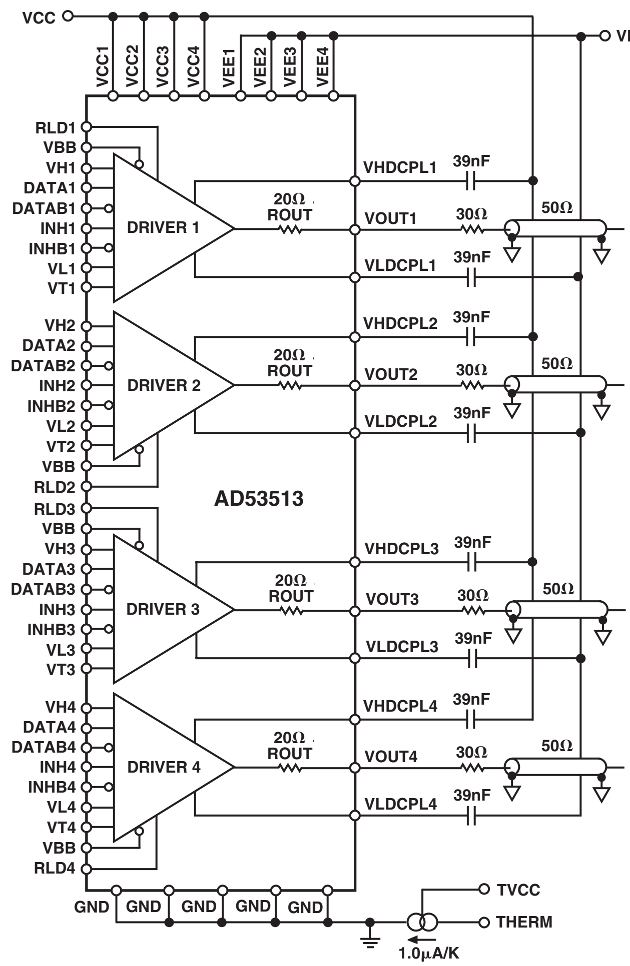
FEATURES
500 MHz Driver Operation (1 Gb/s)
Driver Inhibit Function
100 ps Edge Matching
Guaranteed Industry Specifications
- **20 Ω Output Impedance**
- **5 V/ns Slew Rate**
- **Variable Output Voltages for ECL, TTL, and CMOS**

High-Speed Differential Inputs for Maximum Flexibility
Ultrasmall 100-Lead LQFP Package with Built-In Heat Sink

APPLICATIONS
Automatic Test Equipment
- **Semiconductor Test Systems**
- **Board Test Systems**

Instrumentation and Characterization Equipment

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD53513 is a quad high-speed pin driver designed for use in digital or mixed-signal test systems. Combining a high-speed monolithic process with a convenient surface-mount package, this product attains superb electrical performance while preserving optimum packaging densities and long-term reliability in a 100-lead, LQFP package with built-in heat sink.

Featuring unity gain programmable output levels of –2.5 V to +5.5 V, with output swing capability of less than 200 mV to 8 V, the AD53513 is designed to stimulate ECL, TTL, and CMOS logic families, as well as high-speed memory. The 1.0 Gb/s data rate capacity and matched output impedance allow for real-time stimulation of these digital logic families. To test I/O devices, the pin driver can be switched into a high impedance state (Inhibit Mode), electrically removing the driver from the path. The pin driver leakage current in inhibit is typically 100 nA and output charge transfer entering inhibit is typically less than 20 pC.

The AD53513 transition from HI/LO or to inhibit is controlled through the data and inhibit inputs. The input circuitry uses high-speed differential inputs with a common-mode range of ±2 V. This allows for direct interface to precision differential ECL timing. The analog logic HI/LO inputs are equally easy to interface. Typically requiring 10 µA of bias current, the AD53513 can be directly coupled to the output of a digital-to-analog converter.

Each channel of the AD53513 has a Mode Select Pin RLD, which is a single-sided logic input. The logic threshold is set by the VBB input which is common to all four channels. The RLD Mode Select controls whether inhibit puts the driver in High-Z or V_{TERM} mode. (Refer to Table I.) All of the digital logic inputs (DATA, DATAB, INH, INHB, RLD, VBB), must share a common set of logic levels. The VBB threshold should be set to the midrange of the logic levels. For example, if ECL levels of –0.8 V to –1.8 V are used, VBB should be set to –1.3 V.

The AD53513 is available in a 100-lead, LQFP package with a built-in heat sink and is specified to operate over the ambient commercial temperature range of –25°C to +85°C.

REV. 0

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AD53513–SPECIFICATIONS

(All specifications are at T_J = 85°C ± 5°C, +V_S = +9 V ± 3%, –V_S = –6 V ± 3% unless otherwise noted. All temperature coefficients are measured at T_J = 75°C–95°C). (A 39 nF capacitor must be connected between V_{CC} and V_{HDCPL} and between V_{EE} and V_{LDCPL}.)

Parameter	Min	Typ*	Max	Unit	Test Conditions
DIFFERENTIAL INPUT CHARACTERISTICS					
(Data to $\overline{DATA}$, INH to $\overline{INH}$), RLD, VBB					V_{BB} = –1.3 V
Input Voltage	–2		0	Volts	
Differential Input Range		ECL			
Bias Current	–1		+1	mA	V_{IN} = –2 V, 0.0 V
VBB Threshold Input		Midrange		V	Set to Midrange of Logic Levels
REFERENCE INPUTS (V_L, V_H, V_T)					
Bias Currents	–50		+50	µA	V_L, V_H = 2 V
OUTPUT CHARACTERISTICS					
Logic High Range	–2.3		+5.5	Volts	DATA = H
Logic Low Range	–2.5		+5.3	Volts	DATA = L
Amplitude (V_H–V_L)	0.2		8.0	Volts	
Absolute Accuracy					
V_H Offset	–100		+100	mV	DATA = H, V_H = 0 V, V_L = –2 V, V_T = +3 V
V_H Gain and Linearity Error		±0.3 ±5		% of V_H + mV	DATA = H, V_H = –2 V to +5 V, V_L = –2.5 V, V_T = +3 V
V_L Offset	–100		+100	mV	DATA = L, V_L = 0 V, V_H = +5 V, V_T = +4.5 V
V_L Gain and Linearity Error		±0.3 ±5		% of V_L + mV	DATA = L, V_L = –2 V to +5 V, V_H = +5.5 V, V_T = +4.5 V
V_T Offset	–100		+100	mV	Term Mode, V_T = 0 V, V_L = –1 V, V_H = +3 V
V_T Gain and Linearity Error		±0.3 ±5		% of V_T + mV	Term Mode, V_T = –2.0 V to +5.0 V, V_L = 0, V_H = +3 V
Offset TC, V_H, or V_L, or V_{TERM}		±0.5		mV/°C	V_L, V_H = 0 V
Output Resistance		20		Ω	DATA = H, V_H = 3 V, V_L = 0 V, I_{OUT} = 45 mA
Output Leakage	–1.0		+1.0	µA	V_{OUT} = –2 V to +5 V
Dynamic Current Limit		130		mA	C_{BYP} = 39 nF, V_H = +5 V, V_L = –2 V
Static Current Limit		±85		mA	Output to –2.5 V, V_H = +5.5 V, V_L = –2.5 V, V_T = 0; DATA = H and Output to 5.5 V, V_H = +5.5 V, V_L = –2.5 V, V_T = 0 V_L = –3 V, DATA = L
PSRR, Drive Mode		35		dB	V_S = V_S ± 3%
DYNAMIC PERFORMANCE, DRIVE					
(V_H and V_L)					
Propagation Delay Time	0.3		1.1	ns	Measured at 50%, V_H = 800 mV, 50 Ω Load, V_L = –800 mV
Propagation Delay TC		±0.5		ps/°C	Measured at 50%, V_H = 800 mV, 50 Ω Load, V_L = –800 mV
Delay Matching, Edge to Edge		100		ps	Measured at 50%, V_H = 800 mV, 50 Ω Load, V_L = –800 mV
Rise and Fall Time					
1 V Swing		300		ps	Measured 20%–80%, V_L = 0 V, V_H = 1 V, V_T = –2 V
2 V Swing		450		ps	Measured 10%–90%, V_L = 0 V, V_H = 2 V, V_T = –2 V
3 V Swing		650		ps	Measured 10%–90%, V_L = 0 V, V_H = 3 V, V_T = –2 V
Rise and Fall Time TC					
1 V Swing		±1		ps/°C	Measured 20%–80%, V_L = 0 V, V_H = 1 V, V_T = –2 V
2 V Swing		±1		ps/°C	Measured 10%–90%, V_L = 0 V, V_H = 2 V, V_T = –2 V
3 V Swing		±1		ps/°C	Measured 10%–90%, V_L = 0 V, V_H = 3 V, V_T = –2 V
Overshoot, Undershoot, and Preshoot		±(6% +50 mV)		% of Step + mV	a. V_L, V_H = 0 V, +1 V, V_T = –2 V, 50 Ω b. V_L, V_H = 0 V, +3 V, V_T = –2 V, 50 Ω c. V_L, V_H = 0 V, +5 V, V_T = –2 V, 50 Ω
Settling Time					
to 15 mV		50		ns	V_L = 0 V, V_H = +0.5 V, V_T = –2 V
to 4 mV		10		µs	V_L = 0 V, V_H = +0.5 V, V_T = –2 V
Delay Change vs. Pulsewidth		10		ps	V_L = 0 V, V_H = +2 V, V_T = –2 V, Pulsewidth/Period = 1.0 ns/4.0 ns, 30 ns/120 ns
Minimum Pulsewidth					
2 V Swing		700		ps	700 ps Input, 10%/90% Output, V_T = –2 V, V_L = 0 V, V_H = +2 V, 50 Ω Terminated
Toggle Rate		3.2		GHz	V_L = –1.8 V, V_H = –0.8 V, V_T = –2 V, V_{OUT} > 300 mV p-p at 50 Ω Terminated

Parameter	Min	Typ*	Max	Unit	Test Conditions
DYNAMIC PERFORMANCE, INHIBIT					
Delay Time, Active to Inhibit	1.5		2.5	ns	Measured at 50%, V_H = +2 V, V_L = –2 V, V_T = –2 V
Delay Time, Inhibit to Active	0.7		1.7	ns	Measured at 50%, V_H = +2 V, V_L = –2 V, V_T = –2 V
I/O Spike		<200		mV p-p	V_H = 0 V, V_L = 0 V, V_T = –2 V
Output Capacitance		6		pF	Driver Inhibited
DYNAMIC PERFORMANCE, V_{TERM}					
Delay Time, Active to V_{TERM}	0.50		1.30	ns	Measured at 50%, V_H = +0.8 V, V_L = –0.8 V, V_T = 0 V
Delay Time, V_{TERM} to Active	0.45		1.25	ns	50 Ω Terminated
Overshoot, Undershoot, and Preshoot					V_L = –2 V, V_H = +2 V, V_T = 0 V
V_{TERM} to V_L or V_H		±6%/±75		mV	V_L = –0.8 V, V_H = +0.8 V, V_T = 0 V Output Terminated 50 Ω
POWER SUPPLIES					
Total Supply Range		15		V	
Positive Supply		9		V	
Negative Supply		–6		V	
Positive Supply Current			570	mA	
Negative Supply Current			570	mA	
Total Power Dissipation			8.6	W	
Temperature Sensor Gain Factor		1.0		µA/K	R_{LOAD} = 4.2 kΩ, V_{SOURCE} = 9 V

NOTES
Connecting or shorting the decoupling capacitors to ground will result in the destruction of the device.
*Typical parameters are not production tested but guaranteed through characterization.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage
- $+V_S$ to GND . . . . . 11 V
- $–V_S$ to GND . . . . . –7 V
- $+V_S$ to $–V_S$ . . . . . 18 V

Inputs
- DATA, $\overline{\text{DATA}}$, INH, $\overline{\text{INH}}$, RLD, VBB . . . . . +5 V, –3 V
- DATA to $\overline{\text{DATA}}$, INH to $\overline{\text{INH}}$, RLD, VBB . . . . . ±3 V
- V_H, V_L, V_T to GND . . . . . +7 V, –2 V
- V_H to V_L ($V_H – V_T$) and ($V_T – V_L$) . . . . . ±9 V

Outputs
- V_{OUT} Short Circuit Duration . . . . . Indefinite[2]

V_{OUT} Range in Inhibit Mode
- V_{HDCPL} . . . . . Do Not Connect Except for Capacitor to V_{CC}
- V_{LDCPL} . . . . . Do Not Connect Except for Capacitor to V_{EE}
- THERM . . . . . 11 V, 0 V

Environmental
- Operating Temperature (Junction) . . . . . 175°C
- Storage Temperature . . . . . –65°C to +150°C
- Lead Temperature (Soldering, 10 sec)[3] . . . . . 260°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Absolute maximum limits apply individually, not in combination. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Output short circuit protection is guaranteed as long as proper heat sinking is employed to ensure compliance with the operating temperature limits.
[3]To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in environments at 24°C ±5°C (75°F ±10°F) with relative humidity not to exceed 65%.

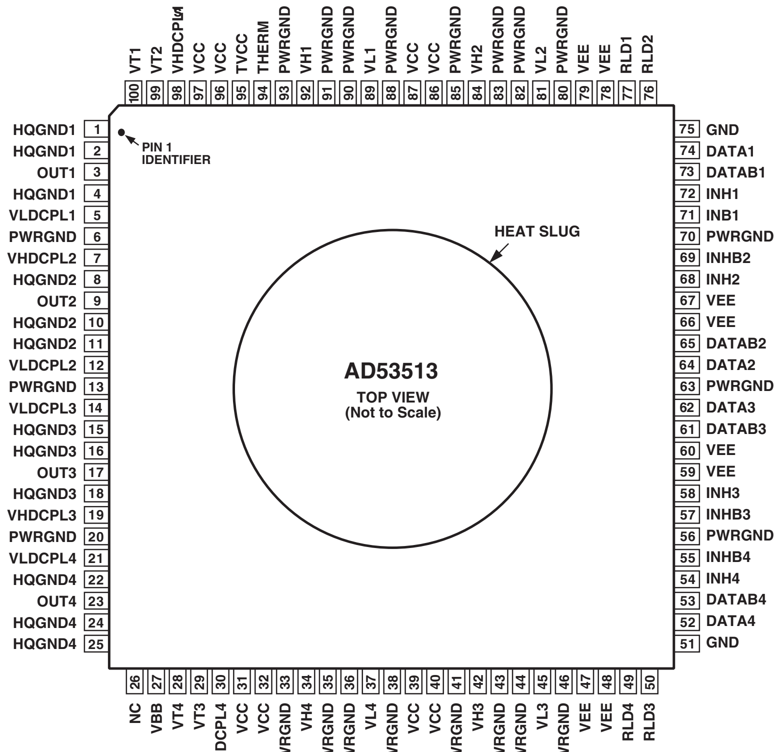
ORDERING GUIDE

Model	Package Description	Shipment Method, Quantity Per Shipping Container	Package Option
AD53513JSQ	100-Lead LQFP-CDQUAD	Tray, 90 Pieces	SQ-100

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53513 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



NC = NO CONNECT

NOTE THAT THE DIE IS MOUNTED TO THE BACK OF THE HEAT SLUG.
THE PACKAGE IS MOUNTED TO THE BOARD HEAT SLUG UP.

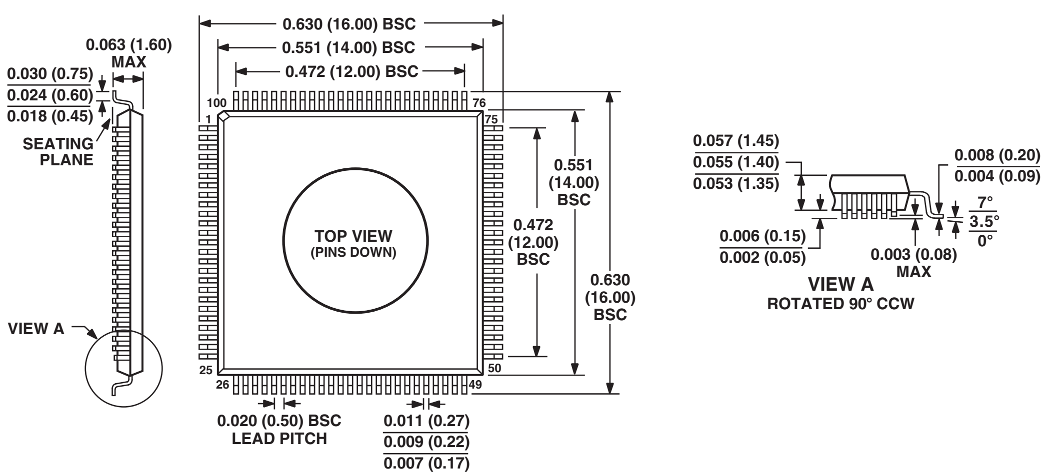
Table I. Driver Truth Table

DATA	$\overline{DATA}$	INH	$\overline{INH}$	RLD	VBB	Output State
0	1	0	1	X	VBB	V_L
1	0	0	1	X	VBB	V_H
X	X	1	0	0	VBB	INH
X	X	1	0	1	VBB	V_{TERM}

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

100-Lead LQFP_ED Package
(SQ-100)



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