

### FEATURES

- Complete 16-channel, 16-bit DAC**
- 8 software-programmable output ranges:  $-20\text{ V}$  to  $0\text{ V}$ ,  $-16\text{ V}$  to  $0\text{ V}$ ,  $-10\text{ V}$  to  $0\text{ V}$ ,  $-10\text{ V}$  to  $+6\text{ V}$ ,  $-12\text{ V}$  to  $+14\text{ V}$ ,  $-16\text{ V}$  to  $+10\text{ V}$ ,  $\pm 5\text{ V}$  and  $\pm 10\text{ V}$**
- Integrated DAC output buffers with  $\pm 20\text{ mA}$  output current capability**
- Integrated reference buffers**
- 2 dither signal input pads**
- Channel monitoring multiplexer**
- 1.8 V logic compatibility**
- Temperature range:  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$**

### APPLICATIONS

- Mach-Zehnder modulator bias control**
- Optical networking**
- Instrumentation**
- Industrial automation**
- Data acquisition systems**
- Analog output modules**

### GENERAL DESCRIPTION

The AD5766-KGD is a 16-channel, 16-bit, voltage output denseDAC<sup>®</sup> digital-to-analog converter (DAC).

The DAC generates output voltage ranges from an external 2.5 V reference. Depending on the voltage range selected, the midpoint of the output span can be adjusted, allowing a minimum output voltage as low as  $-20\text{ V}$  or a maximum output

voltage of up to  $+14\text{ V}$ . Each of the 16 channels can be monitored with an integrated output voltage multiplexer.

The AD5766-KGD has integrated output buffers that can sink or source up to  $20\text{ mA}$ . In conjunction with these buffers, a low frequency signal can be superimposed onto each DAC output via dedicated dither pads. These dedicated dither pads simplify the system design by reducing the number of external components required for a similar external implementation, like operational amplifiers or resistors. The reduction of external components makes the AD5766-KGD suitable for indium phosphide (InP) Mach-Zehnder modulator (MZM) biasing applications.

The device incorporates a power-on reset (POR) circuit that ensures that the DAC outputs are clamped to ground on power-up and remain at this level until the output range of the DAC is configured. The outputs of all DACs are updated through register configuration, with the added functionality of user-selectable DAC channels to be simultaneously updated.

The AD5766-KGD uses a versatile 4-wire serial interface that operates at clock rates of up to  $50\text{ MHz}$  for write mode and is compatible with serial peripheral interface (SPI), QSPI<sup>™</sup>, MICROWIRE<sup>™</sup>, and DSP interface standards. The AD5766-KGD also contains a  $V_{\text{LOGIC}}$  pad intended for 1.8 V/3.3 V/5 V logic.

Additional application and technical information can be found in the [AD5766](#) data sheet.

Known good die (KGD): these die are fully guaranteed to data sheet specifications.

### FUNCTIONAL BLOCK DIAGRAM

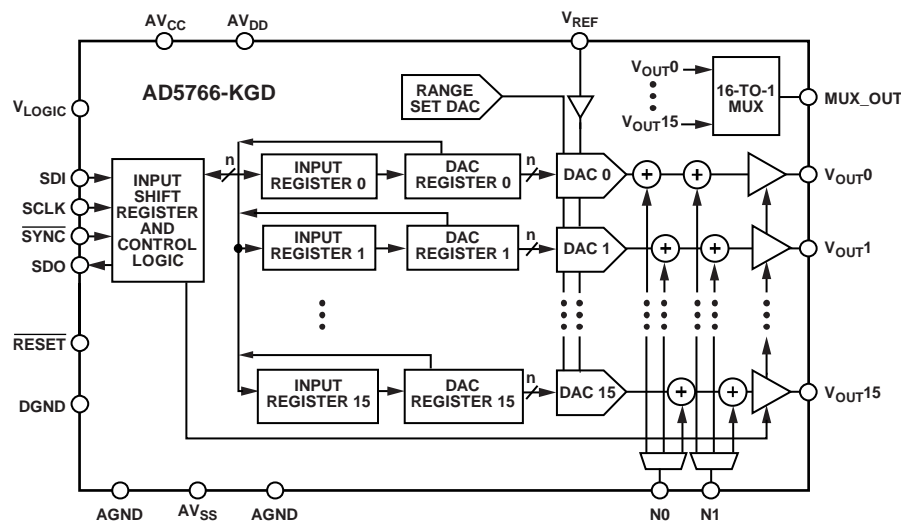


Figure 1.

Rev. 0

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**REVISION HISTORY**

2/2018—Revision 0: Initial Version

## SPECIFICATIONS

$V_{CC} = 2.97\text{ V to }3.6\text{ V}$ ,  $V_{LOGIC} = 1.7\text{ V to }5.5\text{ V}$ ,  $V_{DD} = 2.97\text{ V to }16\text{ V}$ ,  $V_{SS} = -22\text{ V to }-7\text{ V}$ ,  $AGND = DGND = 0\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , output range =  $\pm 5\text{ V}$ ,  $V_{OUTX}$  unloaded, all specifications  $T_{MIN}$  to  $T_{MAX}$ , typical specifications at  $T_A = 25^\circ\text{C}$ , dither powered on, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	16			Bits	
Relative Accuracy (INL)	-16		+16	LSB	
Differential Nonlinearity	-1		+1	LSB	Guaranteed monotonic by design
Bipolar Zero Error	-85	$\pm 12$	+85	mV	$\pm 5\text{ V}$ range
	-110	$\pm 13$	+110	mV	-10 V to +6 V range
	-120	$\pm 15$	+120	mV	$\pm 10\text{ V}$ range
	-145	$\pm 16$	+145	mV	-12 V to +14 V range
	-145	$\pm 16$	+145	mV	-16 V to +10 V range
Bipolar Zero Error Temperature Coefficient (TC)		$\pm 2$		ppm FSR/ $^\circ\text{C}$	
Zero-Scale Error					All 0s loaded to DAC register
	-80	$\pm 25$	+80	mV	-10 V to 0 V range
	-80	$\pm 25$	+80	mV	$\pm 5\text{ V}$ range
	-110	$\pm 35$	+110	mV	-16 V to 0 V range
	-110	$\pm 35$	+110	mV	-10 V to +6 V range
	-130	$\pm 35$	+130	mV	-20 V to 0 V range
	-130	$\pm 35$	+130	mV	$\pm 10\text{ V}$ range
	-140	$\pm 45$	+140	mV	-12 V to +14 V range
	-140	$\pm 45$	+140	mV	-16 V to +10 V range
Zero-Scale Error TC		$\pm 2$		ppm FSR/ $^\circ\text{C}$	
Full-Scale Error					All 1s loaded to DAC register.
	-0.9	$\pm 0.23$	+0.9	% FSR	-10 V to 0 V range
	-0.9	$\pm 0.23$	+0.9	% FSR	$\pm 5\text{ V}$ range
	-0.8	$\pm 0.2$	+0.8	% FSR	-16 V to 0 V range
	-0.8	$\pm 0.2$	+0.8	% FSR	-10 V to +6 V range
	-0.7	$\pm 0.18$	+0.7	% FSR	-20 V to 0 V range
	-0.7	$\pm 0.18$	+0.7	% FSR	$\pm 10\text{ V}$ range
	-0.6	$\pm 0.15$	+0.6	% FSR	-12 V to +14 V range
	-0.6	$\pm 0.15$	+0.6	% FSR	-16 V to +10 V range
Full-Scale Error Drift		$\pm 3$		ppm FSR/ $^\circ\text{C}$	
Gain Error	-0.4	$\pm 0.07$	+0.4	% FSR	
Gain Error TC		$\pm 2$		ppm FSR/ $^\circ\text{C}$	
Offset Error	-80	$\pm 25$	+80	mV	-10 V to 0 V range
	-80	$\pm 25$	+80	mV	$\pm 5\text{ V}$ range
	-110	$\pm 35$	+110	mV	-16 V to 0 V range
	-110	$\pm 35$	+110	mV	-10 V to +6 V range
	-130	$\pm 35$	+130	mV	-20 V to 0 V range
	-130	$\pm 35$	+130	mV	$\pm 10\text{ V}$ range
	-140	$\pm 45$	+140	mV	-12 V to +14 V range
	-140	$\pm 45$	+140	mV	-16 V to +10 V range
Offset Error Drift		$\pm 2$		$\mu\text{V}/^\circ\text{C}$	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Total Unadjusted Error	-0.9	±0.18	+0.9	% FSR	-10 V to 0 V range
	-0.9	±0.18	+0.9	% FSR	±5 V range
	-0.8	±0.15	+0.8	% FSR	-16 V to 0 V range
	-0.8	±0.15	+0.8	% FSR	-10 V to +6 V range
	-0.7	±0.13	+0.7	% FSR	-20 V to 0 V range
	-0.7	±0.13	+0.7	% FSR	±10 V range
	-0.6	±0.12	+0.6	% FSR	-12 V to +14 V range
	-0.6	±0.12	+0.6	% FSR	-16 V to +10 V range
DC Crosstalk		30		μV	Due to output voltage change
		35		μV/mA	Due to load current change (1 LSB)
<b>OUTPUT CHARACTERISTICS</b>					
Output Voltage Ranges <sup>1</sup>	-20		0	V	
	-16		0	V	
	-10		0	V	
	-10		+6	V	
	-12		+14	V	
	-16		+10	V	
	-5		+5	V	
	-10		+10	V	
Output Current	-20		+20	mA	
Capacitive Load Stability			1	nF	
DC Output Impedance		0.2		Ω	
Short-Circuit Current		±60		mA	Single channel only
Output Amplifier Bandwidth		108		kHz	
<b>REFERENCE INPUT</b>					
Reference Input Voltage		2.5		V	±1% for specified performance
Reference Range	2.375		2.625	V	Functional performance only
DC Input Impedance	2.5			MΩ	
Input Current			1	μA	
<b>DITHER INPUTS</b>					
Dither Frequency		10		kHz	Lower -3 dB point
		100		kHz	Upper -3 dB point
Amplitude			0.25	V p-p	Peak-to-peak ac voltage
	0		AV <sub>CC</sub>	V	Peak-to-peak ac and dc voltage
DC Shift	-2	±1	+2	LSB	
Dither Transient					Dither enabled/disabled, N0 and N1 floating
Dither Selected Channel		5		nV-sec	AV <sub>CC</sub> = 2.97 V and AV <sub>CC</sub> = 3.6 V
Dither Nonselected Channels		2		nV-sec	AV <sub>CC</sub> = 2.97 V and AV <sub>CC</sub> = 3.6 V
Dither Crosstalk <sup>1</sup>		-70		dB	10 kHz dither frequency
		-55		dB	100 kHz dither frequency
<b>LOGIC INPUTS</b>					
Input High Voltage, V <sub>IH</sub>	0.7 × V <sub>LOGIC</sub>			V	
Input Low Voltage, V <sub>IL</sub>			0.3 × V <sub>LOGIC</sub>	V	
Input Current	-2		+2	μA	Per pad
	-6		+6	μA	RESET pad pulled high
	-57		+57	μA	RESET pad pulled low
Input Capacitance		2		pF	Per pad
<b>LOGIC OUTPUT</b>					
Output Low Voltage			0.4	V	Sinking 200 μA
Output High Voltage	V <sub>LOGIC</sub> - 0.4			V	Sourcing 200 μA
High Impedance Leakage Current	-1		+1	μA	
High Impedance Output Capacitance		5		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>VOLTAGE MONITOR PAD (MUX_OUT)</b>					
Impedance		1.3		k $\Omega$	
Three-State Leakage Current	-1	0.006	+1	$\mu$ A	
Continuous Current	-1		+1	mA	Die temperature below 105°C
Glitch Impulse		0.2		nV-sec	V <sub>OUTX</sub> glitch due to mux enable
Voltage Settling Time		12		$\mu$ s	¼ to ¾ scale settling to $\pm 0.5$ LSB, $\pm 5$ V range and -10V to 0V range
<b>POWER SUPPLIES</b>					
AV <sub>DD</sub>	2.97		16	V	AV <sub>DD</sub> - AV <sub>SS</sub> must be less than or equal to 30V
AV <sub>SS</sub>	-22		-7	V	AV <sub>DD</sub> - AV <sub>SS</sub> must be less than or equal to 30V
AV <sub>CC</sub>	2.97		3.6	V	
V <sub>LOGIC</sub>	1.7		5.5	V	
Headroom/Footroom		$\pm 0.7$		V	Output voltage offset to $\pm 2$ LSB for 20 mA output load; applies to AV <sub>DD</sub> and AV <sub>SS</sub>
		$\pm 2$		V	Output voltage offset to $\pm 1$ LSB for 20 mA output load; applies to AV <sub>DD</sub> and AV <sub>SS</sub>
<b>Normal Mode</b>					
AI <sub>DD</sub>		6	9	mA	All output ranges, -40°C to +105°C
AI <sub>SS</sub>	-11	-9		mA	All output ranges, -40°C to +105°C
AI <sub>CC</sub>		8.3	10	mA	All output ranges, -40°C to +105°C
IL <sub>LOGIC</sub>		0.02	1	$\mu$ A	All output ranges, -40°C to +105°C, V <sub>IH</sub> = V <sub>LOGIC</sub> , V <sub>IL</sub> = DGND
<b>DC Power Supply Rejection Ratio (PSRR)</b>					
		50		$\mu$ V/V	AV <sub>DD</sub> power supply
		50		$\mu$ V/V	AV <sub>SS</sub> power supply
		3		mV/V	AV <sub>CC</sub> power supply
<b>AC PSRR</b>					
		-80		dB	AV <sub>DD</sub> power supply, at 50 Hz
		-80		dB	AV <sub>SS</sub> power supply, at 50 Hz
		-50		dB	AV <sub>CC</sub> power supply, at 50 Hz

<sup>1</sup> Output amplifier headroom requirement is 2V minimum.

$V_{CC} = 2.97\text{ V to }3.6\text{ V}$ ,  $V_{LOGIC} = 1.7\text{ V to }5.5\text{ V}$ ,  $V_{DD} = 2.97\text{ V to }16\text{ V}$ ,  $V_{SS} = -22\text{ V to }-7\text{ V}$ ,  $AGND = DGND = 0\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , output range =  $\pm 5\text{ V}$ ,  $V_{OUTX}$  unloaded, all specifications  $T_{MIN}$  to  $T_{MAX}$ , typical specifications at  $T_A = 25^\circ\text{C}$ , dither powered off, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BIPOLAR ZERO ERROR	-50	$\pm 11$	+50	mV	$\pm 5\text{ V range}$
	-75	$\pm 12$	+75	mV	-10 V to +6 V range
	-90	$\pm 12$	+90	mV	$\pm 10\text{ V range}$
	-110	$\pm 13$	+110	mV	-12 V to +14 V range
	-110	$\pm 13$	+110	mV	-16 V to +10 V range
ZERO-SCALE ERROR	-50	$\pm 15$	+50	mV	All 0s loaded to DAC register -10 V to 0 V range
	-50	$\pm 15$	+50	mV	$\pm 5\text{ V range}$
	-75	$\pm 20$	+75	mV	-16 V to 0 V range
	-75	$\pm 20$	+75	mV	-10 V to +6 V range
	-90	$\pm 25$	+90	mV	-20 V to 0 V range
	-90	$\pm 25$	+90	mV	$\pm 10\text{ V range}$
	-110	$\pm 35$	+110	mV	-12 V to +14 V range
	-110	$\pm 35$	+110	mV	-16 V to +10 V range
FULL-SCALE ERROR	-0.5	$\pm 0.15$	+0.5	% FSR	All 1s loaded to DAC register; all output ranges
GAIN ERROR	-0.3	$\pm 0.07$	+0.3	% FSR	All output ranges
OFFSET ERROR	-50	$\pm 15$	+50	mV	-10 V to 0 V range
	-50	$\pm 15$	+50	mV	$\pm 5\text{ V range}$
	-75	$\pm 20$	+75	mV	-16 V to 0 V range
	-75	$\pm 20$	+75	mV	-10 V to +6 V range
	-90	$\pm 25$	+90	mV	-20 V to 0 V range
	-90	$\pm 25$	+90	mV	$\pm 10\text{ V range}$
	-110	$\pm 35$	+110	mV	-12 V to +14 V range
-110	$\pm 35$	+110	mV	-16 V to +10 V range	
TOTAL UNADJUSTED ERROR	-0.5	$\pm 0.12$	+0.5	% FSR	All output ranges

**AC PERFORMANCE CHARACTERISTICS**

$AV_{CC} = 2.97\text{ V to }3.6\text{ V}$ ,  $V_{LOGIC} = 1.7\text{ V to }5.5\text{ V}$ ,  $AV_{DD} = 2.97\text{ V to }15\text{ V}$ ,  $AV_{SS} = -22\text{ V to }-7\text{ V}$ ,  $AGND = DGND = 0\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , output range =  $-10\text{ V to }0\text{ V}$ ,  $V_{OUTX}$  unloaded, all specifications  $T_{MIN}$  to  $T_{MAX}$ , typical specifications at  $T_A = 25^\circ\text{C}$ , dither powered on, analog dither signals not applied, unless otherwise noted.

**Table 3.**

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DYNAMIC PERFORMANCE<sup>1</sup></b>					
Output Voltage Settling Time		16			$\frac{1}{4}$ to $\frac{3}{4}$ scale settling to $\pm 0.5$ LSB, $\pm 5\text{ V}$ range and $-10\text{ V to }0\text{ V}$ range
		14			256 LSB step to $\pm 0.5$ LSB
Slew Rate		1		V/ $\mu\text{s}$	
Digital-to-Analog Glitch Energy		10		nV-sec	1 LSB change around major carry for 10 V span
Glitch Impulse Peak Amplitude		8		mV	
Digital Feedthrough		1		nV-sec	
Digital Crosstalk		2		nV-sec	
Analog Crosstalk		15		nV-sec	
DAC-to-DAC Crosstalk		15		nV-sec	
Total Harmonic Distortion		-80		dB	$V_{REF} = 2.5\text{ V} \pm 0.1\text{ V p-p}$ , frequency = 10 kHz, $AV_{CC} = 2.97\text{ V}$ and 3.6 V
		-75		dB	$V_{REF} = 2.5\text{ V} \pm 0.1\text{ V p-p}$ , frequency = 10 kHz, $AV_{CC} = 3.6\text{ V}$
Output Noise Spectral Density <sup>1</sup>		375		nV/ $\sqrt{\text{Hz}}$	$-10\text{ V to }0\text{ V}$ and $\pm 5\text{ V}$ ranges, frequency = 1 kHz
		605		nV/ $\sqrt{\text{Hz}}$	$-16\text{ V to }0\text{ V}$ and $-10\text{ V to }+6\text{ V}$ ranges, frequency = 1 kHz
		750		nV/ $\sqrt{\text{Hz}}$	$-20\text{ V to }0\text{ V}$ and $\pm 10\text{ V}$ ranges, frequency = 1 kHz
		835		nV/ $\sqrt{\text{Hz}}$	$-12\text{ V to }14\text{ V}$ and $-16\text{ V to }+10\text{ V}$ ranges, frequency = 1 kHz
		280		nV/ $\sqrt{\text{Hz}}$	$-10\text{ V to }0\text{ V}$ and $\pm 5\text{ V}$ ranges, frequency = 10 kHz
		440		nV/ $\sqrt{\text{Hz}}$	$-16\text{ V to }0\text{ V}$ and $-10\text{ V to }+6\text{ V}$ ranges, frequency = 10 kHz
		470		nV/ $\sqrt{\text{Hz}}$	$-20\text{ V to }0\text{ V}$ and $\pm 10\text{ V}$ ranges, frequency = 10 kHz
		610		nV/ $\sqrt{\text{Hz}}$	$-12\text{ V to }14\text{ V}$ and $-16\text{ V to }+10\text{ V}$ ranges, frequency = 10 kHz
Output Noise <sup>2</sup>					Dither disabled
		20		$\mu\text{V rms}$	$\pm 5\text{ V}$ range
		23		$\mu\text{V rms}$	$-10\text{ V to }0\text{ V}$ range
		33		$\mu\text{V rms}$	$-10\text{ V to }+6\text{ V}$ range
		38		$\mu\text{V rms}$	$-16\text{ V to }0\text{ V}$ range
		36		$\mu\text{V rms}$	$\pm 10\text{ V}$ range
		45		$\mu\text{V rms}$	$-20\text{ V to }0\text{ V}$ range
		45		$\mu\text{V rms}$	$-16\text{ V to }10\text{ V}$ range
		45		$\mu\text{V rms}$	$-12\text{ V to }14\text{ V}$ range

<sup>1</sup> DAC code = midscale.  $AV_{DD} = V_{OUT\_MAX} + 2\text{ V}$ .  $AV_{SS} = V_{OUT\_MIN} - 2\text{ V}$ .

<sup>2</sup> 0.1 Hz to 10 Hz.  $AV_{DD} = V_{OUT\_MAX} + 2\text{ V}$ .  $AV_{SS} = V_{OUT\_MIN} - 2\text{ V}$ .

**TIMING CHARACTERISTICS**

All input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  (10% to 90% of  $AV_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ . See Figure 2, Figure 3, and Figure 4.  $AV_{CC} = 2.97 \text{ V}$  to  $3.6 \text{ V}$ ,  $V_{LOGIC} = 1.7 \text{ V}$  to  $5.5 \text{ V}$ ,  $V_{REF} = 2.5 \text{ V}$ , all specifications  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ , dither powered on, unless otherwise noted.

Table 4.

Parameter	Limit at $T_{MIN}, T_{MAX}$	Unit	Description
$t_1^1$	20	ns min	SCLK cycle time
$t_2$	10	ns min	SCLK high time
$t_3$	10	ns min	SCLK low time
$t_4$	15	ns min	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time
$t_5$	15	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge time
$t_6$	20	ns min	Minimum $\overline{\text{SYNC}}$ high time (write mode)
$t_7$	5	ns min	Data setup time
$t_8$	5	ns min	Data hold time
$t_9$	4	$\mu\text{s}$ typ	DAC output settling time, 32 code step to $\pm 0.5$ LSB at 12-bit resolution (see Table 3)
$t_{10}$	100	ns typ	$\overline{\text{RESET}}^2$ pulse width low
$t_{11}$	100	ns typ	$\overline{\text{RESET}}^2$ pulse activation time
$t_{12}$	10	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK falling edge
$t_{13}$	40	ns max	SCLK rising edge to SDO valid ( $C_{L\_SDO}^3 = 15 \text{ pF}$ )
$t_{14}$	80	ns min	Minimum $\overline{\text{SYNC}}$ high time (readback/daisy-chain mode)
$t_{15}$	5	$\mu\text{s}$ typ	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{SYNC}}$ rising edge (DAC register updates)

<sup>1</sup> Maximum SCLK frequency is 50 MHz for write mode and 10 MHz for readback mode.  
<sup>2</sup> Minimum time between a reset and the subsequent successful write is typically 25 ns.  
<sup>3</sup>  $C_{L\_SDO}$  is the capacitive load on the SDO output.

**Timing Diagrams**

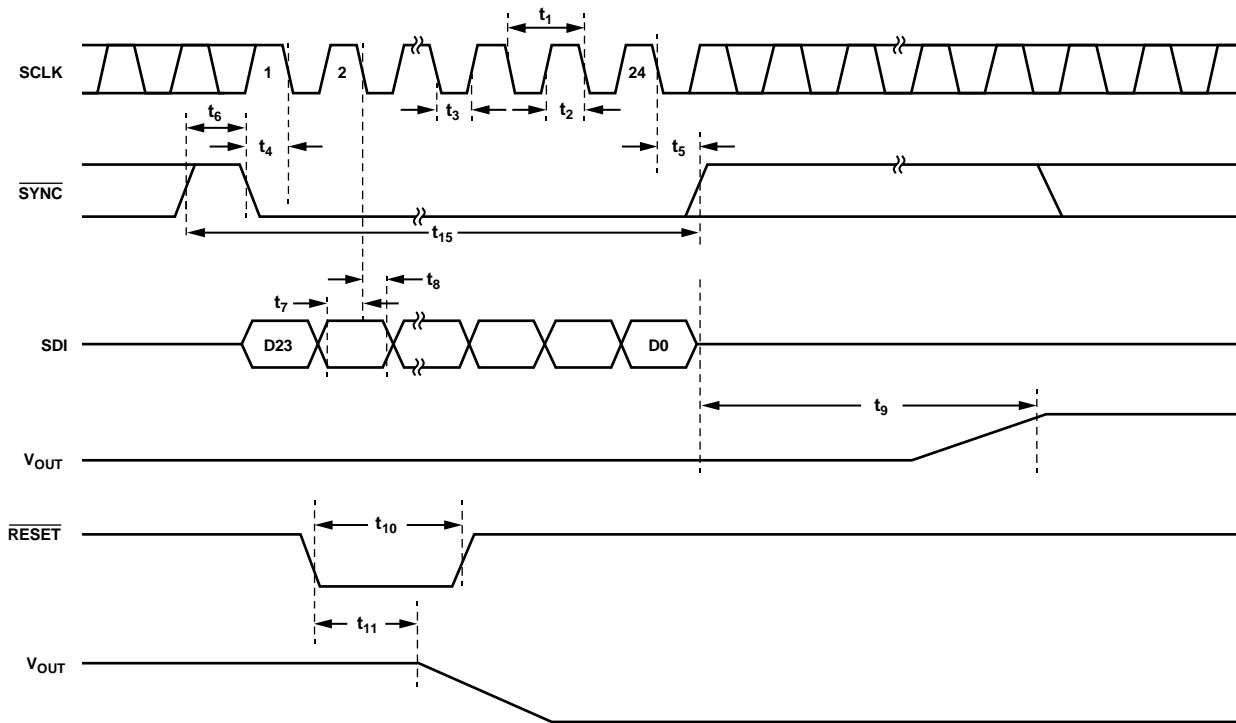


Figure 2. Serial Interface Timing Diagram

18461-1002



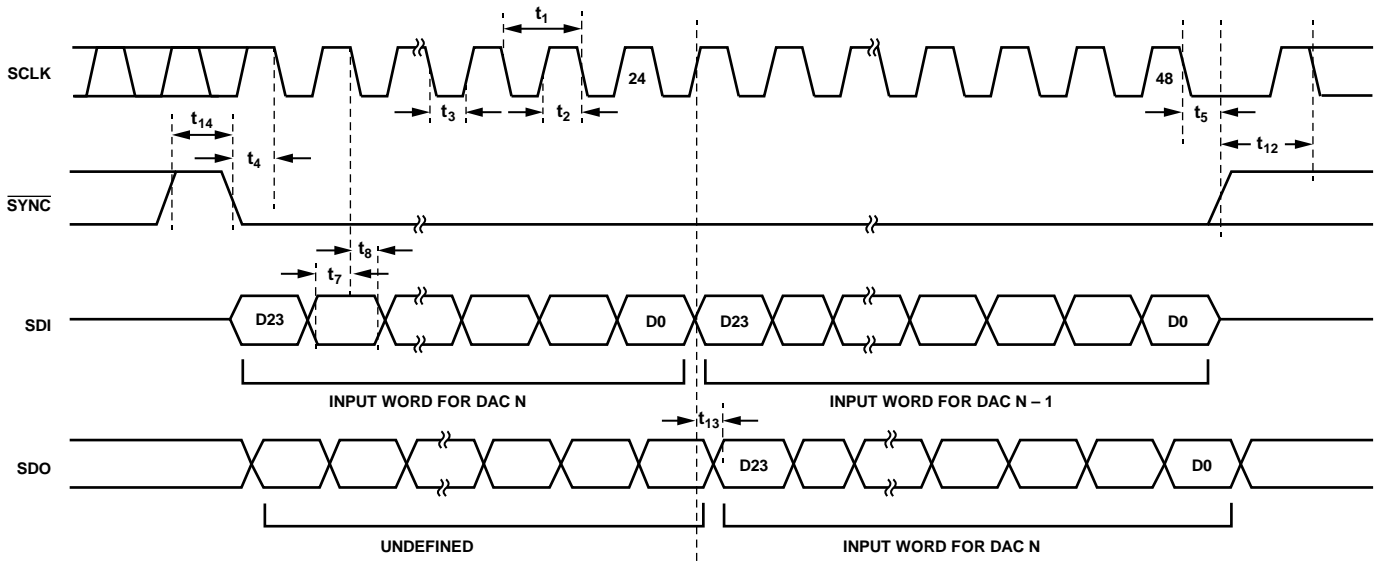
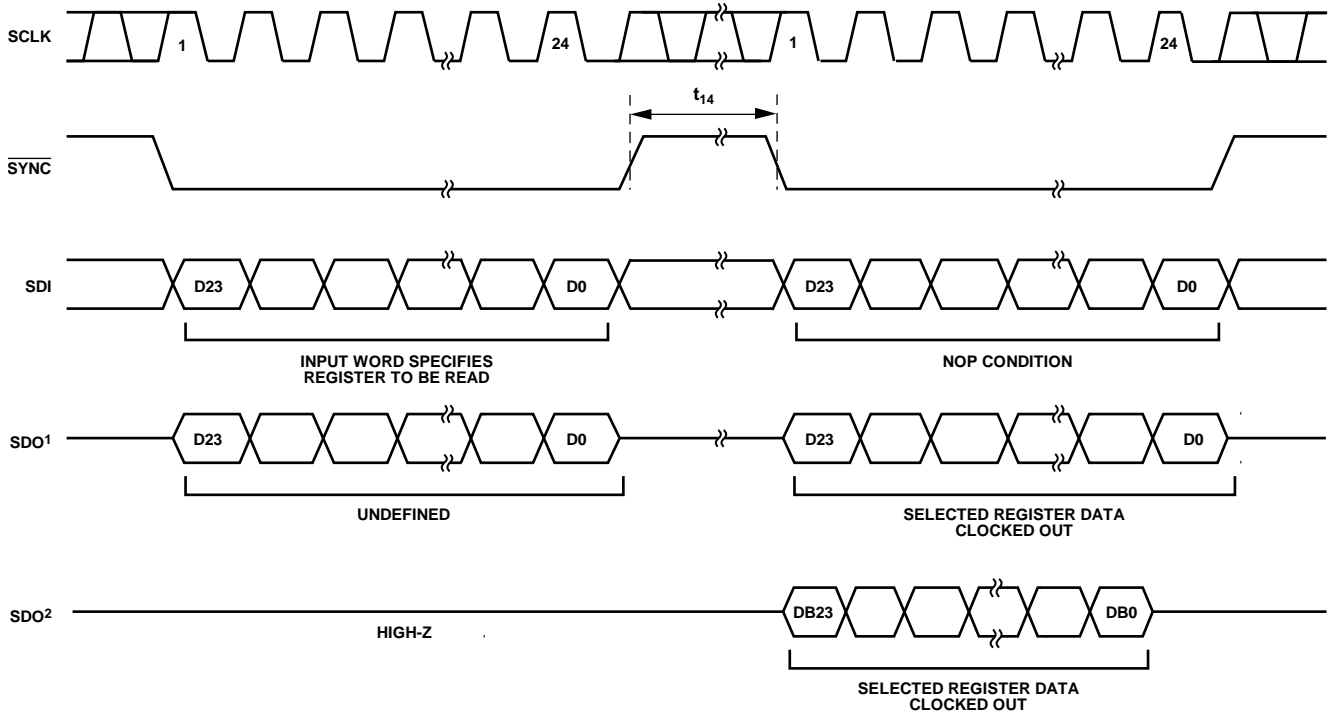


Figure 3. Daisy-Chain Timing Diagram

16461-003



<sup>1</sup>SDO OUTPUT BUFFER ENABLED  
<sup>2</sup>SDO OUTPUT BUFFER DISABLED

Figure 4. Readback Timing Diagram

16461-004

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted. Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 5.

Parameter	Rating
$AV_{DD}$ to AGND	-0.3 V to +34 V
$AV_{SS}$ to AGND	+0.3 V to -34 V
$AV_{DD}$ to $AV_{SS}$	-0.3 V to +34 V
$AV_{CC}$ to AGND	-0.3 V to +7 V
$AV_{CC}$ to AGND	-0.3 V to $AV_{DD} + 0.3$ V
$V_{LOGIC}$ to DGND	-0.3 V to +7 V
Digital Inputs <sup>1</sup> to DGND	-0.3 V to $V_{LOGIC} + 0.3$ V
Digital Output (SDO) to DGND	-0.3 V to $V_{LOGIC} + 0.3$ V
N0, N1 to AGND	-0.3 V to $AV_{CC} + 0.3$ V
$V_{REF}$ to AGND	-0.3 V to $AV_{CC} + 0.3$ V
$V_{OUTX}$ to AGND	$AV_{SS} - 0.3$ V to $AV_{DD} + 0.3$ V
AGND to DGND	-0.3 V to +0.3 V
Operating Temperature Range, $T_A$ Industrial	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature, $T_{JMAX}$	150°C
Power Dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Lead Temperature Soldering Reflow	260°C, as per JEDEC J-STD-020

<sup>1</sup> The digital inputs include  $\overline{\text{RESET}}$ , SCLK,  $\overline{\text{SYNC}}$ , and SDI.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

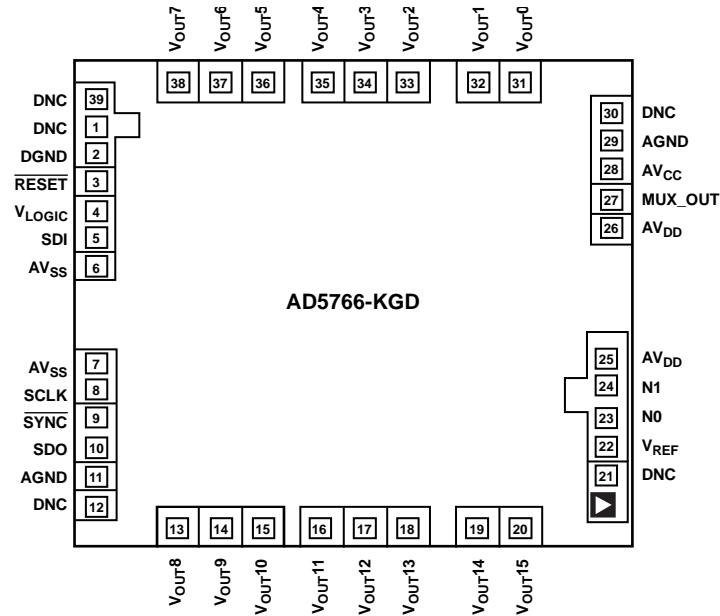
### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 5. Pad Configuration

16461-005

Table 6. Pad Function Descriptions

Pad No.	X-Axis (μm)	Y-Axis (μm)	Mnemonic	Description
Do Not Connect				
1	-1862.63	+1622.02	DNC	Do Not Connect. Do not connect to these pads.
12	-1857.46	-1682.62	DNC	Do Not Connect. Do not connect to these pads.
21	+1861.32	-1437.35	DNC	Do Not Connect. Do not connect to these pads.
30	+1861.32	+1646.88	DNC	Do Not Connect. Do not connect to these pads.
39	-1862.63	+1718.03	DNC	Do Not Connect. Do not connect to these pads.
Power Supplies and Reference Input				
2	-1862.63	+1520	DGND	Digital Ground.
4	-1878.06	+1165.93	V <sub>LOGIC</sub>	Digital Power Supply.
6	-1857.13	-828.93	AV <sub>SS</sub>	Output Amplifier Negative Analog Supply.
7	-1864.86	+897.51	AV <sub>SS</sub>	Output Amplifier Negative Analog Supply.
11	-1862.63	-1415.57	AGND	Analog Ground.
22	+1862	-1296.25	V <sub>REF</sub>	Reference Input Voltage. For specified performance, V <sub>REFIN</sub> = 2.5 V.
25	+1861.93	-962.93	AV <sub>DD</sub>	Output Amplifier Positive Analog Supply.
26	+1862	+962.81	AV <sub>DD</sub>	Output Amplifier Positive Analog Supply.
28	+1861.89	+1445.29	AV <sub>CC</sub>	Power Supply Input. The AD5766-KGD operates from 2.97 V to 3.6 V. Decouple AV <sub>CC</sub> with a 10 μF capacitor in parallel with a 0.1 μF capacitor to analog ground.
29	+1862	+1550.99	AGND	Analog Ground.

Pad No.	X-Axis ( $\mu\text{m}$ )	Y-Axis ( $\mu\text{m}$ )	Mnemonic	Description
<b>Logic Inputs and Outputs</b>				
3	-1880	+1319.88	$\overline{\text{RESET}}$	Active Low Reset Input. Asserting this pad logic low returns the AD5766-KGD to its default power-on state. After this pad returns to logic high, the device comes out of the reset mode and is ready to accept a new SPI command. This pad can be left floating because there is a weak internal pull-up resistor.
5	-1880.01	+1039.88	SDI	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
8	-1880.01	-950.62	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz for write mode and 10 MHz for readback mode and daisy-chain mode.
9	-1880	-1125.02	$\overline{\text{SYNC}}$	Active Low Control Input. $\overline{\text{SYNC}}$ is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and SDI buffers and enables the input shift register. Data is transferred in on the falling edges of the next 24 clocks. If $\overline{\text{SYNC}}$ is taken high before the 24 <sup>th</sup> falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the device.
10	-1852.98	-1242.64	SDO	Serial Data Output. This pad clocks data from the serial register in daisy-chain mode or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
<b>Analog Outputs</b>				
13	-1495.41	-1878.98	$V_{\text{OUT}8}$	Analog Output Voltage from DAC 8.
14	-1071.15	-1878.98	$V_{\text{OUT}9}$	Analog Output Voltage from DAC 9.
15	-639.89	-1878.98	$V_{\text{OUT}10}$	Analog Output Voltage from DAC 10.
16	-215.63	-1878.98	$V_{\text{OUT}11}$	Analog Output Voltage from DAC 11.
17	+215.63	-1878.98	$V_{\text{OUT}12}$	Analog Output Voltage from DAC 12.
18	+639.89	-1878.98	$V_{\text{OUT}13}$	Analog Output Voltage from DAC 13.
19	+1069.12	-1878.98	$V_{\text{OUT}14}$	Analog Output Voltage from DAC 14.
20	+1495.41	-1878.98	$V_{\text{OUT}15}$	Analog Output Voltage from DAC 15.
31	+1495.41	+1878.98	$V_{\text{OUT}0}$	Analog Output Voltage from DAC 0.
32	+1071.14	+1878.98	$V_{\text{OUT}1}$	Analog Output Voltage from DAC 1.
33	+639.88	+1878.98	$V_{\text{OUT}2}$	Analog Output Voltage from DAC 2.
34	+215.63	+1878.98	$V_{\text{OUT}3}$	Analog Output Voltage from DAC 3.
35	-215.63	+1878.98	$V_{\text{OUT}4}$	Analog Output Voltage from DAC 4.
36	-639.89	+1878.98	$V_{\text{OUT}5}$	Analog Output Voltage from DAC 5.
37	-1071.15	+1878.98	$V_{\text{OUT}6}$	Analog Output Voltage from DAC 6.
38	-1495.41	+1878.98	$V_{\text{OUT}7}$	Analog Output Voltage from DAC 7.
<b>Dither</b>				
23	+1862	-1191.72	N0	Dither Signal Input Pad 0. A signal connected to this pad can be added to the DAC outputs via register commands. If unused, connect this pad to ground.
24	+1862	-1087.19	N1	Dither Signal Input Pad 1. A signal connected to this pad can be added to the DAC outputs via register commands. If unused, connect this pad to ground.
<b>Channel Monitoring</b>				
27	+1861.98	+1190.26	MUX_OUT	Monitor Output. This pad acts as the output of a 16 to 1 channel multiplexer that can be programmed to multiplex one of 16 channels, Channel 0 to Channel 15, to the MUX_OUT pad.

## OUTLINE DIMENSIONS

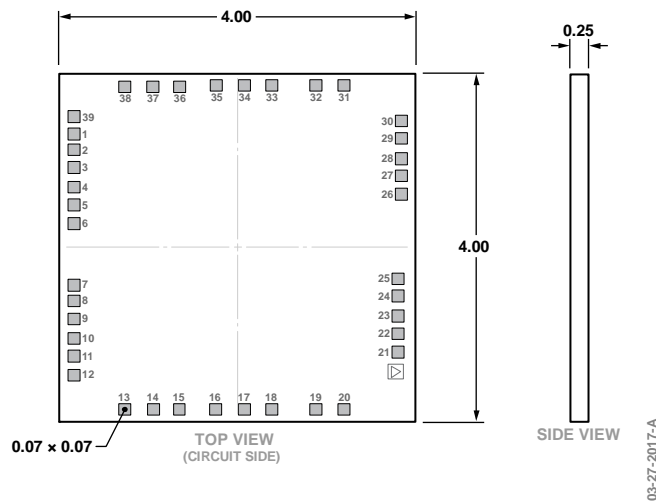


Figure 6. 39-Pad Bare Die [CHIP]  
(C-39-1)  
Dimensions shown in millimeters

## DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 7. Die Specifications

Parameter	Value	Unit
Die Size (Maximum)	4000 × 4000	μm
Bond Pad (Minimum)	70 × 70	μm
Thickness	250	μm
Scribe Line Width	80	μm
Bond Pad Composition	AICu (0.5%)	%
Passivation Type	10 kÅ high density plasma, undoped silicate glass (HDP-USG)	Not applicable
Backside Bias	1.5 kÅ oxide + 6 kÅ nitride GND	Not applicable

Table 8. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy adhesive
Thermosonic Ball Bonding Method <sup>1</sup>	Ø 25 μm (1.0 mil), 2N gold wire <sup>2</sup>

<sup>1</sup> Wedge bonding not recommended.

<sup>2</sup> Evaluate gold wire diameter, material, and composition for suitability before use.

## ORDERING GUIDE

Model	Resolution (Bits)	Temperature Range	Package Description	Package Option
AD5766-KGD-PT	16	−40°C to +105°C	39-Pad Bare Die [CHIP]	C-39-1