10-Bit VCM Driver for Autofocus

ADI Confidential

AD5823/AD5823-1

FEATURES

10-bit VCM driver for autofocus
ARC and ESRC enabled for fast autofocus capture
Available in 2 × 3 array, 1.1 mm² WLCSP
2-wire (I²C-compatible), 1.8 V serial interface
10-bit resolution DAC
100 mA output current sink
Integrated current sense resistor
2.3 V to 3.6 V power supply
Guaranteed monotonic over all codes
Power-down to 5 µA maximum
Internal reference
Ultralow noise preamplifier
Power-on reset

APPLICATIONS

Camera phones
Camera/image modules
Lens autofocus
Shutter/NDF/iris control
Camera enabled PDA
Web cameras

FUNCTIONAL BLOCK DIAGRAM

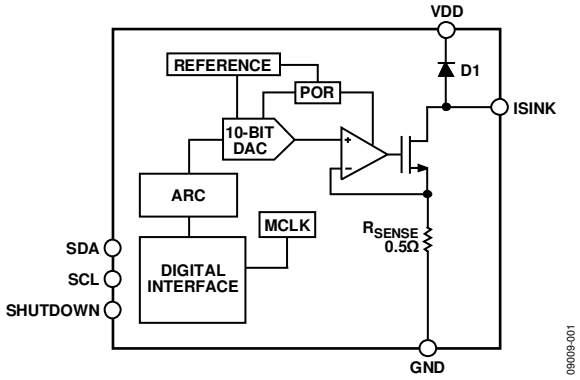

Figure 1.

GENERAL DESCRIPTION

The AD5823[1] and AD5823-1 are single, 10-bit DACs with 100 mA output current sink capability and integrated Actuator Response Control™ (ARC™) technology. ARC is a revolutionary autofocus capture time and image quality enhancing technology developed by Analog Devices, Inc., and integrated into the AD5823/AD5823-1 VCM drivers.

ARC circuitry applies specialized, patented waveform and application technology to underdamped voice coil motors (VCMs) to reduce mechanical ringing. This technology enables the user to achieve very fast mechanical settling times and, as a result, greatly enhances autofocus capture times, image quality, and user experience.

The AD5823/AD5823-1 feature an internal reference and operate from a single 2.3 V to 3.6 V supply. The DAC is controlled via a 2-wire (I²C-compatible) serial interface that operates at clock rates up to 400 kHz. The 7-bit I²C address for the AD5823/AD5823-1 is 0xC.

The AD5823/AD5823-1 also incorporate a power-on reset circuit, which ensures that the DAC output powers up to 0 V and remains at 0 V until a valid write takes place. To ensure that minimal power is consumed in shutdown mode, the user can select the power-down polarity: the AD5823 SHUTDOWN pin is active low; the AD5823-1 SHUTDOWN pin is active high.

The AD5823/AD5823-1 were designed for autofocus applications in camera modules, camera phones, digital still cameras, and camcorders.

The AD5823/AD5823-1 have many industrial applications, such as controlling temperature, light, and movement over the temperature range of −40°C to +85°C without derating.

[1] Protected by U.S. Patent 5,969,657; other patents pending.

Rev. Sp0

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REVISION HISTORY

7/10—Revision Sp0: Initial Version

SPECIFICATIONS

VDD = 2.3 V to 3.6 V, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC PERFORMANCE, VCM DRIVER STAGE					
Resolution		10		Bits	97.65 µA/LSB
Relative Accuracy		±1.5	±4	LSB	
Differential Nonlinearity[1]			±1	LSB	Guaranteed monotonic over all codes
Code 0 Error[2]		0	0.0025	LSB	All 0s loaded to DAC
Code 16 Error		±0.5	±3.5	LSB	T_A = 25°C
Code 16 Error Drift[3]			±0.08	LSB/°C	
Full-Scale Error		±1	±5	LSB	T_A = 25°C
Full-Scale Error Drift[3]			±0.33	LSB/°C	
OUTPUT CHARACTERISTICS, VCM DRIVER STAGE					
Maximum Output Current		100		mA	
Output Current During Power-Down		80		nA	SHUTDOWN = 0 V
Output Compliance	0.17		VDD	V	Output voltage range over which maximum sink current is available
Power-Up Time[3]					Time to exit power-down mode, VDD = 3.6 V
AD5823		100		µs	
AD5823-1		100		µs	
INTERNAL CLOCK					
Clock Frequency		20		MHz	
Clock Accuracy		±1	±2.5	%	
DIGITAL INPUTS, SHUTDOWN					
Input High Voltage, V_{IH}	1.26	1.8	3.6	V	
Input Low Voltage, V_{IL}	0		0.54	V	
Input Current			±1	µA	
I^2C INTERFACE					
SDA, SCL Input High Voltage, V_{IH}	1.26	1.8	3.6	V	
SDA, SCL Input Low Voltage, V_{IL}	0		0.54	V	
Glitch Rejection			50	ns	
Input Leakage Current			±1	µA	
SDA (Open-Drain Output)[3]					
Output Low Voltage, V_{OL}			0.4	V	ISINK = 3 mA, bus supply > 2 V
			0.2 × VDD	V	ISINK = 3 mA, bus supply < 2 V
POWER SUPPLY					
VDD Pin	2.3		3.6	V	
Quiescent Current					
AD5823		0.78	2.2	mA	SHUTDOWN pin high, VCM inactive
AD5823-1		0.78	2.2	mA	SHUTDOWN pin low, VCM inactive
Shutdown Current					
AD5823		0.25	5	µA	SHUTDOWN pin low
AD5823-1		0.25	5	µA	SHUTDOWN pin high

[1] Linearity is tested using a reduced code range: Code 32 to Code 992.
[2] To achieve near zero output current, use the power-down feature.
[3] Guaranteed by characterization and design; not production tested.

AC SPECIFICATIONS

VDD = 2.3 V to 3.6 V, GND = 0 V, load resistance (R_L) = 15 Ω connected to VDD, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
AC SPECIFICATIONS					
Output Current Settling Time		55		µs	L_L = 680 µH (in series with R_L), ¼ scale to ¾ scale change (0x100 to 0x300), settled to ±4 LSB accuracy
Slew Rate		1.4		mA/µs	
Major Code Change Glitch Impulse		0.15		nA-sec	1 LSB change around major carry
Digital Feedthrough		0.06		nA-sec	

I²C SERIAL INTERFACE SPECIFICATIONS

Table 3.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2 (t_{HIGH})	0.6	µs min	SCL high time
t_3 (t_{LOW})	1.3	µs min	SCL low time
t_4 ($t_{HD, STA}$)	0.6	µs min	Start/repeated start condition hold time
t_5 ($t_{SU, DAT}$)	100	ns min	Data setup time
t_6 ($t_{HD, DAT}$)[1]	0.9	µs max	Data hold time
	0	µs min	
t_7 ($t_{SU, STA}$)	0.6	µs min	Setup time for repeated start
t_8 ($t_{SU, STO}$)	0.6	µs min	Stop condition setup time
t_9 (t_{BUF})	1.3	µs min	Bus-free time between a stop condition and a start condition
t_{10} (t_R)	300	ns max	Rise time of SDA when transmitting
	0	ns min	Rise time of SCL and SDA when receiving (CMOS compatible)
t_{11} (t_F)	0	ns min	Fall time of SDA when receiving (CMOS compatible)
	300	ns max	Fall time of SCL and SDA when receiving
	20 + 0.1 C_B	ns min	Fall time of SCL and SDA when transmitting
	300	ns max	Fall time of SDA when transmitting
C_B[2]	400	pF max	Capacitive load for each bus line

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[2] C_B is the total capacitance of one bus line in picofarads (pF); t_R and t_F measured between 0.3 × V_{DD} and 0.7 × V_{DD}.

Timing Diagram

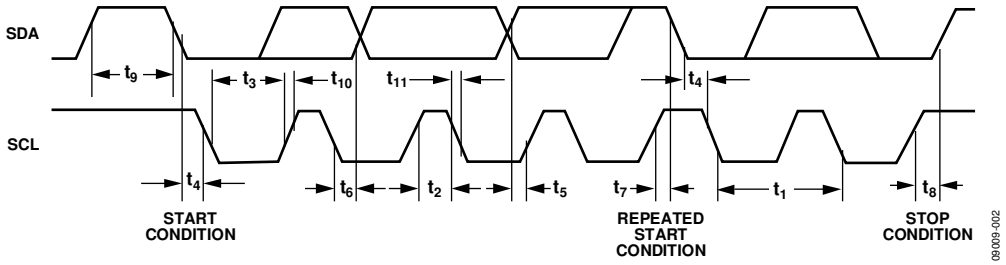

Figure 2. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VDD to GND	−0.3 V to +4.2 V
Digital Inputs	−0.3 V to VDD + 0.3 V
ISINK to GND	−0.3 V to VDD + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
WLCSP (CB-6-11)	160[1]	°C/W

[1] For an S2P2 board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

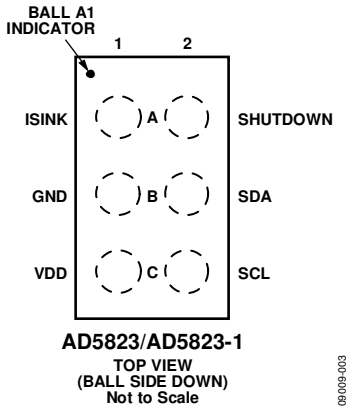

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	ISINK	Output Current Sink.
A2	SHUTDOWN	Asynchronous Power-Down Signal. Active low for the AD5823; active high for the AD5823-1.
B1	GND	Analog Ground Pin.
B2	SDA	I^2C Interface Signal.
C1	VDD	Supply Voltage.
C2	SCL	I^2C Interface Signal.

TYPICAL PERFORMANCE CHARACTERISTICS

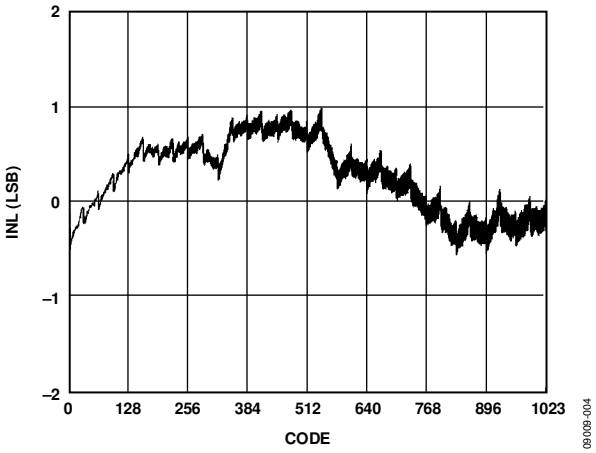

Figure 4. Typical INL Plot

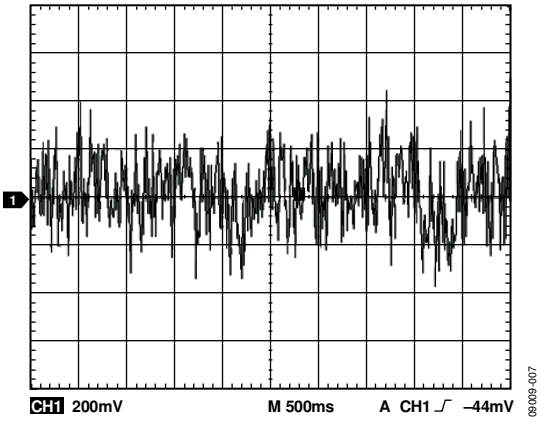

Figure 7. 0.1 Hz to 10 Hz Noise Plot, VDD = 3 V

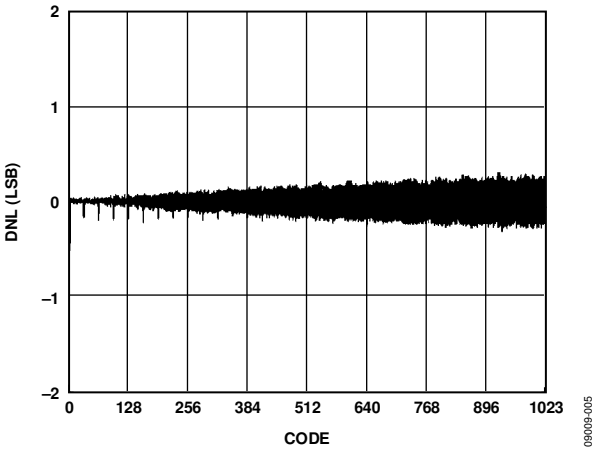

Figure 5. Typical DNL Plot

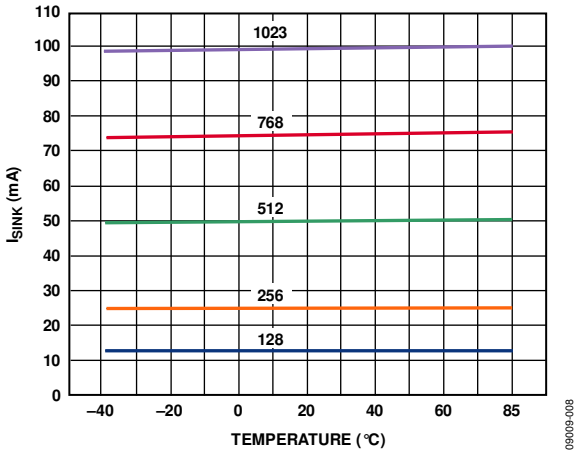

Figure 8. Sink Current and Code vs. Temperature, VDD = 3 V

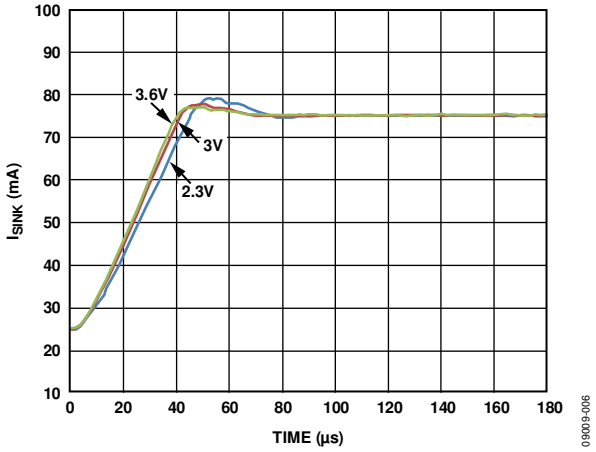

Figure 6. Output Current Settling Time, ¼ Scale to ¾ Scale Change

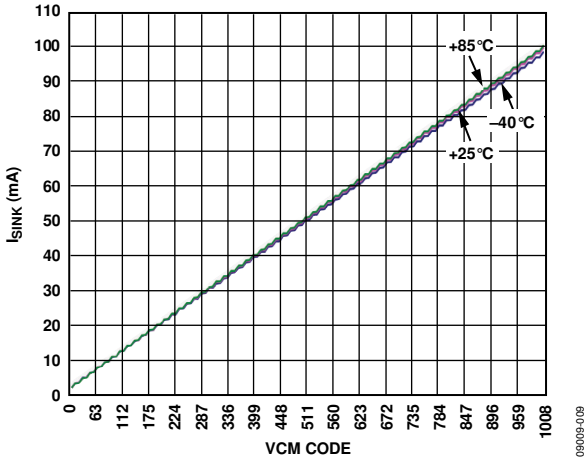

Figure 9. Sink Current vs. Code over Temperature, VDD = 3 V

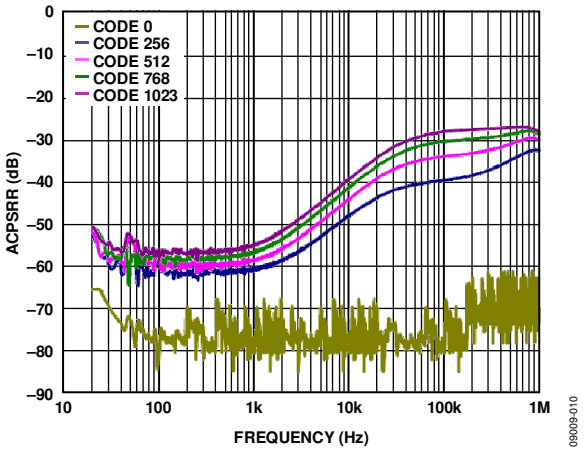

Figure 10. AC Power Supply Rejection Ratio, VDD = 3 V

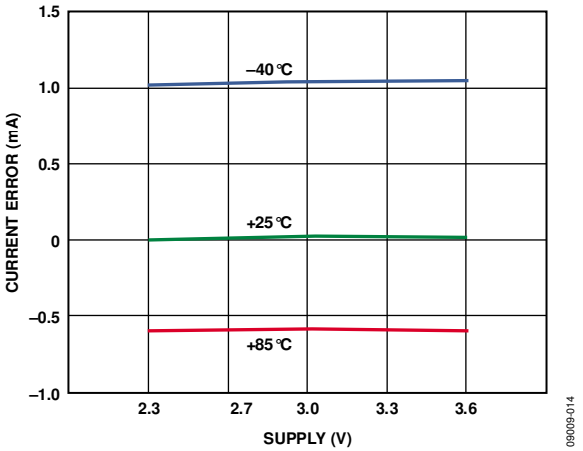

Figure 11. Full-Scale Error vs. Supply Voltage over Temperature

THEORY OF OPERATION

The AD5823/AD5823-1 feature a fully integrated, 10-bit DAC with 100 mA output current sink capability designed to drive voice coil motor (VCM) actuators in applications such as lens autofocus, image stabilization, and optical zoom. The functional block diagram of the AD5823/AD5823-1 is shown in Figure 12.

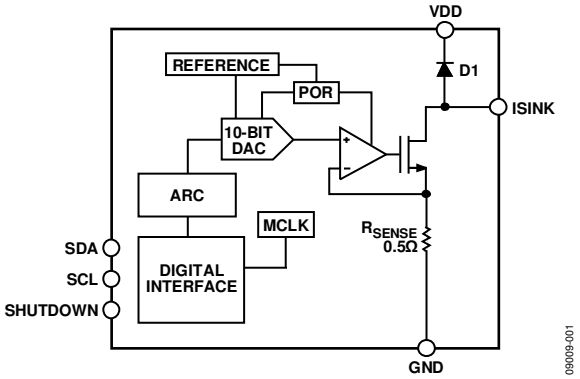

Figure 12. Functional Block Diagram

The AD5823/AD5823-1 autofocus system controllers feature the following functions:

- 10-bit digital-to-analog converter (DAC)
- 0.5 Ω current sense resistor
- Enhanced Slew Rate Control™ (ESRC™) technology
- Actuator Response Control (ARC) technology

SHUTDOWN OPTIONS

The AD5823/AD5823-1 allow the user to choose a VCM driver that can interface with image signal processors (ISPs) using an active high or an active low hardware shutdown output.

- The AD5823 has an active low SHUTDOWN pin. When SHUTDOWN is taken low, the AD5823 enters power-down mode and consumes minimal power.
- The AD5823-1 has an active high SHUTDOWN pin. When SHUTDOWN is taken high, the AD5823-1 enters power-down mode and consumes minimal power.

Shutdown Mode

Shutdown mode is entered when VDD is between 2.3 V and 3.6 V, and the SHUTDOWN pin is active (low for the AD5823, high for the AD5823-1). These are the hardware power-down states for the AD5823/AD5823-1. In shutdown mode, all internal blocks are powered down.

AUTOFOCUS DRIVER STAGE AND PATTERN GENERATOR

A 10-bit voltage output DAC drives the noninverting input of the operational amplifier, configuring it as a follower (see Figure 12). The DAC voltage also appears across the R_{SENSE} resistor and generates the sink current required to drive the voice coil.

The temperature coefficient of the DAC resistors and that of R_{SENSE} are matched; therefore, the output drift over temperature is minimized. Diode D1 is an output protection diode.

The AD5823/AD5823-1 are designed to drive both spring-preloaded and nonspring linear voice coil motors used in applications such as lens autofocus, image stabilization, and optical zoom. The operational principle of the spring-preloaded VCM is that the lens position is controlled by the balancing of a voice coil and a spring.

The requirement to reduce optical module form factors has led to a reduction in the size of VCM actuators. As VCM actuators are reduced in size, the preloaded balance spring strength is also reduced. When large current transitions occur, the momentum of the lens can often lead to overshoot, and the VCM can take some time to settle to its final position, as shown in Figure 13.

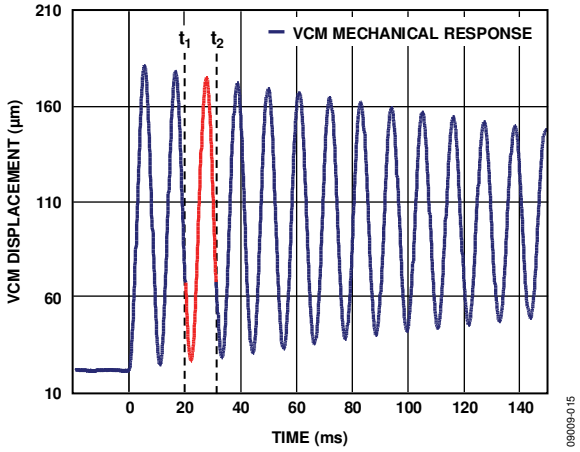

Figure 13. VCM Mechanical Response to a Step Current Input, $t_{RES} = t_2 - t_1$

This phenomenon (often described as mechanical ringing) varies with output current step size and, for large lens displacements, can lead to unacceptably long autofocus times.

Ringing Control

Ringing control is enabled or disabled on the AD5823/AD5823-1 using the RING_CTRL bit (Bit 2 in the VCM_CODE_MSB register, Address 0x04). When RING_CTRL = 0, direct load mode is used.

In direct load mode, the VCM_MOVE_TIME register (Address 0x03) is ignored, and the output increments or decrements to the target code in a single step. The target code is written to the VCM_CODE_MSB and VCM_CODE_LSB registers, Address 0x04 and Address 0x05. No ringing control is used in direct load mode.

When ringing control is enabled (by setting RING_CTRL = 1), the AD5823/AD5823-1 allow the user to overcome the mechanical limitations associated with reductions in VCM form factor. The AD5823/AD5823-1 VCM drivers can operate in one of four different ringing control modes:

- Mode 0—ARC RES1
- Mode 1—ARC RES0.5
- Mode 2—ARC RES2
- Mode 3—ESRC

When ESRC mode is used (by setting the MODE[1:0] bits to 11 in the MODE register, Address 0x02), the user decides the required move time and uses the following equation to determine the value to be written to the VCM_MOVE_TIME register (Address 0x03).

$$VCM\_MOVE\_TIME = (t_{RES}\ (\mu s)/51.2\ \mu s) - Offset$$

where *Offset* = value of HIGH_FREQ_RANGE (default = 0x80).

In ESRC mode, the output increments or decrements to the target code in single-code steps in the required actuation time.

When one of the ARC modes is used, the VCM_MOVE_TIME register should be loaded with a value equivalent to the VCM mechanical resonance period (t_{RES}). This value can be calculated using the following equation:

$$VCM\_MOVE\_TIME = (t_{RES}\ (\mu s)/51.2\ \mu s) - Offset$$

where *Offset* = value of HIGH_FREQ_RANGE (default = 0x80).

The mechanical resonance period of a VCM can be found by applying a step current to the VCM and measuring the time taken for one complete oscillation. This is shown in Figure 13, where

$$t_{RES} = t_2 - t_1$$

The output increments or decrements to the target code using ARC technology.

ACTUATOR RESPONSE CONTROL (ARC) TECHNOLOGY

Mechanical ringing is an inherent problem in voice coil motors. It is an artifact of an underdamped system and is dependent on many factors, but primarily on the integrity of the mechanical springs employed in the actuator assembly.

ARC is a revolutionary autofocus response time and image quality enhancing technology, which has been developed by Analog Devices and integrated into the AD5823/AD5823-1 VCM drivers. ARC circuitry applies specialized, patented waveform and application technology to underdamped voice coil motors to reduce mechanical ringing. This technology enables the user to achieve very fast mechanical settling times and, as a result, greatly enhances autofocus response times, image quality, and user experience. This technology is completely proprietary to Analog Devices and patents are pending.

ARC technology incorporates a wide band of tolerance around the resonant period of the VCM to compensate for manufacturing variability in the mechanical resonance period (t_{RES}) of the VCM. ARC technology can allow for variations of ±20% (for example, manufacturing variations and variations over time and temperature) in the VCM resonant period while still greatly enhancing autofocus response times and image quality. This band of tolerance varies, depending on the ARC option used.

One of the main advantages of ARC is its ability to maintain the same actuation time, regardless of the size (in DAC codes) of the step required. This is clearly illustrated in Figure 14, where it is shown that a step of 100 codes and a step of 500 codes both settle in 15.1 ms. Each of the three ARC options achieves a different actuation time. A faster actuation time leads to a narrower resonant period tolerance band (see Figure 14 and Table 7).

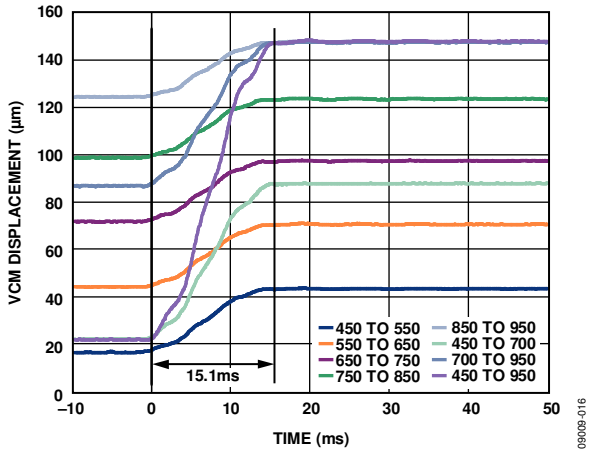

Figure 14. ARC Actuation Time Is Always the Same, Regardless of Step Size

Table 7. Actuation Times and Tolerances of ARC Options

ARC Option	Actuation Time	Tolerance
ARC RES0.5	0.5 × t_{RES}	±3%
ARC RES1	1.07 × t_{RES}	±10%
ARC RES2	2.13 × t_{RES}	±20%

Figure 15 illustrates all the output modes of the AD5823/AD5823-1 and clearly shows the significant impact that ESRC and ARC technology has on the settling time and the amount of mechanical ringing and overshoot in a sample VCM.

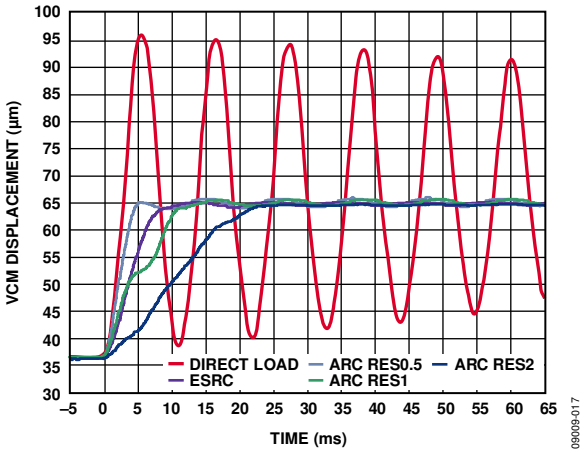

Figure 15. Comparing Direct Load, ESRC, and ARC Modes Using a Sample VCM

MOVING THROUGH THE VCM THRESHOLD

The AD5823/AD5823-1 are designed to drive both spring-preloaded and nonspring linear voice coil motors. The operational principle of the spring-preloaded VCM is that the lens position is controlled by the balancing of a voice coil and spring. Figure 16 shows an example transfer curve of a spring-preloaded VCM. The key points of this transfer function are displacement, which is the actual distance moved by the lens, and the current through the motor. The recommended transfer curve crosses the threshold once and then operates between the infinite and macro focus positions without returning below the threshold, as shown in Figure 16.

A threshold current is associated with spring-preloaded VCMs; this current must be overcome for any displacement in the lens to occur. The threshold value can vary across VCM models and manufacturers. Care must be taken in overcoming this threshold because a step displacement through the threshold can introduce a mechanical shock to the VCM, which, in turn, causes mechanical ringing. Mechanical ringing increases the settling time, distorts the image, and may also shorten the lifetime of the VCM.

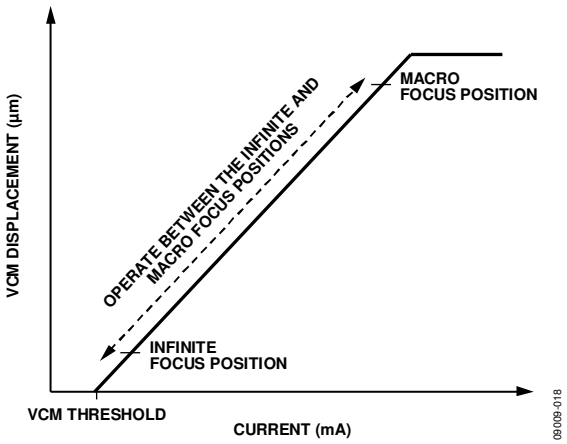

Figure 16. Recommended Transfer Curve of Spring-Preloaded VCM

Because of the mechanical ringing in the VCM associated with moving through the threshold, the optimum mode of operation is to ensure that the VCM is operated in its linear region—that is, between the infinite focus position and the macro focus position—as shown in Figure 16. To ensure the fastest autofocus times, the user should ensure that the threshold is crossed only on the initial move to the infinite focus position. After the threshold is crossed, any subsequent moves should be made between the infinite focus position and the macro focus position. Operating in this linear region above the threshold leads to more predictable and accurate lens movements and allows the user to take full advantage of ESRC or ARC technology.

The AD5823/AD5823-1 have one threshold option that is used to efficiently move through the VCM threshold. The device crosses the threshold and reaches the target code in the calculated actuation time. The VCM threshold value for the device is programmed in the VCM_THRESHOLD_MSB and VCM_THRESHOLD_LSB registers (Address 0x06 and Address 0x07). The closer this value is to the actual VCM threshold, the smaller the overshoot is.

Figure 17 shows the DAC codes incrementing over time. Figure 18 shows the DAC codes decrementing over time.

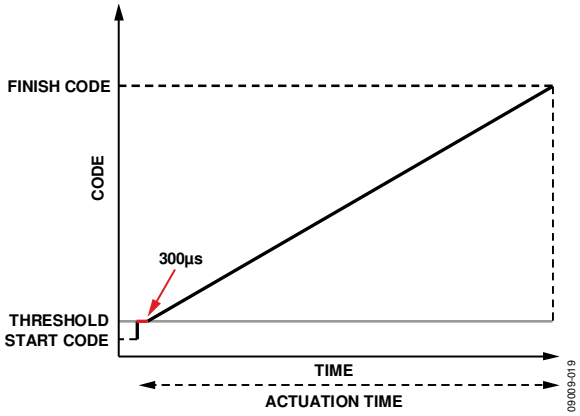

Figure 17. Moving from a Code Below the VCM Threshold to a Code Above the Threshold

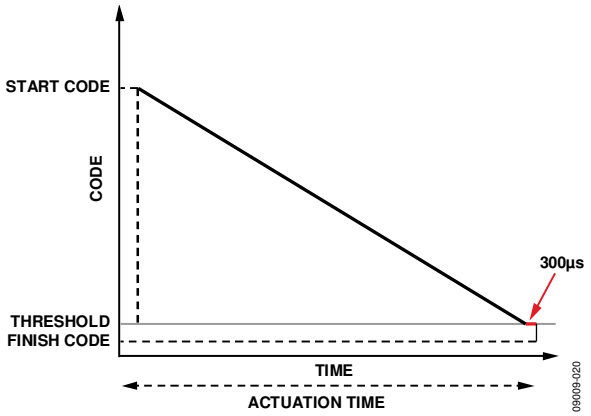

Figure 18. Moving from a Code Above the VCM Threshold to a Code Below the Threshold

I²C INTERFACE

The I²C interface specification for the AD5823/AD5823-1 is as follows:

Address: 0001 100
Write command: 0001 1000
Read command: 0001 1001

The AD5823/AD5823-1 have a 2-wire, I²C-compatible serial interface (refer to *I²C Bus Specification*, Version 2.1, January 2000, available from Philips Semiconductor). The AD5823/AD5823-1 can be connected to an I²C bus as slave devices under the control of a master device.

The AD5823/AD5823-1 support standard (100 kHz) and fast (400 kHz) operating frequencies and transfer data using 7-bit addressing. The R/$\overline{W}$ bit, as well as the start (S), repeated start (Sr), acknowledge (A), no acknowledge ($\overline{A}$), and stop (P) conditions comply with the *I²C Bus Specification*, Version 2.1, January 2000.

The address byte is eight data bits, consisting of a 7-bit address (0001 100), plus a read/write bit (0 if data is to be written to a device, and 1 if data is to be read from a device). Each slave device on an I²C bus must have a unique address. The 7-bit address of the AD5823/AD5823-1 is 0001 100 (0xC). Because the address bits plus the R/$\overline{W}$ bit always equal eight bits of data, the write address of the AD5823/AD5823-1 is 0001 1000 (0x18), and the read address is 0001 1001 (0x19).

Data bytes are transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The 2-wire serial bus protocol for write and read operations is described in the following sections.

WRITE OPERATION

1. The master initiates a data transfer by establishing a start condition.
2. The next byte consists of the seven address bits followed by the R/$\overline{W}$ bit (0).
3. If the address bits match, the AD5823/AD5823-1 generate an ACK on the ninth bit of the sequence.
4. Because the R/$\overline{W}$ bit = 0, the AD5823/AD5823-1 expect to receive data from the master. The master sends the 8-bit register pointer followed by the 8-bit data to be written to the selected register.
5. For each of the transmitted bytes, the AD5823/AD5823-1 generate an ACK.
6. When the master is finished transmitting its data, it generates a stop condition.

This sequence is also known as a write to random location in some protocols.

7-Bit Addressing, 8-Bit Register Pointer, and 8-Bit Data for Write Operations

S	**7-Bit Address**	**R/$\overline{W}$ = 0**	**A**	**Register Pointer**	**A**	**Data**	**A**	**P**

For example, when writing 0xCA to the VCM_MOVE_TIME register at Address 0x03, the sequence is as follows:

S	**0001 100**	**0**	**A**	**0000 0011**	**A**	**1100 1010**	**A**	**P**

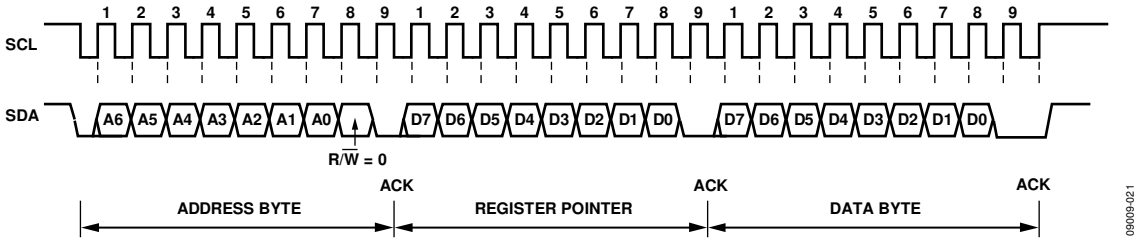

Figure 19. I²C Write Operation

READ OPERATION

1. The master initiates a data transfer by establishing a start condition.
2. The next byte consists of the seven address bits followed by the R/$\overline{W}$ bit (0).
3. If the address bits match, the AD5823/AD5823-1 generate an ACK on the ninth bit of the sequence.
4. Because the R/$\overline{W}$ bit = 0, the AD5823/AD5823-1 expect to receive data from the master. The master sends the 8-bit register pointer.
5. After receiving an ACK from the AD5823/AD5823-1, the master generates a repeated start condition (Sr).
6. The repeated start condition is followed by the address bits and the R/$\overline{W}$ bit, which is set to 1 for a read command.
7. After the AD5823/AD5823-1 generate an ACK, the AD5823/AD5823-1 become transmitters, and the master device becomes a receiver.
8. The AD5823/AD5823-1 transmit the data contained in the register that is selected by the register pointer.
9. Because only one byte is to be read by the master, the master generates a NACK, followed by a stop condition to finish the operation.

This sequence is also known as a read from random location in some protocols.

7-Bit Addressing, 8-Bit Register Pointer, and 8-Bit Data for Read Operations

S	7-Bit Address	R/$\overline{W}$ = 0	A	Register Pointer	A	Sr	7-Bit Address	R/$\overline{W}$ = 1	A	Data	$\overline{A}$	P

For example, when reading the contents, 0xCA, of the VCM_MOVE_TIME register at Address 0x03, the sequence is as follows:

S	0001 100	0	A	0000 0011	A	Sr	0001 100	1	A	1100 1010	$\overline{A}$	P

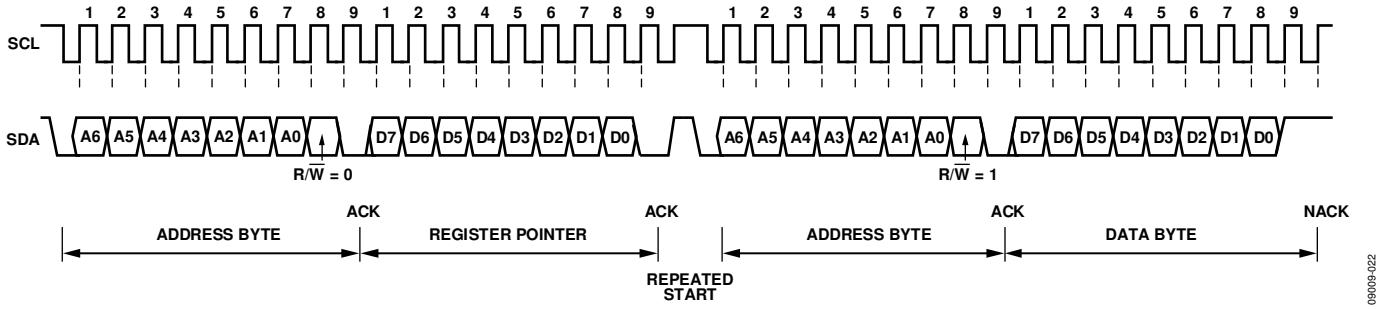

Figure 20. I²C Read Operation

OTHER READ/WRITE OPERATIONS

The AD5823/AD5823-1 also support several other read and write operations: a single read from the current location, a sequential read starting from a random location, a sequential read from the current location, and a sequential write starting from a random location. These read and write operations are shown in Figure 21 through Figure 24.

Single Read from the Current Location

It is possible to read from the last used index by addressing the slave with a read operation. The slave responds by setting the data from the last used index to the SDA line (note that the last used index refers to the last register address plus 1). This is shown in Figure 21. The master terminates the read operation by setting a no acknowledge and stop condition.

Figure 21. I²C Single Read from the Current Location

Sequential Read Starting from a Random Location

The sequential read starting from a random location is shown in Figure 22. The master performs a dummy write to the desired index, issues a repeated start condition after receiving an acknowledge from the slave, and addresses the slave again with a read operation. If the master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation continues from the next index. When the master has read the last data byte, it issues a no acknowledge and stop condition.

Figure 22. I²C Sequential Read Starting from a Random Location

Sequential Read from the Current Location

The sequential read starting from the current location is similar to a sequential read from a random location. The only difference is that there is no dummy write operation (see Figure 23). The master terminates the read operation by setting a no acknowledge and stop condition.

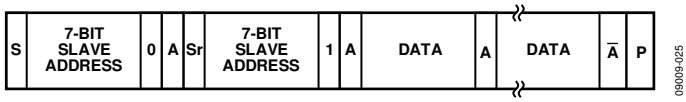

Figure 23. I²C Sequential Read from the Current Location

Sequential Write Starting from a Random Location

The sequential write starting from a random location is shown in Figure 24. The slave auto-increments the index after each data byte. The master terminates the sequential write operation by setting a stop condition.

Figure 24. I²C Sequential Write Starting from a Random Location

APPLICATIONS INFORMATION

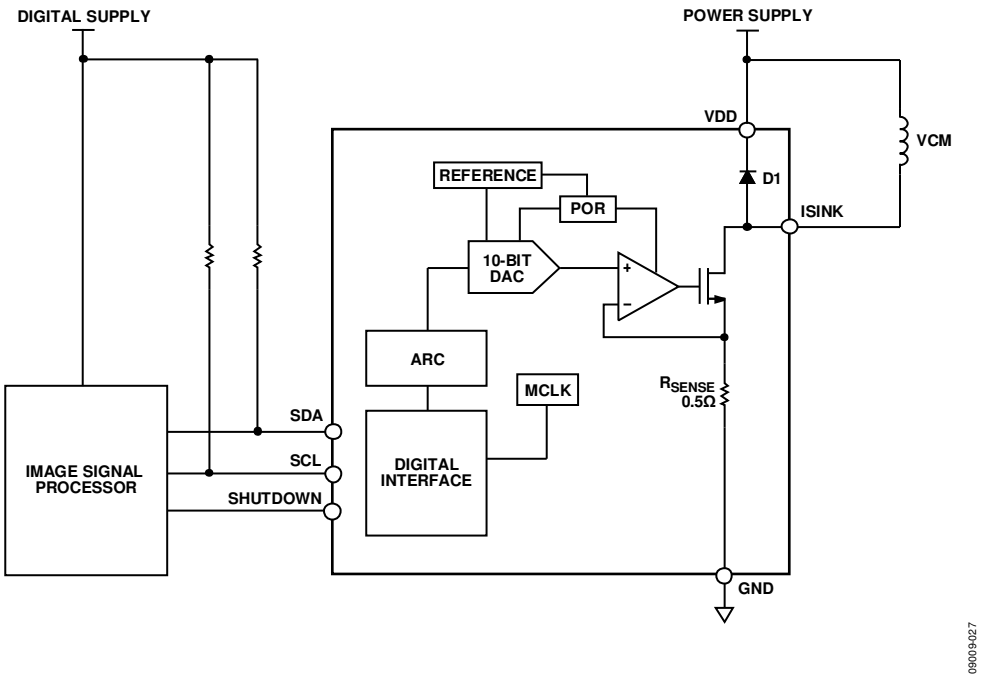

Figure 25. Example AD5823/AD5823-1 Application Setup

REGISTER DESCRIPTIONS

The registers for the AD5823/AD5823-1 are eight bits wide. For registers that use fewer than eight bits, the unused bits are written as 0s during a write operation and are read back as 0s during a read operation. Registers are right justified; 0s for unused bits are on the MSB side.

Table 8. Register Descriptions

Address				Number of	
Decimal	Hex	Register Name	Description	R/W Bits	Default
1	0x01	RESET	RESET register. Bit 0 resets all registers.	1	0x00
2	0x02	MODE	Configures the AD5823/AD5823-1 mode of operation.	6	0x00
3	0x03	VCM_MOVE_TIME	Actuation time for the ISINK output.	8	0x80
4	0x04	VCM_CODE_MSB	AD5823/AD5823-1 DAC MSB register. Also includes VCM transition mode bit.	3	0x00
5	0x05	VCM_CODE_LSB	AD5823/AD5823-1 DAC LSB register. The ISINK output is updated when this register is written to.	8	0x00
6	0x06	VCM_THRESHOLD_MSB	MSBs of the mechanical dead band of the VCM.	2	0x00
7	0x07	VCM_THRESHOLD_LSB	LSBs of the mechanical dead band of the VCM.	8	0x10

Table 9. Register Map

Reg	Addr	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
1	0x01	RESET	0	0	0	0	0	0	0	SW_RESET	0x00
2	0x02	MODE	0	0	HIGH_FREQ _RANGE	STEP_RATIO[2:0]			MODE[1:0]		0x00
3	0x03	VCM_MOVE_TIME	VCM_MOVE_TIME[7:0]								0x80
4	0x04	VCM_CODE_MSB	0	0	0	0	0	RING_CTRL	D[9:8]		0x00
5	0x05	VCM_CODE_LSB	D[7:0]								0x00
6	0x06	VCM_THRESHOLD_MSB	0	0	0	0	0	0	VCM_THRESHOLD[9:8]		0x00
7	0x07	VCM_THRESHOLD_LSB	VCM_THRESHOLD[7:0]								0x10

REGISTER BIT DESCRIPTIONS

Table 10. RESET Register, Address 0x01, Default = 0x00

Bits	Bit Name	Default	Description
[7:1]	Not used	0000000	Not used.
0	SW_RESET	0	Resets all registers to their default settings. 0 = no reset (default). 1 = reset all registers to their default settings.

Table 11. MODE Register, Address 0x02, Default = 0x00

Bits	Bit Name	Default	Description	
[7:6]	Not used	00	Not used.	
5	HIGH_FREQ_RANGE	0	0 = 0x80 (decimal 128) is added to VCM_MOVE_TIME. Recommended for voice coil actuators with a resonance frequency lower than 152 Hz. 1 = 0x01 (decimal 1) is added to VCM_MOVE_TIME. Recommended for voice coil actuators with a resonance frequency higher than 152 Hz.	
[4:2]	STEP_RATIO[2:0]	000	Programs the uneven steps ratio for the Actuator Response Control (ARC).	
			Setting	**Steps Ratio**
			000	0.5 and 0.5
			001	0.53125 and 0.46875
			010	0.5625 and 0.4375
			011	0.59375 and 0.40625
			100	0.625 and 0.375
			101	0.65625 and 0.34375
			110	0.6875 and 0.3125
			111	0.71875 and 0.28124
[1:0]	MODE[1:0]	00	Sets the ringing control mode. The RING_CTRL bit (Address 0x04, Bit 2) must be set to 1.	
			Setting	**Mode**
			00	Mode 0: ARC RES1
			01	Mode 1: ARC RES0.5
			10	Mode 2: ARC RES2
			11	Mode 3: ESRC

Table 12. VCM_MOVE_TIME Register, Address 0x03, Default = 0x80

Bits	Bit Name	Default	Description
[7:0]	VCM_MOVE_TIME	10000000	When one of the ARC modes is used (MODE[1:0] bits are set to 00, 01, or 10), this register should be loaded with a value equivalent to the VCM mechanical resonance period (t_{RES}). For more information, see the Ringing Control section. When ESRC mode is used (MODE[1:0] bits are set to 11), the user decides the required move time and uses the following equation to determine the value to be written to this register: *VCM_MOVE_TIME* = (t_{RES} (µs)/51.2 µs) − *Offset*, where *Offset* = value of HIGH_FREQ_RANGE (default = 0x80).

Table 13. VCM_CODE_MSB Register, Address 0x04, Default = 0x00

Bits	Bit Name	Default	Description
[7:3]	Not used	00000	Not used.
2	RING_CTRL	0	Enable or disable ringing control. 0 = direct load mode (no ringing control, default). 1 = mode as set by the MODE[1:0] bits in the MODE register (Address 0x02).
[1:0]	D[9:8]	00	DAC output target code MSBs.

Table 14. VCM_CODE_LSB Register, Address 0x05, Default = 0x00

Bits	Bit Name	Default	Description
[7:0]	D[7:0]	00000000	DAC output target code LSBs.

Table 15. VCM_THRESHOLD_MSB Register, Address 0x06, Default = 0x00

Bits	Bit Name	Default	Description
[7:2]	Not used	000000	Not used.
[1:0]	VCM_THRESHOLD[9:8]	00	VCM threshold MSBs.

Table 16. VCM_THRESHOLD_LSB Register, Address 0x07, Default = 0x10

Bits	Bit Name	Default	Description
[7:0]	VCM_THRESHOLD[7:0]	00010000	VCM threshold LSBs.

OUTLINE DIMENSIONS

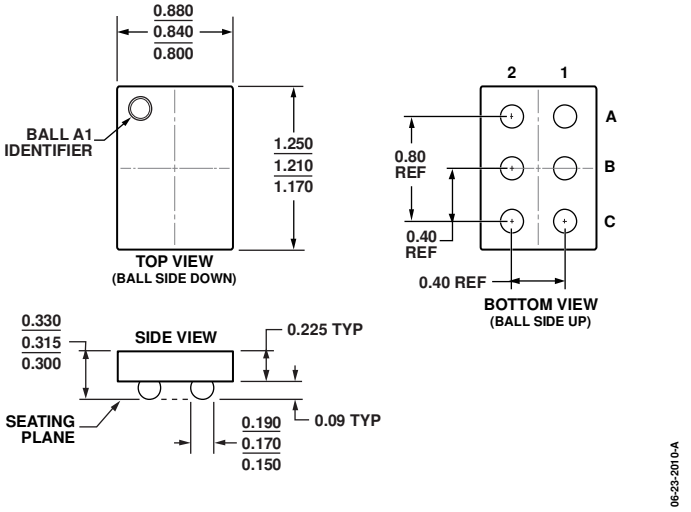

Figure 26. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	SHUTDOWN Pin	Package Option	Branding
AD5823BCDZ-RL	−40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	Active Low	CB-6-11	4P
AD5823BCDZ-RL7	−40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	Active Low	CB-6-11	4P
AD5823-1BCDZ-RL	−40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	Active High	CB-6-11	58
AD5823-1BCDZ-RL7	−40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	Active High	CB-6-11	58
EVAL-AD5823EBZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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