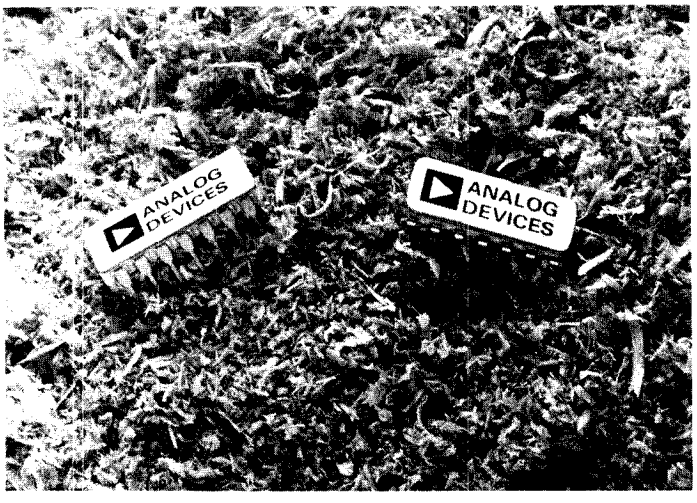
IC Sample and Hold Gated Op Amp

AD583

FEATURES
High Sample-to-Hold Current Ratio: 10^5
High Slew Rate: 5V/μs
High Bandwidth: 2MHz
Low Aperture Time: 50ns
Low Charge Transfer: 10pC
DTL/TTL Compatible
May Be Used as Gated Op Amp

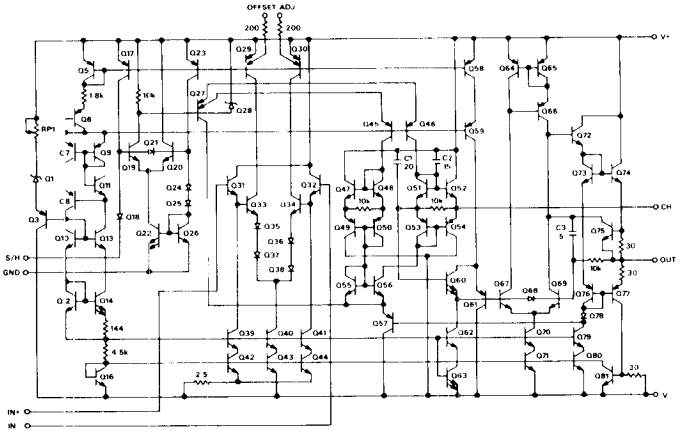


PRODUCT DESCRIPTION

The AD583 is a monolithic sample and hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier. An external holding capacitor, connected to the switch output, completes the sample-and-hold or track-and-hold function.

With the analog switch closed, the AD583 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open the capacitor holds the output at its previous level.

The AD583 may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.



Schematic Diagram

PRODUCT HIGHLIGHTS

1. Sample-and-hold operation is obtained with the addition of one external capacitor.
2. Low charge transfer (10pC) and high sample-to-hold current ratio insure accurate tracking.
3. Any gain or frequency response is available using standard op amp feedback networks.
4. High slew rate and low aperature time permit sampling of rapidly changing signals.
5. Output, gated through a low leakage analog switch, also makes the AD583 useful for applications such as analog switches, peak holding circuits, etc.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise specified)

MODEL	AD583K
OPEN LOOP GAIN R_L = 2kΩ, T_{min} to T_{max}	25k min (50k typ)
OUTPUT VOLTAGE SWING R_L = 2kΩ, T_{min} to T_{max}	±10V min
OUTPUT CURRENT	±10mA min
OUTPUT RESISTANCE	5Ω
OFFSET VOLTAGE T_{min} to T_{max}	6mV max (3mV typ) 8mV max (4mV typ)
BIAS CURRENT T_{min} to T_{max}	200nA max (50nA typ) 400nA max
OFFSET CURRENT T_{min} to T_{max}	50nA max (10nA typ) 100nA max
INPUT RESISTANCE	5MΩ min (10MΩ typ)
COMMON MODE RANGE	±10V min
COMMON MODE REJECTION T_{min} to T_{max}	74dB min (90dB typ)
GAIN BANDWIDTH PRODUCT	2MHz
SLEW RATE Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = ±10V p-p	5V/μs
RISE TIME Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	100ns
OVERSHOOT Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	20%
DIGITAL INPUT CURRENT V_{in} = 0, T_{min} to T_{max} V_{in} = +5.0V, T_{min} to T_{max}	 0.8V max (Logic "Sample") 2.0V min (Logic "Hold")
DIGITAL INPUT VOLTAGE Low T_{min} to T_{max} High T_{min} to T_{max}	 0.8V max 2.0V min
ACQUISITION TIME Av = +1, R_L = 2kΩ, C_L = 50pF to 0.1% of final value	4μs
APERTURE TIME	50ns
DRIFT CURRENT T_{min} to T_{max}	50pA max (5pA typ) 1.0nA max (0.05nA typ)
CHARGE TRANSFER	20pC max (10pC typ)
SUPPLY CURRENT	5.0mA max (2.5mA typ)
POWER SUPPLY REJECTION	74dB min (90dB typ)
OPERATING TEMP	0 to +70°C
STORAGE TEMP	-65 to +150°C

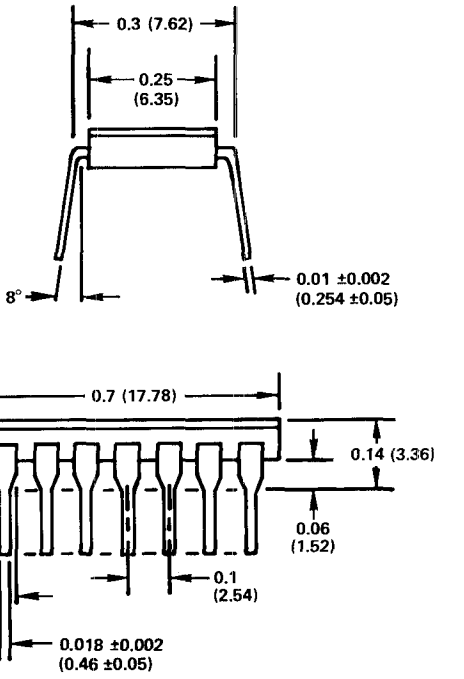
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- Terminals	40V
Differential Input Voltage	±30V
Digital Voltage (Pin 14)	+8V, -15V
Output Current	Short Circuit Protected
Internal Power Dissipation	30mW (Derate power dissipation by 4.3mW/°C above +150°C ambient temperature)

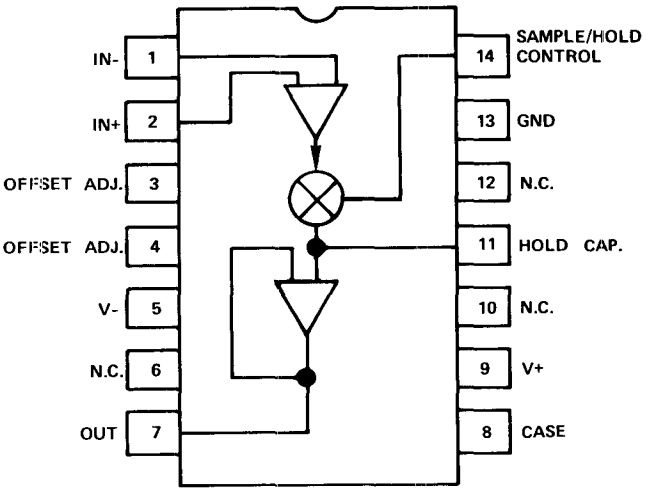
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



ALL DIMENSIONS ±0.010 UNLESS OTHERWISE SHOWN

PIN CONFIGURATION



APPLYING THE AD583

Figure 1 shows the AD583 connected in a simple sample and hold configuration with unity gain and offset nulling. Any other standard op amp gain and frequency response configuration may also be used. Note that the holding capacitor, C_H, should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), teflon or Mica types are recommended.

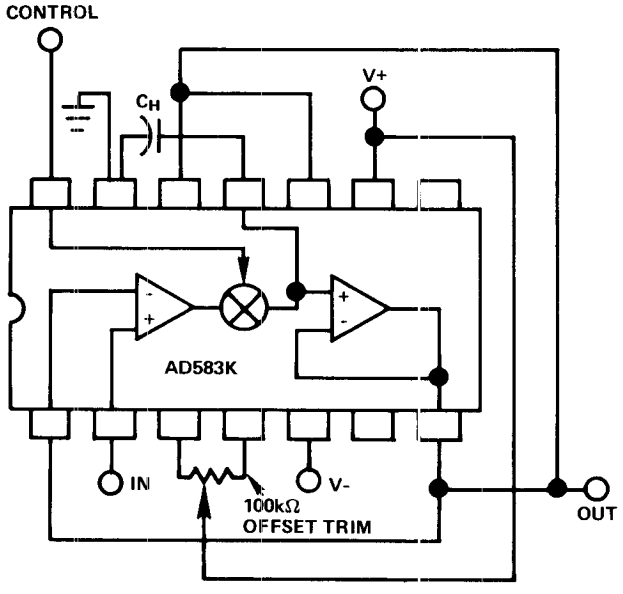


Figure 1. Basic Track-and-Hold/Sample-and-Hold

Figure 2 shows the guard ring used to reduce leakage paths between the pc board and the package. This minimizes drift during the hold command.

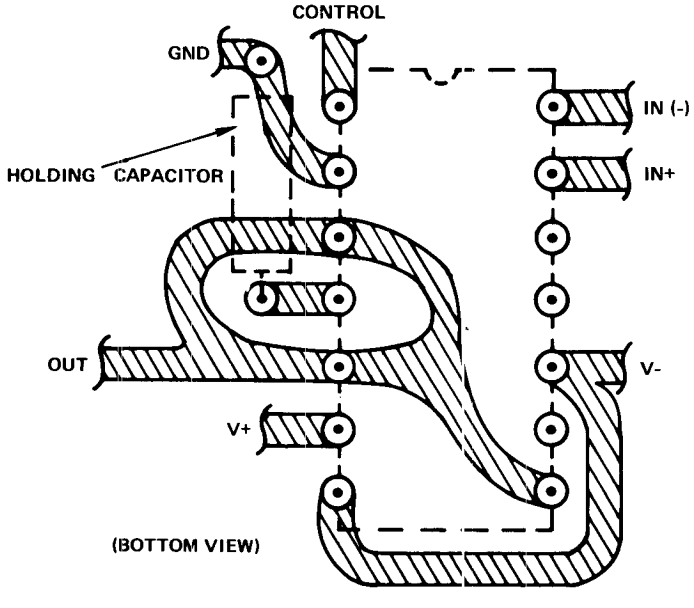


Figure 2. Guard Ring Layout

Also note that the input amplifier of the AD583 may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

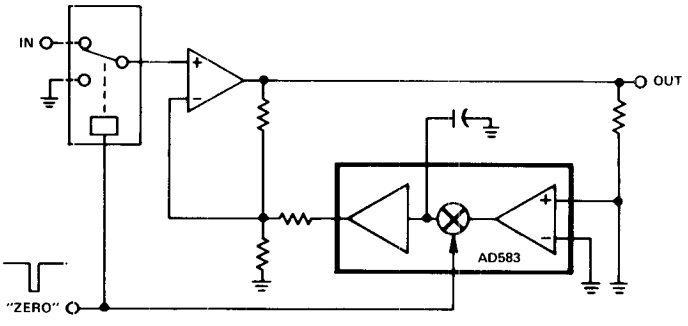


Figure 3. Automatic Offset Zeroing

The circuit of Figure 3 illustrates how the AD583 may be used to automatically zero a high gain amplifier. Basically, the input is periodically grounded and the output offset is then sampled and fed back to cancel the error. This technique is useful in A/D conversion, instrumentation, DVM's to eliminate offset drift errors by periodically rezeroing the system.

Care should be taken to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

DEFINITION OF TERMS

Acquisition Time:

Acquisition Time is the time required by the device to reach its final value within ±0.1% after the sample command has been given. This includes switch delay time, slewing time, and settling time and is the minimum sample time required to obtain a given accuracy.

Charge Transfer:

Charge Transfer is the small charge transferred to the holding capacitor from the interelectrode capacitance of the switch when the unit is switched to the sample mode. Sample-to-hold offset error is directly proportional to this charge, where:

$$\text{Offset Error (V)} = \frac{\text{Charge (pC)}}{C_H\text{(pF)}}$$

Aperture Time:

The time required after the "hold" command until the switch is fully open. This delays the effective sample timing with rapidly changing input signals.

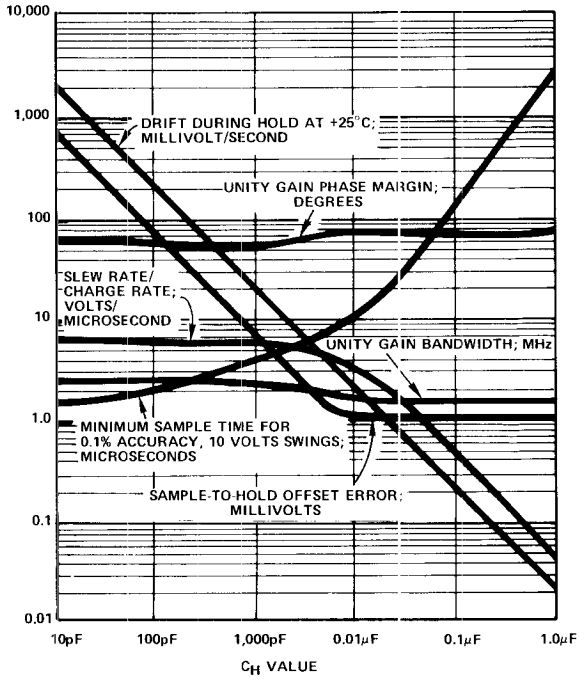
Drift Current:

Leakage currents from the holding capacitor during the sample mode cause the output voltage to drift. Drift rate (or droop rate) is calculated from drift current values using the formula:

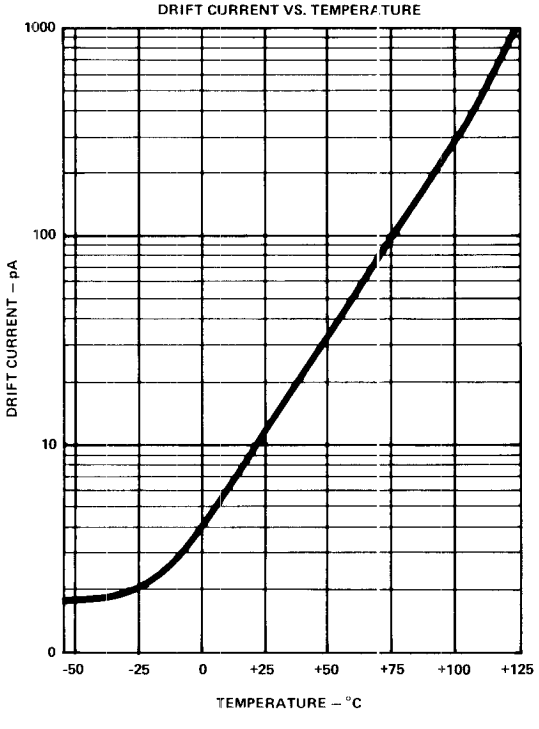
$$\frac{\Delta V}{\Delta T}\ \text{(Volts/sec)} = \frac{\text{I(pA)}}{C_H\text{(pF)}}$$

Performance Curves

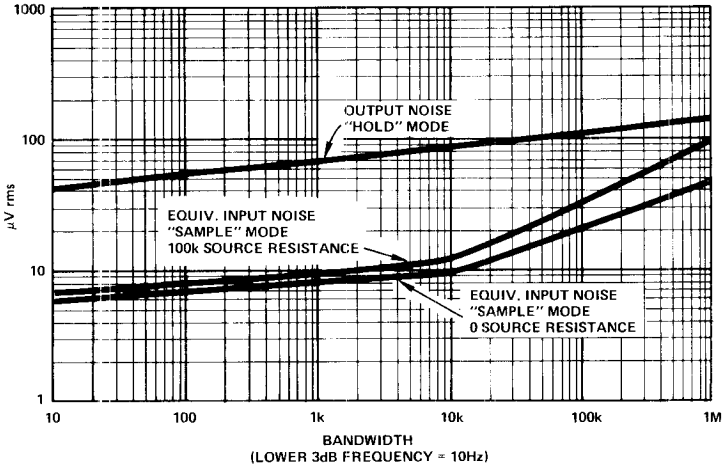
V_{SUPPLY} = ±15V dc, T_A = +25°C, C_H = 1,000pF unless otherwise specified)



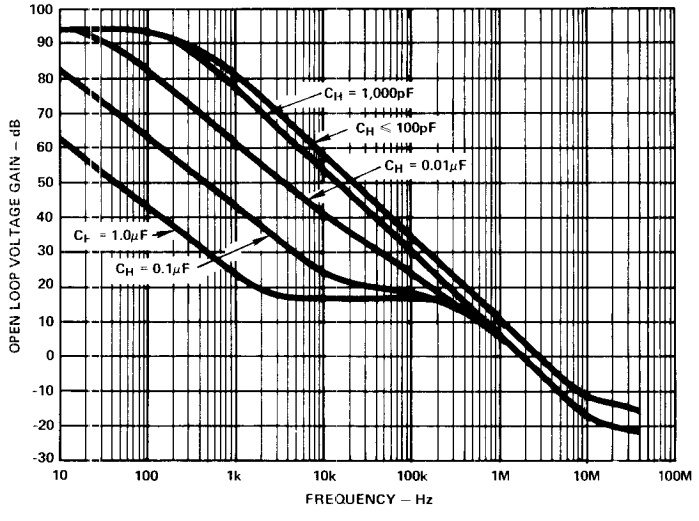
Typical Sample-and-Hold Performance as a Function of Holding Capacitance



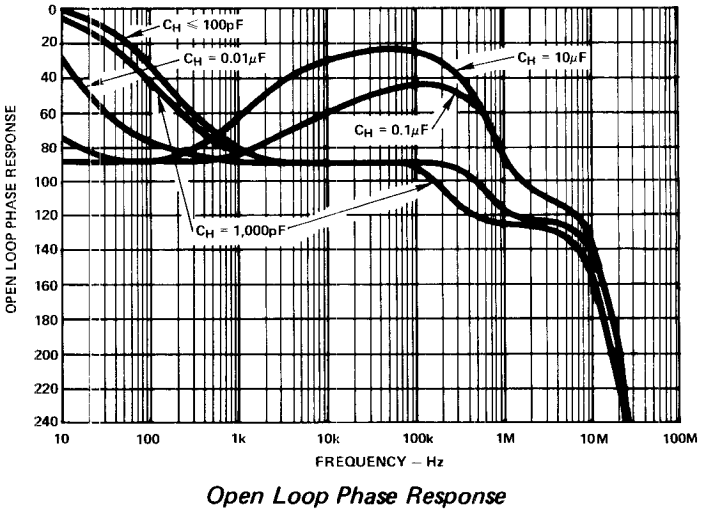
Drift Current vs. Temperature



Broadband Noise Characteristics



Open Loop Frequency Response



Open Loop Phase Response