USB Audio Controller & Line-in Interface With Class-D Power Amplifier and Headphone Driver

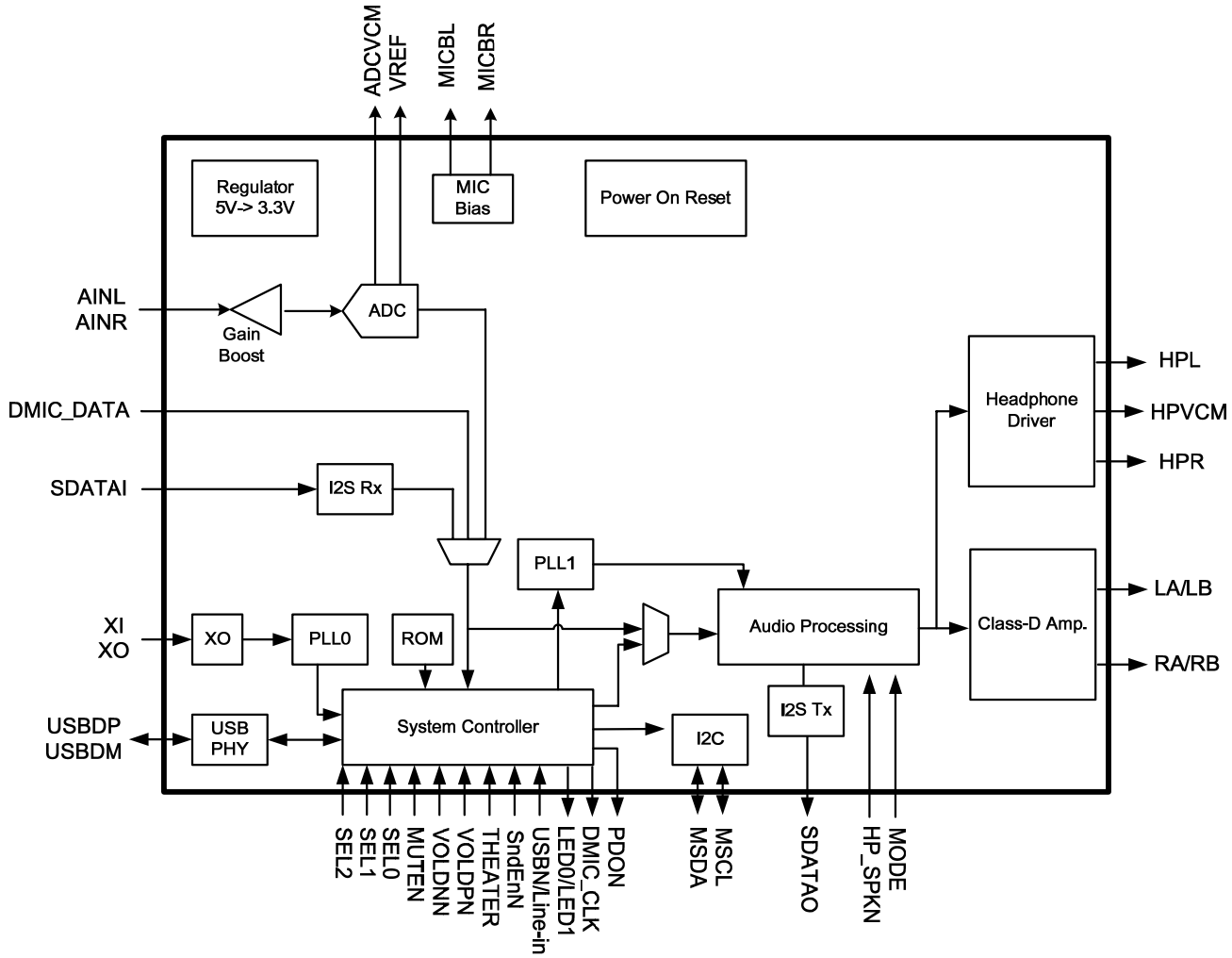
Features

- Compliant with USB Specification v1.1, and USB 2.0 full speed
- Compliant with USB 3.0 super speed operation
- Embedded high efficiency, high performance class-D stereo amplifier
- Embedded headphone driver
- Loudspeaker PSNR & DR (A-weighting, I^2S input)
  88dB (PSNR), 91dB (DR) with bead filter@8ohm
- Headphone PSNR & DR (A-weighting, I^2S input)
  91dB (PSNR), 91dB (DR) with @32ohm
- Embedded stereo ADC with microphone boost
- Embedded Power-On-Reset circuit
- Support I^2S input (master and slave mode) and I^2S output interface (master mode)
- +6dB gain enhancement (Theater function)
- Support sampling frequency 44.1/48KHz for playback and recording
- Pin to set recording source from internal ADC or external ADC
- Pin to set speaker or headphone mode
- Support microphone and line-in function switching
- Support volume/mute control with external button
- LED indicator function for playback, mute and recording mute
- Support 3D surround sound
- Support microphone bias
- Support digital microphone interface for recording
- Power Clipping function for speaker protection
- External EEPROM interface for vendor specific and hardware configuration via I^2C
- I^2S input port allows AD62553 to receive ESMT's high performance ADC (i.e. AD12250)
- I^2S output port allows AD62553 to control ESMT's high performance audio devices (i.e. AD82586/AD83586/AD82581)
- PWM output port to drive ESMT's high performance PWM class-D audio device (i.e. AD9258)
- Loudspeaker output power with external power
  2.1W x2CH into 4Ω@10% THD+N
  1.4W x2CH into 8Ω@10% THD+N
- Efficiency with bead filter
  75% for 8Ω load @ Po = 1.4W x 2CH
  70% for 4Ω load @ Po = 2.1W x 2CH
- Built-in 5V to 3.3V regulator for internal device operation
- Anti-pop design
- Over-temperature protection
- Under-voltage shutdown
- Short-circuit detection
- Single 12 MHz crystal input
- 3.3V operation with 5V tolerate I/O
- Supports Windows Me/2000/XP/Vista/7, Linux and Mac OS
- Integration circuit quality meet Win7 *and Win8 Hardware Logo* requirement
- 64-pin LQFP (7mmx7mm) package

Description

AD62553 is a highly integrated USB single chip for Stereo/Mono speaker or headphone. Many useful features are programmable with pins or I^2C control. When using the power supplied from the USB port (USB 3.0), AD62553 can drive a pair of up to 2.1W into 4ohm speakers due to the built-in, high efficiency and high performance class-D amplifiers. The device also has an I^2S input port and I^2S output port interface. The I^2S input port allows other external audio sources to use the class-D amplifier to share the speakers. The I^2S output port allows other high performance or high output power audio device requirement (i.e. AD82586/AD83586/AD82587).

Functional Block Diagram



Order Informaton

Product ID	Package	Packing / MPQ	Comments
AD62553-LH64NAY	LQFP-64L (7x7 mm)	2.5K Units / Small Box (250 Units / Tray, 10 Trays / Small Box)	Green
AD62553-LH64NAR	LQFP-64L (7x7 mm)	2K Units / Reel	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jt}(℃/W)	Exposed Thermal Pad
LQFP-64L	AD62553	27.4	1.33	6.0	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface.

Note 1.4: Ψ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface center.

Marking Information

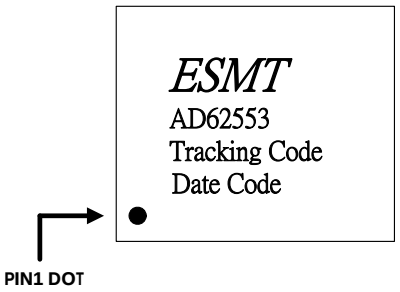
AD62553

Line 1 : LOGO

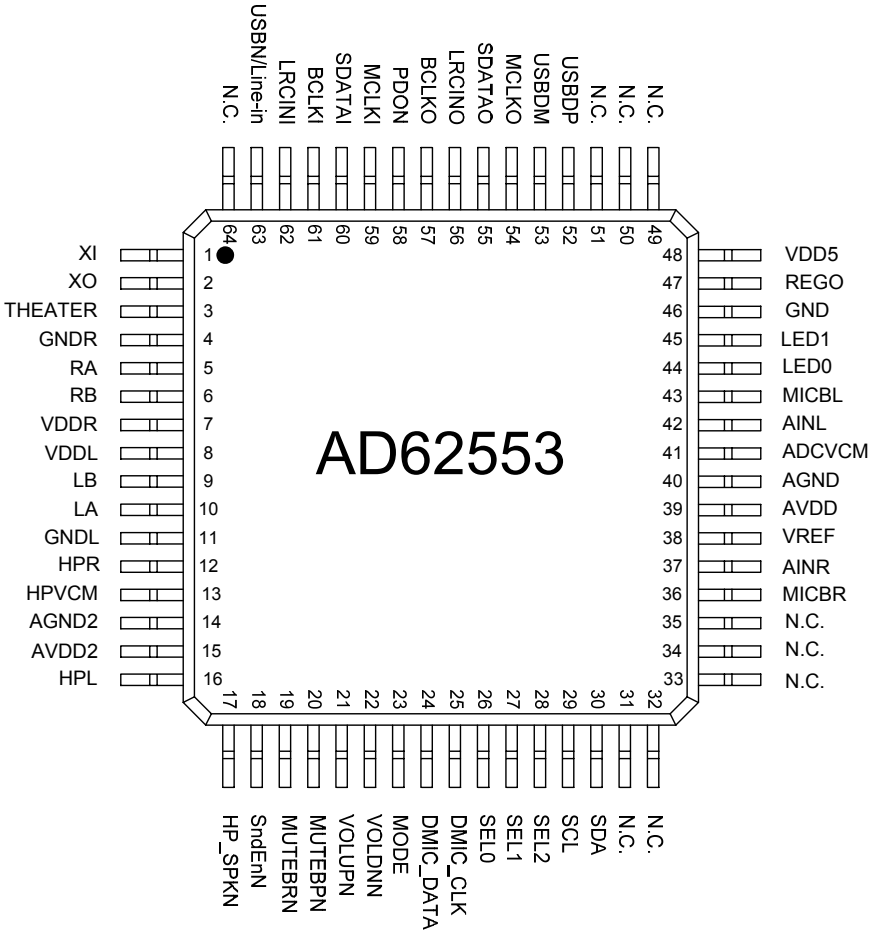
Line 2 : Product no.

Line 3 : Tracking Code

Line 4 : Date Code



Pin Assignment



Pin Description

Pin	Name	Type	Description	Characteristics
1	XI	I	Crystal input	With internal 1Mohm resistor connected to the pin of XO
2	XO	O	Crystal output	
3	THEATER	I	Theater mode, high active	5V tolerant Schmitt trigger TTL input buffer
4	GNDR	P	Ground for right channel	
5	RA	O	Right channel output+	
6	RB	O	Right channel output-	
7	VDDR	P	Supply for right channel	
8	VDDL	P	Supply for left channel	
9	LB	O	Left channel output-	
10	LA	O	Left channel output+	
11	GNDL	P	Ground for left channel	

12	HPR	O	Headphone right channel output	
13	HPVCM	O	Headphone common-mode voltage decoupling pin	
14	AGND2	P	Headphone ground	
15	AVDD2	O	Headphone 5V supply	
16	HPL	O	Headphone left channel output	
17	HP_SPKN	I	0: Speaker mode + I2S output mode 1: Headphone mode	3.3V tolerant Schmitt trigger TTL input buffer
18	SndEnN	I	Surround enable, low active	With internal 100kohm pull-up resistor
19	MUTEBRN	I	Recording mute, low active	With internal 100kohm pull-up resistor
20	MUTEBPN	I	Power-down and mute of Class D, low active	With internal 100kohm pull-up resistor
21	VOLUPN	I	Volume up, low active	With internal 100kohm pull-up resistor
22	VOLDNN	I	Volume down, low active	With internal 100kohm pull-up resistor
23	MODE	I	0 : Output depend HP_SPKN setting 1: Both of speaker & headphone output simultaneously	With internal 100kohm pull-up resistor
24	DMIC_DATA	I	Data input to AD3150	3.3V tolerant Schmitt trigger TTL input buffer
25	DMIC_CLK	O	Clock output to AD3150	
26	SEL0	I	0:AD82581 1:AD82586/AD83586	
27	SEL1	I	0: internal ADC 1: external ADC	
28	SEL2	I	SEL1 : 0 → 1 : ADC as Microphone; 0: ADC as Line-in SEL1 : 1 → 1 : Use DMIC ; 0: Use AD12250	
29	SCL	I/O	I^2C's SCL, with a 4.7kohm pull high (this pin floating is prohibited)	
30	SDA	I/O	I^2C's SDA, with a 4.7kohm pull high (this pin floating is prohibited)	
31	N.C.		Not connected	
32	N.C.		Not connected	
33	N.C.		Not connected	
34	N.C.		Not connected	

35	N.C.		Not connected	
36	MICBR	O	Microphone right channel voltage supply (3mA)	
37	AINR	I	Analog signal right channel	
38	VREF	O	Reference voltage	
39	AVDD	P	ADC's 3.3V supply	
40	AGND	P	ADC's Ground	
41	ADCVCM	O	ADC common mode voltage decoupling pin	
42	AINL	I	Analog signal left channel	
43	MICBL	O	Microphone Left channel voltage supply (3mA)	
44	LED0	O	LED indicator for playback	
45	LED1	O	LED indicator for recording	
46	GND	P	Ground	
47	REGO	P	Regulator output	
48	VDD5	P	5V supply voltage	
49	N.C.		Not connected	
50	N.C.		Not connected	
51	N.C.		Not connected	
52	USBDP	I/O	USB data D+	With internal 1.5kohm pull-up resistor
53	USBDM	I/O	USB data D-	
54	MCLKO	O	AD8XXX series Master clock(256xFs)	
55	SDATAO	O	AD8XXX series Serial audio output	
56	LRCINO	O	AD8XXX series L/R clock output	
57	BCLKO	O	AD8XXX series BCLK output	
58	PDON	O	Power-down output indicator pin $\overline{\text{USB}}$/LineIn = 0; $\overline{\text{PDO}}$ = Low during USB device unconfiguration $\overline{\text{PDO}}$ = High during USB device configuration $\overline{\text{USB}}$/LineIn = 1; $\overline{\text{PDO}}$ = Low during D+/D- at reset state (USBDP=0, USBDM=0)	

			$\overline{PDO}$ = High during D+/D- at non-reset state	
59	MCLKI	I/O	ADC I2S Master clock (256xFs) input port	
60	SDATAI	I	Serial audio data input	3.3V tolerant Schmitt trigger TTL input buffer
61	BCLKI	I/O	ADC I2S BCLK inout port	
62	LRCINI	I/O	ADC I2S L/R clock inout port	
63	USBN/Line-in	I	Output source select pin; 0: USB mode 1: Line-in mode	3.3V tolerant Schmitt trigger TTL input buffer
64	N.C.		Not connected	

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
VDD5	Supply for regulator input pin of VDD5	-0.3	6	V
PVDD	Supply for the pin of VDDL and VDDR	-0.3	6	V
AVDD2	Supply for the pin of AVDD2	-0.3	6	V
AVDD	Supply for the pin of AVDD	-0.3	3.6	V
V_i	Input Pin Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
VDD5	Supply for regulator input pin of VDD5	4.5~5.5	V
PVDD	Supply for the pin of VDDL and VDDR	4.5~5.5	V
AVDD2	Supply for the pin of AVDD2	4.5~5.5	V
AVDD	Supply for the pin of AVDD	3.15~3.45	V
T_J	Junction Operating Temperature	0~125	°C
T_A	Ambient Operating Temperature	0~70	°C

Digital Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	2.0		3.45	V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{OH}	High-Level Output Voltage	2.4		V_{REGO}	V
V_{OL}	Low-Level Output Voltage			0.4	V
C_I	Input Capacitance		6.4		pF

General Electrical Characteristics

1. Condition: T_A=25℃ unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}	Supply current during suspend mode			350		uA
	USB controller operation current	3.3V		75		mA
V_{REGO}	Regulator output voltage	4.5V≦VDD5 ≦5.5V	3.15	3.3	3.45	V
	Regulator current limit				100	mA
T_{SENSOR}	Junction temperature for driver shutdown			150		°C
	Temperature hysteresis for recovery			30		°C
UV_H	Under voltage disabled (for VDD5 and PVDD)			3.8		V
UV_L	Under voltage enabled (for VDD5 and PVDD)			3.7		V

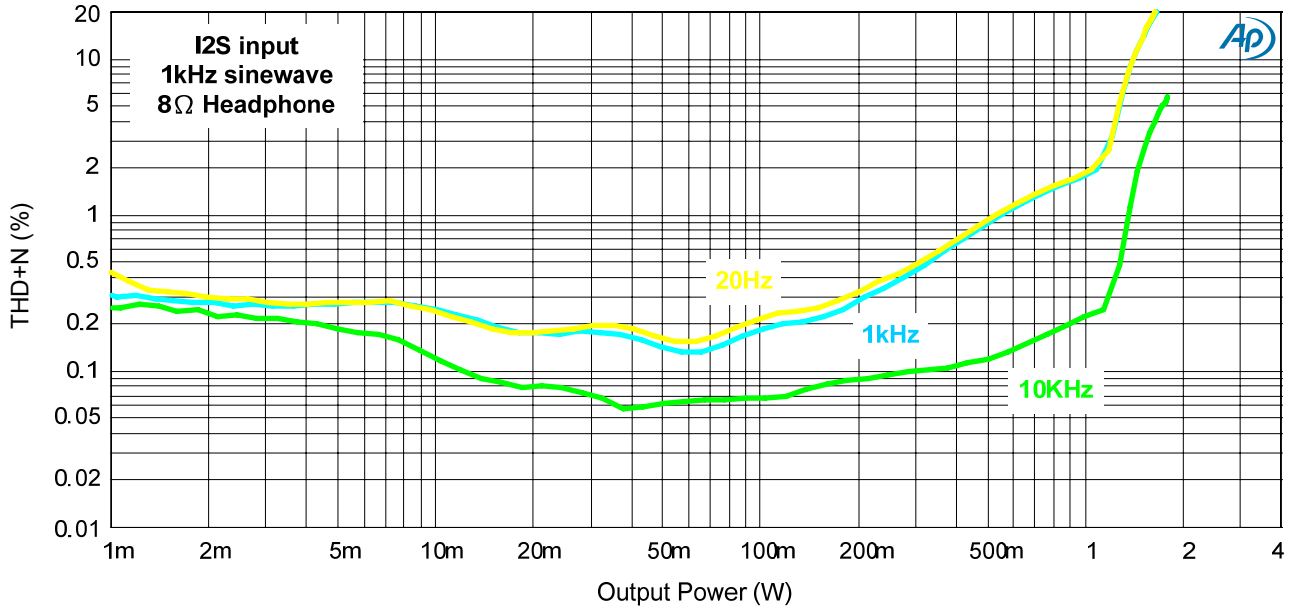
Electrical Characteristics and Specifications for Speaker

1. Condition: T_A=25℃; VDD5=PVDD=5V; AVDD=3.3V; F_S=48kHz; I2S input; Load=8Ω with Bead filter; Input is 1kHz sinewave unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O	RMS Output Power for Each Channel	THD+N=10%			1.4		W
		THD+N=1%			0.54		W
THD+N	Total Harmonic Distortion + Noise	P_O=270mV			0.38		%
SNR	Signal to Noise Ratio ***(Note 1)***	P_O=1.1W	-1dB		88		dB
DR	Dynamic Range ***(Note 1)***		-60dB		91		dB
	Channel Separation	P_O=1W			90		dB
	Noise Level				150		uV

Note 1: Measured with A-weighting filter and external power.

THD+N vs. Output Power (Load: 8ohm)



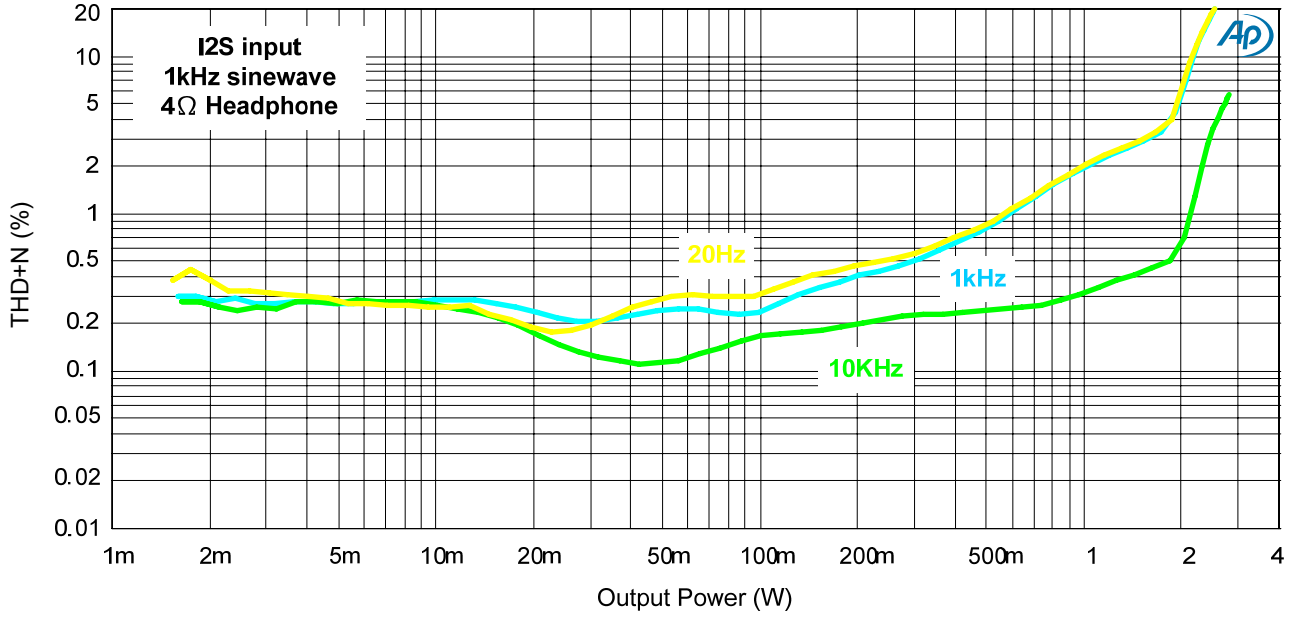
Electrical Characteristics and Specifications for Speaker (cont.)

1. Condition: T_A=25℃; VDD5=PVDD=5V; AVDD=3.3V; F_S=48kHz; I2S input; Load=4Ω with Bead filter; Input is 1kHz sinewave unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O	RMS Output Power for Each Channel	THD+N=10%			2.1		W
		THD+N=1%			0.58		W
THD+N	Total Harmonic Distortion + Noise	P_O=290mV			0.5		%
SNR	Signal to Noise Ratio ***(Note 1)***	P_O=1.1W	-1dB		85		dB
DR	Dynamic Range ***(Note 1)***		-60dB		90		dB
	Channel Separation	P_O=1W			87		dB
	Noise Level				135		uV

Note 1: Measured with A-weighting filter and external power.

THD+N vs. Output Power (Load: 4ohm)



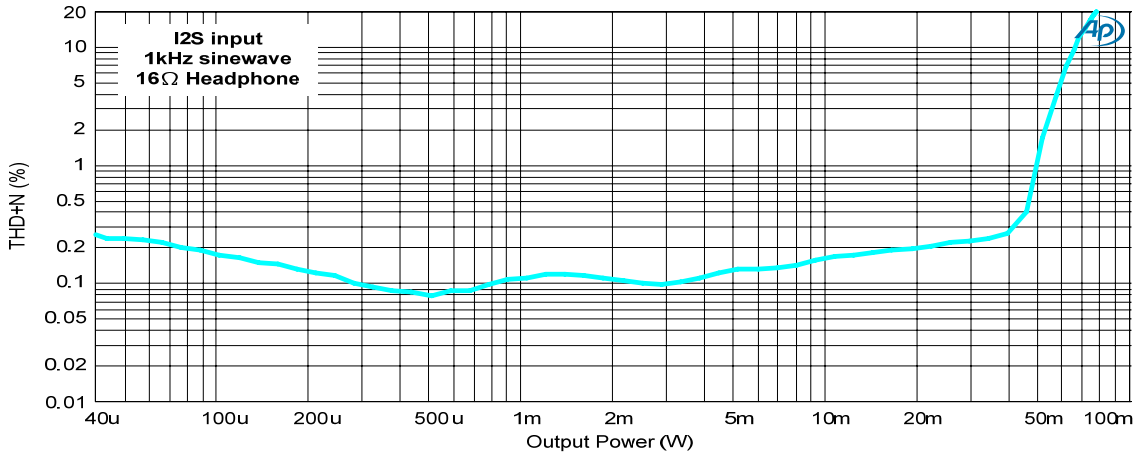
Electrical Characteristics and Specifications for Headphone

1. Condition: T_A=25℃; VDD5=PVDD=AVDD2=5V; AVDD=3.3V; F_S=48kHz; I2S input; Load=16Ω; Input is 1kHz sinewave unless otherwise specified.

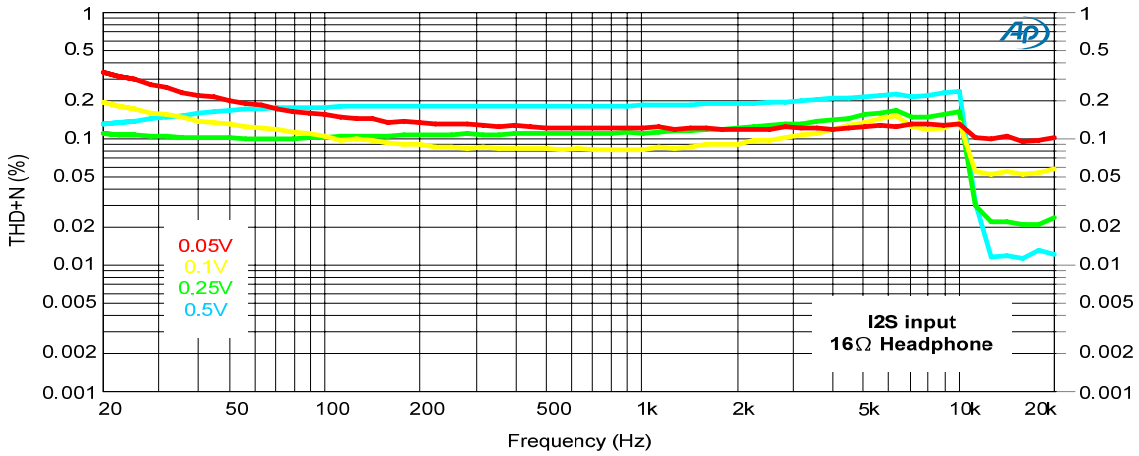
Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O	RMS Output Power for Each Channel	THD+N=10%			66		mW
		THD+N=1%			49		mW
THD+N	Total Harmonic Distortion + Noise	10mW			0.17		%
		1mW			0.11		%
SNR	Signal to Noise Ratio ***(Note 1)***		-1dB		89		dB
DR	Dynamic Range ***(Note 1)***		-60dB		91		dB
	Channel Separation	@1kHz	P_O=0.5V		84		dB
	Noise level				46		uV

Note 1: Measured with A-weighting filter and external power.

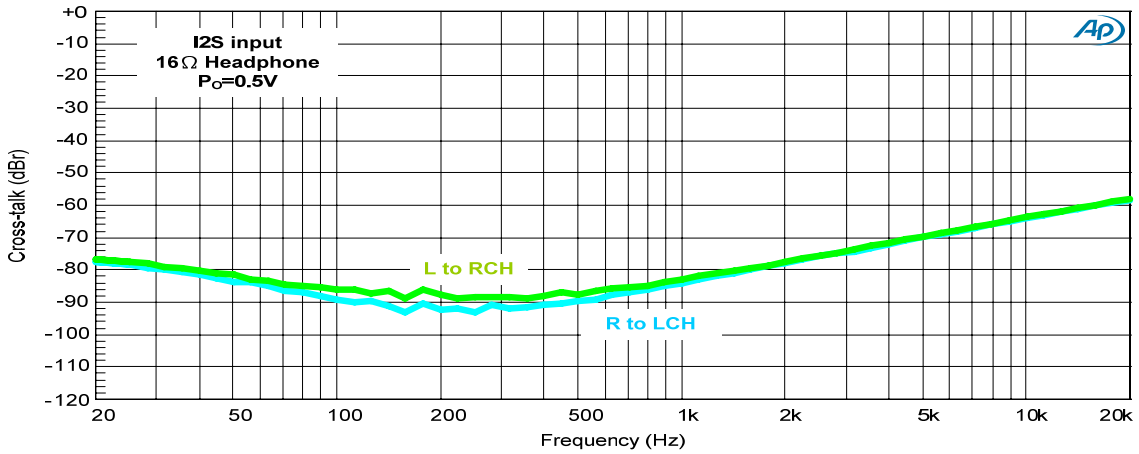
THD+N vs. Output Power (Load: 16ohm)



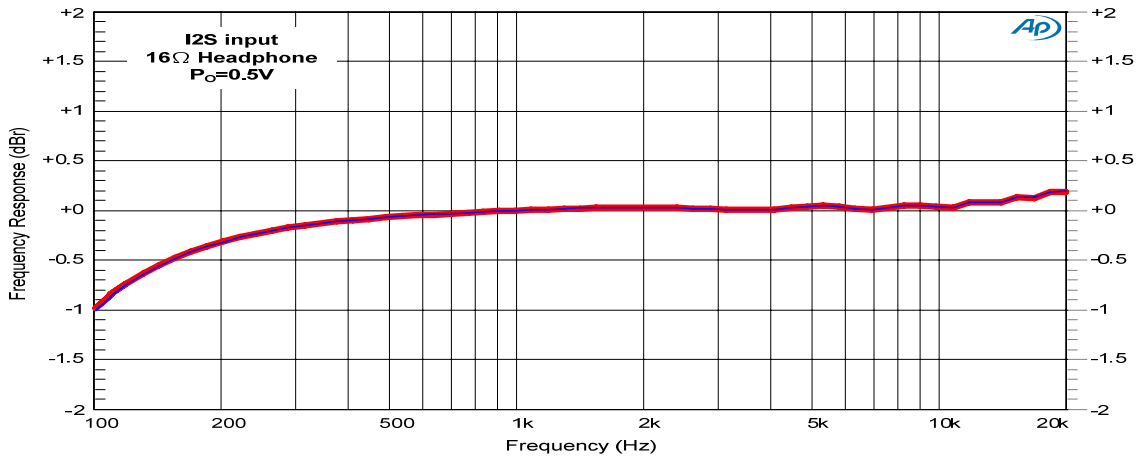
THD+N vs. Frequency (Load: 16ohm)



Channel Separation (Load: 16ohm)



Frequency Response (Load: 16ohm)



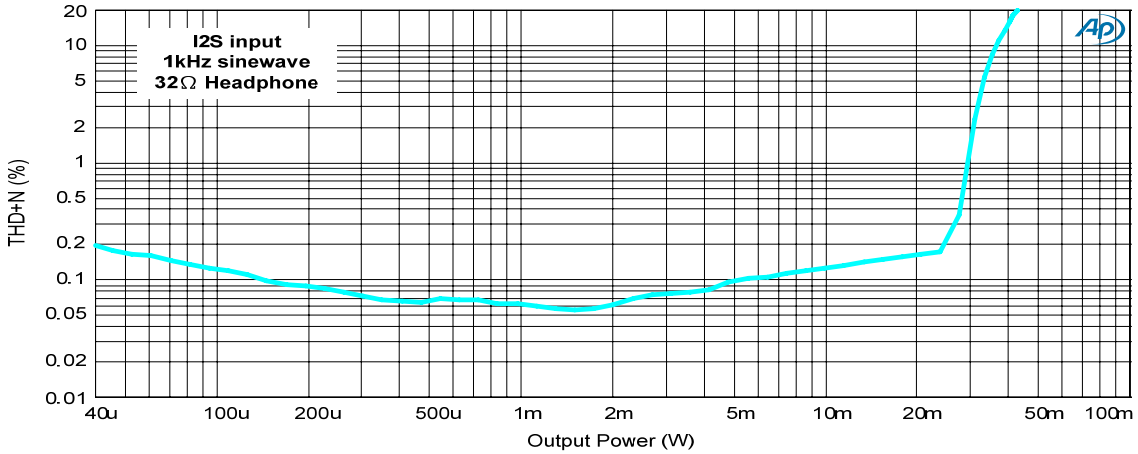
Electrical Characteristics and Specifications for Headphone

1. Condition: T_A=25℃; VDD5=PVDD=AVDD2=5V; AVDD=3.3V; F_S=48kHz; I2S input; Load=32Ω; Input is 1kHz sinewave unless otherwise specified.

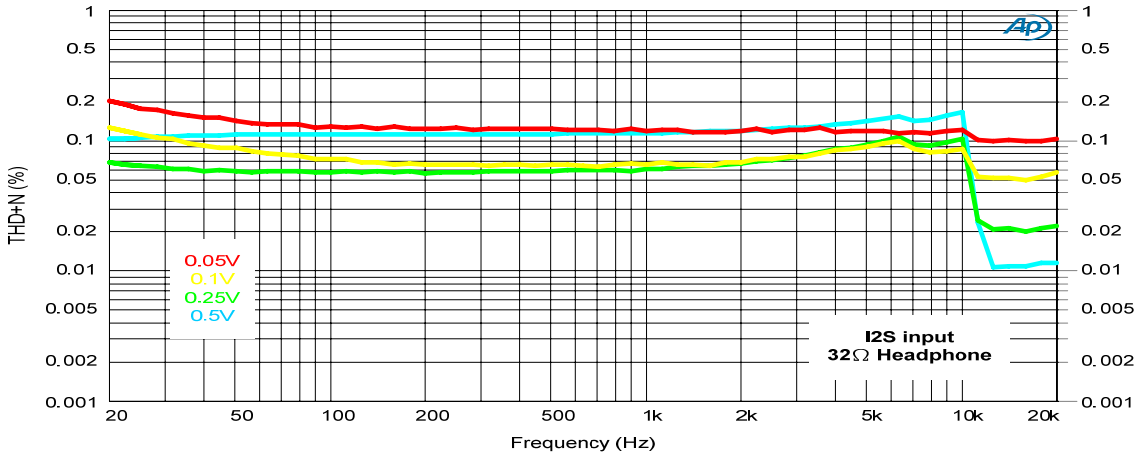
Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O	RMS Output Power for Each Channel	THD+N=10%			37		mW
		THD+N=1%			29		mW
THD+N	Total Harmonic Distortion + Noise	10mW			0.13		%
		1mW			0.06		%
SNR	Signal to Noise Ratio ***(Note 2)***		-1dB		91		dB
DR	Dynamic Range ***(Note 2)***		-60dB		91		dB
	Channel Separation	@1kHz	P_O=0.5V		89		dB
	Noise level				45		uV

Note 2: Measured with A-weighting filter and external power.

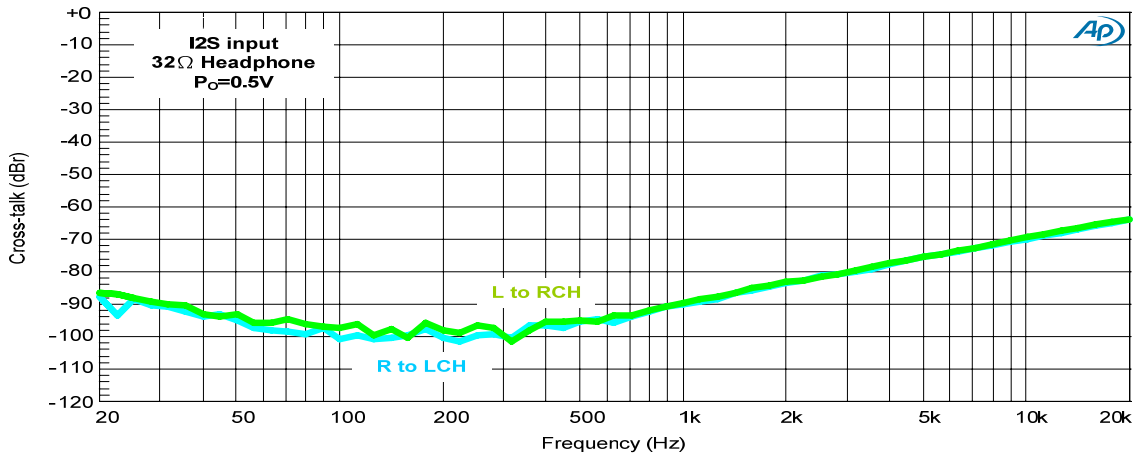
THD+N vs. Output Power (Load: 32ohm)



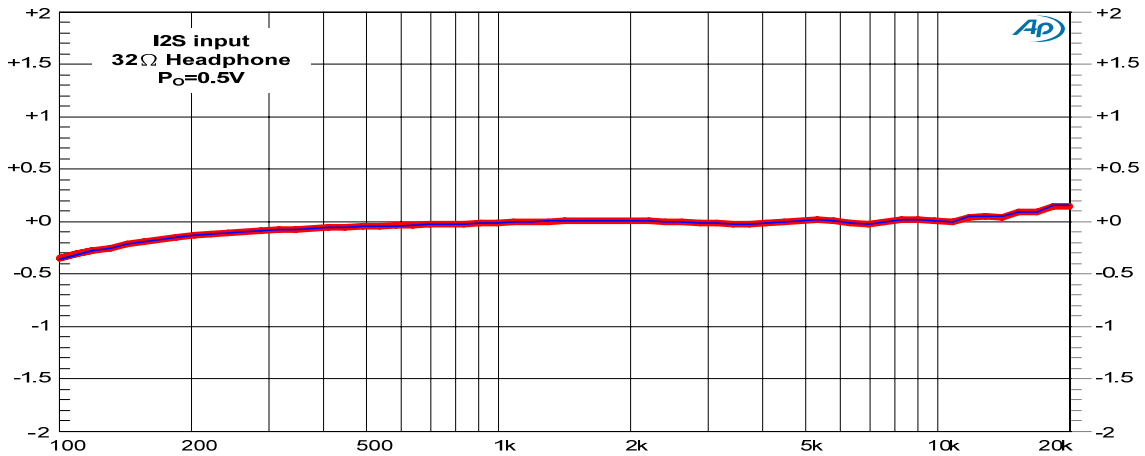
THD+N vs. Frequency (Load: 32ohm)



Channel Separation (Load: 32ohm)

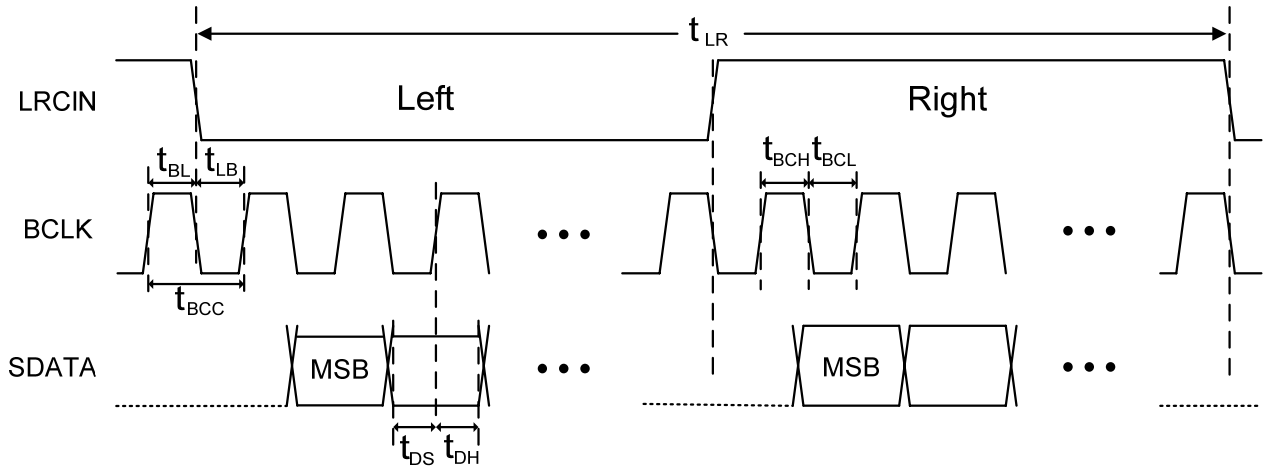


Frequency Response (Load: 32ohm)



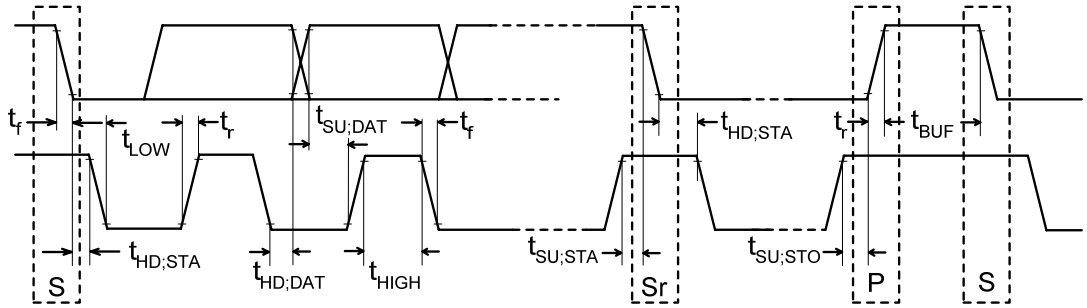
Interface Configuration

- I^2S



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	10.41		125	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	50			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	50			ns
t_{BCC}	BCLK Period ($1/64F_S$)	162.76		1953	ns
t_{BCH}	BCLK Pulse Width High	81.38		976.5	ns
t_{BCL}	BCLK Pulse Width Low	81.38		976.5	ns
t_{DS}	SDATA Set-Up Time	50			ns
t_{DH}	SDATA Hold Time	50			ns

- I^2C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition	$t_{HD,STA}$	4.0	---	0.6	---	μs
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	μs
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	μs
Data hold time for I^2C bus devices	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Data setup time	$t_{SU;DAT}$	250	---	100	---	ns
Rise time of both SDA and SCL signals	t_r	---	1000	20+0.1Cb	300	ns
Fall time of both SDA and SCL signals	t_f	---	300	20+0.1Cb	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	---	1.3	---	μs
Capacitive load for each bus line	C_b		400		400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	---	$0.1V_{DD}$	---	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	---	$0.2V_{DD}$	---	V

I²C-Bus Transfer Protocol

- Introduction

  AD62553 employs I²C-bus transfer protocol. Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock (SCL) on the bus. AD62553 is also a slave device in all of its communications.

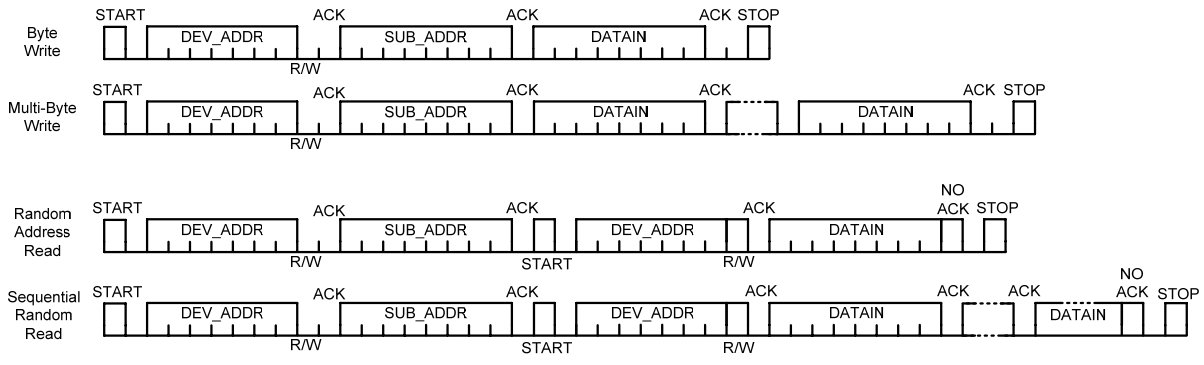
- Protocol
  - START and STOP condition

    START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must be preceding any command for data transfer. A low to high transition on the SDA line while SCL is high defines a STOP condition. A STOP condition terminates communication between AD62553 and the master device on the bus.
  - Data validity

    The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low. AD62553 samples the SDA signal at rising edge of the clock signal SCL.
  - Device addressing

    The master generates 7-bit address to recognize slave device. When AD62553 receives 7-bit address matched with 7'b0111010, AD62553 will acknowledge at 9th bit time (8th bit time is for R/W bit). The bytes following the device identification address are interpreted as internal sub-addresses.
  - Data transferring

    Every byte put on SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with MSB first. As the figure shown below, in both write and read operation, AD62553 supports single-byte and multi-byte. Please refer to the figure shown below for detail data-transferring protocol.



Operation Descriptions

The following figure illustrates two more advanced applications that use AD62553, together with an internal ADC or an external ADC, e.g., AD12250 from ESMT that can convert stereo line-in audio to I^2S output to send to AD62553, and/or an external high-end Class-D amplifier such as AD82586x/AD82587x via AD62553's I^2S output.

Both applications, a switch used to select audio stream from either USB port or Line-in port. When the audio stream is from Line-in port, the device is operating as "docking station" mode. When the audio stream is from USB port, the device is operating as "USB headphone" mode. When AD82586x/AD82587x is used, since it can deliver 10Wx2 + 20W (subwoofer) power or 20Wx2 power, USB bus power may be insufficient and local power supply is required. Functional description follows.

SEL2, SEL1, SEL0

	0	1
SEL0	AD8287x	AD82586x/AD83586

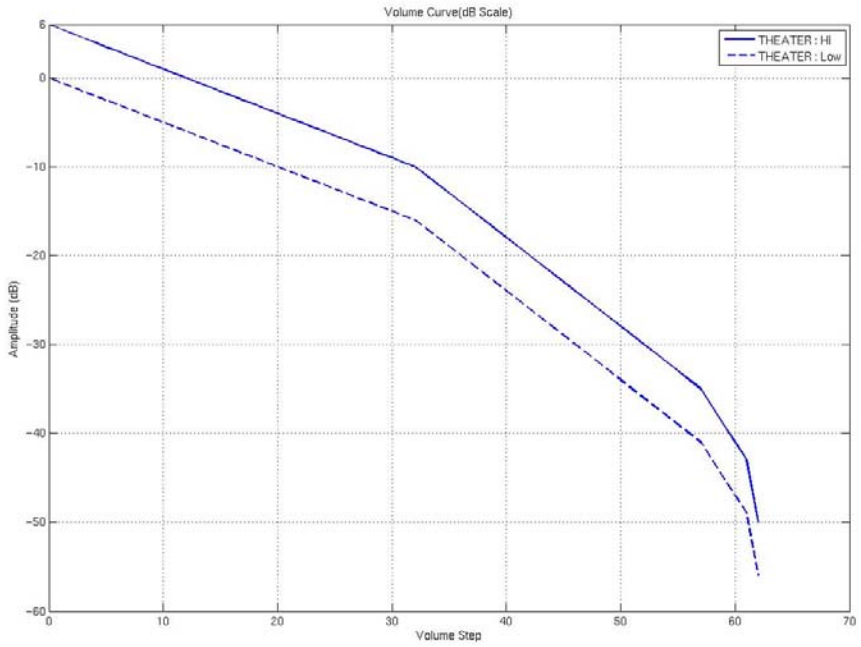
SEL2	SEL1	Audio Source
0	0	Internal ADC as line-in
1	0	Internal ADC as Microphone
0	1	I2S data in
1	1	PDM data in

RESET

The AD62553 has embedded power on reset circuit. When AD62553 power on, need wait 0.5ms reset process for the system ready.

Volume Control of Playback

Audio volume control up/down is low active by VOLUPB/VOLDNB pins. Duration of low level must be longer than 3ms. The highest volume gain is +6dB for THEATER pin is logic High and 0dB for THEATER pin is logic Low, referred to the original input signal level. The volume gain range is from +6dB to -50dB at THEATER pin is High or 0dB to -56dB at THEATER pin is Low.



Volume Control of Recording

The volume gain range is from +6 dB to -50 dB the same as the playback.

Mute control

Both MUTEBN and MUTEBRN are low active. It also supports USB HID device class for host panel control synchronization. Duration of low level must be longer than 3ms.

Stereo dual ADC

AD62553 has a dual channel stereo ADC input as microphone or line-in recording source according to SEL1 and SEL2 pins. After USB plug in, the USB descriptor can be changed accordingly.

LED display

LED0 can be used as USB operation indicator when data transmit. LED1 can be used as recording mute indicator.

Microphone Gain Boost

When use internal ADC as microphone in the AD62553, the internal gain boost has two stages. One is 20dB and the other can select from 0dB to 22.5dB.

Self-protection circuit

AD62553 has built-in thermal, short-circuit and under-voltage detection circuits. If the internal thermal detection junction temperature is higher than 150°C, the output will be turned off. The thermal detection circuit has a temperature hysteretic characteristic such that the AD62553 will return to normal operation when the device is cooled down to about 30°C. Due to the process variation, the triggering temperature values can have around 10% variation.

To protect loudspeaker power stages when the loudspeaker output are shorted each other or shorted to GND, the output loading detection circuits are built-in and proper protection action will take place once the short circuit condition is detected.

To protect headphone power driver when the headphone output are shorted each other or shorted to VDD or GND, the output loading detection circuits are built-in and proper protection action will take place once the short circuit condition is detected.

For normal operation, the loudspeaker output resistance larger than 3.4Ω is required. Once the short-circuit condition is detected, the output power stages will be shut off. After the short-circuit condition is happened, the AD62553 will be auto release the output power stages at every 42ms if the short-circuit condition is removed.

Anti-pop design

AD62553 is has an anti-pop circuit to suppress the annoying pop sounds during initial power on, power down/up, mute, power off and volume level change.

Under Voltage protection circuit

Once the V_{DD5} is lower than 3.7V, AD62553 will turn off its headphone driver and the digital circuit will cease operation. When V_{DD5} becomes larger than 3.8V, AD62553 will return to normal operation.

Switching between USB mode and docking station mode

When the USBN/Line-in pin is low, the input audio stream is from USB port as USB speaker (or headphone) mode. When this pin is high, the input audio stream is from AINL/AINR, I^2S input port or DMIC_DATAL/DMIC_DATAR as docking station mode.

Switching between headphone mode and speaker mode

When the HP_SPKN pin is low, it is speaker mode and the audio output is from pins LA/LB and RA/RB. When this pin is HP_SPKN pin is high, it turns to headphone mode and the output is from pins HPL and HPR.

Audio Recording

AD62553 can record external audio source from AINL/AINR microphone/line in, I^2S SDATAI or DMIC_DATAL/DMIC_DATAR digital microphone by SEL1 and SEL2 pins. Supports 44.1kHz and 48kHz sampling frequency for audio recording, the default setting is 48kHz for audio recording in AD62553.

3D Surround sound Mode

When SndEnN pin is low, 3D surround sound Mode is enabled. AD62553 provides the virtual surround sound technology with greater separation and depth for stereo signals and synthesizes a 3D stereo sound field.

Power Consideration

AD62553 can be powered by the USB port directly. However, the maximum current supplied by each USB port is limited 500mA. If the total power requirement of the USB audio subsystem is higher than this, local power supply, e.g., a local AC adaptor will have to be used. If the audio subsystem is attached to an USB hub, which is not locally powered, the maximum power from each USB port is only limited to 100mA, and local power must be supplied.

Power Clipping

AD62553 support power clipping function for protect speaker. There are 16 levels can be set through I^2C.

I^2C master/slave mode

AD62553 can also operate as master or slave in a system when LRCINO is pulled low or high with 1MΩ at power up initially (during 15ms after 90% of V_{REGO}). When LRCINO is pulled low, the AD62553 operates as I^2C master mode. In I^2C master mode, the AD62553 also can control the external class-D amp. AD82586/AD82581 via I^2C. When LRCINO is pulled high, the AD62553 operates as I^2C slave mode. When operating as a slave mode, AD62553's functions are controlled by micro-controller. Functions in PC are all disable.

I²S master/slave mode

The pins LRCINI, BCLKI and MCLKI of the AD62553 can also operate as I^2S master or slave mode in a system when BCLKO is pulled low or high with 1MΩ at power up initially (during 15ms after 90% of V_{REGO}). When BCLKO is pulled low, the AD62553 operates as I^2S master mode. In I^2S master mode, the pins LRCINI, BCLKI and MCLKI are output pins can drive the other devices. When BCLKO is pulled high, the AD62553 operates as I2S slave mode. When operating as a slave mode, the pins LRCINI, BCLKI and MCLKI are input pins need the other device provide clocks.

Note 1: In slave mode, it must be followed the frequency ratio of MCLKI = 256×LRCINI for correct operation.

Note 2: In slave mode, AD62553 only support I2S source playback and can't support USB source playback/recording.

Mixing mode

The AD62553 can mix USB audio signal and anlog/I^2S audio signal to the output when MCLKO is pulled high with 1MΩ at power up initially (during 15ms after 90% of V_{REGO}). When MCLKO is pulled high, the volume of mixing signal can control through address 8 and 9 via I^2C. Also can mute and un-mute mixing signal through the bit 5 and 6 of the address 1.

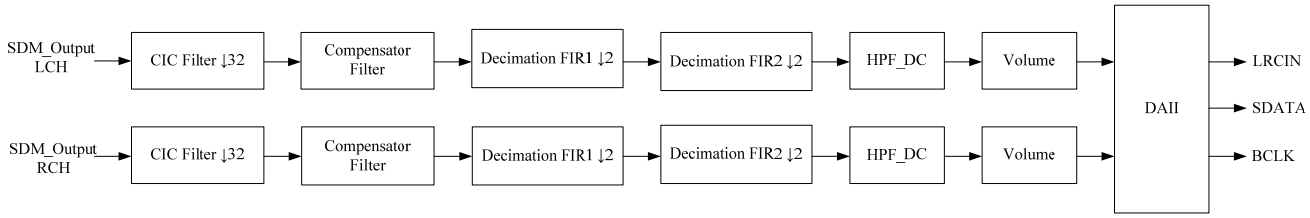
Stereo/Mono mode

The output of the AD62553 can configure the stereo or mono mode when SDATAO is pulled high or low with 1MΩ at power up initially (during 15ms after 90% of V_{REGO}). When SDATAO is pulled low, the output of the AD62553 is the stereo mode. When SDATAO is pulled high, the output of the AD62553 is the mono mode and the audio signal is mix from the left and right channel.

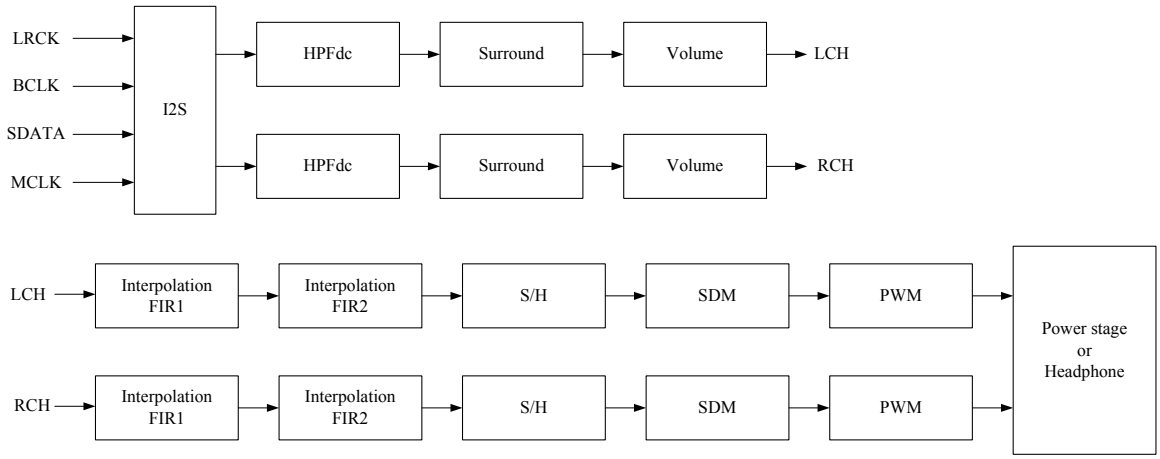
Register Table

The audio signal processing data flow is shown as the following figure. Users can control these functions by programming appropriate setting to register table, which is summarized in this section. More detail information will be described in next section.

Recording signal processing flow



Playback signal processing flow



Add.	Name	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0X00	PB_CTL	Reserved	MIX_CH1_MUTE	MIX_CH2_MUTE	PB_ZDEN	PB_SRSEN	PB_HPF	PB_CH1_MUTE	PB_CH2_MUTE
0X01	PB_LVOL	Reserved		PB_CH1Vol [5]	PB_CH1Vol [4]	PB_CH1Vol [3]	PB_CH1Vol [2]	PB_CH1Vol [1]	PB_CH1Vol [0]
0X02	PB_RVOL	Reserved		PB_CH2Vol [5]	PB_CH2Vol [4]	PB_CH2Vol [3]	PB_CH2Vol [2]	PB_CH2Vol [1]	PB_CH2Vol [0]
0X03	RE_CTL	ADC_V3	ADC_V2	ADC_V1	ADC_V0	ADC_BOOST	RE_HPF	RE_CH1_Mute	RE_CH2_Mute
0X04	RE_LVOL	C1V[7]	C1V[6]	RE_CH1Vol [5]	RE_CH1Vol [4]	RE_CH1Vol [3]	RE_CH1Vol [2]	RE_CH1Vol [1]	RE_CH1Vol [0]
0X05	RE_RVOL	C2V[7]	C2V[6]	RE_CH2Vol [5]	RE_CH2Vol [4]	RE_CH2Vol [3]	RE_CH2Vol [2]	RE_CH2Vol [1]	RE_CH2Vol [0]
0X06	ZD&MICB	ZD_LEVEL[1]	ZD_LEVEL[0]	Reserved			MICBPDB	MBVSEL[1]	MBVSEL[0]
0X07	PL	Reserved			PL_EN	PL_Level [3]	PL_Level [2]	PL_Level [1]	PL_Level [0]

Detail Description for Register

In this section, please note that the highlighted columns are the default value of these tables. If no highlighted, it is because the default setting of this bit is determined by external pin.

Address 0: Playback State control

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	Reserved			
B[6]	MIX_CH1_MUTE	Mixing Channel1 Mute	1	Mute
			0	Un-mute
B[5]	MIX_CH2_MUTE	Mixing Channel2 Mute	1	Mute
			0	Un-mute
B[4]	PB_ZDEN	Playback Zero-Detection Enable	1	Enable
			0	Disable
B[3]	PB_SRSEN	Playback Surround Enable	1	Enable
			0	Disable
B[2]	PB_HPF	Playback High Pass Filter	1	Enable
			0	Disable
B[1]	PB_CH1_MUTE	Playback Channel1 Mute	1	Mute
			0	Un-mute
B[0]	PB_CH2_MUTE	Playback Channel2 Mute	1	Mute
			0	Un-mute

Address 1: Playback Left Channel Volume Control

BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	PB_CH1Vol[5:0]	Playback Left Channel Volume Control	000000	+6dB
			000001	+5.5dB
			…	…
			001100	+0dB
			001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Address 2: Playback Right Channel Volume Control

BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	PB_CH2Vol[5:0]	Playback Right Channel Volume Control	000000	+6dB
			000001	+5.5dB
			…	…
			001100	+0dB
			001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Address 3: Recording State control

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	ADC_V3	DESCRIPTION 2nd OP Gain control	0000	0 dB
			0001	5 dB
			0010	8 dB
			0011	10 dB
B[6]	ADC_V2		0100	12 dB
			0101	14 dB
			0110	15 dB
			0111	16.6 dB
B[5]	ADC_V1		1000	17.6 dB
			1001	18.6 dB
			1010	19.2 dB
			1011	19.8 dB
B[4]	ADC_V0		1100	20.4 dB
			1101	21 dB
			1110	21.7 dB
			1111	22.5 dB
B[3]	ADC_BOOST	1st OP Gain boost enable	1	Enable
			0	Disable
B[2]	RE_HPF	Recording High Pass Filter	1	Enable
			0	Disable
B[1]	RE_CH1_Mute	Recording Channel1 Mute	1	Mute
			0	Un-mute
B[0]	RE_CH2_Mute	Recording Channel2 Mute	1	Mute

			0	Un-mute

Address 4: Recording Left Channel Volume Control

BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	PB_CH1Vol[5:0]	Recording Left Channel Volume Control	000000	+6dB
			000001	+5.5dB
			…	…
			001100	+0dB
			001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Address 5: Recording Right Channel Volume Control

BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	PB_CH2Vol[5:0]	Recording Right Channel Volume Control	000000	+6dB
			000001	+5.5dB
			…	…
			001100	+0dB
			001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Address 6: Zero-Detection and Mic. Bias Setting

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	ZD_LEVEL	Zero Detection Level	11	-60dB
			10	-70dB
			01	-80dB
			00	zero
B[5]	Reserved			
B[4]	Reserved			
B[3]	Reserved			
B[2]	MICBPDB	Microphone Bias Voltage PowerDown	0	Power down
			1	Power up
B[1:0]	MBVSEL	Microphone Bias Voltage Control	11	0.9*AVDD
			10	0.8*AVDD
			01	0.6*AVDD
			00	0.5*AVDD

Address 7: Power Clipping Setting

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	Reserved			
B[6]	Reserved			
B[5]	Reserved			
B[4]	PC_EN	Power Clipping Enable	1	Enable
			0	Disable
B[3]	PC_Level	Power Clipping Level	0000	0dB
			0001	-2dB
B[2]			0010	-4 dB
			0011	-6dB
B[1]			0100	-8 dB
			…	
B[0]			1110	-28 dB
			1111	-30 dB

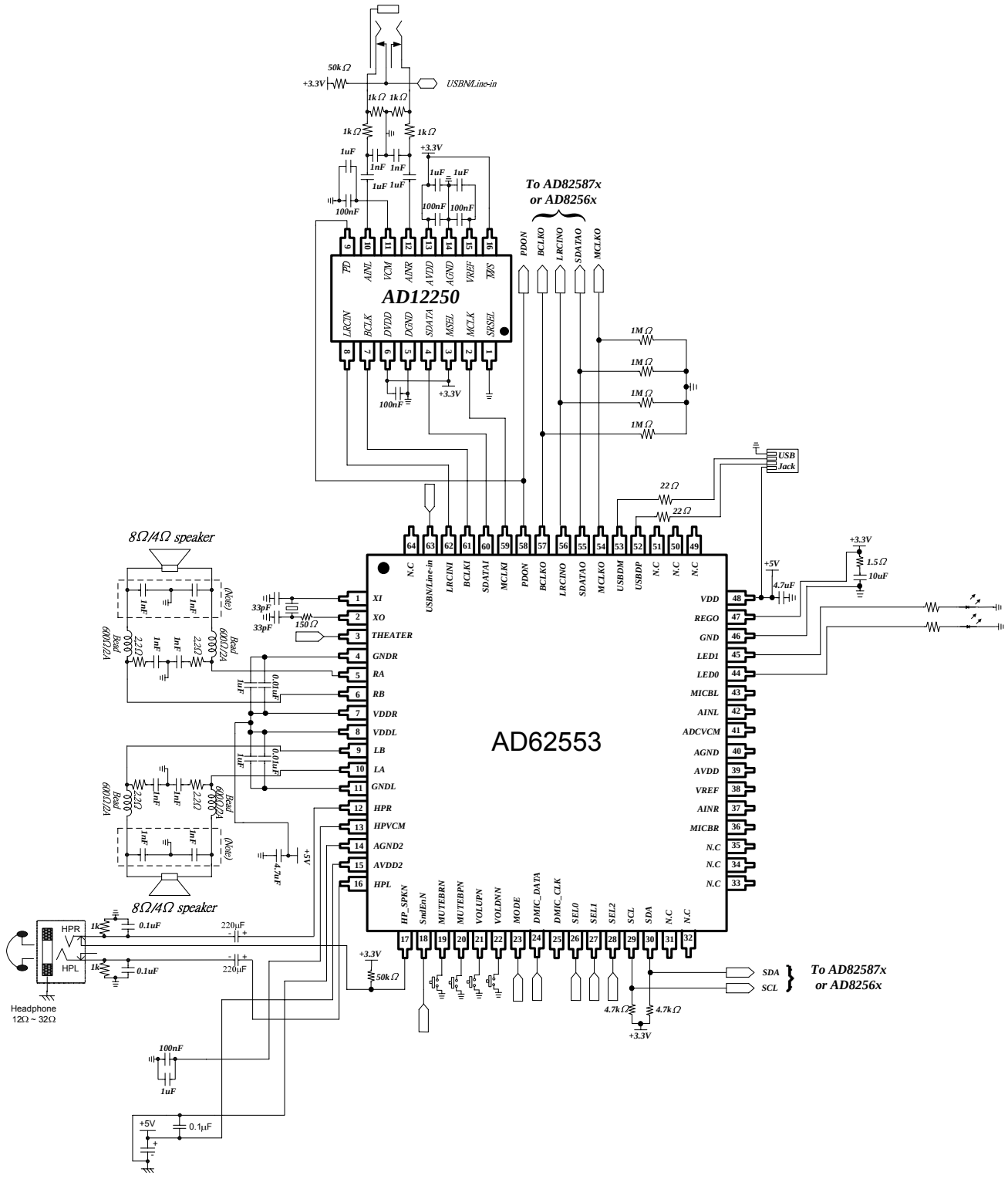
Address 8: Mixing Left Channel Volume Control

BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	Mix_CH1Vol[5:0]	Mixing Left Channel Volume Control	000000	+6dB
			000001	+5.5dB
			…	…
			001100	+0dB
			001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Address 9: Mixing Right Channel Volume Control

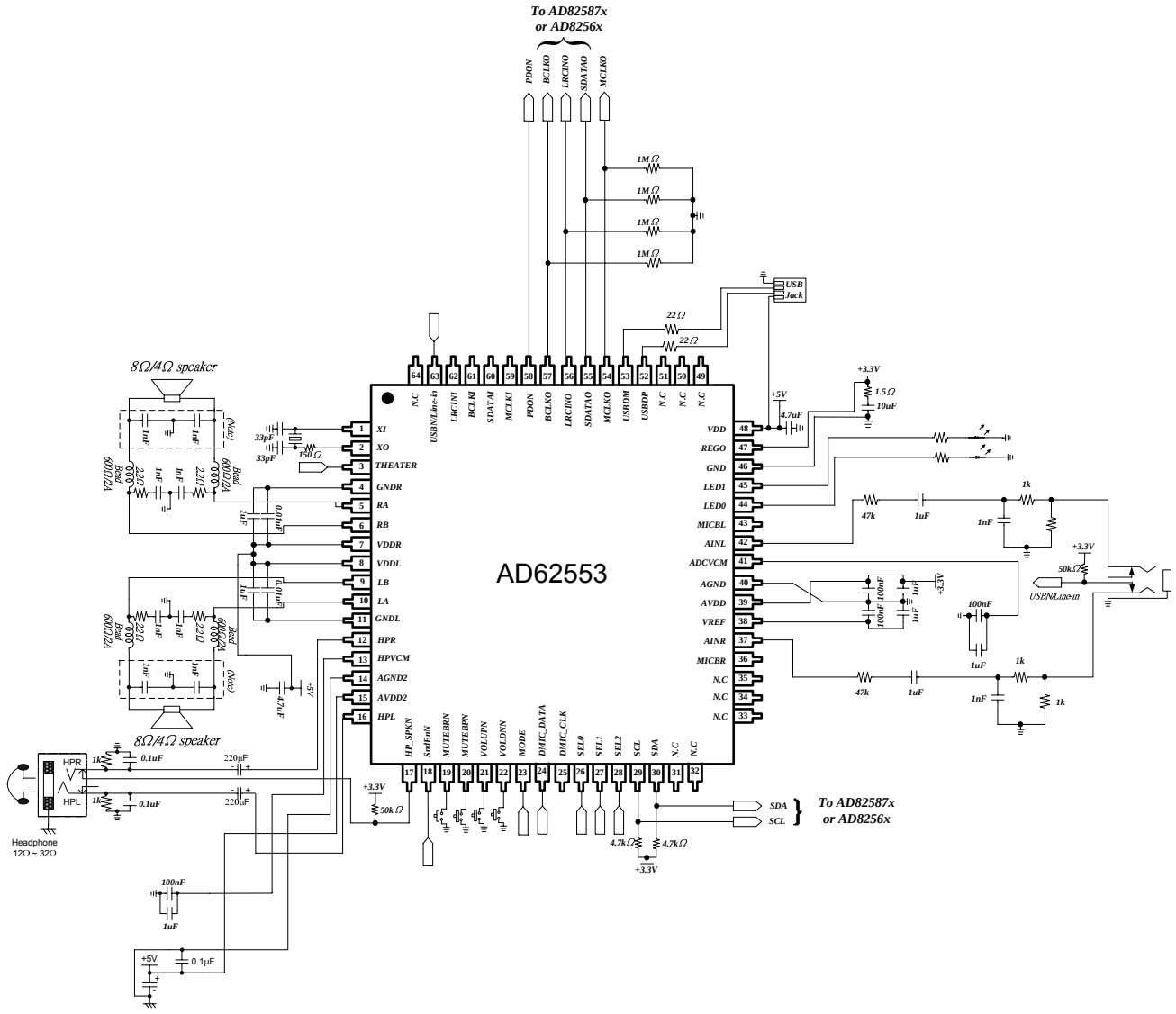
BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	Mix_CH2Vol[5:0]	Mixing Right Channel Volume Control	000000	+6dB
			000001	+5.5dB
			…	…
			001100	+0dB
			001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Application Circuit Examples, external ADC as Line-in



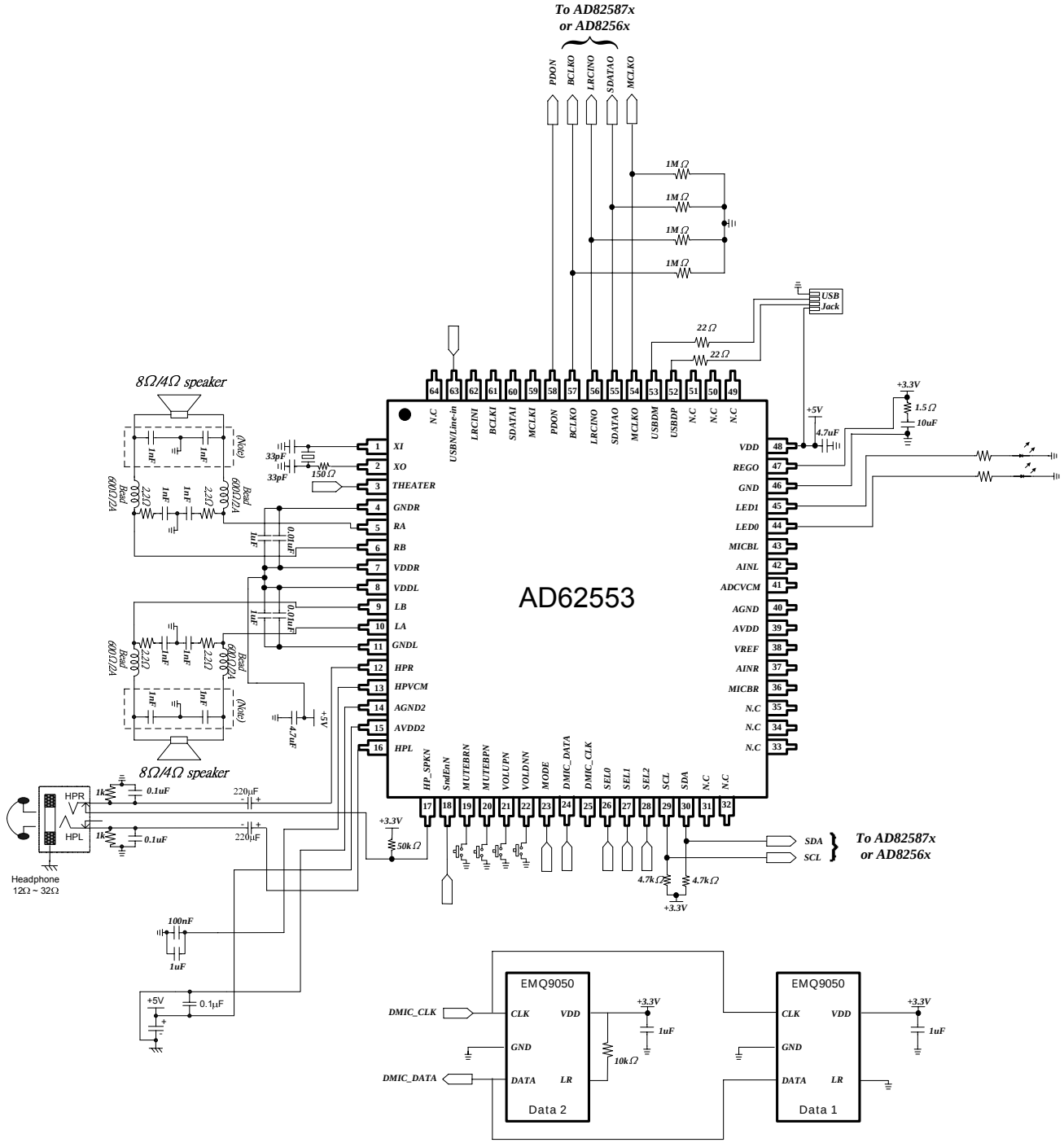
Note. EMI option components.

Application Circuit Examples, Internal ADC as Line-in



Note. EMI option components.

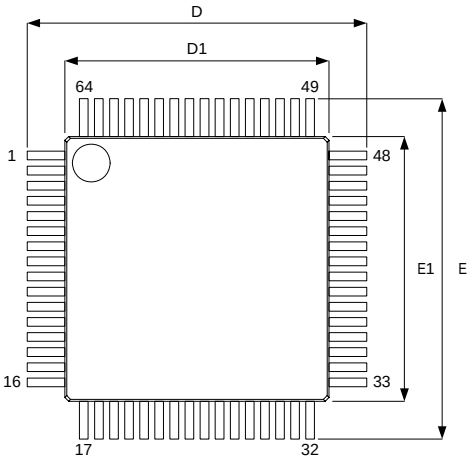
Application Circuit Examples with Digital Microphone Module input



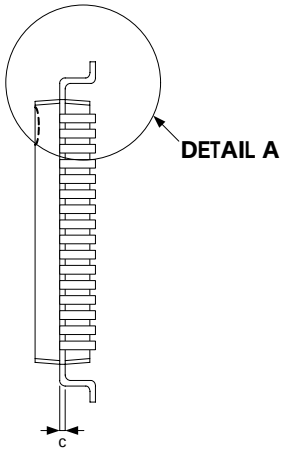
Note. EMI option components.

Package Outline Drawing

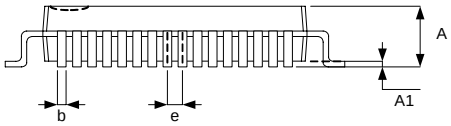
LQFP-64 (7x7 mm)



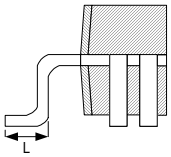
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.13	0.23
c	0.09	0.20
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.40 BSC	
L	0.45	0.75

Revision History

Revision	Date	Description
0.1	2014.08.04	Original version.
1.0	2015.03.04	Remove preliminary word and modify version to 1.0
1.1	2015.03.24	Update POD figure
1.2	2017.03.29	Update order information to add T/R packing (page 3)

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