USB Audio Controller with Class-D Power Amplifier
## & with Microphone/Line-in Interface

Features

- Compliant with USB Specification v1.1, and USB 2.0 full speed
- Compliant with USB 3.0 super speed operation
- Embedded stereo ADC with Microphone Boost
- Embedded Power-On-Reset circuit
- Embedded high efficiency, high performance Class-D stereo amplifier
- Support I^2S input (master and slave mode) and I^2S output interface (master mode)
- Support sampling frequency 44.1/48KHz for playback and recording
- Pin to set recording source from internal ADC or external ADC
- Pin to set speaker mode or I^2S output mode
- Support Microphone and line-in function switching
- Support volume/mute control with external button
- LED indicator function for playback, mute and recording mute
- Support 3D surround sound
- Support Microphone bias
- Support Digital microphone interface for recording
- Power Clipping function for speaker protection
- External EEPROM interface for vendor specific and hardware configuration via I^2C
- I^2S input port allows AD62557 to receive ESMT's high performance ADC(i.e. AD12250)
- I^2S output port allows AD62557 to control ESMT's high performance audio devices (i.e. AD82586/AD82581)
- PWM output port to drive PWM Class-D audio device (i.e. AD9258)
- Loudspeaker PSNR & DR (A-weighting, I^2S input) 86dB (PSNR), 88dB (DR) with bead filter
- Loudspeaker output power with external power
  2.1W x2CH into 4Ω@10% THD+N
  1.4W x2CH into 8Ω@10% THD+N
- Efficiency with bead filter
  75% for 8Ω load @ Po = 1.4W x 2CH
  70% for 4Ω load @ Po = 2.1W x 2CH

- Built-in 5V to 3.3V regulator for internal device operation
- Anti-pop design
- Over-temperature protection
- Under-voltage shutdown
- Short-circuit detection
- Single 12 MHz Crystal Input
- 3.3V operation I/O
- Supports Windows Me/2000/XP/Vista/7/8, Linux and MacOS
- Integration circuit quality meet Win7 *and Win8 Hardware Logo* requirement
- 48-pin E-LQFP Pb-free package

Description

AD62557 is a highly integrated USB single chip for Stereo/Mono speaker. Many useful features are programmable with pins or I^2C control. When using the power supplied from the USB port (USB 3.0), AD62557 can drive a pair of up to 2.1W into 4ohm speakers due to the built-in, high efficiency and high performance Class-D amplifiers. The device also has an I^2S input port and I^2S output port. The I^2S input port allows other external audio sources to use the Class-D amplifier to share the speakers. The I^2S output port allows other high performance audio device (i.e. AD82586/AD82581).

Functional Block Diagram
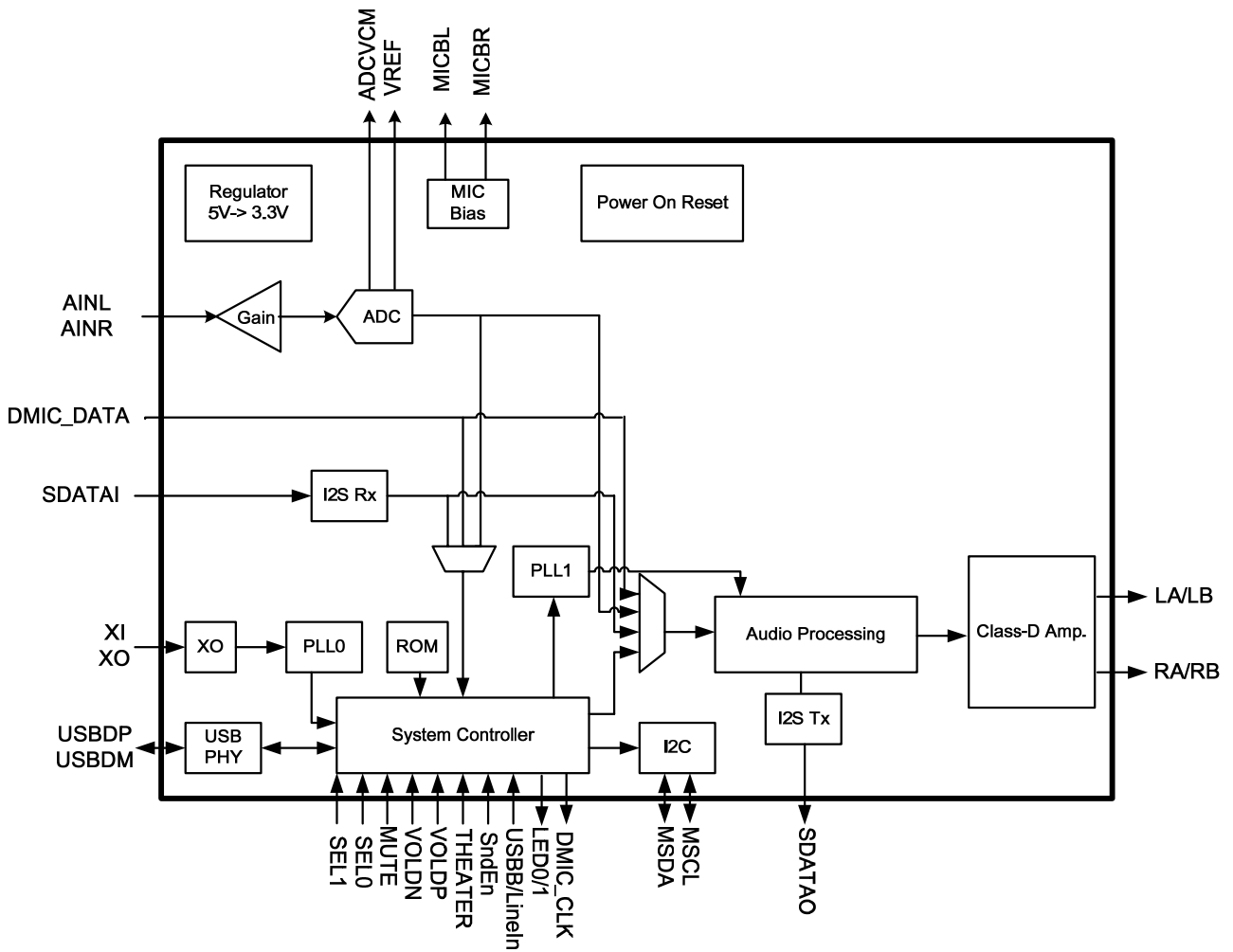
Order Informaton

Product ID	Package	Packing / MPQ	Comments
AD62557-LG48NAY	E-LQFP-48L (7x7 mm)	2.5K Units / Small Box (250 Units / Tray, 10 Trays / Small Box	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jt}(℃/W)	Exposed Thermal Pad
E-LQFP-48L	AD62557	27.4	1.33	6.0	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface.

Note 1.4: Ψ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface center.
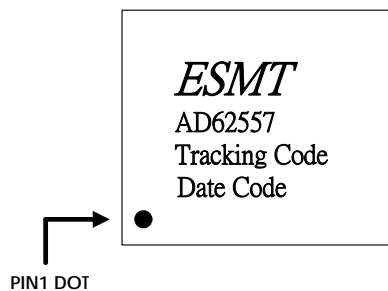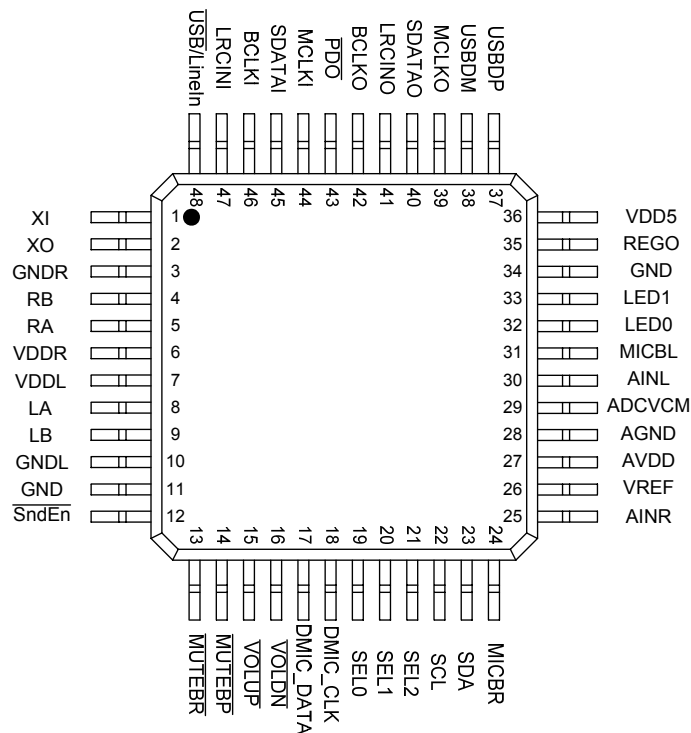
Marking Information

AD62557

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code

Line 4 : Date Code

ESMT
AD62557
Tracking Code
Date Code

PIN1 DOT

Pin Assignment

Pin Description

Pin	Name	Type	Description	Characteristics
1	XI	I	Crystal input	With internal 1Mohm resistor connected to the pin of XO
2	XO	O	Crystal output	
3	GNDR	P	Ground for right channel	
4	RA	O	Right channel output+	
5	RB	O	Right channel output-	
6	VDDR	P	Supply for right channel	
7	VDDL	P	Supply for left channel	
8	LB	O	Left channel output-	
9	LA	O	Left channel output+	
10	GNDL	P	Ground for left channel	
11	GND	P	Ground	
12	$\overline{SndEn}$	I	Surround enable	With internal 100kohm pull-up resistor
13	$\overline{MUTEBR}$	I	Recording Mute	With internal 100kohm pull-up resistor
14	$\overline{MUTEBP}$	I	Power-down and mute of Class-D	With internal 100kohm pull-up resistor
15	$\overline{VOLUP}$	I	Volume up, low active	With internal 100kohm pull-up resistor

16	$\overline{\text{VOLDN}}$	I	Volume down, low active	With internal 100kohm pull-up resistor
17	DMIC_DATA	I	Data input to AD3150	3.3V Schmitt trigger TTL input buffer
18	DMIC_CLK	O	Clock output to AD3150	
19	SEL0	I	0:AD82581 1:AD82586/AD83586	
20	SEL1	I	0: internal ADC 1: external ADC	
21	SEL2	I	SEL1 : 0 → 1 : ADC as Microphone; 0: ADC as Line-in SEL1 : 1 → 1 : Use DMIC ; 0: Use AD12250	
22	SCL	I/O	I²C's SCL, with a 4.7kohm pull high (this pin floating is prohibited)	
23	SDA	I/O	I²C's SDA, with a 4.7kohm pull high (this pin floating is prohibited)	
24	MICBR	O	Microphone right channel voltage supply (3mA)	
25	AINR	I	Analog signal right channel	
26	VREF	O	Reference voltage	
27	AVDD	P	ADC's 3.3V supply	
28	AGND	P	ADC's Ground	
29	ADCVCM	O	ADC common mode voltage decoupling pin	
30	AINL	I	Analog signal left channel	
31	MICBL	O	Microphone Left channel voltage supply (3mA)	
32	LED0	O	LED indicator for playback	
33	LED1	O	LED indicator for recording	
34	GND	P	Ground	
35	REGO	P	Regulator output	
36	VDD5	P	5V supply voltage	
37	USBDP	I/O	USB data D+	With internal 1.5kohm pull-up resistor
38	USBDM	I/O	USB data D-	
39	MCLKO	O	AD8XXX series Master clock(256xFs)	
40	SDATAO	O	AD8XXX series Serial audio output	
41	LRCINO	O	AD8XXX series L/R clock output	
42	BCLKO	O	AD8XXX series BCLK output	
43	$\overline{\text{PDO}}$	O	Power-down output	

44	MCLKI	I/O	ADC I2S Master clock (256xFs) input port	
45	SDATAI	I	Serial audio data input	3.3V Schmitt trigger TTL input buffer
46	BCLKI	I/O	ADC I2S BCLK input port	
47	LRCINI	I/O	ADC I2S L/R clock input port	
48	$\overline{USB}$/LineIn	I	Output source select pin; 0: USB mode 1: Line-in mode	3.3V Schmitt trigger TTL input buffer

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
VDD5	Supply for regulator input pin of VDD5	-0.3	6	V
PVDD	Supply for the pin of VDDL and VDDR	-0.3	6	V
AVDD	Supply for the pin of AVDD	-0.3	3.6	V
V_i	Input Pin Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	^{o}C
T_J	Junction Operating Temperature	0	150	^{o}C

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
VDD5	Supply for regulator input pin of VDD5	4.5~5.5	V
PVDD	Supply for the pin of VDDL and VDDR	4.5~5.5	V
AVDD	Supply for the pin of AVDD	3.15~3.45	V
T_J	Junction Operating Temperature	0~125	^{o}C
T_A	Ambient Operating Temperature	0~70	^{o}C

Digital Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	2.0		3.45	V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{OH}	High-Level Output Voltage	2.4		V_{REGO}	V
V_{OL}	Low-Level Output Voltage			0.4	V
C_I	Input Capacitance		6.4		pF

General Electrical Characteristics

● Condition: T_A=25℃ unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}	Supply current during suspend mode			350		uA
	USB controller operation current	3.3V		75		mA
V_{REGO}	Regulator output voltage	4.5V≦VDD5 ≦5.5V	3.15	3.3	3.45	V
	Regulator current limit				100	mA
T_{SENSOR}	Junction temperature for driver shutdown			150		^{o}C
	Temperature hysteresis for recovery			30		^{o}C
UV_H	Under voltage disabled (for VDD5 and PVDD)			3.8		V
UV_L	Under voltage enabled (for VDD5 and PVDD)			3.7		V

Electrical Characteristics and Specifications for Speaker

●   Condition: T_A=25℃; VDD5=PVDD=5V; AVDD=3.3V; F_S=48kHz; I2S input; Load=8Ω with Bead filter; Input is 1kHz sinewave unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O	RMS Output Power for Each Channel	THD+N=10%			1.4		W
		THD+N=1%			0.54		W
THD+N	Total Harmonic Distortion + Noise	P_O=270mV			0.38		%
SNR	Signal to Noise Ratio *(Note 1)*	P_O=1.1W	-1dB		88		dB
DR	Dynamic Range *(Note 1)*		-60dB		91		dB
	Channel Separation	P_O=1W			90		dB
	Noise Level				150		uV

Note 1: Measured with A-weighting filter and external power.

THD+N vs. Output Power (Load: 8ohm)
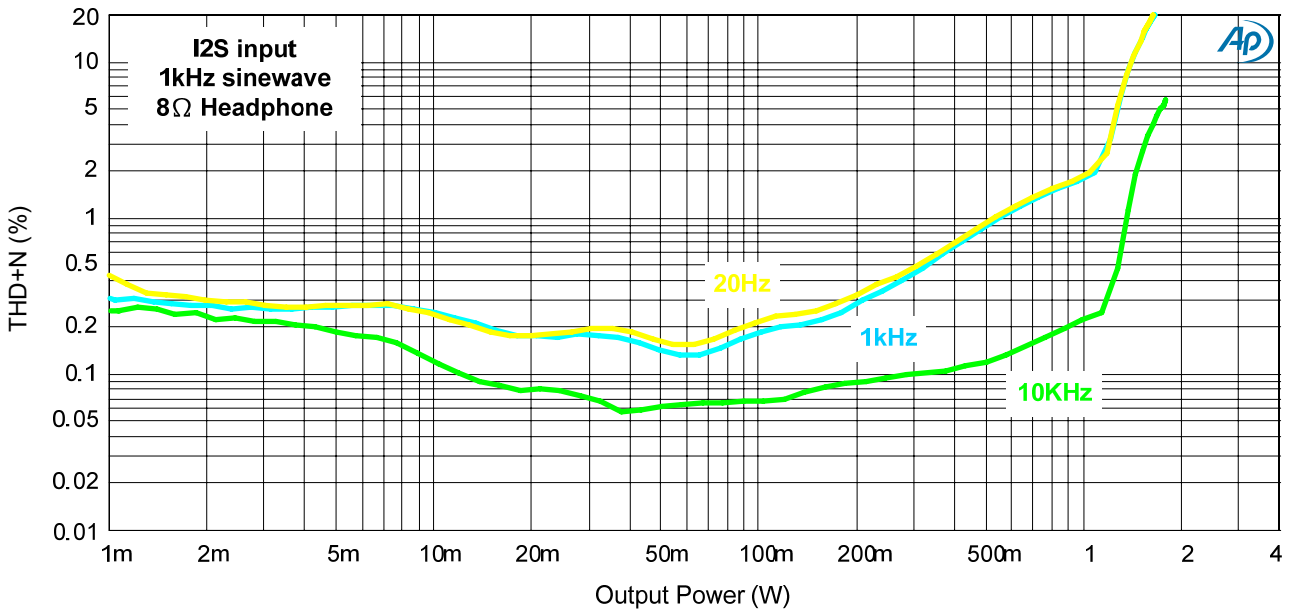
Electrical Characteristics and Specifications for Speaker (cont.)

● Condition: T_A=25℃; VDD5=PVDD=5V; AVDD=3.3V; F_S=48kHz; I2S input; Load=4Ω with Bead filter; Input is 1kHz sinewave unless otherwise specified.

| Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O	RMS Output Power for Each Channel	THD+N=10%			2.1		W
		THD+N=1%			0.58		W
THD+N	Total Harmonic Distortion + Noise	P_O=290mV			0.5		%
SNR	Signal to Noise Ratio *(Note 1)*	P_O=1.1W	-1dB		85		dB
DR	Dynamic Range *(Note 1)*		-60dB		90		dB
	Channel Separation	P_O=1W			87		dB
	Noise Level				135		uV

Note 1: Measured with A-weighting filter and external power.

THD+N vs. Output Power (Load: 4ohm)
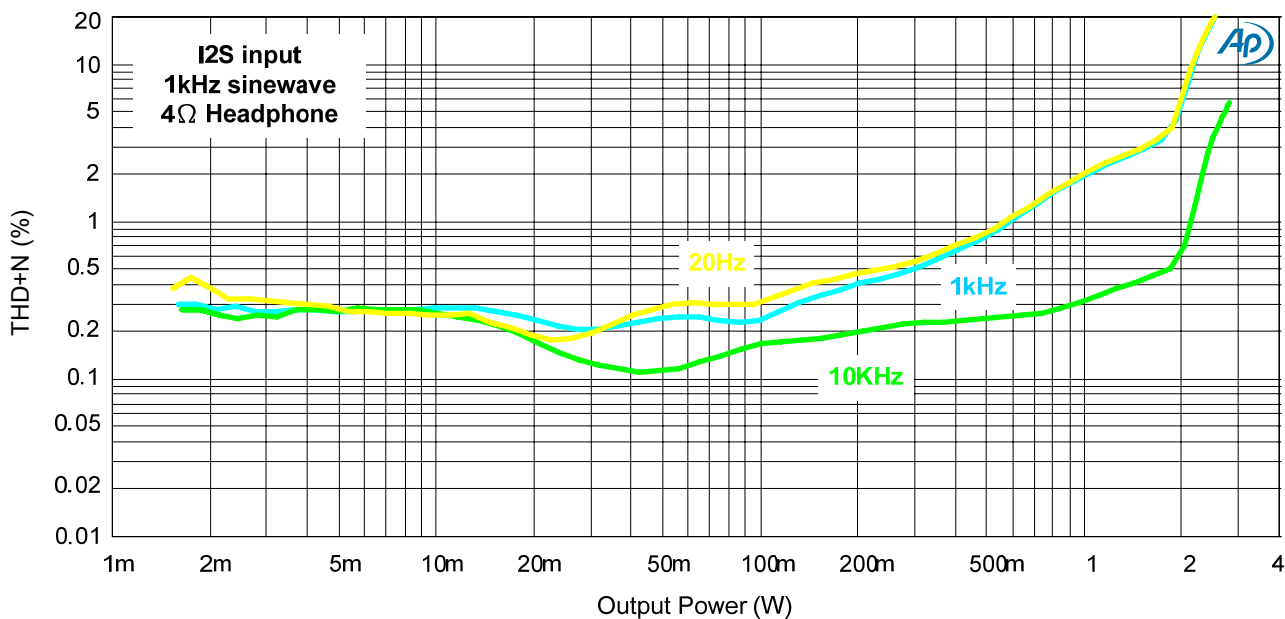
Interface Configuration

- I^2S
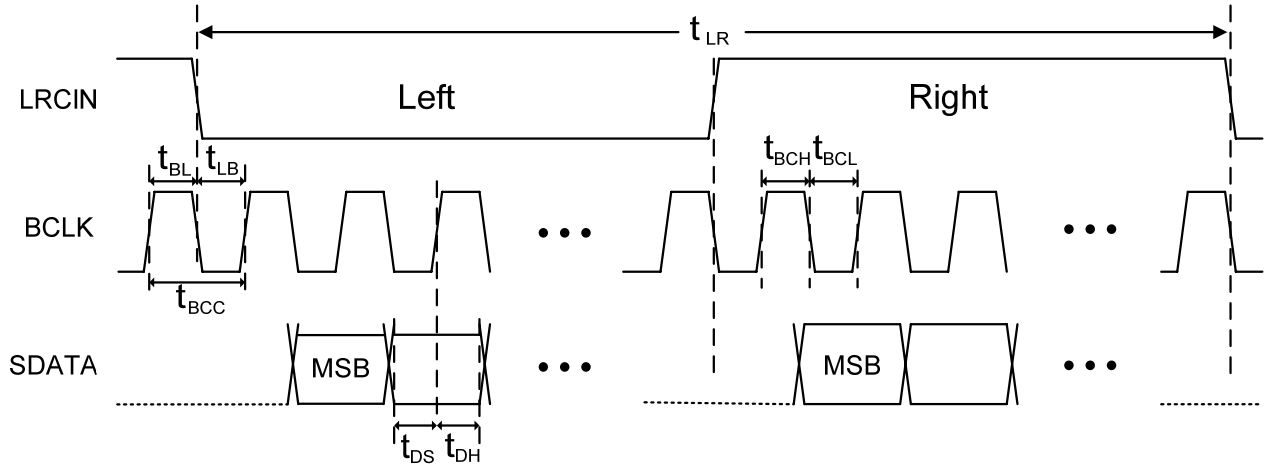
Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period (1/F_S)	10.41		125	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	50			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	50			ns
t_{BCC}	BCLK Period (1/64F_S)	162.76		1953	ns
t_{BCH}	BCLK Pulse Width High	81.38		976.5	ns
t_{BCL}	BCLK Pulse Width Low	81.38		976.5	ns
t_{DS}	SDATA Set-Up Time	50			ns
t_{DH}	SDATA Hold Time	50			ns

● I^{2}C Timing
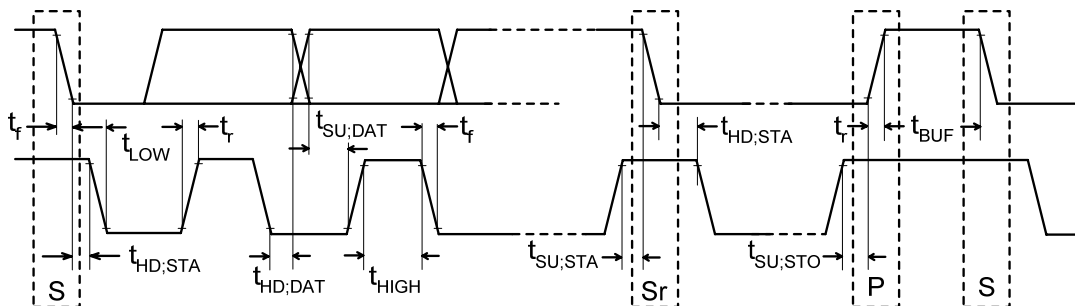
Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition	$t_{HD,STA}$	4.0	---	0.6	---	μs
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	μs
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	μs
Data hold time for I^{2}C bus devices	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Data setup time	$t_{SU;DAT}$	250	---	100	---	ns
Rise time of both SDA and SCL signals	t_r	---	1000	20+0.1Cb	300	ns
Fall time of both SDA and SCL signals	t_f	---	300	20+0.1Cb	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	---	1.3	---	μs
Capacitive load for each bus line	C_b		400		400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	---	$0.1V_{DD}$	---	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	---	$0.2V_{DD}$	---	V

I²C-Bus Transfer Protocol

- Introduction

  AD62557 employs I²C-bus transfer protocol. Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock (SCL) on the bus. AD62557 is also a slave device in all of its communications.

- Protocol

  - START and STOP condition

    START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must be preceding any command for data transfer. A low to high transition on the SDA line while SCL is high defines a STOP condition. A STOP condition terminates communication between AD62557 and the master device on the bus.

  - Data validity

    The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low. AD62557 samples the SDA signal at rising edge of the clock signal SCL.

  - Device addressing

    The master generates 7-bit address to recognize slave device. When AD62557 receives 7-bit address matched with 7'b0111010, AD62557 will acknowledge at 9th bit time (8th bit time is for R/W bit). The bytes following the device identification address are interpreted as internal sub-addresses.

  - Data transferring

    Every byte put on SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with MSB first. As the figure shown below, in both write and read operation, AD62557 supports single-byte and multi-byte. Please refer to the figure shown below for detail data-transferring protocol.
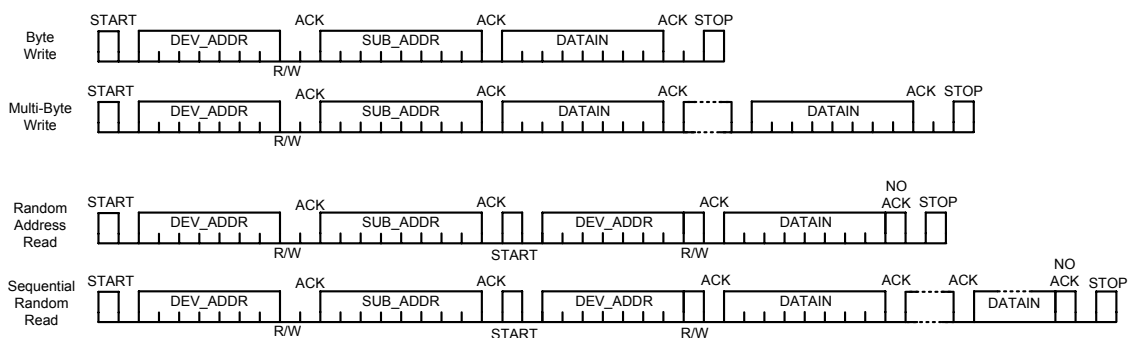
Operation Descriptions

The following figure illustrates two more advanced applications that use AD62557, together with an internal ADC or an external ADC, e.g., AD12250 from ESMT that can convert stereo line-in audio to I^{2}S output to send to AD62557, and/or an external high-end Class-D amplifier such as AD82586x/AD82587x via AD62557's I^{2}S output.

Both applications, a switch used to select audio stream from either USB port or Line-in port. When the audio stream is from Line-in port, the device is operating as "docking station" mode. When the audio stream is from USB port, the device is operating as "USB headphone" mode. When AD82586x/AD82587x is used, since it can deliver 10Wx2 + 20W (subwoofer) power or 20Wx2 power, USB bus power may be insufficient and local power supply is required. Functional description follows.

SEL2, SEL1, SEL0

	0	**1**
SEL0	**AD8287x**	**AD82586x/AD83586**

SEL2	**SEL1**	**Audio Source**
0	**0**	**Internal ADC as line-in**
1	**0**	**Internal ADC as Microphone**
0	**1**	**use AD12250 as line-in**
1	**1**	**use AD3150 as Microphone**

RESET
The AD62557 has embedded power on reset circuit. When AD62557 power on, need wait 0.5ms reset process for the system ready.

Volume Control of Playback
Audio volume control up/down is low active by VOLUPB/VOLDNB pins. Duration of low level must be longer than 3ms. The default volume gain is +6dB referred to the original input signal level.
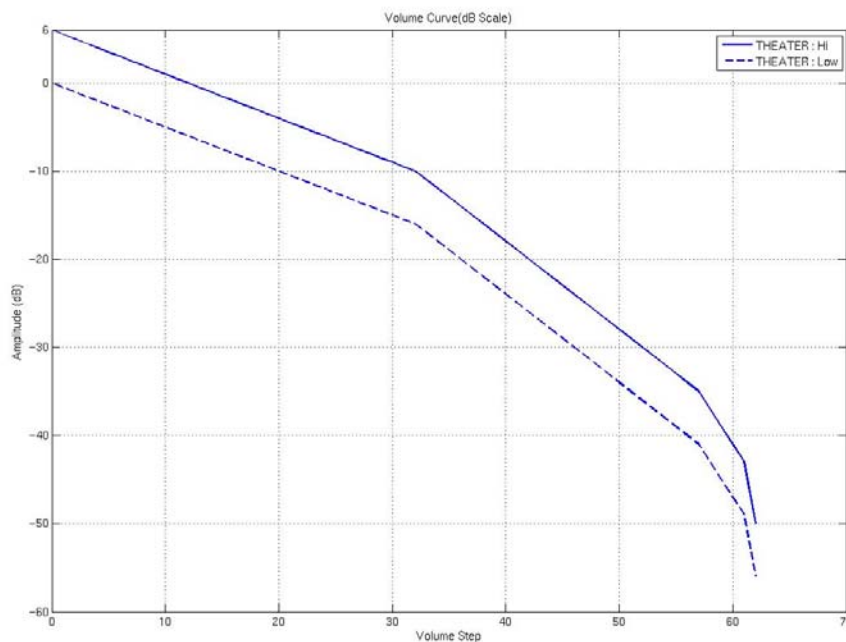
The volume gain range is from +6 dB to -50 dB.

Volume Control of Recording

The volume gain range is from +6 dB to -50 dB the same as the playback.

Mute control

Both MUTEB and MUTEBR are low active. It also supports USB HID device class for host panel control synchronization. Duration of low level must be longer than 3ms.

Stereo dual ADC

AD62557 has a dual channel stereo ADC input as microphone or line-in recording source according to SEL1 and SEL2 pins. After USB plug in, the USB descriptor can be changed accordingly.

LED display

LED0 can be used as USB operation indicator when data transmit. LED1 can be used as recording mute indicator.

Microphone Gain Boost

When use internal ADC as microphone in the AD62557, the internal gain boost has two stages. One is 20dB and the other can select from 0dB to 22.5dB.

Self-protection circuit

AD62557 has built-in thermal, short-circuit and under-voltage detection circuits. If the internal thermal detection junction temperature is higher than 150°C, the output will be turned off. The thermal detection circuit has a temperature hysteretic characteristic such that the AD62557 will return to normal operation when the device is cooled down to about 30°C. Due to the process variation, the triggering temperature values can have around 10% variation.

To protect loudspeaker power stages when the loudspeaker output are shorted each other or shorted to GND, the output loading detection circuits are built-in and proper protection action will take place once the short circuit condition is detected.

For normal operation, the loudspeaker output resistance larger than 3.4Ω is required. Once the short-circuit condition is detected, the output power stages will be shut off. After the short-circuit condition is happened, the AD62557 will be auto release the output power stages at every 42ms if the short-circuit condition is removed.

Anti-pop design

AD62557 is has an anti-pop circuit to suppress the annoying pop sounds during initial power on, power down/up, mute, power off and volume level change.

Under Voltage protection circuit

Once the V_{DD5} is lower than 3.7V, AD62557 will turn off its headphone driver and the digital circuit will cease operation. When V_{DD5} becomes larger than 3.8V, AD62557 will return to normal operation.

Switching between USB mode and docking station mode

When the $\overline{USB}/LineIn$ pin is low, the input audio stream is from USB port as USB headphone mode. When this pin is high, the input audio stream is from AINL/AINR, I^{2}S input port or DMIC_DATAL/DMIC_DATAR as docking station mode.

Audio Recording

AD62557 can record external audio source from AINL/AINR microphone/line in, I^{2}S SDATAI or DMIC_DATAL/DMIC_DATAR digital microphone by SEL1 and SEL2 pins. Supports 44.1kHz and 48kHz sampling frequency for audio recording, the default setting is 48kHz for audio recording in AD62557.

3D Surround sound Mode

When SndEn pin is low, 3D surround sound Mode is enabled. AD62557 provides the virtual surround sound technology with greater separation and depth for stereo signals and synthesizes a 3D stereo sound field.

Power Consideration

AD62557 can be powered by the USB port directly. However, the maximum current supplied by each USB port is limited 500mA. If the total power requirement of the USB audio subsystem is higher than this, local power supply, e.g., a local AC adaptor will have to be used. If the audio subsystem is attached to an USB hub, which is not locally powered, the maximum power from each USB port is only limited to 100mA, and local power must be supplied.

Power Clipping

AD62557 support power clipping function for protect speaker. There are 16 levels can be set through I2C.

I^{2}C master/slave mode

AD62557 can also operate as master or slave in a system when LRCINO is pulled low or high with 1MΩ at power up initially (during 15ms after 90% of V$_{REGO}$). When LRCINO is pulled low, the AD62557 operates as I2C master mode. In I2C master mode, the AD62557 also can control the external class-D amp. AD82586/AD82581 via I2C. When LRCINO is pulled high, the AD62557 operates as I2C slave mode. When operating as a slave mode, AD62557's functions are controlled by micro-controller. Functions in PC are all disable.

I^{2}S master/slave mode

The pins LRCINI, BCLKI and MCLKI of the AD62557 can also operate as I2S master or slave mode in a system when BCLKO is pulled low or high with 1MΩ at power up initially (during 15ms after 90% of V$_{REGO}$). When BCLKO is pulled low, the AD62557 operates as I2S master mode. In I2S master mode, the pins LRCINI, BCLKI and MCLKI are output pins can drive the other devices. When BCLKO is pulled high, the AD62557 operates as I2S slave mode. When operating as a slave mode, the pins LRCINI, BCLKI and MCLKI are input pins need the other device provide clocks.

Note: In slave mode, it must be followed the frequency ratio of MCLKI = 256×LRCINI for correct operation.

Note 2: In slave mode, AD62557 only support I2S source playback and can't support USB source playback/recording.

Mixing mode

The AD62557 can mix USB audio signal and anlog/I2S audio signal to the output when MCLKO is pulled high with 1MΩ at power up initially (during 15ms after 90% of V_{REGO}). When MCLKO is pulled high, the volume of mixing signal can control through address 8 and 9 via I2C. Also can mute and un-mute mixing signal through the bit 5 and 6 of the address 1.

Stereo/Mono mode

The output of the AD62557 can configure the stereo or mono mode when SDATAO is pulled high or low with 1MΩ at power up initially (during 15ms after 90% of V_{REGO}). When SDATAO is pulled low, the output of the AD62557 is the stereo mode. When SDATAO is pulled high, the output of the AD62557 is the mono mode and the audio signal is mix from the left and right channel.

Register Table

The audio signal processing data flow is shown as the following figure. Users can control these functions by programming appropriate setting to register table, which is summarized in this section. More detail information will be described in next section.

Recording signal processing flow
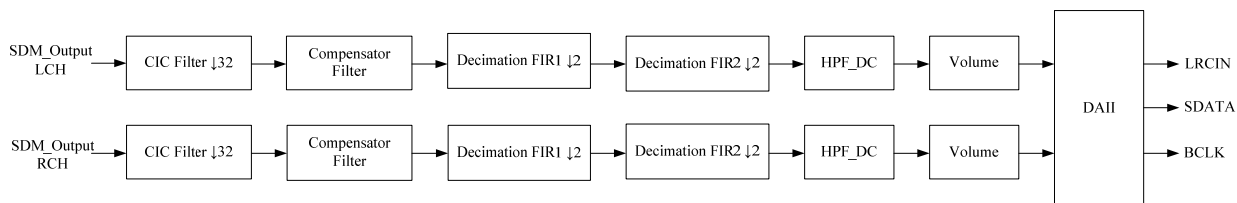
Playback signal processing flow
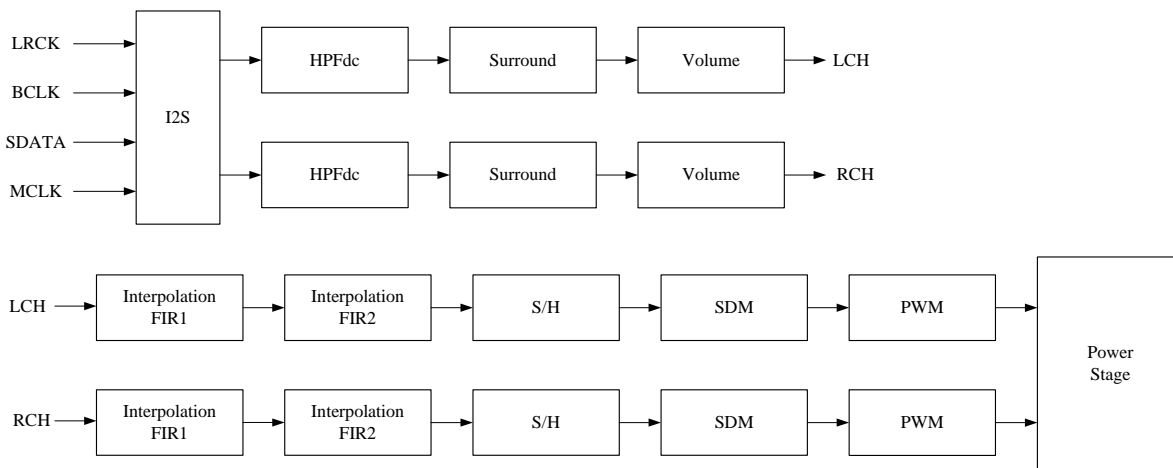
Add.	Name	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0X00	PB_CTL	Reserved	MIX_CH1_MUTE	MIX_CH2_MUTE	PB_ZDEN	PB_SRSEN	PB_HPF	PB_CH1_MUTE	PB_CH2_MUTE
0X01	PB_LVOL	Reserved		PB_CH1Vol [5]	PB_CH1Vol [4]	PB_CH1Vol [3]	PB_CH1Vol [2]	PB_CH1Vol [1]	PB_CH1Vol [0]
0X02	PB_RVOL	Reserved		PB_CH2Vol [5]	PB_CH2Vol [4]	PB_CH2Vol [3]	PB_CH2Vol [2]	PB_CH2Vol [1]	PB_CH2Vol [0]
0X03	RE_CTL	ADC_V3	ADC_V2	ADC_V1	ADC_V0	ADC_BOOST	RE_HPF	RE_CH1_Mute	RE_CH2_Mute
0X04	RE_LVOL	C1V[7]	C1V[6]	RE_CH1Vol [5]	RE_CH1Vol [4]	RE_CH1Vol [3]	RE_CH1Vol [2]	RE_CH1Vol [1]	RE_CH1Vol [0]
0X05	RE_RVOL	C2V[7]	C2V[6]	RE_CH2Vol [5]	RE_CH2Vol [4]	RE_CH2Vol [3]	RE_CH2Vol [2]	RE_CH2Vol [1]	RE_CH2Vol [0]
0X06	ZD&MICB	ZD_LEVEL[1]	ZD_LEVEL[0]	Reserved			MICBPDB	MBVSEL[1]	MBVSEL[0]
0X07	PL	Reserved			PL_EN	PL_Level [3]	PL_Level [2]	PL_Level [1]	PL_Level [0]

Detail Description for Register

In this section, please note that the highlighted columns are the default value of these tables. If no highlighted, it is because the default setting of this bit is determined by external pin.

Address 0: Playback State control

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	Reserved			
B[6]	MIX_CH1_MUTE	Mixing Channel1 Mute	1	Mute
			0	Un-mute
B[5]	MIX_CH2_MUTE	Mixing Channel2 Mute	1	Mute
			0	Un-mute
B[4]	PB_ZDEN	Playback Zero-Detection Enable	1	Enable
			0	Disable
B[3]	PB_SRSEN	Playback Surround Enable	1	Enable
			0	Disable
B[2]	PB_HPF	Playback High Pass Filter	1	Enable
			0	Disable
B[1]	PB_CH1_MUTE	Playback Channel1 Mute	1	Mute
			0	Un-mute
B[0]	PB_CH2_MUTE	Playback Channel2 Mute	1	Mute
			0	Un-mute

Address 1: Playback Left Channel Volume Control

BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	PB_CH1Vol[5:0]	Playback Left Channel Volume Control	000000	+6dB
			000001	+5.5dB
			…	…
			001100	+0dB
			001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Address 2: Playback Right Channel Volume Control

| BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	PB_CH2Vol[5:0]	Playback Right Channel Volume Control	000000	+6dB
			000001	+5.5dB
			…	…
			001100	+0dB
			001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Address 3: Recording State control

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	ADC_V3		0000	0 dB
			0001	5 dB
			0010	8 dB
			0011	10 dB
B[6]	ADC_V2		0100	12 dB
			0101	14 dB
			0110	15 dB
		DESCRIPTION 2nd OP Gain control	0111	16.6 dB
			1000	17.6 dB
B[5]	ADC_V1		1001	18.6 dB
			1010	19.2 dB
			1011	19.8 dB
B[4]	ADC_V0		1100	20.4 dB
			1101	21 dB
			1110	21.7 dB
			1111	22.5 dB
B[3]	ADC_BOOST	1st OP Gain boost enable	1	Enable
			0	Disable
B[2]	RE_HPF	Recording High Pass Filter	1	Enable
			0	Disable
B[1]	RE_CH1_Mute	Recording Channel1 Mute	1	Mute
			0	Un-mute
B[0]	RE_CH2_Mute	Recording Channel2 Mute	1	Mute
			0	Un-mute

Address 4: Recording Left Channel Volume Control

| BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	PB_CH1Vol[5:0]	Recording Left Channel Volume Control	000000	+6dB
			000001	+5.5dB
			…	…
			001100	+0dB
			001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Address 5: Recording Right Channel Volume Control

BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	PB_CH2Vol[5:0]	Recording Right Channel Volume Control	000000	+6dB
			000001	+5.5dB
			…	…
			001100	+0dB
			001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Address 6: Zero-Detection and Mic. Bias Setting

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	ZD_LEVEL	Zero Detection Level	11	-60dB
			10	-70dB
			01	-80dB
			00	zero
B[5]	Reserved			
B[4]	Reserved			
B[3]	Reserved			
B[2]	MICBPDB	Microphone Bias Voltage PowerDown	0	Power down
			1	Power up
B[1:0]	MBVSEL	Microphone Bias Voltage Control	11	0.9*AVDD
			10	0.8*AVDD
			01	0.6*AVDD
			00	0.5*AVDD

Address 7: Power Clipping Setting

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	Reserved			
B[6]	Reserved			
B[5]	Reserved			
B[4]	PC_EN	Power Clipping Enable	1	Enable
			0	Disable
B[3]			0000	0dB
			0001	-2dB
B[2]			0010	-4 dB
			0011	-6dB
	PC_Level	Power Clipping Level	0100	-8 dB
B[1]			…	
			1110	-28 dB
B[0]			1111	-30 dB

Address 8: Mixing Left Channel Volume Control

BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	Mix_CH1Vol[5:0]	Mixing	000000	+6dB
		Left	000001	+5.5dB
		Channel	…	…
		Volume	001100	+0dB
		Control	001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Address 9: Mixing Right Channel Volume Control

BIT	NAME	DESCRIPTION	Value	FUNCTION
B[5:0]	Mix_CH2Vol[5:0]	Mixing	000000	+6dB
		Right	000001	+5.5dB
		Channel	…	…
		Volume	001100	+0dB
		Control	001101	-0.5dB
			…	…
			100000	-10dB
			100001	-11dB
			…	…
			111111	-∞dB

Application Circuit Example with External ADC as Line-in
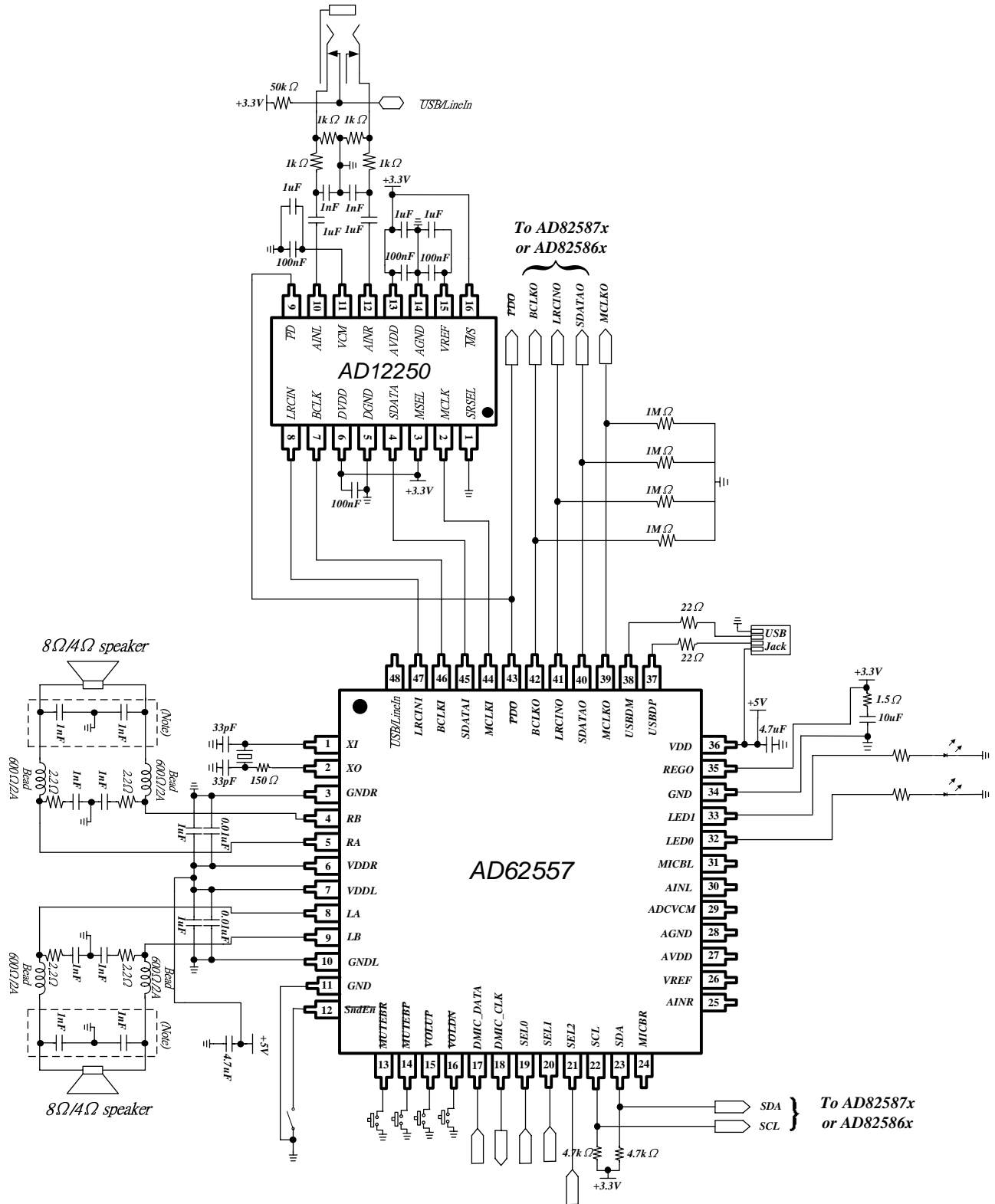
Note. EMI option components.

Application Circuit Example with Internal ADC as Line-in
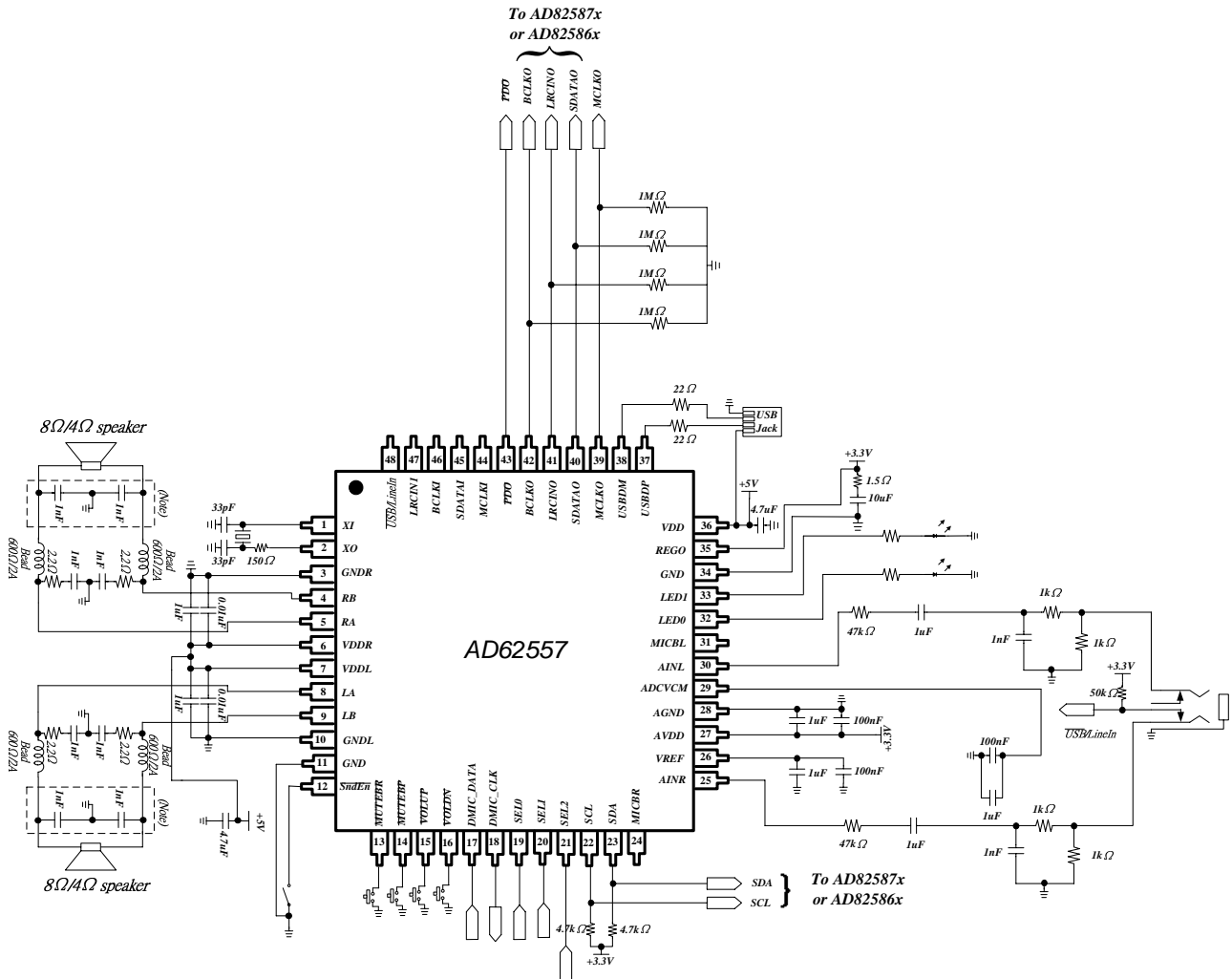
Note. EMI option components.

Application Circuit Example with Internal ADC as Microphone
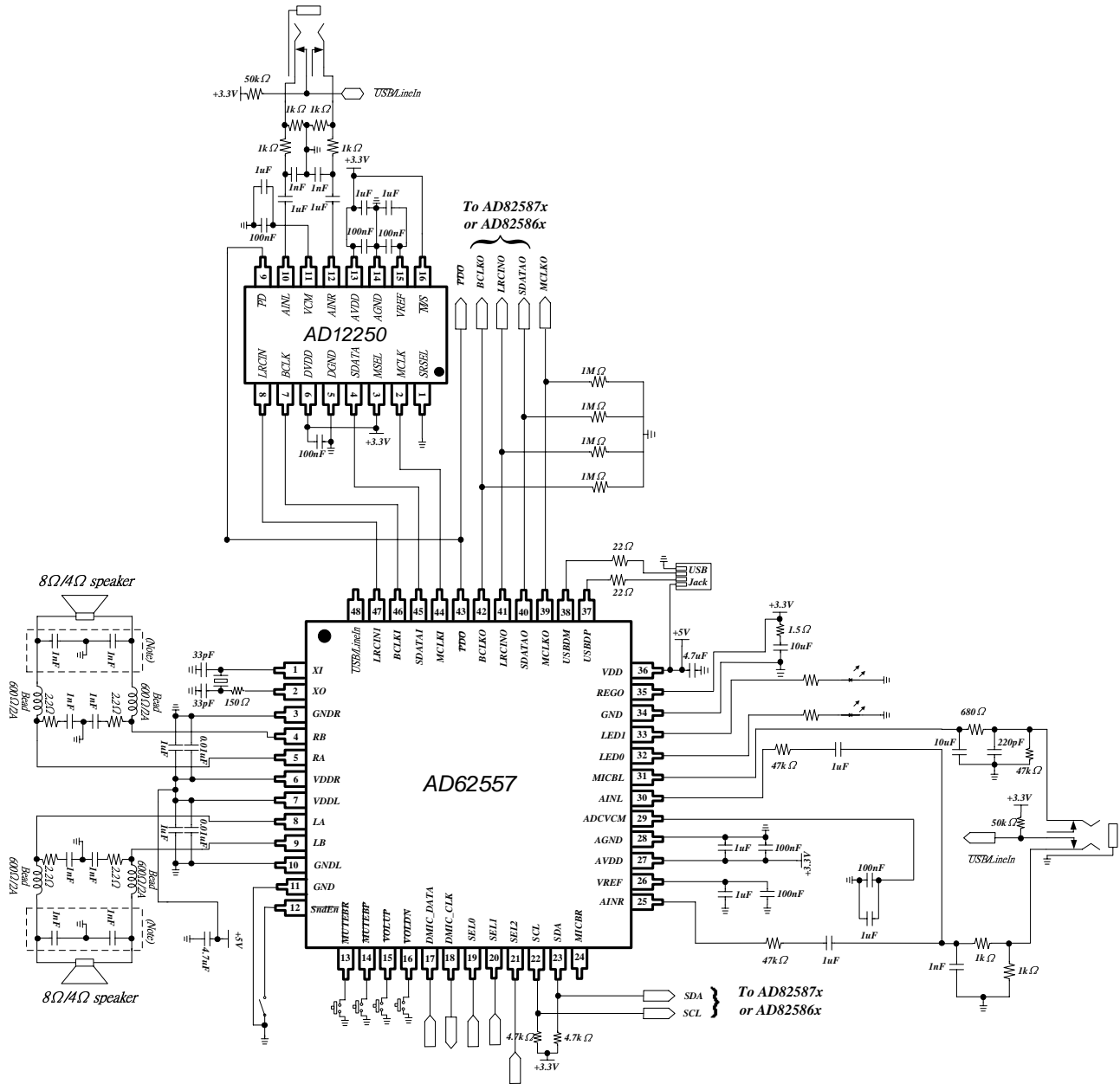
Note. EMI option components.

Application Circuit Examples for Headphone, Digital Microphone input
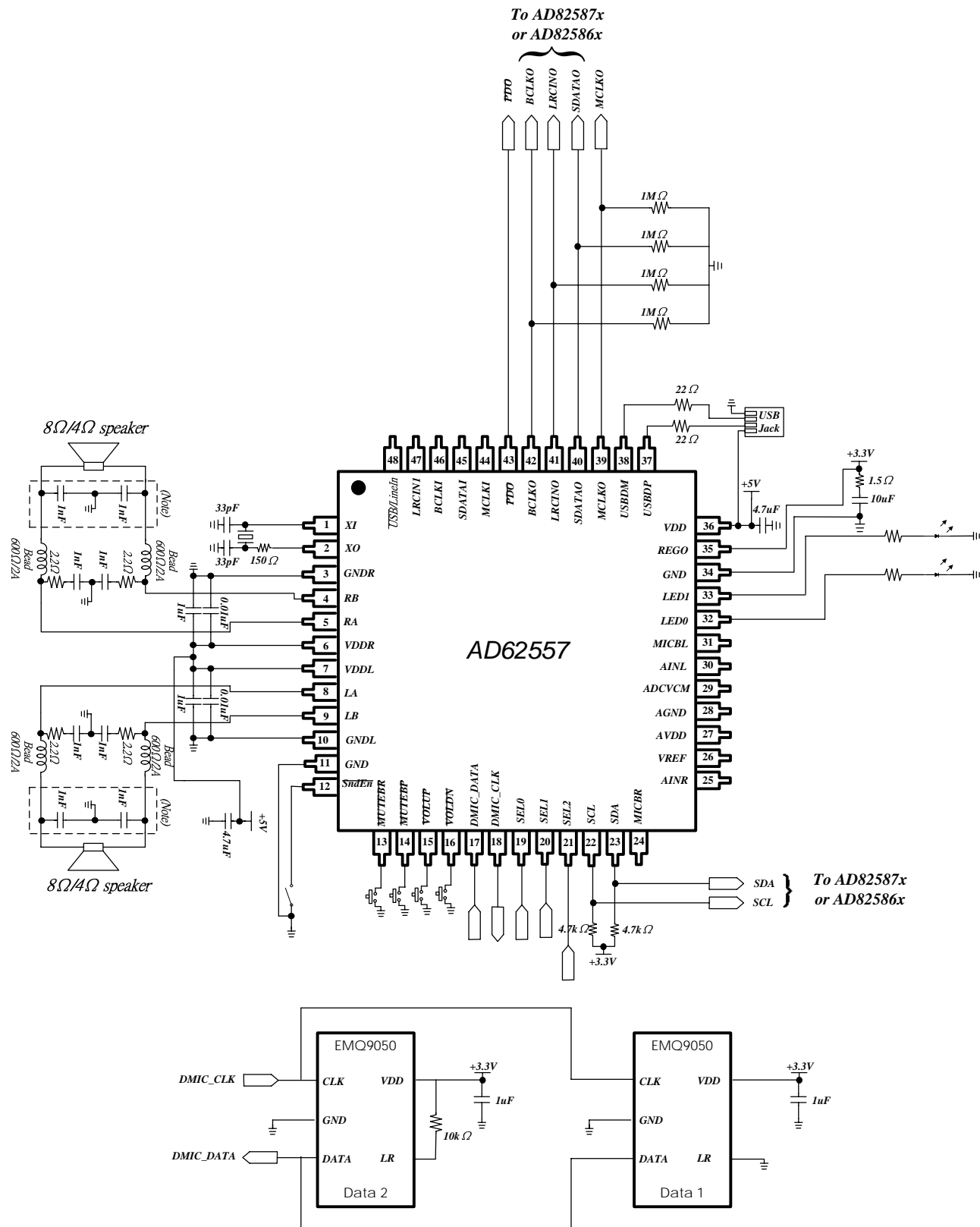
Note. EMI option components.

Application Circuit Examples for Mono
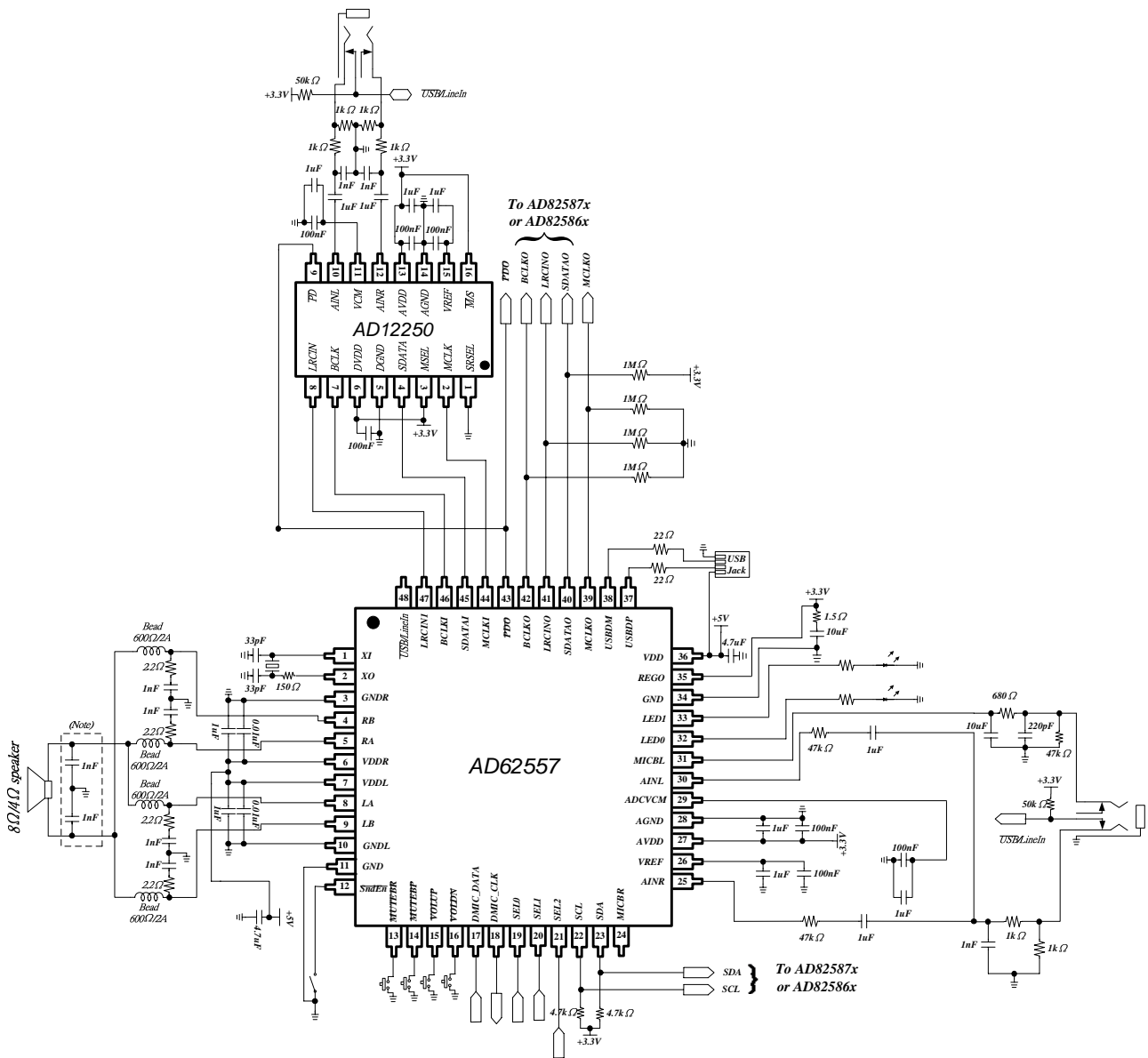
Note. EMI option components.

Package Dimensions

● **E-LQFP 48L (7x7mm)**
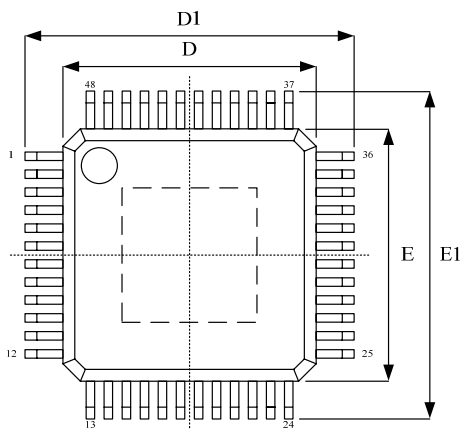
TOP VIEW
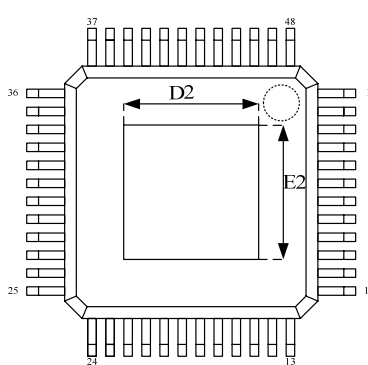
BOTTOM VIEW
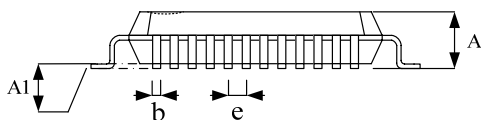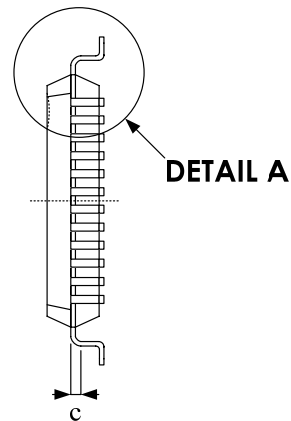
DETAIL A

SIDE VIEW
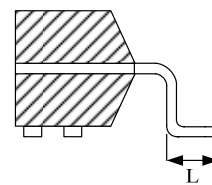
DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.17	0.27
c	0.09	0.20
D	6.90	7.10
D1	8.90	9.10
E	6.90	7.10
E1	8.90	9.10
e	0.50 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	4.31	5.21
E2	4.31	5.21

Revision History

Revision	Date	Description
0.1	2013.10.24	Original version.
0.2	2014.08.01	1) Add feature note about I2S Master/Slave mode. 2) Modify Pin Description Table(SDA, SCL)
0.3	2016.12.01	1) Add Application Circuit Examples For Mono

Important Notice