Baseband Processor for TD-HSDPA TD-SCDMA and GSM/GPRS/EGPRS Handsets and Data Modems

Preliminary Technical Data **AD6905**

INTRODUCTION

The AD6905 is an advanced, low power baseband processor that meets the demanding requirements of TD-HSDPA and GSM/GPRS/EGPRS terminals with advanced system power management and multimedia capabilities. The chip integrates a powerful Blackfin® DSP processor along with an ARM926EJ-S® microcontroller and an extensive set of peripheral interfaces that support features such as a digital camera sensor, USB OTG, Multimedia Card, SD (Secure Digital) Card, IrDA, thumbwheel, color displays, and other peripheral devices such as Bluetooth, WiLAN, and A-GPS modules.

With integrated 3G/TDD hardware acceleration to support High Speed Downlink Packet Access (TD-HSDPA) at data rates up to 2.8Mbps, the AD6905 enables new levels of wireless connectivity.

FEATURES

MCU Control Processor Subsystem

32-bit ARM926EJ-S® MCU Control Processor
260 MHz operation at 1.5V
16KB instruction cache
16KB data cache
4kB Instruction Tightly Coupled Memory (TCM)
2-Mbit On-chip System SRAM
Ciphering coprocessor supporting GEA1 and GEA2 and GEA3 encryption algorithms
Dedicated multi-channel DMA controller

DSP Subsystem

Blackfin 16-bit fixed-point DSP Processor
260 MHz operation at 1.5V
Memory:
- L1 program space: 64 kB SRAM and 16 kB configurable as instruction cache or SRAM
- L1 data space: Two banks of 16K bytes, each with 8K bytes of dedicated SRAM and an additional 8K bytes that can be configured as either cache or SRAM
- L2 space: 64KB SRAM

Ciphering coprocessor supporting A5/1, A5/2, A5/3, GEA1, GEA2, GEA3, f8 and f9 ciphering algorithms
Dedicated multi-channel DMA controller
Hardware acceleration for TD-SCDMA 384kbps and TD-HSDPA up to 2.8Mbps

Peripherals Subsystem

Support for Burst-mode, Page-mode, and NAND Flash memory
Support for SRAM, SDRAM, and PSRAM (CellularRAM)
Full-Speed USB 2.0 Dual-Role Interface with On-The-Go (OTG) Host Mode or traditional Peripheral-only mode
Serial Display Interface
8x8 Keypad Interface
Thumbwheel Interface
4 Independent Programmable Backlights plus a Service Light
1.8V and 3.0V, 64 kbps USIM Interface
Universal System Connector Interface
Multimedia Card (MMC) Interface
Secure Digital (SD) Card Interface and SDIO
IrDA transceiver interfaces, including Fast IrDA (4 Mbps baud)
2 Configurable Generic Serial Ports (GSPs)
7 Configurable Enhanced Generic Serial Ports (eGSPs)

Applications Subsystem for Enhanced Multimedia

Parallel Peripheral Interface (PPI) for 10-bit dedicated camera sensor or video input interface (including ITU-656 and ITU-601 digital video)
Separate parallel bus interface for LCD displays or other peripherals
Dedicated multi-channel 2-D DMA controller

Other Features

Real-Time Clock (RTC) with Alarm
Four General-Purpose Timers
Dedicated Interfaces to Audio/Baseband Codec Chip
Compatible with Othello® radio subsystem
Highly configurable interrupt controller architecture
Programmable bus arbitration to optimize system performance
Supports 13MHz and 26 MHz Input Clocks
Programmable Power Management and Clock Management
- Slow Clocking Scheme for Low Idle Mode Current
- Power Down modes
- Dynamic Core Voltage Scaling from 1.1 - 1.5V

Independent I/O Voltage Domains
Embedded Trace Macrocell for MCU Debug
JTAG Interface for Test and In-Circuit Emulation of both the MCU and DSP
Advanced features for security
Boot directly from NAND

APPLICATIONS

Dual-Mode TD-SCDMA HSDPA (voice + 2.8Mbps data) and GSM/GPRS/EGPRS handsets (Class 12 Multi-slot EDGE)
Single or Dual-Mode TD-HSDPA wireless data modems

GENERAL DESCRIPTION

The AD6905 is an advanced, low-power baseband processing solution from Analog Devices, and is part of the AD20msp500 SoftFone® chipset family. The AD6905 is intended for use in a wide variety of feature-rich phones with TD-HSDPA / GSM / GPRS / EGPRS system connectivity. It is designed to interface easily to an application/OS processor, or to stand alone as a fully integrated and easy-to-use solution for mobile handset and wireless modem applications.

The processing speeds of the ARM9 and Blackfin DSP cores enable advanced applications such as Streaming Audio and Video services, various decoders supported by 3GPP such as H.264, and H.263, and Multimedia services (MMS) and Enhanced Message Service (EMS). Other supported audio applications include various vocoders including FR, EFR, HR, and AMR; software-generated polyphonic ringtones; and advanced voice functions such as echo-cancellation, hands-free (speakerphone) operation, intelligibility enhancement, and noise reduction. Both core processors also support software-based multimedia functions such as MP3 audio encoding and playback, and MPEG4 video encoding and decoding. The AD6905 includes interfaces for burst- and page-mode NOR flash memories, SDRAM, PSRAM (cellular RAM), and NAND flash memory. The AD6905 is able to boot directly from NAND, offering the possibility to eliminate NOR flash from the system altogether.

The Blackfin DSP is a high-performance, low-power, 16-bit Digital Signal Processor (DSP) optimized for communications and multimedia applications. The DSP is a resource for implementing various signal processing functions in the communications task such as speech processing, channel equalization, and channel codec functions. Because of its performance and programmability, this DSP architecture offers increased flexibility in supporting audio and video processing functions in software such as those used in MMS.

The AD6905 supports adaptive multi-rate speech codecs as well as a full range of TD-SCDMA data services including circuit switched and packet switched, up to 384kbps data class. The processor also supports High-Speed Downlink Packet Access (HSDPA) for data transfers as fast as 2.8Mbps. In addition, it supports A5/1, A5/2, and A5/3—GEA1, GEA2, and GEA3—encryption algorithms as well as operation in non-encrypted mode. The highly programmable architecture and sophisticated internal communication channels of the AD6905 offer maximum flexibility to system designers. It can adapt to tighter requirements led by changes in standards and multi-standard handset implementation.

The AD6905 interfaces to all the peripheral subsystems of a terminal, including the keypad, memories, display driver, USIM, data interface and radio. It also has several general-purpose interfaces that can be used to support additional handset options such as multiple displays, Bluetooth modules, or cameras. The AD6905 supports 16 external interrupts that are highly programmable, enhancing the flexibility to interface with external devices. The AD6905 interfaces to the AD6857 Advanced Audio/Baseband Codec and Power Management chip through dedicated serial ports.

The AD6905 has a full-speed USB 2.0 On-The-Go (OTG) interface. USB OTG provides low-cost connectivity for consumer mobile devices such as cell phones, digital still cameras, and MP3 players, allowing these devices to transfer data via a point-to-point USB connection without a PC host.

The AD6905 also integrates a multimedia control module, providing interface to external multimedia cards. These support modules, along with the powerful processing capabilities of the AD6905, allow extensive MMS (Multimedia Services) applications to transfer data or programs from storage devices, execute them on the baseband processor, and transmit them over the wireless network. Such applications include MP3 playback, processing of video clips, compression and decompression of JPEG or MPEG4 images.

In addition to the MMS capability, the AD6905 allows mobile phone users to connect to the Internet, download pictures and ring tones to their phone and add EMS (Enhanced Message Service) capability to their phone. EMS, an extension of the SMS text messaging service, allows the user to send a combination of simple melodies, pictures, sounds, animations, modified text and standard text.

TEST AND DEBUG

The MCU JTAG interface, in conjunction with a 3rd party In-Circuit Emulator (ICE), can be used for test and debug during system integration. Through the Universal System Connector (USC), and selected General Purpose I/O (GPIO) pins. DSP emulation can be performed using Analog Devices' in-circuit emulation tools, which are part of the CROSSCORE Development and Debug Tools Suite. The CROSSCORE components include the VisualDSP++™ software development environment, EZ-KIT Lite™ evaluation systems, and emulators for rapid on-chip debugging. In addition to the DSP development tools suite, ADI offers a superset of the development tools for the baseband system, called VisualFone™. The VisualFone Evaluation and Development Environment provides the capabilities needed to evaluate, develop, test, and debug mobile terminals based on the AD6905 baseband processor.

ORDERING GUIDE

Model	Temp. Range	Package
AD6905XBCZ	-20°C to +85°C	291 Ball mBGA (Pb Free)
AD6905XBCZ-REEL	-20°C to +85°C	291 Ball mBGA (Pb Free)

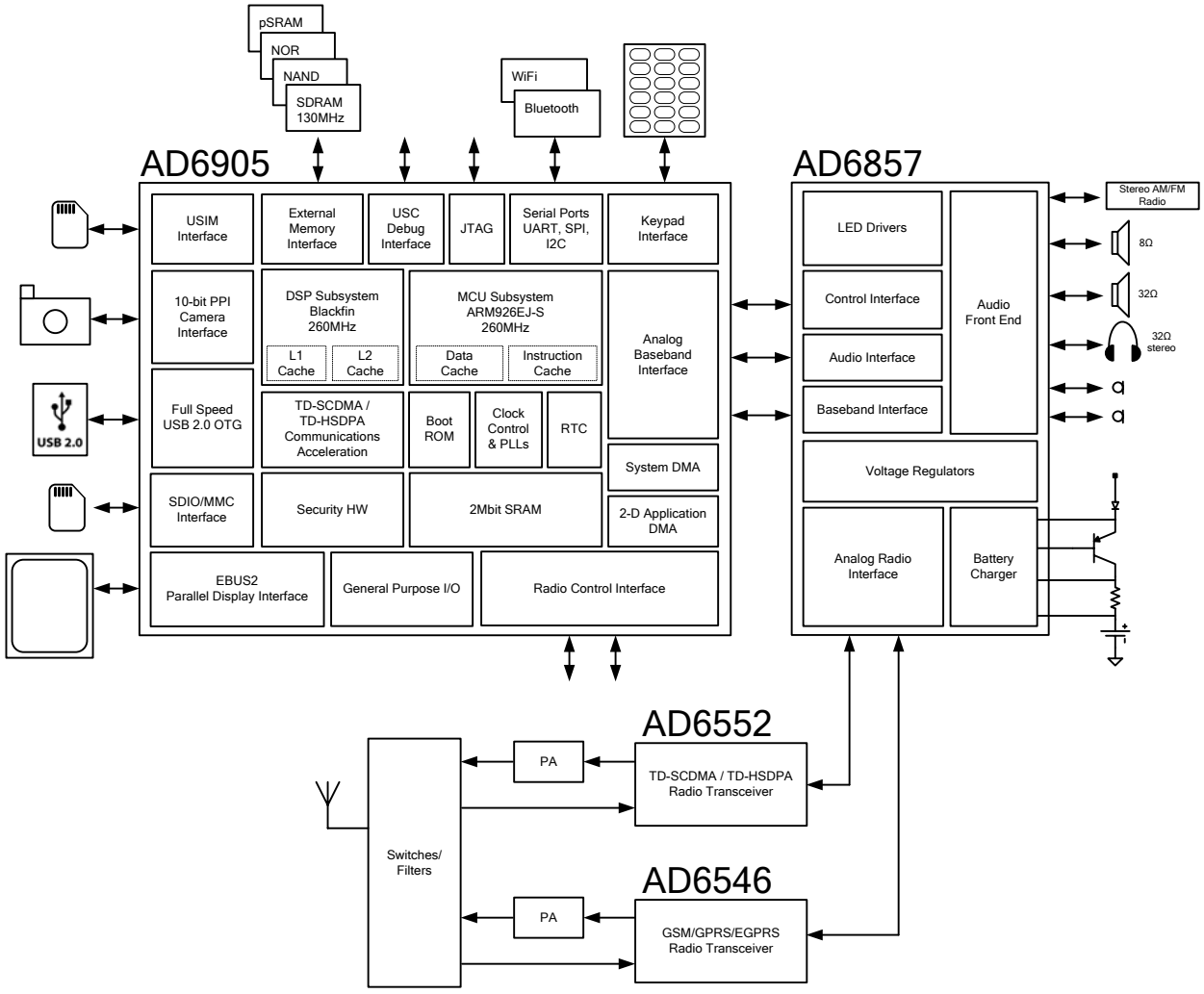


Figure 1: Example GSM/GPRS/EGPRS/TD-HSDPA Dual-Mode System

Table of Contents

PIN MUXING TABLE

Functional Group	Pin Name (Reset)	{I/O}	Supply	Default/Typical Usage	Alternate Functions Alt 1	Alt 2	Alt 3
CONTROL	CLKIN	I	V_{PLL}	13 MHz or 26 MHz XTAL System Clock Input			
	CLKON (H)	O	V_{EXT}	Oscillator Power Control Signal (on/off)			
	nRESET	I	V_{MEM}	System Reset Input			
	OSCIN	I	V_{RTC}	32.768 kHz Crystal Input - Inverted (GND if no Crystal)			
	OSCOUT (n/a)	O	V_{RTC}	32.768 kHz Oscillator Output and Feedback to Crystal			
	PWRON(L)	O	V_{RTC}	Power ON/OFF Control			
	TESTMODE	I	V_{MEM}	Must be tied to GND			
EBUS External Memory Interface	GPIO_24 (L)	I/O	V_{MEM}	Address - 32M words	ADD[25]	CLKMUXOUT2	
	GPIO_32 (L)	I/O	V_{MEM}	Address - 16M words	ADD[24]		
	ADD[23] (L)	O	V_{MEM}	Address - 8M words	GPIO_39		
	ADD[22:1] (L)	O	V_{MEM}	Address Bus			
	ADD[0] (L)	O	V_{MEM}	Display_A0	GPIO_40		
	DATA[15:8] (L)	I/O	V_{MEM}	Data Bus			
	DATA[7:0] (L)	I/O	V_{MEM}	Data Bus			
	nRD (H)	O	V_{MEM}	Read Enable			
	nHWR / nUBS / CLE / SDQM[1] (H)	O	V_{MEM}	High Write Strobe / Byte Strobe / Command Latch Enable / Data Mask	GPIO_41		
	nLWR / nLBS / ALE / SDQM[0] (H)	O	VMEM	Low Write Strobe / Byte Strobe / Address Latch Enable / Data Mask	GPIO_42		
	nWE (H)	O	V_{MEM}	Write Enable			
	nWAIT	I	V_{MEM}	External device wait request	GPIO_43		
	nADV (H)	O	V_{MEM}	Valid Address (burst)	GPIO_44		
	BURSTCLK (H)	O	V_{MEM}	Burst Clock	GPIO_45		
	nA0CS (H)	O	V_{MEM}	General Purpose Chip Select			
	nA1CS (H)	O	V_{MEM}	General Purpose Chip Select	GPIO_46		
	nA2CS (H)	O	V_{MEM}	General Purpose Chip Select	GPIO_47		
	nA3CS (H)	O	V_{MEM}	General Purpose Chip Select	GPIO_48		
	GPIO_49 (I+)	I/O	V_{MEM}	General Purpose Chip Select	nB0CS		
	GPIO_50 (I+)	I/O	V_{MEM}	General Purpose Chip Select	nB1CS		
	GPIO_51 (I+)	I/O	V_{MEM}		SDQM[1]		
	GPIO_52 (I+)	I/O	V_{MEM}	Flash 2 Chip Select	nA5CS		
	GPIO_53 (I+)	I/O	V_{MEM}	Flash 3 Chip Select	nA4CS		CLKMUXOUT2

Functional Group	Pin Name (Reset)	{I/O}	Supply	Default/Typical Usage	Alternate Functions Alt 1	Alt 2	Alt 3
	GPIO_54 (I+)	I/O	V_{MEM}		SDQM[0]		CLKMUXOUT2
	GPIO_55 (L)	I/O	V_{EXT}		Alert Light	ETM_TRIGGER0	TimerInD
	GPIO_56 (L)	I/O	V_{EXT}		TimerInABC	PPLLCLKIN	CLKMUXOUT1
SDRAM	nSDRAS (H)	O	V_{MEM}	SDRAM Row Address Strobe	GPIO_101		
	nSDCAS (H)	O	V_{MEM}	SDRAM Column Address Strobe	GPIO_102		
	nSDWE (H)	O	V_{MEM}	SDRAM Write Enable	GPIO_103		
	nSDCS (H)	O	V_{MEM}	SDRAM Chip Select	GPIO_104		
	SDA10 (L)	O	V_{MEM}	SDRAM A[10] Address Pin	GPIO_105		
	SCKE (H)	O	V_{MEM}	SDRAM Clock Enable	GPIO_106		
	SCLKOUT (↕)	O	V_{MEM}	SDRAM Clock Output	GPIO_107		
NAND Flash	nNDCS (H)	O	V_{MEM}	NAND Flash Chip Select	GPIO_108		
	nNDBUSY	I	V_{MEM}	NAND Flash Busy Request	GPIO_109		
	nNDWP (L)	O	V_{MEM}	NAND Flash Write Protect	GPIO_110		
SIM	SIMDATAIO (L)	I/O	V_{SIM}	SIM Data I/O			
	SIMCLK (L)	O	V_{SIM}	SIM Clock			
	GPIO_100 (L)	I/O	V_{SIM}	SIM Reset			
Radio Control	GPIO_57 (L)	I/O	V_{INT1}	Rx_On (to ABB)		GPIO_111	
	GPIO_58 (L)	I/O	V_{INT1}	Tx_On (to ABB)		GPIO_112	
	GPIO_59 (L)	I/O	V_{EXT}		General Timer Out	GPIO_121	
	GPIO_60 (L)	I/O	V_{EXT}			GPIO_122	
	GPIO_61 (L)	I/O	V_{EXT}		CLKMUXOUT1	RNGOUT[0]	
	GPIO_62 (L)	I/O	V_{INT1}	ASM (to ABB)		GPIO_125	
	GPIO_63 (L)	I/O	V_{INT1}		CLKMUXOUT3	DBGACK	
	GPIO_64 (L)	I/O	V_{EXT}			GPIO_126	
	GPIO_65 (L)	I/O	V_{EXT}	TR_SW2		GPIO_127	
	GPIO_66 (L)	I/O	V_{EXT}	TR_SW1	not (GPIO_65)	GPIO_178	
	GPIO_67 (L)	I/O	V_{EXT}	TR_SW3		GPIO_179	
	GPIO_68 (L)	I/O	V_{EXT}	TR_SW4	not (GPIO_67)	GPIO_180	
	GPIO_69 (L)	I/O	V_{EXT}	GSM_ON	eGSPe[0]	FIO[2]	
	GPIO_70 (L)	I/O	V_{EXT}	DCS_ON	eGSPe[1]		
	GPIO_71 (L)	I/O	V_{EXT}		eGSPe[2]		
	GPIO_72 (L)	I/O	V_{EXT}	SYNTHEN	eGSPe[3]		
	GPIO_73 (L)	I/O	V_{EXT}	SYNTHDATA	eGSPe[4]	FIO[3]	
	GPIO_74 (L)	I/O	V_{EXT}	SYNTHCLK	eGSPe[5]	FIO[4]	
Analog Baseband Interface	CLKOUT (L)	O	V_{INT1}	Clock Output to ABB			
	CLKOUT_GATE (I)	I	V_{INT1}	Hardware CLKOUT On/Off Switching	GPIO_75		
	GPIO_76 (L)	I/O	V_{INT1}	ABB_RESET			
	GPIO_78 (I)	I/O	V_{EXT}	ABB_IRQ			

Functional Group	Pin Name (Reset)	{I/O}	Supply	Default/Typical Usage	Alternate Functions Alt 1	Alt 2	Alt 3
	CSDI (I)	I	V_{INT1}	CSPORT Data Input			
	CSFS (L)	O	V_{INT1}	CSPORT Framing Signal			
	CSDO (L)	O	V_{INT1}	CSPORT Data Output			
	BSDO (L)	O	V_{INT1}	BSPORT Data Output			
	BSOFS (I)	I	V_{INT1}	BSPORT Output Framing Signal	GPIO_119		
	BSDI (I)	I	V_{INT1}	BSPORT Data Input	GPIO_120		
	BSIFS (I)	I	V_{INT1}	BSPORT Input Framing Signal			
	ASDO (L)	O	V_{INT1}	ASPORT Data Output			
	ASDI (I)	I	V_{INT1}	ASPORT Data Input			
	ASFS (I)	I	V_{INT1}	ASPORT Framing Signal (Optional)			
	WDDI (I)	I	V_{INT2}	WSPORT Downlink (Receive) I Samples	GSPy[0]	GPIO_114	
	WDDQ (I)	I	V_{INT2}	WSPORT Downlink (Receive) Q Samples	GSPy[1]	GPIO_115	
	WUDI (H)	O	V_{INT2}	WSPORT Uplink (Transmit) I Samples	GSPy[2]	GPIO_116	
	WUDQ (H)	O	V_{INT2}	WSPORT Uplink (Transmit) Q Samples	GSPy[3]	GPIO_117	
	UCLK (I)	I	V_{INT2}	WSPORT 30.72 MHz Clock	GSPy[4]	GPIO_118	GSPz[2]
	GPIO_123 (L)	I/O	V_{INT2}	ARSM2 (to ABB)	GSPz[1]		
	GPIO_124 (L)	I/O	V_{INT2}	ATSM2 (to ABB)	GSPz[0]		
Universal System Connector	USC[0] (I)	I/O	V_{EXT}				
	USC[1] (I)	I/O	V_{EXT}				
	USC[2] (I)	I/O	V_{EXT}				
	USC[3] (I)	I/O	V_{EXT}				
	USC[4] (I)	I/O	V_{EXT}				
	USC[5] (I)	I/O	V_{EXT}				
	USC[6] (I)	I/O	V_{EXT}				
USB	USB_DP	I/O	V_{USB}	USB D+			
	USB_DM	I/O	V_{USB}	USB D–			
	USB_ID	I	V_{USB}	USB ID			
MMI/ Peripherals	MC_CLK (L)	I/O	V_{MMC}	MC_CLK	GPIO_79	eGSPg[0]	
	MC_CMD (I)	I/O	V_{MMC}	MC_CMD	GPIO_80	eGSPg[1]	
	MC_DAT[3] (I)	I/O	V_{MMC}	MC_DAT[3]	GPIO_81	eGSPg[2]	
	MC_DAT[2] (I)	I/O	V_{MMC}	MC_DAT[2]	GPIO_82	eGSPg[3]	
	MC_DAT[1] (I)	I/O	V_{MMC}	MC_DAT[1]	GPIO_83	eGSPg[4]	
	MC_DAT[0] (I)	I/O	V_{MMC}	MC_DAT[0]	GPIO_84	eGSPg[5]	
	GPIO_22 (I)	I/O	V_{EXT}	MC_WR_PROTECT			
	GPIO_0 (I)	I/O	V_{EXT}	IrDA_Tx	eGSPb[0]		MONITOR[0]
	GPIO_1 (I)	I/O	V_{EXT}	IrDA_Rx	eGSPb[1]		MONITOR[1]
	GPIO_2 (H)	I/O	V_{EXT}	nIrDA_EN	eGSPb[2]		MONITOR[2]

Functional Group	Pin Name (Reset)	{I/O}	Supply	Default/Typical Usage	Alternate Functions		
					Alt 1	Alt 2	Alt 3
	GPIO_3 (L)	I/O	V_{EXT}	Vibrator	eGSPb[3]		MONITOR[3]
	GPIO_4 (L)	I/O	V_{EXT}	Display Backlight 3	eGSPb[4]	BACKLIGHT3	MONITOR[4]
	GPIO_5 (H)	I/O	V_{EXT}	Bluetooth Enable	eGSPb[5]	TWA Phase A	MONITOR[5]
	GPIO_6 (I)	I/O	V_{EXT}	SPI MISO / I2C Data	eGSPd[0]		MONITOR[6]
	GPIO_7 (I)	I/O	V_{EXT}	SPI SCK / I2C Clk	eGSPd[1]		MONITOR[7]
	GPIO_8 (I)	I/O	V_{EXT}	SPI Sel / I2C En	eGSPd[2]	BUZZER1	MONITOR[8]
	GPIO_9 (I)	I/O	V_{EXT}	SPI MOSI / I2C_Tx	eGSPd[3]	BUZZER2	MONITOR[9]
	GPIO_10 (I)	I/O	V_{EXT}	Flip-switch detect	eGSPd[4]	General Timer Out	MONITOR[10]
	GPIO_11 (I)	I/O	V_{EXT}	Camera Flash	eGSPd[5]	TimerInABC	MONITOR[11]
	GPIO_12 (L)	I/O	V_{EXT}	SubDisplay Backlight	eGSPc[0]	BACKLIGHT2	MONITOR[12]
	GPIO_13 (I)	I/O	V_{EXT}	Service Light	eGSPc[1]	Alert Light	BF_TRST_B
	GPIO_14 (I)	I/O	V_{EXT}	Serial Display CLK	eGSPc[2]	TWA Phase B	BF_TCK
	GPIO_15 (I)	I/O	V_{EXT}	Serial Display A0	eGSPc[3]	TWA Phase A	BF_TDI
	GPIO_16 (I)	I/O	V_{EXT}	Serial Display EN	eGSPc[4]	TWB Phase B	BF_TDO
	GPIO_17 (I)	I/O	V_{EXT}	Serial Display DI/DO	eGSPc[5]	TWB Phase A	BF_TMS
	GPIO_33 (I)	I/O	V_{EXT}	Bluetooth Rx	KeyPadRow[7]	HSL[0]	eGSPf[0]
	GPIO_34 (I)	I/O	V_{EXT}	Bluetooth Tx	KeyPadRow[6]	HSL[1]	eGSPf[1]
	GPIO_35 (I)	I/O	V_{EXT}	Multimedia card detect	KeyPadRow[5]	Alert Light	eGSPf[2]
	GPIO_36 (I)	I/O	V_{EXT}	Melody IC IRQ	KeyPadCol[7]	TWA Phase B	eGSPf[3]
	GPIO_37 (I)	I/O	V_{EXT}	Camera IRQ	KeyPadCol[6]	BUZZER1	eGSPf[4]
	GPIO_38 (I)	I/O	V_{EXT}	GPIO	KeyPadCol[5]	BUZZER2	eGSPf[5]
	GPIO_85 (I)	I/O	V_{EXT}	Buzzer	BUZZER1	PPLLCLKIN	BF_EMU_B
	GPIO_86 (L)	I/O	V_{EXT}	Keypad Backlight	BACKLIGHT0	eGSPa[5]	
	GPIO_87 (L)	I/O	V_{EXT}	Display Backlight 1	BACKLIGHT1	eGSPg[5]	DBGRQ
	KEYPADROW[4] (I+)	I/O	V_{EXT}	KEYPADROW[4]	eGSPa[0]	GPIO_88	
	KEYPADROW[3] (I+)	I/O	V_{EXT}	KEYPADROW[3]	eGSPa[1]	GPIO_89	
	KEYPADROW[2] (I+)	I/O	V_{EXT}	KEYPADROW[2]	eGSPa[2]	GPIO_90	
	KEYPADROW[1] (I+)	I/O	V_{EXT}	KEYPADROW[1]	eGSPa[3]	GPIO_91	
	KEYPADROW[0] (I+)	I/O	V_{EXT}	KEYPADROW[0]	eGSPa[4]	GPIO_92	
	KEYPADCOL[4] (TRI)	O/Tri	V_{EXT}	KEYPADCOL[4]	eGSPg[0]	GPIO_93	
	KEYPADCOL[3] (TRI)	O/Tri	V_{EXT}	KEYPADCOL[3]	eGSPg[1]	GPIO_94	
	KEYPADCOL[2] (TRI)	O/Tri	V_{EXT}	KEYPADCOL[2]	eGSPg[2]	GPIO_95	
	KEYPADCOL[1] (TRI)	O/Tri	V_{EXT}	KEYPADCOL[1]	eGSPg[3]	GPIO_96	
	KEYPADCOL[0] (TRI)	O/Tri	V_{EXT}	KEYPADCOL[0]	eGSPg[4]	GPIO_97	
	GPIO_113 (I)	I/O	V_{EXT}	BootControl[2]			
	GPIO_98 (I)	I/O	V_{EXT}	BootControl[0]			
	GPIO_99 (I)	I/O	V_{EXT}	BootControl[1]			

Functional Group	Pin Name (Reset)	{I/O}	Supply	Default/Typical Usage	Alternate Functions Alt 1	Alt 2	Alt 3
JTAG	JTAGEN / nTRST (I-)	I-	V_{EXT}	JTAG Enable Pull Down			
	GPIO_18 (I)	I/O	V_{EXT}	JTAG Test Clock (TCK {I})			
	GPIO_19 (I)	I/O	V_{EXT}	JTAG Test Mode Select (TMS {I} | DAIRESET)	FIO[5]		
	GPIO_20 (I)	I/O	V_{EXT}	JTAG Test Data Input (TDI {I} | DAI[1])	FIO[1]		
	GPIO_21 (I)	I/O	V_{EXT}	JTAG Test Data Output (TDO {O} | DAI[0])	FIO[0]		
	GPIO_177 (I)	I/O	V_{EXT}	RTCK			
PPI	PPI_DATA[9] (I)	I	V_{VID}	PPI Data Input		EB2_ADDR[19]	GPIO_136
	PPI_DATA[8] (I)	I	V_{VID}	PPI Data Input		EB2_ADDR[18]	GPIO_137
	PPI_DATA[7] (I)	I	V_{VID}	PPI Data Input		EB2_ADDR[17]	GPIO_130
	PPI_DATA[6] (I)	I	V_{VID}	PPI Data Input		EB2_ADDR[16]	GPIO_131
	PPI_DATA[5] (I)	I	V_{VID}	PPI Data Input			GPIO_132
	PPI_DATA[4] (I)	I	V_{VID}	PPI Data Input			GPIO_133
	PPI_DATA[3] (I)	I	V_{VID}	PPI Data Input			GPIO_134
	PPI_DATA[2] (I)	I	V_{VID}	PPI Data Input			GPIO_135
	PPI_DATA[1] (I)	I	V_{VID}	PPI Data Input		eGSPg[4]	GPIO_128
	PPI_DATA[0] (I)	I	V_{VID}	PPI Data Input		eGSPg[5]	GPIO_129
	PPI_HSYNC (I)	I	V_{VID}	PPI Frame Sync		EB2_ADDR[15]	GPIO_138
	PPI_VSYNC (I)	I	V_{VID}	PPI Frame Sync		EB2_ADDR[14]	GPIO_139
	PPI_CLK (L)	I/O	V_{VID}	PPI Clock		EB2_ADDR[13]	GPIO_140
EBUS2	GPIO_141 (I-)	I/O	V_{VID}		PPI_DATA[9]		EB2_DATA[15]
	GPIO_142 (I-)	I/O	V_{VID}		PPI_DATA[8]		EB2_DATA[14]
	GPIO_143 (I-)	I/O	V_{VID}		PPI_DATA[7]		EB2_DATA[13]
	GPIO_144 (I-)	I/O	V_{VID}		PPI_DATA[6]		EB2_DATA[12]
	GPIO_145 (I-)	I/O	V_{VID}		PPI_DATA[5]		EB2_DATA[11]
	GPIO_146 (I-)	I/O	V_{VID}		PPI_DATA[4]		EB2_DATA[10]
	GPIO_147 (I-)	I/O	V_{VID}		PPI_DATA[3]		EB2_DATA[9]
	GPIO_148 (I-)	I/O	V_{VID}		PPI_DATA[2]		EB2_DATA[8]
	GPIO_149 (I-)	I/O	V_{VID}		PPI_DATA[1]		EB2_DATA[7]
	GPIO_150 (I-)	I/O	V_{VID}		PPI_DATA[0]		EB2_DATA[6]
	GPIO_151 (I-)	I/O	V_{VID}				EB2_DATA[5]
	GPIO_152 (I-)	I/O	V_{VID}				EB2_DATA[4]
	GPIO_153 (I-)	I/O	V_{VID}				EB2_DATA[3]
	GPIO_154 (I-)	I/O	V_{VID}				EB2_DATA[2]
	GPIO_155 (I-)	I/O	V_{VID}				EB2_DATA[1]
	GPIO_156 (I-)	I/O	V_{VID}				EB2_DATA[0]
	EB2_nRD (H)	O	V_{VID}	EBUS2 Read Enable			GPIO_157
	EB2_nWE (H)	O	V_{VID}	EBUS2 Write Enable			GPIO_158
	EB2_ADDR[12] (L)	O	V_{VID}	EBUS2 Address	eGPSg[0]		GPIO_159

Functional Group	Pin Name (Reset)	{I/O}	Supply	Default/Typical Usage	Alternate Functions Alt 1	Alt 2	Alt 3
	EB2_ADDR[11] (L)	O	V_{VID}	EBUS2 Address	eGSPg[1]		GPIO_160
	EB2_ADDR[10] (L)	O	V_{VID}	EBUS2 Address	eGSPg[2]		GPIO_161
	EB2_ADDR[9] (L)	O	V_{VID}	EBUS2 Address	EB2_DATA[17]	eGSPa[3]	GPIO_162
	EB2_ADDR[8] (L)	O	V_{VID}	EBUS2 Address	EB2_DATA[16]	eGSPa[4]	GPIO_163
	EB2_ADDR[7] (L)	O	V_{VID}	EBUS2 Address		eGSPa[5]	GPIO_164
	EB2_ADDR[6] (L)	O	V_{VID}	EBUS2 Address		eGSPa[0]	GPIO_165
	EB2_ADDR[5] (L)	O	V_{VID}	EBUS2 Address		eGSPa[1]	GPIO_166
	GPIO_167 (I-)	I/O	V_{VID}			eGSPa[2]	EB2_ADDR[4]
	EB2_ADDR[3] (L)	O	V_{VID}	EBUS2 Address	eGSPg[3]		GPIO_168
	EB2_ADDR[2] (L)	O	V_{VID}	EBUS2 Address			GPIO_169
	EB2_ADDR[1] (L)	O	V_{VID}	EBUS2 Address			GPIO_170
	EB2_ADDR[0] (L)	O	V_{VID}	EBUS2 Address	CLKMUXOUT3		GPIO_171
	GPIO_172 (I+)	I/O	V_{VID}		CLKMUXOUT3		EB2_nCS[3]
	GPIO_173 (I+)	I/O	V_{VID}		TimerInD	EB2_DATA[17]	EB2_nCS[2]
	GPIO_174 (I+)	I/O	V_{VID}			EB2_DATA[16]	EB2_nCS[1]
	GPIO_175 (I+)	I/O	V_{VID}				EB2_nCS[0]
	EB2_nWAIT (I+)	I	V_{VID}	EBUS2 Wait Request			GPIO_176
Power	V_{CORE}[10:1]	PWR	N/A	Core Power Supply			
	V_{RTC}	PWR	N/A	RTC Power Supply			
	V_{SIM}	PWR	N/A	SIM Power Supply			
	V_{MEM}[4:1]	PWR	N/A	Memory Power Supply			
	V_{EXT}[4:1]	PWR	N/A	External Device Power Supply			
	V_{INT1}	PWR	N/A	ABB Interface Power Supply 1			
	V_{INT2}	PWR	N/A	ABB Interface Power Supply 2			
	V_{USB}	PWR	N/A	USB Power Supply			
	V_{BUS}	PWR	N/A	5V USB power supply from cable			
	V_{MMC}	PWR	N/A	Multimedia Card Interface Supply			
	V_{VID}[3:1]	PWR	N/A	Video power supply (for APBUS)			
	V_{PLL}	PWR	N/A	Power Supply for PLLs, CLKIN buffer			
	V_{CPRO}[2:1]	PWR	N/A	Power Supply for Communications Accelerator Core			
	GND[28:1]	PWR	N/A	Ground			

ARCHITECTURE OVERVIEW

The digital baseband architecture supports two processing cores: the ARM926EJ microcontroller from ARM Ltd., (referred to as the MCU), and Analog Devices' Blackfin DSP processor (referred to as the DSP). The two processors both have shared access to all peripherals and memory subsystems through a unified system address map, and unified system interrupt maps.

Unlike conventional DSP architectures, the Blackfin DSP architecture supports a flexible microcontroller instruction set, including a byte-addressed memory map. This feature, along with a common (unified) memory map between the DSP and the MCU (excluding control registers local to each processor), and a flexible interrupt controller which allows any system interrupt to be mapped to either processor, greatly simplifies the programming model for a heterogeneous multiprocessor system.

Software tasks can easily migrate to either processor, to simplify load balancing as the software evolves over time. In particular, the AD6905 is specifically designed to accommodate as much of the protocol stack as possible on the DSP, leaving the MCU free for other applications.

All system resources in the AD6905 are memory mapped. The flat, 32-bit byte-address memory map of the AD6905 is comprised of four main subsystems, as shown in the following diagram:

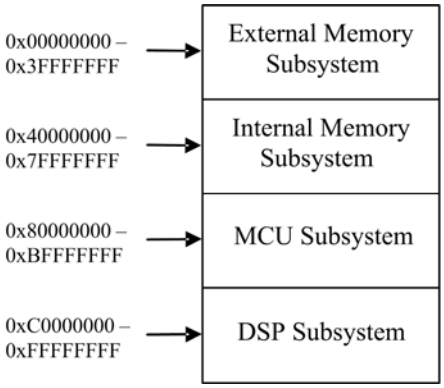


Figure 2: AD6905 Shared Memory Map

The AD6905 has three DMA controllers to relieve the MCU and DSP from repetitive operations, such as servicing I/O devices and performing transfers from one memory block to another. In addition to the DSP DMA controller and MCU (System) DMA controller, the Applications subsystem has its own dedicated DMA controller. These DMA controllers are shared resources, although typically the DSP programs the DSP DMA while the MCU programs the System DMA and Applications DMA.

The two processor subsystems each have their own dedicated interrupt controllers, JTAG TAP controllers, ciphering units, and local control/status registers.

The internal logic, analog PLL, RTC, and the periphery I/O can each be driven off separate power supplies, allowing for simple I/O interfacing while minimizing core power consumption. Level-shifting logic at each of these interfaces ensures valid communication between each power domain, and prevents excess current flow between the domains. The level-shifting logic also minimizes current flow between the domains when voltage to one of the power domains is disabled.

As the internal logic voltage is increased, control software is able to increase the MCU and DSP clock frequencies, providing more processing capability (i.e. MIPs). These frequencies are produced by a single analog PLL, which multiplies to a programmable output frequency. This signal is divided to obtain the desired DSP clock frequency, MCU clock frequency, and other internal synchronous clocks.

The AD6905 device interfaces to an AD6857 mixed-signal Analog Baseband Codec (ABB), which performs the ADC/DAC and filtering for the speech channel (microphone, speaker), as well as the modulation and demodulation for the up- and downlinks of the communications channel. An auxiliary interface supports additional ADC for functions such as battery and temperature monitoring, and the power management control communication. For the other system components, additional flexibility is provided in the signaling to support a wider range of components, including large memory systems and accessory devices.

A development bond-out package will be available to support more extensive debug and emulation facilities, but significant support is maintained in the production package via the JTAG port and the Universal System Connector. This includes hardware signal monitoring, high-throughput data and instruction trace logging, and serial port (Voice data, I/Q data, Messaging) access, as well as emulation of the MCU and DSP processing cores.

The JTAG port available in the production bond-out package is fully IEEE-compatible, and can be used to support full boundary-scan PCB testing. Note that the boundary scan function can be disabled, to prevent unauthorized reprogramming of the FLASH memory via this interface. This port also supports debug and emulation control of both the MCU and DSP cores.

Internal Architecture

The block diagram below shows the AD6905 system organization.

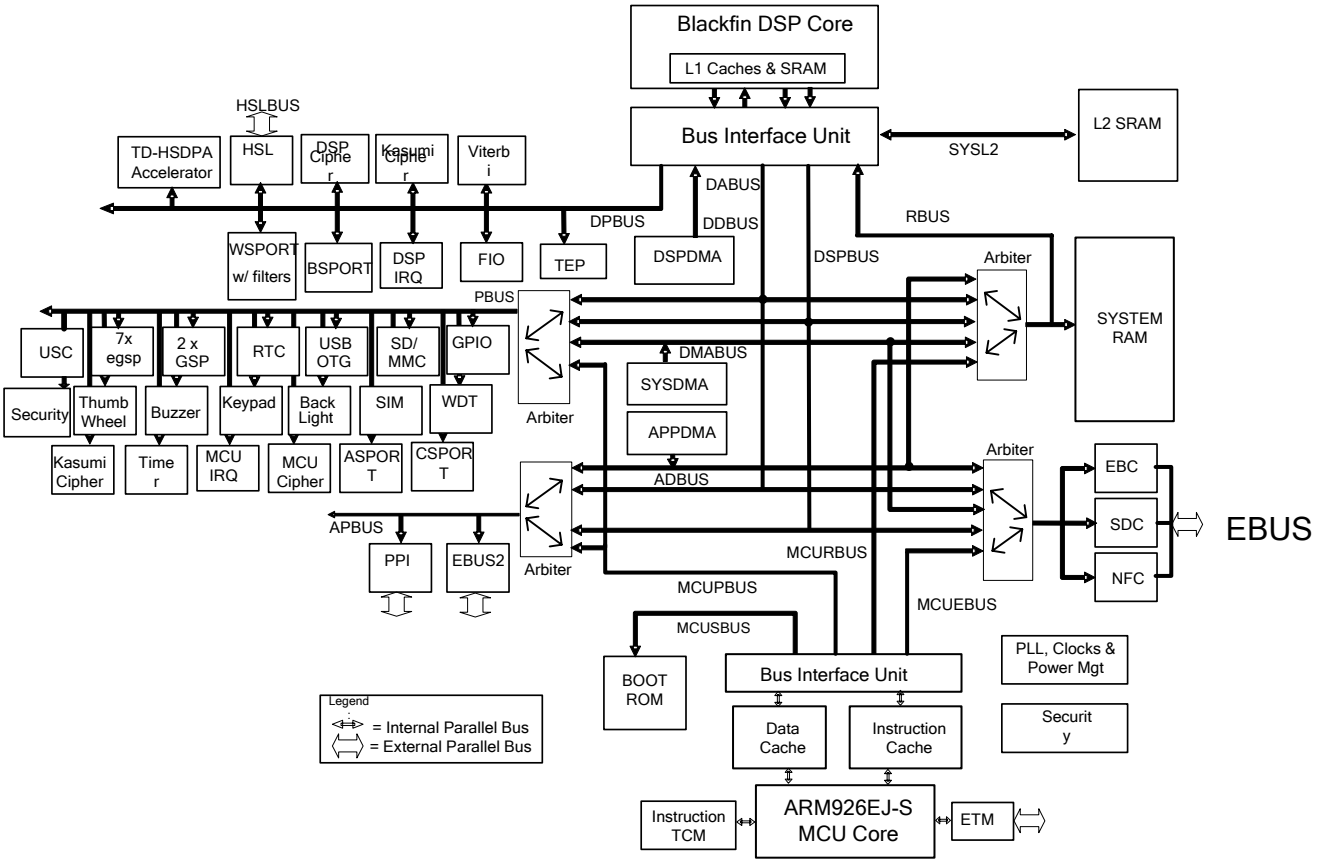


Figure 3: AD6905 Block Diagram

The system is served by 13 main bus systems. The bus interface units and bus arbiters provide a high degree of concurrency, to support the real-time requirements of this multimaster system. For example, DSP, MCU, System DMA, DSP DMA, and Applications DMA transfers can often occur in parallel, with no conflicts or collisions.

The Blackfin DSP also has three dedicated high-speed buses to support DSP access to the system and one dedicated interface for system access to L1 memory.

Internal Modules

The AD6905 architecture is partitioned into five main subsystems:

- MCU Subsystem—ARM926EJ-S core, MCU Bus Interface Unit, MCU Data Cache, MCU Instruction Cache, Boot ROM, and Embedded Trace Macrocell (ETM)
- DSP Subsystem—Blackfin DSP core, DSP Bus Interface Unit, L1 and L2 Memories, DSP Peripherals, and DSPDMA controller
- Peripheral Subsystem—Communications peripherals, housekeeping peripherals, man-machine interface peripherals, and SYSDMA controller
- Applications Subsystem—Parallel Port Interface (PPI), LCD controller Interface (EBUS2), and APPDMA controller
- Memory Subsystem—System SRAM and External Bus Interface, including SDRAM and NAND FLASH interfaces. The System RAM is fast RAM which can store code and data for either processor.

System Clocking Overview

The AD6905 system has one primary clock input (CLKIN), from which all internal timing is derived, except for the internal logic which operates on asynchronous clock domains (e.g., RTC, USB, serial ports). This clock can be either 13 or 26 MHz. The AD6905 can accept a low voltage swing, low harmonic content clock input for reduced power. Conversely, the clock input can be driven by a full rail-to-rail, square wave input. The AD6905 provides two integrated PLLs. One produces all high frequency internal clocks required for the processor and memory subsystems. The other PLL provides the high frequency clocks required for the USB and IrDA interfaces.

Extensive clock and power management control on the AD6905 provides the capability to switch system clock frequencies on the fly, and to move in and out of PLL bypass on the fly.

DSP Subsystem

The DSP subsystem, shown below, consists of the Blackfin DSP core enhanced with a dedicated DMA controller, an interrupt controller, and a cache/RAM memory hierarchy. System timing accuracy and sequencing are provided by the Timing Event Processor (TEP). This subsystem also includes two serial port controllers, a high-speed data logging unit (HSL), Programmable Flag I/O, a cipher coprocessor, Kasumi cipher coprocessor, Viterbi coprocessor and TD-HSDPA accelerator.

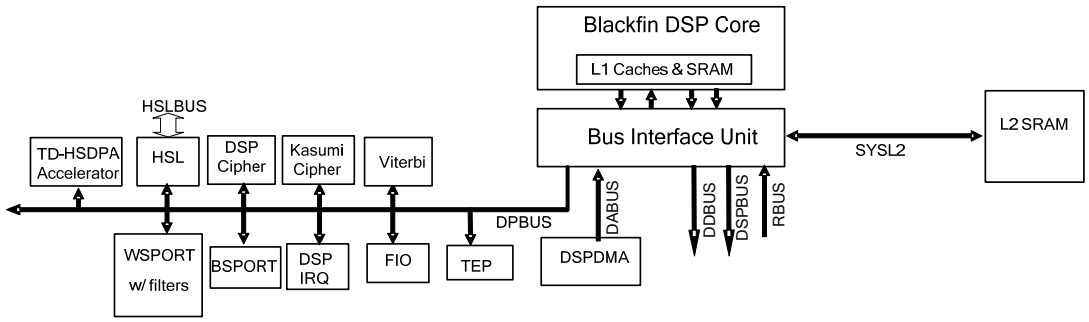


Figure 4: DSP Subsystem Block Diagram

Blackfin DSP Processor

The Blackfin is a digital signal processor (DSP) with added functionality to realize many of the programming advancements normally associated with microcontrollers.

The Blackfin core is a dual datapath, modified Harvard architecture processor that is optimized for both DSP and microcontroller functions. The DSP features of the architecture include one instruction and two separate data ports to a unified 4GB memory space, two 16-bit single-cycle throughput MACs, two 40-bit split ALUs, four auxiliary 8-bit ALUs, two DAGs with circular and bit-reversed addressing, two loop counters that allow nested zero overhead looping, and hardware support for on-the-fly saturation and clipping. The microcontroller features include arbitrary bit manipulation, mixed 16- and 32-bit instruction encoding for code density, memory protection, stack pointers and scratch SRAM for context switching, flexible power management, and a nested and prioritized interrupt controller for real-time control. Execution time predictability is achieved with lockable caches that can optionally be configured as SRAM, and data-independent instruction execution.

The DSP is supported by a hierarchical memory system to minimize power consumption while providing high bandwidth and low latency. The Level 1 (L1) memory directly supports the Harvard architecture of the DSP core with separate instruction and data memories. Each of these memory systems is banked, to support concurrent accesses. The L1 memory is organized as follows:

- Instruction memory, consisting of:
  - 64K bytes of Instruction SRAM
  - 16K bytes of configurable Instruction Cache (or SRAM); cache is 2-way set associative, lockable by way, 32B cache lines
- Two data memory banks, each consisting of:
  - 8K bytes of dedicated SRAM and an additional 8K bytes that can be configured as either cache or SRAM; 2-way set associativity, 32B lines, writeback or write-through

The Level 2 memory (L2) consists of 64KB of SRAM, with a 64-bit interface to the DSP. The L2 memory can provide a 32-byte cache line fill to the DSP in 7 L2 clock cycles. The L2 memory is clocked at half the DSP clock frequency if the DSP clock > 150MHz. Below 150MHz, L2 memory can clock at a 1:1 ratio.

The L2 memory provides unified code and data storage for the DSP, and is also accessible by the DSP DMA controller and the MCU.

The bus interface unit performs the bus bridging functions for the DSP subsystem. The bus interface unit functions as an

asymmetric crossbar switch, routing requests from the Blackfin DSP core, the DSP DMA controller, and the microcontroller subsystem (microcontroller and system DMA), to the appropriate slaves (DPBUS peripherals, L1 RAM on the Blackfin core, L2 RAM, or system resources via the DSP bus). The bus interface unit provides parallel and concurrent data transfer capability between the various busses.

DSP Peripherals

The Baseband serial port (BSPORT) provides the full-duplex serial data channel for GSM/GPRS/EGPRS baseband data.

The Wideband CDMA serial port (WSPORT), with associated RRC filtering, supports TD-SCDMA baseband data transfers. The WSPORT is a full-duplex serial port interface between the AD6905 and an AD6857 analog baseband (ABB) device. The WSPORT is used to transmit uplink data and receive downlink data as I/Q samples. Uplink transfers are initiated by the AD6905, and downlink transfers are initiated by the ABB.

The Timing and Event Processor (TEP) provides all on-air interface timing. The Flag Input/Output (FIO) module provides dedicated bit-level communication between the DSP subsystem and other system entities, such as the USC.

The Cipher coprocessor is designed mainly for, but not restricted to GPRS/EGPRS. This eases the bandwidth requirements for ciphering. Once configured and programmed, this engine runs autonomously with minimal intervention from the DSP. The cipher engine supports an instruction set capable of computing cipher streams for GEA and GEA2 (A5/1, A5/2) encryption algorithms.

The Kasumi cipher coprocessor handles A5/3 GEA3 encryption and decryption.

The Viterbi coprocessor provides decoding of convolutional encoded data and channel equalization. This coprocessor is primarily intended for convolutional decoding in WCDMA TDD applications.

The TD-HSDPA accelerator manages communications functions for HSDPA and LCR downlink channels.

MCU Subsystem

The MCU subsystem is shown in
Figure 5. It consists of an ARM926EJ-S central processing unit, a boot ROM, an interrupt controller, data cache, instruction cache, Tightly Coupled Memory (TCM) and control registers for MCU configuration. The main function of the MCU subsystem in a GSM system is to execute the Man Machine Interface (MMI) software and other user application functions.

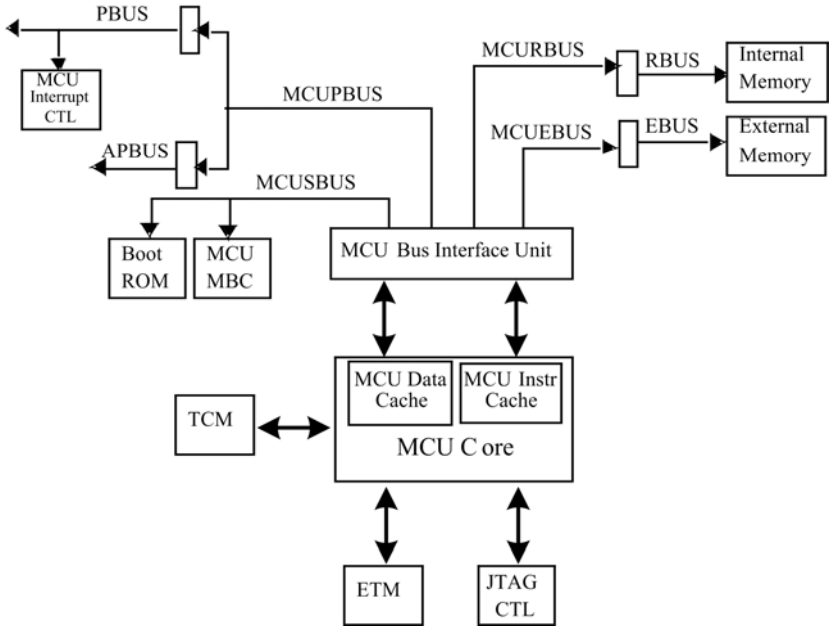


Figure 5: The ARM® Microcontroller Subsystem

The MCU has access to resources located on the PBUS, RBUS, and EBUS:

- EBUS: Flash Memory, optional RAM, and optional off-chip hardware modules
- RBUS: Internal RAM, and DSP subsystem
- PBUS: Watch Dog Timer (WDT), General Timers, interrupt controller, USB, SPI, etc.

The MCU subsystem is designed to obtain the highest possible utilization of the MIPs available from the ARM9 processor -- optimum clock generation, fast access to system RAM, etc. . The system is also designed for low power consumption with

powerdown mode and clock disabled while the MCU is idling or waiting for access to one of the buses.

The ARM926EJ-S processor is a high-performance, single-cycle RISC machine. The architecture is based on a 16/32 bit instruction set that supports 8/16/32 bit data formats. The ARM926EJ-S includes the Thumb 16-bit instruction set optimized for code density. This is a well-recognized microcontroller architecture widely used in communication applications. It offers low power consumption and good code density and is supported by many third party software vendors and software development tools.

The MCU subsystem includes a 16kB instruction cache and a 16 kB data cache. Each cache line is 32 bytes (8 words) long. There is also a 4kB Tightly Coupled Memory (TCM) used for MCU instructions.

The Boot ROM contains MCU code for basic communication between the MCU and one of the serial ports in the Universal System Connector (USC) subsystem. This ROM code is used to initialize the MCU system and allows a very simple communication scheme that can be used to load more sophisticated code for a more effective communication protocol into the internal SRAM. The boot code reads the state of the boot control pins, which can be configured for different booting modes. This boot mechanism can be used in the absence of off-chip memory or when the external Flash Memory is not initialized. At the end of RESET, if a unique synchronization character is detected at the USC's serial data input, the MCU starts executing software from the Boot ROM. Otherwise, the MCU starts executing software from external Flash memory. Alternately, the device can be configured to boot through the USB port.

DMA Controllers

The DSP and Applications subsystems each have dedicated multichannel DMA controllers, and there is a separate system DMA controller for use by the MCU. The DMA controllers can initiate, move and complete data transfers from any address location on one system bus to any address on another system bus. The DMA transfer is defined by software executed either on the DSP or on the MCU. The transfer itself may be triggered by one of the processors or by interrupts issued from the interrupt controller. The DMA controllers handle data transfer for both I/O devices (interrupt-driven) and memory devices. Each DMA controller consists of separate full-duplex channels with identical functionality. Each channel is controlled and configured by either the MCU or the DSP. Each DMA controller can move a programmable number of data bytes after which it sends an interrupt to the IRQ controller.

The DMA controllers are used to perform different functions in the system:

- Implement a RAM buffer in the system, between an I/O data peripheral and the MCU system, for example, for interrupt count reduction and easy handling of I/O data. In that case, the DMA transfers a burst of data between a RAM module, such as the SRAM and an I/O peripheral.
- Move a block of data (e.g. tables or program) from the external Flash memory to the DSP's L1 or L2 memory, during booting, dynamic download, etc.
- Copying large memory blocks from one location to another in the system software memory space.

The AD6905 supports a chaining DMA feature, which automatically sets up a new DMA channel to continue transferring data, after completing the data transfer from the current DMA channel. This feature provides more relaxed timing constraints for postprocessing of data that has been transferred, and decreased risks for simultaneously working on the same set of data.

The DMA controllers also include a burst mode (of four transfers) for even higher DMA bandwidth.

On some channels, the source and destination for DMA transfers may be two-dimensional (2D) memory buffers. These are particularly useful for reordering data in image buffers, and lower the DMA management overhead. 2D addressing defines two transfer address loops, an inner loop and an outer loop, with each loop having a programmable count and address increment.

PERIPHERAL SUBSYSTEM

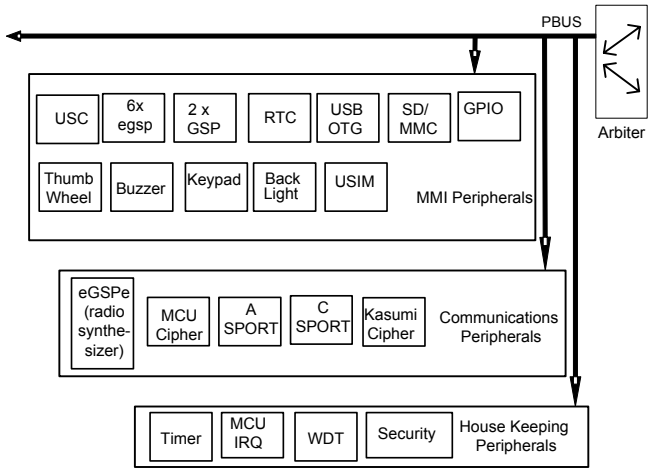


Figure 6: Peripherals Subsystem

The peripherals subsystem shown in Figure 6 contains three major groups:

- Man-Machine Interface (MMI)
- Housekeeping peripherals
- Communications peripherals

Man-Machine Interface (MMI)

The Man-Machine Interface (MMI) is a collection of all the functionality needed to implement a complete user interface including keyboard, display, backlight, Real Time Clock (RTC), General Purpose I/O etc. A major part of the MMI is also the Universal System Connector (USC) that can be made available at the bottom of the mobile phone. The USC allows the same 5-10 pins to be used for: two synchronous or asynchronous serial data connections, multiplexed serial voice and communications, DAI interface, high speed logging emulation of the processors in the system, etc.

General Purpose Input/Output (GPIO)

The AD6905 includes 181 General Purpose Input/Output signal pins. Each of these pins can be configured as inputs or outputs. They also can be configured to trigger one of 32 MCU or DSP interrupts. The TEP can control the output state of 47 of the GPIO pins. All GPIO pins are shared with other functional pins and GPIO functionality must be selected in the pin multiplexing control registers.

Each GPIO consists of separate input, input enable, output, and output enable functions, and the pin is configured by a set of registers:

- INPUT, contains the sampled input value of the pin
- OUTPUT, sets the output value of the pin
- Output Enable, enables the output.
- Function SELECT, to select between GPIO functionality and the normal (or alternative) function of the pin (e.g. address bus bits, chip select signals, etc.)

Backlight Interface

The basic backlight controller provides 4 independent backlight controls whose duty cycle and frequency can be set by software. The duty cycle is programmable in 128 steps from 1/128 to 127/128 and the frequency can be selected from a variety of predefined frequencies. The 4 outputs can be individually enabled and their input clock sources can be either the 13 MHz system clock or the 32 kHz clock. There is also a service light that can be independently configured.

Keypad Interface

The Keyboard interface supports a Row/Column decoding of a keyboard matrix of up to 8 Rows and 8 Columns. The scanning functionality is handled by software. The interface generates an interrupt when any key is pressed, and the interrupt is routed through the interrupt controller to the MCU. No hardware debouncing is provided within the AD6905.

Buzzer

The AD6905 contains a Tone Generator module that can be used to output custom tones defined by duration, frequency, and power level. Additionaly, it contains a sigma-delta modulator that can be used to play back melodies derived from an input data stream. Both outputs can be made available independently, or shared via the same GPIO interface.

Thumwheel

The AD6905 supports 2 identical thumwheel channels (A and B). Each channel accepts two signals coming from the

thumwheel in quadrature of phase. The interface debouces and decodes these to produce a direction indicator (up/down). Each channel can also generate an interrupt that, if enabled, indicates thumbwheel movement has occurred.

Real Time Clock (RTC)

If a 32 kHz crystal is attached to the system, the AD6905 supports a Real Time Clock function. A total of 25pF +/– 10% capacitance to ground is required (including board trace capacitance) on each of OSCIN and OSCOUT. RTC functionality allows the application software to implement standard clock, calendar, or organizer functions such as:

- Time and date display
- Programmable alarm
- Programmable mobile activation

The RTC interrupt is routed through the IRQ controller to the MCU or the DSP, as defined by software in the interrupt configuration registers. The RTC has a 365 day alarm setting.

Universal Subscriber Identity Module (USIM) Interface

The USIM interface supports the functionality of the GSM Phase 1 specification, the functionality of the GSM Phase 2+ specification for FAST 64 kbps SIM (intended for use with a SIM application Toolkit), and the functionality of the TD-SCDMA specification. All USIM interrupts are routed through the IRQ controller to the MCU, DSP or DMA.
The DMA supports autobuffering of the communication between the processor and the USIM interface.

Both 1.8V and 3.0V USIMs are supported.

Multimedia Card and Secure Digital Interface (MMC/SD)

The AD6905 integrates an interface for Multimedia Cards (MMC), Secure Digital Memory Cards (SD Card) and Secure Digital Input/Output Cards (SDIO). A separate power supply domain allows use with cards of varying voltages.

Enhanced Generic Serial Ports (eGSPs)

The AD6905 includes a total of seven highly flexible generic serial protocol controllers which allow a wide range of serial protocols to be supported. Each eGSP can implement a number of serial port protocols, from single-wire to full asynchronous modem and synchronous interfaces. Among the serial communication protocols that can be implemented are:

- UART, full-duplex or half-duplex, with data modem support (i.e. CTS, RTS, RI, and DTR)
- SPI
- Two-wire synchronous serial port compatible with I^2C
- IrDA (SIR, MIR, and FIR, up to 4Mbps baud rate)
- I^2S

The eGSPs also support synchronous serial protocols requiring frame synchronization signals such as:

- Synthesizer port for radio programming
- Serial displays
- Digital Audio Interface (DAI)
- Battery Management Control (BMC)

Generic Serial Ports (GSPs)

In addition to the eGSPs, the AD6905 includes two lower-functionality Generic Serial Ports (GSPs), which are typically used as UARTs.

Universal Serial Bus

The AD6905 provides serial communications through a full-speed (12 Mb/s) USB 2.0 dual-role interface, with OTG (On-The-Go) host mode or traditional peripheral-only mode. USB OTG provides a low-cost connectivity solution for consumer mobile devices such as cell phones, digital still cameras, and MP3 players, allowing these devices to transfer data via a point-to-point USB connection without the need for a PC host.

The AD6905 integrates the USB transceiver on-chip and only an external pull-up resistor is required to connect to a USB host. The USB interface can be used for Flash download and applications such as PC synchronization, MP3 download, etc.

Data is transferred to and from the USB port through any of the 7 Transmit and 7 Receive endpoint FIFOs. The number of active endpoints at one time is only limited by device requirements or system bandwidth, since each endpoint operates independently.

Universal System Connector (USC)

The Universal System Connector (USC) subsystem is an intelligent crosspoint switch between the limited number of signal pins that are available in a mobile system connector and the various interfaces in the system that must be brought outside the mobile phone.

The USC block diagram of Figure 7 shows the possible connections to the system. The USC includes:

- Five serial communication ports, implemented via Enhanced Generic Serial Ports, which can be configured in different modes, e.g. RS-232 or synchronous communication. The eGSPa and eGSPb ports are intended for external communication with the AD6905 chip, for data services (if not onboard), Flash Memory programming, debugging, etc.
- a JTAG interface to support in-circuit emulation of the embedded ARM processor.
- a High Speed Logging and trace interface for monitoring data flowing in the DSP system, providing a snapshot of a voice buffer and for other debugging functions.
- a direct interface to the audio serial port (ASPORT), allowing the user to directly connect the System Simulator for Full Type Approval. This interface can also be used for production test of the audio path. The only external devices that may be required are level shifters.

- a direct interface for monitoring the Rx I/Q signals (through the BSPORT), to permit measurement of Signal to Noise Ratio (SNR) of the radio during production test.
- the Wideband CDMA serial port (WSPORT)
- a JTAG interface for DSP emulation.
- GPIO

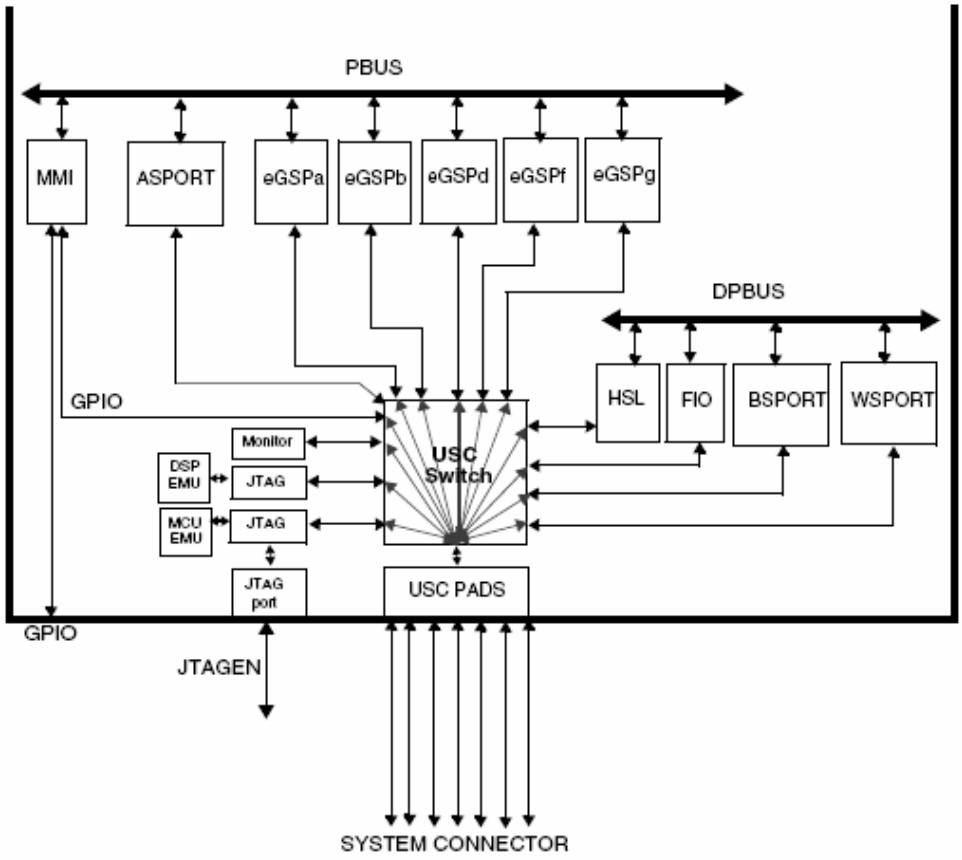


Figure 7: Universal System Connector (USC)

Communications

The communications module provides functionality to support data communications, including Audio Serial Port (ASPORT), Control Serial Port (CSPORT), Cipher Coprocessor, Kasumi Coprocessor and Radio Synthesizer Port.

Audio Serial Port (ASPORT)

The Audio Serial Port (ASPORT) supports general audio data transfers for both the DSP and MCU subsystems.

Control Serial Port (CSPORT)

Communications with the analog baseband (ABB) chips is through the Control SPORT (CSPORT). The CSPORT serial interface to the ABB allows the transfer of control information from AD6905 to ABB chips.

MCU Cipher

The MCU cipher module on the PBUS is identical to the DSP's cipher coprocessor.

Kasumi Cipher

The Kasumi cipher module on the PBUS is identical to the DSP's Kasumi cipher coprocessor.

Radio Synthesizer Port (eGSPe)

The radio synthesizer interface is controlled via an enhanced generic serial port, eGSPe. This interface is a Serial Synthesizer Port (SSP) used to communicate with the radio synthesizer. The SSP provides a flexible solution for programming the radio synthesizer through a serial interface. This programmability of the port enables various radio synthesizers to be easily interfaced. The synthesizer port can also support read-back from the radio.

Housekeeping

The Housekeeping module groups traditional microcontroller peripheral functionality, including several different submodules: the Watch Dog Timer, General Timers, Security, and Interrupt Controller for interrupts to the MCU, DSP, and DMA. In the AD6905 architecture, these modules are placed on the PBUS to achieve a high degree of freedom in their use. For example, both the DSP and the MCU have access and can change the interrupt routing and prioritization as needed.

Watch Dog Timer

The Watch Dog Timer (WDT) is used to supervise the execution of software from a system point of view, and identify malfunctions. An identified software malfunction generates a non-maskable interrupt to the processors, MCU or DSP. After such an interrupt, dedicated software routines handle corrective actions, for example switching off or restarting the handset. The interrupt is routed through the IRQ controller to the MCU or DSP.

General Timers

The AD6905 provides four independent timers. The general timer functionality in the system supports the MCU and DSP processors with a timer interrupt, intended for use in a Real Time Operating System. The Timer system supports both one shot timing and cyclic timing. All timer interrupts are routed through the IRQ controller to the MCU, DSP, or DMA. The clock source for each timer can be selected from the system clock, 32 kHz clock, TEP clocks, GPIO pin, or another timer.

Security

The AD6905 provides a secure environment that enables application software to use secure protocols. An example of a secure protocol that may be implemented on the AD6905 is Content Protection for Recordable Media (CPRM). Implementing CPRM or other secure protocols on the AD6905 involves a combination of hardware and software components. Together these components protect secure memory spaces and restrict control of security features to authenticated application code.

APPLICATIONS SUBSYSTEM

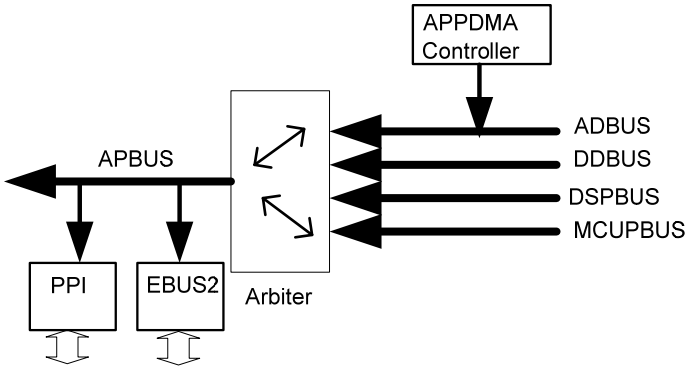


Figure 8: Applications Subsystem

EBUS2 Parallel Display Interface

The AD6905's EBUS2 is a separate external interface for parallel-bus LCD displays. Keeping this separate reduces noise and loading on the signal lines of the main EBUS memory interface.

The EBUS2 is primarily intended to be used as an LCD controller interface, but may also be used to accept camera input data or interface to ASIC devices. It provides four display and auxiliary device interface segments, each with an associated chip select signal.

Parallel Peripheral Interface

The Parallel Peripheral Interface (PPI) is an input-only parallel external port that can connect directly to camera modules. The PPI accommodates up to 10 bits of data, in a variety of RGB and YUV color formats. In addition, ITU-656 (CCIR656) and ITU-601 (CCIR601) compatible data transfers are supported.

The PPI feature set includes:

- Data transfer rates up to 32.5 MB/s
- Two frame syncs (horizontal and vertical), with programmable polarity
- Bidirectional clock pin, with programmable output clock rate up to 65 MHz
- Synchronization by detection of embedded preamble codes or by using frame synchronization pins
- ITU standard and counter controlled data transfers
- 8-bit data packing to reduce DMA bandwidth for image data
- Data re-ordering to reduce DMA bandwidth for YUV 4:2:2 data
- 32-word by 16-bit input FIFO

The PPI offers specific configurations to support still image and video data inputs. It also provides Active Video Only and Entire Field operational modes. In all modes, data packing options optimize DMA transfer bandwidth for YUV 4:2:2 and other data formats.

Applications DMA (APPDMA)

The APPDMA is a full-featured DMA controller intended to relieve the MCU and DSP from repetitive data transfers involving APBUS peripherals and/or shared system memory. The APPDMA is a 16-channel DMA and supports 2-D burst transfers to and from internal or external memory.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		Min	Typ	Max	Unit
V_{CORE}	Core Supply Voltage	TBD	1.5	1.65	V
V_{PLL}	PLL Supply Voltage	1.35	1.5	1.65	V
V_{CPRO}	Communications Accelerator Core Supply Voltage	TBD	1.5	1.65	V
V_{RTC}	Real Time Clock Supply Voltage	1.2	1.8	2.0	V
V_{SIM}	SIM Supply Voltage (High)	2.7	2.8	3.3	V
V_{SIM}	SIM Supply Voltage (Low)	1.7	1.8	1.95	V
V_{MEM}	Memory Supply Voltage	1.7	1.8	1.95	V
V_{EXT}	External Device Supply Voltage	2.7	2.8	3.3	V
V_{INT1}	ABB Interface Supply Voltage 1	1.7	1.8	1.95	V
V_{INT2}	ABB Interface Supply Voltage 2	1.7	1.8	1.95	V
V_{MMC}	Multimedia Card Interface Supply Voltage (Low)	1.7	1.8	1.95	V
V_{MMC}	Multimedia Card Interface Supply Voltage (High)	2.7	2.8	3.6	V
V_{USB}	USB Interface Supply Voltage	3.0	3.3	3.6	V
V_{VID}	EBUS2 LCD Interface Supply Voltage (Low)	1.7	1.8	1.95	V
V_{VID}	EBUS2 LCD Interface Supply Voltage (High)	2.7	2.8	3.0	V
T_A	Ambient Operating Temperature	–20		+85	°C

DC CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage	$Vpin^{[1]} = Vpin_{max}$	0.7 * Vpin			V
V_{IL}	Lo-Level Input Voltage	$Vpin^{[1]} = Vpin_{min}$			0.3 * Vpin	V
V_{OH}	Hi-Level Output Voltage	$Vpin^{[1]} = Vpin_{min}$, I_{OH} = -0.5 mA	Vpin – 0.2		$Vpin^{[2]}$	V
V_{OL}	Lo-Level Output Voltage	$Vpin^{[1]} = Vpin_{min}$, I_{OL} = 2 mA	$GND^{[2]}$		0.2	V
$V_{OLPWRON}$	Lo-Level Output Voltage	$Vpin^{[1]} = Vpin_{min}$, I_{OL} = 30µA	$GND^{[2]}$		0.3	V
I_{IH}	Input Current	$Vpin^{[1]} = Vpin_{max}$, $V_{IN} = Vpin_{max}$	-1.0		1.0	µA
I_{IH_P}	Input Current [pin with internal pull-down]	$Vpin^{[1]} = Vpin_{max}$, $V_{IN} = Vpin_{max}$	15		100	µA
I_{IL}	Input Current	$Vpin^{[1]} = Vpin_{max}$, V_{IN} = 0 V	-1.0		1.0	µA
I_{IL_P}	Input Current [pin with internal pull-up]	$Vpin^{[1]} = Vpin_{max}$, V_{IN} = 0 V	-100		-15	µA
I_{OZL}	Lo-Level Output 3-State Leakage Current	$Vpin^{[1]} = Vpin_{max}$, $V_{IN} = Vpin_{max}$	-1.0		1.0	µA
I_{OZH}	Hi-Level Output 3-State Leakage Current	$Vpin^{[1]} = Vpin_{max}$, V_{IN} = 0 V	-1.0		1.0	µA
I_{CORE}	Supply Current (Deep Sleep)	V_{CORE} = 1.1V, T_A = +25°C, f_{OSCIN} = 32kHz		TBD	TBD	µA
I_{RTC}	RTC Supply Current (Deep Sleep)	V_{RTC} = 2.0V, T_A = +25°C, f_{OSCIN} = 32kHz		TBD	TBD	µA
I_{CPRO}	Supply Current (Deep Sleep)	V_{CPRO} = 1.1V, T_A = +25°C, f_{OSCIN} = 32 kHz		TBD	TBD	µA
$C_{IN/OUT}$	Input/Output Pin Capacitance			TBD		pF
$C_{DPLUS/DMINUS}$	USB D+/D- Pin Capacitance				TBD	pF
C_{OSCIN}	OSCIN Pin Capacitance		TBD	TBD	TBD	pF
C_{OSCOUT}	OSCOUT Pin Capacitance		TBD	TBD	TBD	pF

ABSOLUTE MAXIMUM RATINGS[3]

Operating Temperature Range (Ambient) ..... -20°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature ..... +150°C

Voltage with Respect to Ground:
Power Supply Pins ..... -0.3V to ($Vpin^{[1]}_{max}$ + 0.3V)
Signal Pins ..... -0.3V to ($Vpin^{[1]}$ + 0.3V)
LFBGA (Mini-BGA) Q_{JA} Thermal Impedance ..... 60 °C/W

Lead temperature, Soldering:
Infrared (15 sec) ..... +235°C

Notes:
[1] Vpin refers to the supply voltage associated with a particular pin (see pin functionality table at the beginning of this document). For example, if a pin is driven by the V_{EXT} supply, then Vpin = V_{EXT}; $Vpin_{min}$ = V_{EXTmin} = 2.7 V; $Vpin_{max}$ = V_{EXTmax} = 3.3 V
[2] Guaranteed by design.
[3] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SUSCEPTIBILITY

CAUTION: The AD6905 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 Volts readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6905 chip features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING CHARACTERISTICS

System Clock Input

Note: All AC measurements made from the 50% point of signal transition.

Parameter	Comments	Min	Typ	Max	Unit
T_{CLKI_13}	13 MHz Input Clock Period		76.9		ns
T_{CLKI_26}	26 MHz Input Clock Period		38.45		ns
V_{CLK}	Input Clock Peak-to-Peak Amplitude	400		1300	mV

Table 1: System Clock Timing

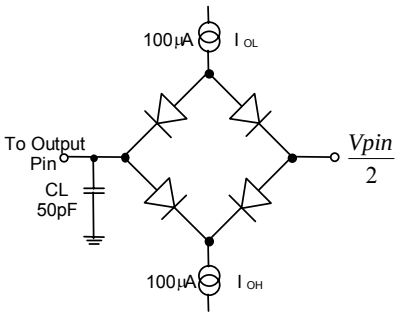


Figure 9: Load Circuit for Timing Specifications

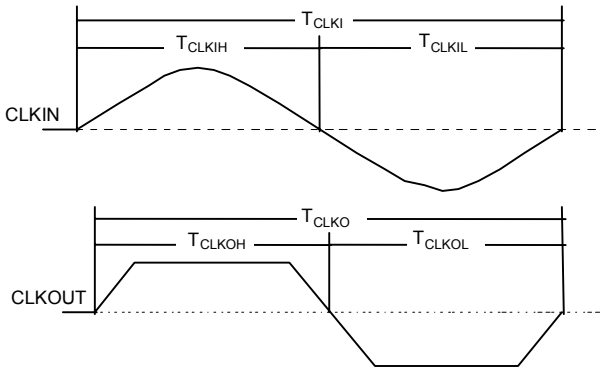


Figure 10: System Clock Timing

TIMING CHARACTERISTICS

RESET and CLKIN

Parameter	Comments	Min	Max	Unit
TdRST	RESET Active, Valid CLKIN	1000		Cycles

Table 2: RESET and CLKIN Timing

The System RESET is active low, and requires stable supply voltages and running input clock on CLKIN. The minimum active time is expressed in terms of 13MHz or 26MHz input clock cycles. After RESET, the start-up delay defines the period before the internal reset is released.

Figure 11: RESET and CLKIN Timing

TIMING CHARACTERISTICS

Asynchronous Memory Access

Table 3: Asynchronous Memory Access Times

NOTE: Access Times are listed as typical and are intended to provide general timing functionality, based on the type of access and number of Wait States. The unit of measure is BCLK periods.

Parameter	Comments	Min	Typ	Max	Unit
Taccess1[1][2]	32-bit Access to 16-bit Target		2 * (N + 1)		T_{clk}
Taccess2[1][2]	32-bit Access to 8-bit Target		4 * (N + 1)		T_{clk}
Taccess3[1][2]	16-bit Access to 16-bit Target		(N + 1)		T_{clk}
Taccess4[1][2]	16-bit Access to 8-bit Target		2 * (N + 1)		T_{clk}
Taccess5[1][2]	8-bit Access to 16-bit Target		(N + 1)		T_{clk}
Taccess6[1][2]	8-bit Access to 8-bit Target		(N + 1)		T_{clk}
Taccess7[1][2][3]	8 Half-Word (16-bit) Page Access		(N + 7M + 8)		T_{clk}
Taddr[1][2]	Address Valid Time		(N + 1)		T_{clk}

Table 4: EBUS Asynchronous Memory Access Timing

Parameter	Comments	Min	Typ	Max	Unit
TsARD[1]	Address Setup to nRD	0.5*Tclk – 2			ns
ThARD	Address Hold from nRD	-3.5			ns
TsCSRD	nCS Setup to nRD	0.5*Tclk - 4			ns
ThCSRD	nCS Hold from nRD	-3.5			ns
TwlRD	nRD Width Low	(N+0.5)*Tclk			ns
TwhRD	nRD Width High	0.5*Tclk - 3.5			ns
TsDi	Read Data Setup	8			ns
ThDi	Read Data Hold	0			ns
TsPDi	Read Data Setup to Address Change, Page Mode	7.5			ns
ThPDi	Read Data Hold from Address Change, Page Mode	0			ns
TsACS	Address Setup to nCS	-2.5			ns
TsAWE	Address Setup to nWE	0.5*Tclk – 2			ns
ThAWE	Address Hold from nWE	0.5*Tclk + 1			ns
TsCSWE	nCS Setup to nWE	0.5*Tclk - 3.5			ns
ThCSWE	nCS Hold from nWE	0.5*Tclk – 7			ns
TwlWE	nWE Width Low	N*Tclk - 1.5			ns
TwhWE	nWE Width High	Tclk			ns
TdDo	Write Data Delay			0.5	ns
ThWEDo	Write Data Hold from nWE	Tclk – 0.5			ns
ThBSDo	Write Data Hold from nLBS / nubs	0.5*Tclk-2.5			ns
ThACS	Address Hold from Chip Select	-2			ns
ThAUB	Address Hold from nUBS	-3.5			ns
ThALB	Address Hold from nLBS	-3.5			ns
TsADD	Address Setup to Data			(N+1)*Tclk – 4	ns
TsCSD	nCS Setup to Data			(N+1)*Tclk – 3	ns
TsRDD	nRD Setup to Data			(N+0.5)*Tclk – 3	ns
TsPADD	Address Setup to Data, during Page Access			(P+1)*Tclk – 4	ns
TdRDWE	Delay from nRD High to nWE Low	Tclk – 10			ns
TdWERD	Delay from new High to nRD Low	0.5*Tclk + 7			ns

Parameter	Comments	Min	Typ	Max	Unit
TsUBD	nUBS Setup to Data			(N+0.5)*Tclk – 2.5	ns
TsLBD	nLBS Setup to Data			(N+0.5)*Tclk – 2.5	ns
TwlUB	nUBS Width Low	(N+0.5)*Tclk			ns
TwlLB	nLBS Width Low	(N+0.5)*Tclk			ns
TwhUB	nUBS Width High	0.5*Tclk – 4			ns
TwhLB	nLBS Width High	0.5*Tclk – 4			ns
TsUBWE	nUBS Setup to nWE	-0.5			ns
TsLBWE	nLBS Setup to nWE	-0.5			ns
ThUBWE	nUBS Hold from nWE	0.5*Tclk + 0.5			ns
ThLBWE	nLBS Hold from nWE	0.5*Tclk + 0.5			ns
TsUBRD	nUBS Setup to nRD	-0.5			ns
TsLBRD	nLBS Setup to nRD	-0.5			ns
ThUBRD	nUBS Hold to nRD	-0.5			ns
ThLBRD	nLBS Hold to nRD	-1			ns

All timing characterization was performed with a BCLK frequency of 65 MHz with 1 extra wait state.

[1] Note: Tclk, in the above formulas, represents one BCLK period

[2] Note: a. N, in the above formulas, represents the total number of wait states ($N \geq 1$).
b. Each additional wait state adds one T_{clk} to the timing values shown.
(For example: If three (3) wait states are used, the calculation for Taccess1 is $8 * T_{clk}$.)

[3] Note: a. M, in the above formula, represents the number of page mode wait states (M = 0 or 1).
b. If M =0, then no wait states are added for the Q1 – Q7 accesses. If M = 1, then one wait state is added for the Q1 – Q7 accesses. N defines the wait state for the Q0 access.

[4] Note: P represents number of page wait states inserted

TIMING CHARACTERISTICS

Burst Flash Interface

Table 5: EBUS Burst NOR Read Timing

Parameters	Comments	Min	Typ	Max	Unit
TCLK	BURSTCLK cycle time		15.38		ns
TsDCLK	Data in setup to Burst Clock Active edge	7.5			ns
ThDCLK	Data in hold from Burst Clock Active edge	0			ns
TsWCLK	nWAIT high/low setup to Burst Clock Active edge	8.5			ns
ThWCLK	nWAIT high/low hold from Burst Clock Active edge	0			ns
TsACLK	Address setup to Burst Clock Active edge	Tclk - 3			ns
ThACLK	Address hold to Burst Clock Active edge	0.5			ns
TsADVCLK	nADV setup to Burst Clock Active edge	0.5 * Tclk - 3			ns
TwlADV	nADV low width	Tclk - 1			ns
TsCSADV	nCS low setup to nADV high	1.5 * Tclk - 3			ns
TsCSCLK	nCS low setup to Burst Clock Active edge	Tclk - 5			ns
ThCSCLK	nCS low hold to Burst Clock Active edge	2			ns
TsRDCLK	nRD low setup to Burst Clock Active edge	0.5 * Tclk - 3			ns
ThRDCLK	nRD low hold to Burst Clock Active edge	0.5			ns
TsBSCLK	nUB/nLB low setup to Burst Clock Active edge	0.5 * Tclk - 3			ns
ThBSCLK	nUB/nLB low hold to Burst Clock Active edge	0.5			ns
TdCSW	nCS low setup to nWait low	Tclk - 14			ns

TIMING CHARACTERISTICS

Burst PSRAM Interface

Table 6: EBUS PSRAM Burst Read Timing

Parameters	Comments	Min	Typ	Max	Unit
TCLK	Burst Clock cycle time		15.38		ns
TsDCLK	Data in setup to Burst Clock Active edge	7.5			ns
ThDCLK	Data in hold from Burst Clock Active edge	0			ns
TsWCLK	nWAIT high/low setup to Burst Clock Active edge	7.5			ns
ThWCLK	nWAIT high/low hold from Burst Clock Active edge	0			ns
TsACLK	Address setup to Burst Clock Active edge	Tclk - 4			ns
ThACLK	Address hold to Burst Clock Active edge	1			ns
TsADVCLK	nADV setup to Burst Clock Active edge	0.5 * Tclk - 3.5			ns
TwlADV	nADV low width	Tclk - 0.5			ns
TsCSADV	nCS low setup to nADV high	1.5 * Tclk - 3			ns
TsCSCLK	nCS low setup to Burst Clock Active edge	Tclk - 5.5			ns
ThCSCLK	nCS low hold to Burst Clock Active edge	2			ns
TsRDCLK	nRD low setup to Burst Clock Active edge	0.5 * Tclk - 3			ns
ThRDCLK	nRD low hold to Burst Clock Active edge	1			ns
TsBSCLK	nUB/nLB low setup to Burst Clock Active edge	0.5 * Tclk - 3			ns
ThBSCLK	nUB/nLB low hold to Burst Clock Active edge	1			ns
TdCSW	nCS low setup to nWait low	Tclk - 14			ns

TIMING CHARACTERISTICS

Burst Flash Interface

Table 7: EBUS PSRAM Burst Write Timing

Parameters	Comments	Min	Typ	Max	Unit
TCLK	Burst Clock cycle time		15.38		ns
TsWCLK	nWAIT low setup to Burst Clock Active edge	7.5			ns
ThWCLK	nWAIT high hold from Burst Clock Active edge	0			ns
TsACLK	Address setup to Burst Clock Active edge	Tclk - 3			ns
ThACLK	Address hold to Burst Clock Active edge	1			ns
TsADVCLK	nADV setup to Burst Clock Active edge	0.5 * Tclk - 3.5			ns
ThADVCLK	nADVlow hold to Burst Clock Active edge	Tclk - 7			ns
TwlADV	nADV low width	Tclk - 1			ns
TsCSADV	nCS low setup to nADV high	1.5 * Tclk - 3			ns
TsCSCLK	nCS low setup to Burst Clock Active edge	Tclk - 5.5			ns
ThCSCLK	nCS low hold to Burst Clock Active edge	0.5 * Tclk + 2.5			ns
TsWECLK	nWE low setup to Burst Clock Active edge	0.5 * Tclk - 3.5			ns
ThWECLK	nWE low hold to Burst Clock Active edge	0.5 * Tclk + 1			ns
TsBSCLK	nUB/nLB low setup to Burst Clock Active edge	0.5 * Tclk - 3.5			ns
ThBSCLK	nUB/nLB low hold to Burst Clock Active edge	0.5 * Tclk + 1			ns
TsDCLK	Output Data setup to Burst Clock Active edge	0.5 * Tclk + 1.5			ns
ThDCLK	Output Data hold from Burst Clock Active edge	0.5 * Tclk + 1			ns

TIMING CHARACTERISTICS

NAND Flash Interface

Table 8: NAND Interface Timing

Parameter	Comments	Min	Typ*	Max	Unit
TsDRD	nRD Setup to Data	7			ns
ThDRD	Data Hold from nRD	0			ns
TdNCSW	nWE low delay to nNDCS negative edge			Tclk+3.5	ns
ThNCSW	nNDCS low hold to nWE positive edge	2*Tclk – 1.5			ns
TdCLW	nWE low delay to CLE valid edge			0.5*Tclk+0.5	ns
ThCLW	CLE hold to nWE positive edge	0.5*Tclk			ns
TdALW	nWE low delay to ALE valid edge			1.5*Tclk – 1	ns
ThALW	ALE hold to nWE positive edge	2.5*Tclk+1.5			ns
TdDWE	Data valid delay to nWE negative edge			0.5*Tclk+2	ns
ThDWE	Data hold to nWE negative edge			0.5*Tclk+2	ns
TdNCSR	nRD low delay to nNDCS negative edge			Tclk+0.5	ns
ThNCSR	nNDCS low hold to nRD positive edge	2*Tclk+0.5			ns
TdALR	nRD low delay to ALE valid edge			1.5*Tclk – 1	ns
TdCLR	nRD low delay to CLE valid edge			1.5*Tclk – 1	ns

TIMING CHARACTERISTICS

Table 9: SDRAM Timing

Parameter	Comments	Min	Typ	Max	Unit
TwSDCLK	SDCLK Cycle Time		7.69		ns
TwSDCLKl	SDCLK low pulse width		3.8		ns
TwSDCLKh	SDCLK high pulse width		3.8		ns
TsSDDin*	Data setup to SDCLK positive edge	TBD			ns
ThSDDin*	Data hold to SDCLK positive edge	TBD			ns
TdSDCS	nSDCS low output delay to SDCLK positive edge	TBD		TBD	ns
ThSDCS	nSDCS low hold to SDCLK positive edge	TBD			ns
TdSDRAS	nSDRAS low output delay to SDCLK postive edge	TBD		TBD	ns
ThSDRAS	nSDRAS low hold to SDCLK postive edge	TBD			ns
TdSDCAS	nSDCAS low output delay to SDCLK positive edge	TBD		TBD	ns
ThSDCAS	nSDCAS low hold to SDCLK positive edge	TBD			ns
TdSDADD	ADDR[16:1] valid output delay to SDCLK positive edge	TBD		TBD	ns
ThSDADD	ADDR[16:1] valid hold to SDCLK positive edge	TBD			ns
TdSDBK	ADDR[19:18] valid output delay to SDCLK positive edge	TBD		TBD	ns
ThSDBK	ADDR[19:18] valid hold to SDCLK positive edge	TBD			ns
TdSDA10	SDA10 valid output delay to SDCLK positive edge	TBD		TBD	ns
ThSDA10	SDA10 valid hold to SDCLK positive edge	TBD			ns
TdSDWE	nSDWE valid output delay to SDCLK positive edge	TBD		TBD	ns
ThSDWE	nSDWE low hold to SDCLK positive edge	TBD			ns
TdSDDout	DTAT[15:0] valid output delay to SDCLK positive edge	TBD		TBD	ns
ThSDDout	DTAT[15:0] valid output hold to SDCLK positive edge	TBD			ns
TdSDCKE	nSDCKE output delay to SDCLK positive edge	TBD		TBD	ns
ThSDCKE	nSDCKE valid hold to SDCLK positive edge	TBD			ns

*TsSDDin, ThSDDin are characterized for different values of SDCLKDLY as V_{CORE} varies:

Table 10: V_{CORE} vs SDCLKDLY

V_{CORE} (V)	SDC_SDCLKDLY Register
1.2	0x5F5
1.3	0x5F6
1.4	0x5F7
1.5	0x5F8

TIMING CHARACTERISTICS

32-bit Access, 16-bit Target, One Wait State

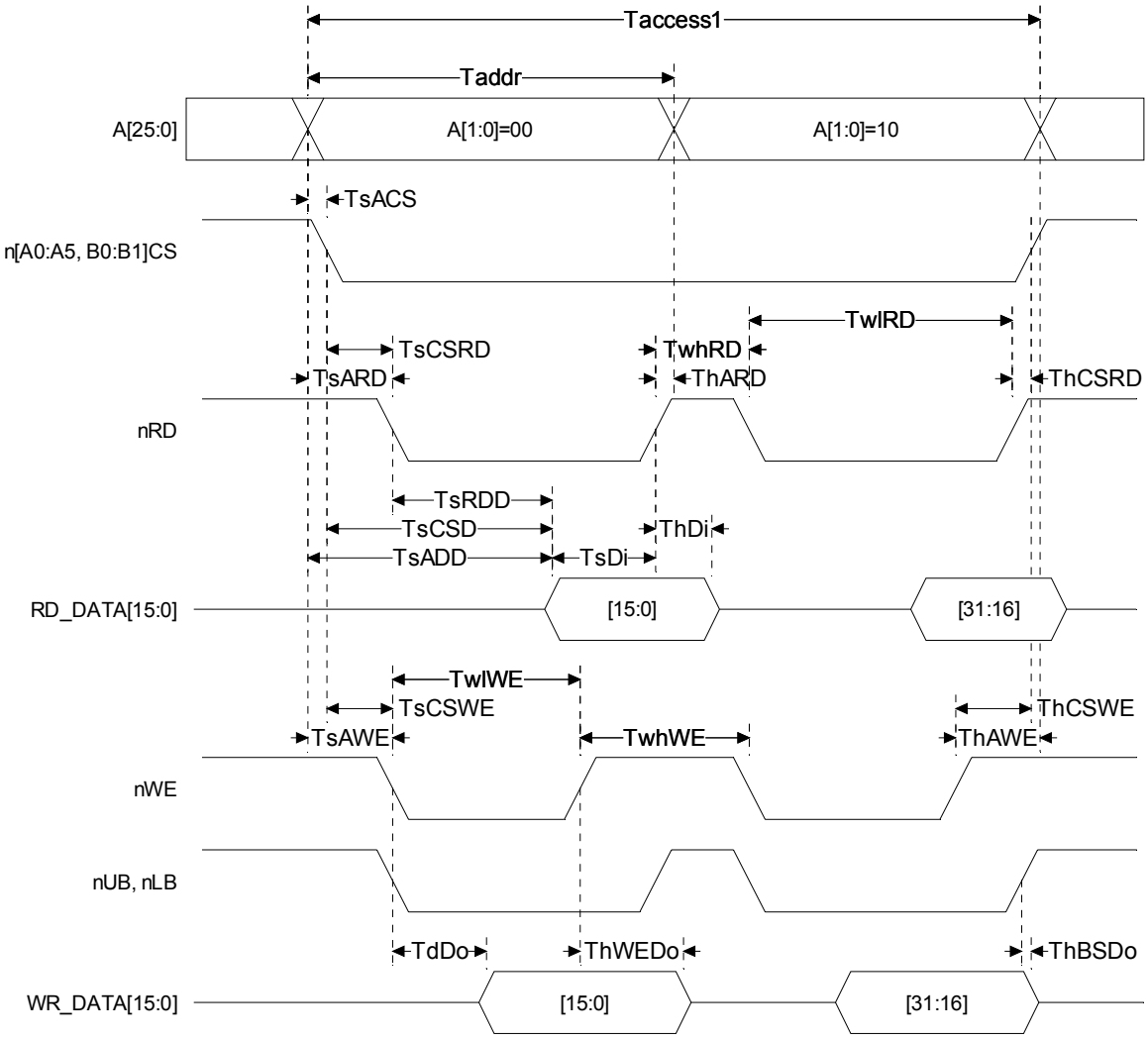
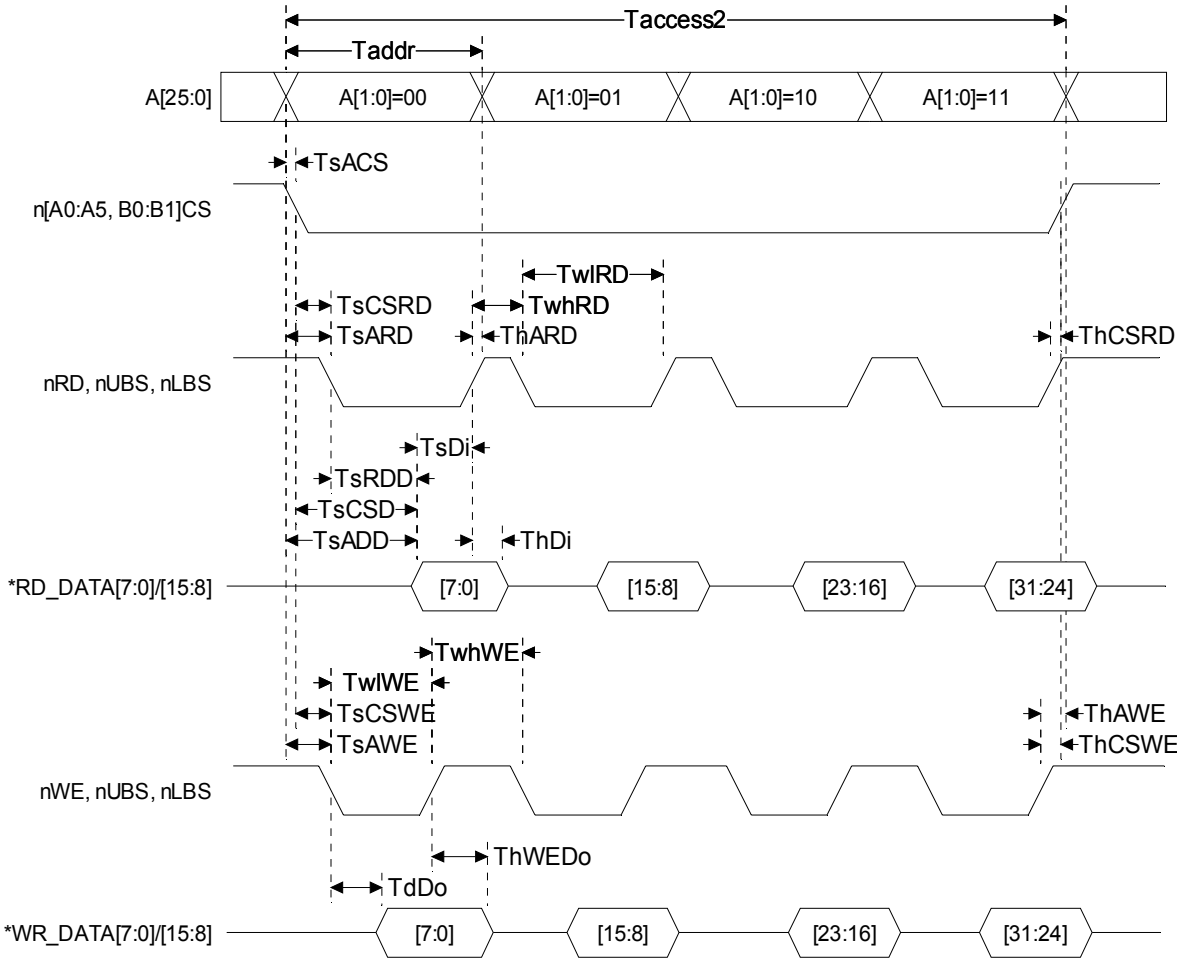


Figure 12: 32-bit Access, 16-bit Target, One Wait State

TIMING CHARACTERISTICS

32-bit Access, 8-bit Target, One Wait State



*For an 8-bit targe, the unused byte as defined by the Location Byte flag,
Will be driven with the last latched value for both read and write access.

Figure 13: 32-bit Access, 8-bit Target, One Wait State

*** NOTE:** Programming options in the EBUS Arbiter allow for 8-bit data reads and writes to be selected for DATA[7:0] or DATA[15:8] on the AD6905 Memory Interface. For 8-bit reads and writes, the unused byte will be driven with the last latched value. Since the DATA[15:0] pads contain bus holders, there will be no transition on tristating.

TIMING CHARACTERISTICS

16-bit Access, 16-bit Target, One Wait State

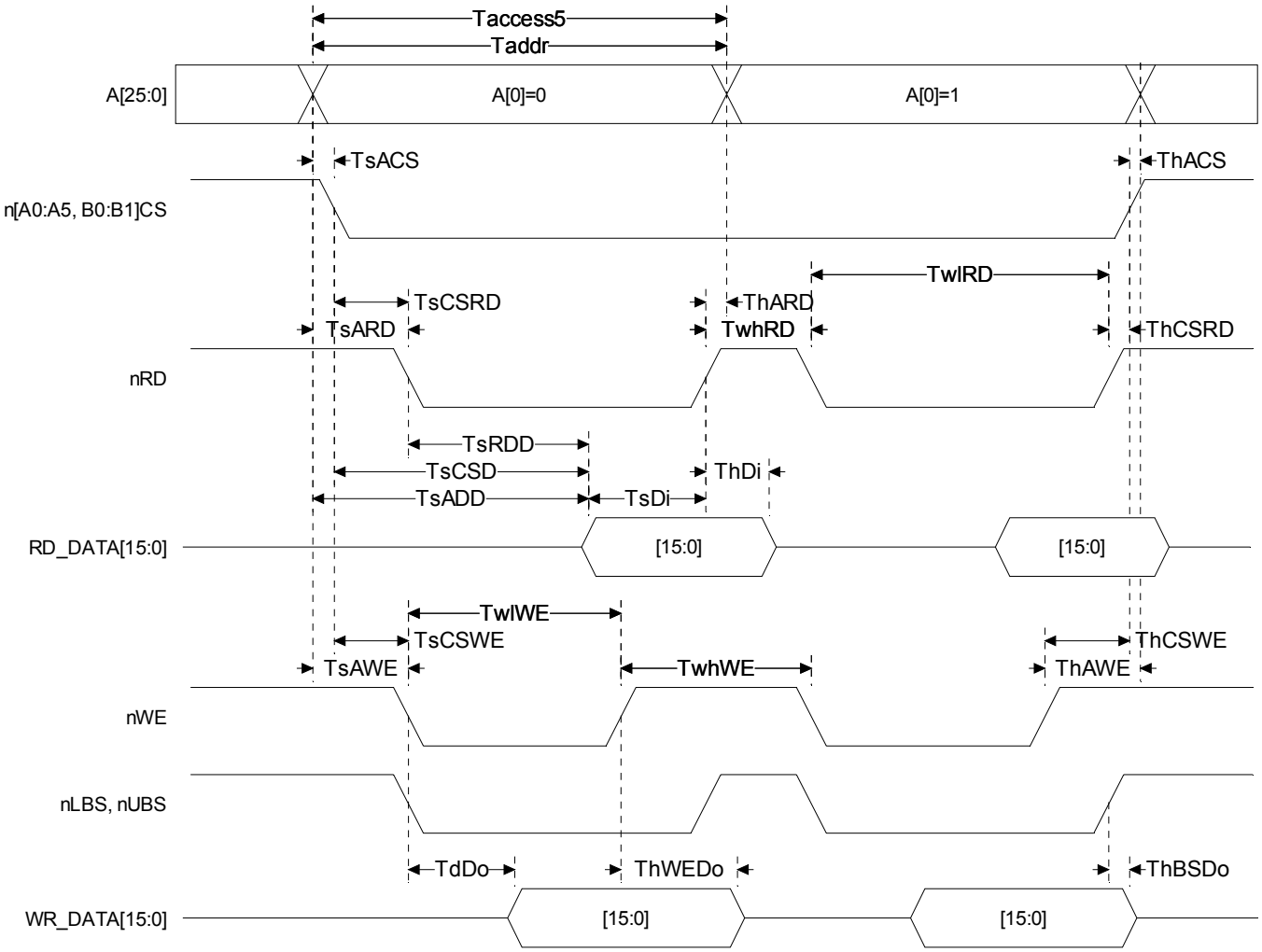
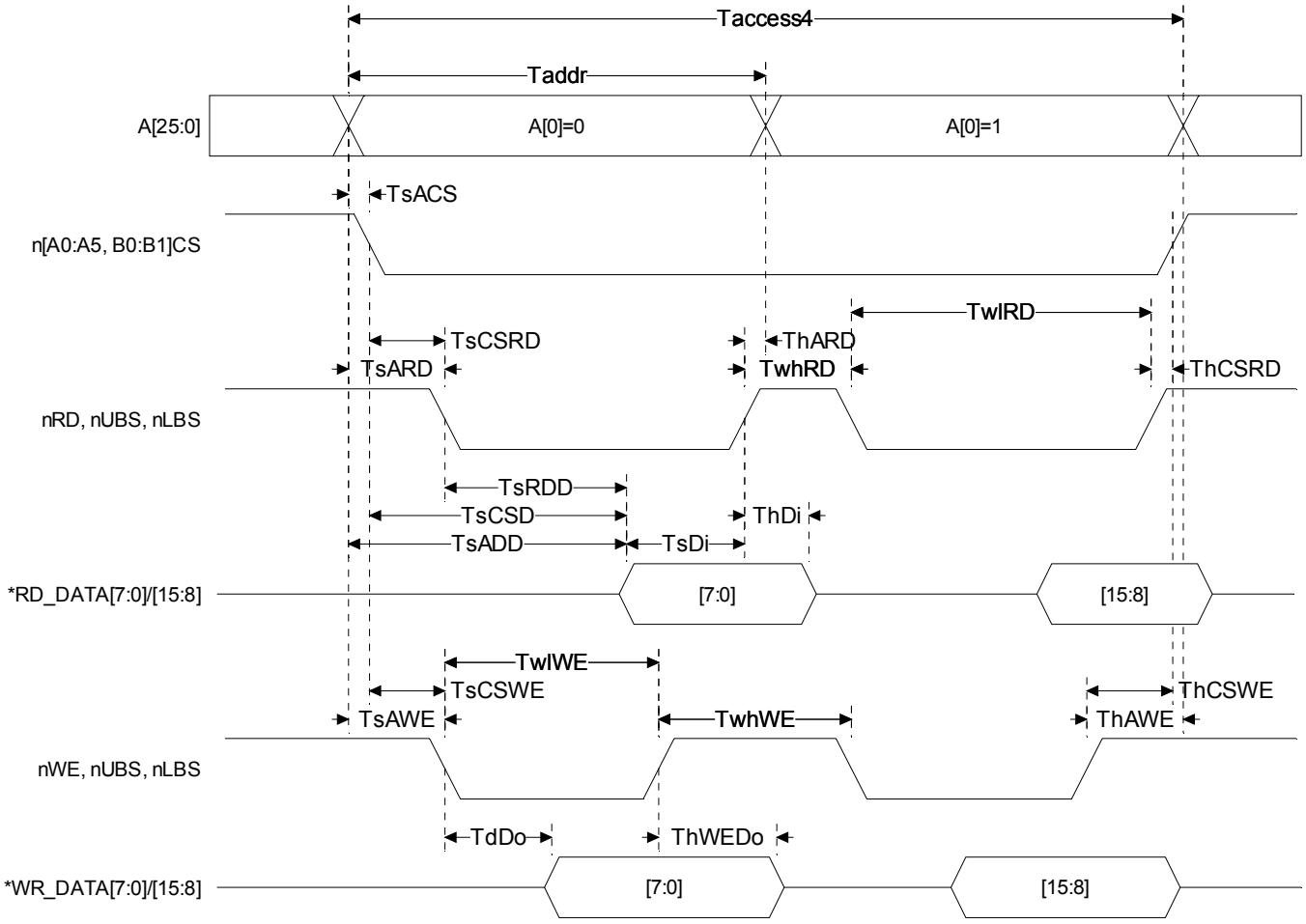


Figure 14: 16-bit Access, 16-bit Target, One Wait State

TIMING CHARACTERISTICS

16-bit Access, 8-bit Target, One Wait State



*For an 8-bit targe, the unused byte as defined by the Location Byte flag,
Will be driven with the last latched value for both read and write access.

Figure 15: 16-bit Access, 8-bit Target, One Wait State

*** NOTE:** Programming options in the EBUS Arbiter allow for 8-bit data reads and writes to be selected for DATA[7:0] or DATA[15:8] on the AD6905 Memory Interface. For 8-bit reads and writes, the unused byte will be driven with the last latched value. Since the DATA[15:0] pads contain bus holders, there will be no transition on tri-stating.

TIMING CHARACTERISTICS

8-bit Access, 16-bit Target, One Wait State

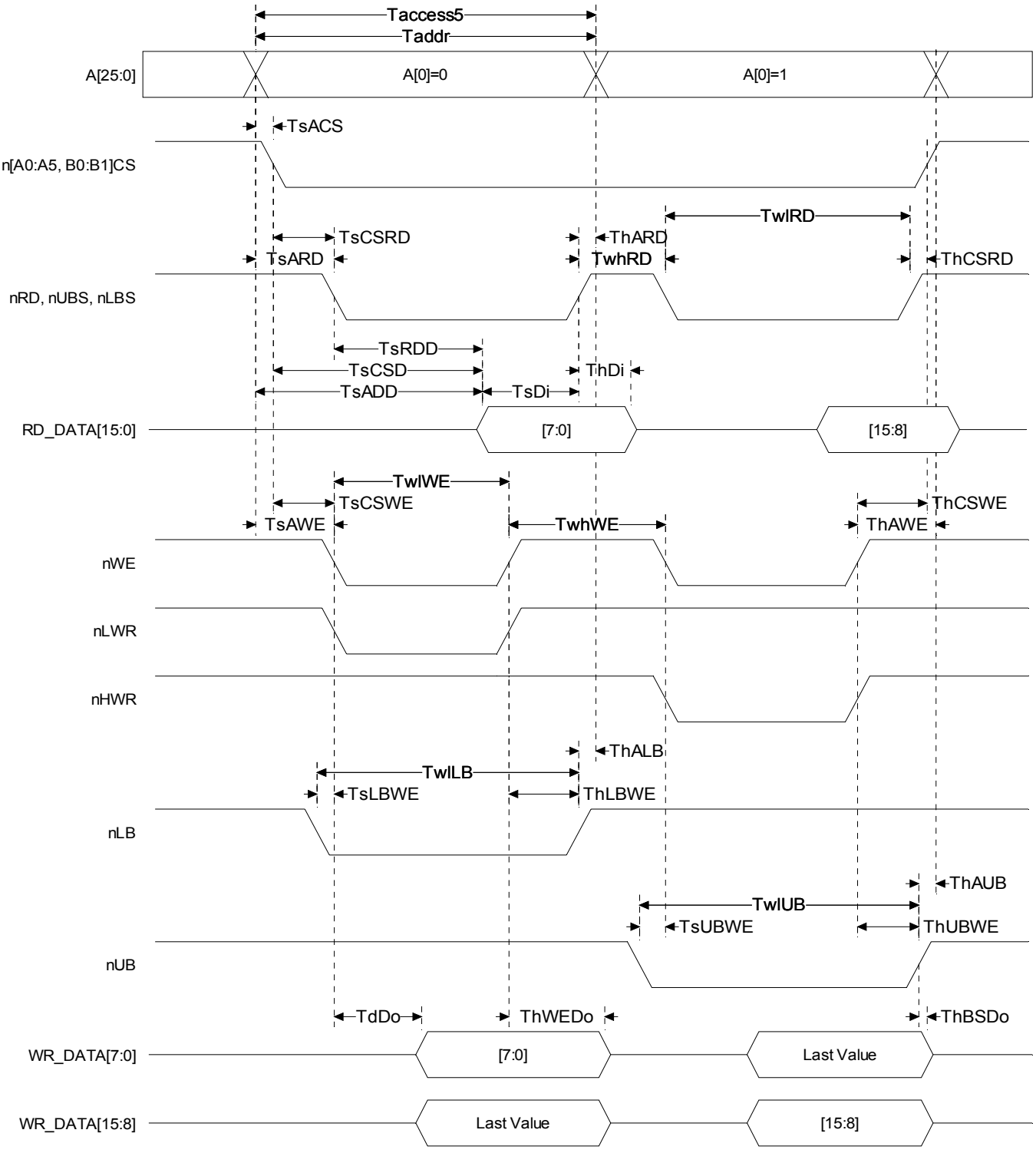
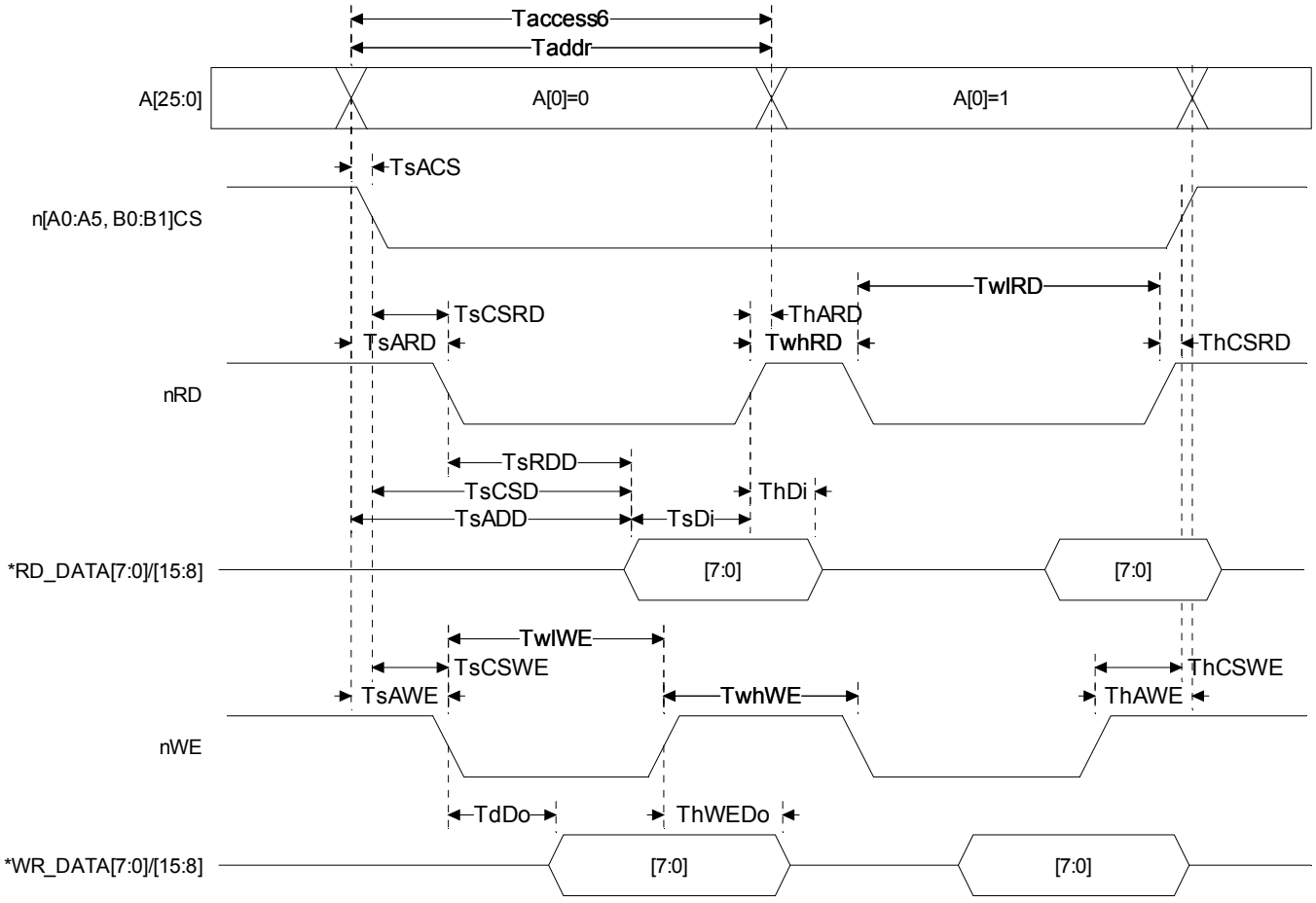


Figure 16: 8-bit Access, 16-bit Target, One Wait State

*** NOTE:** For a read cycle, the full Data [15:0] is expected to be driven, though only either Data [7:0] or Data [15:0] is used.

TIMING CHARACTERISTICS

8-bit Access, 8-bit Target, One Wait State



*For an 8-bit targe, the unused byte as defined by the Location Byte flag,
Will be driven with the last latched value for both read and write access.

Figure 17: 8-bit Access, 8-bit Target, One Wait State

*** NOTE:** Programming options in the EBUS Arbiter allow for 8-bit data reads and writes to be selected for DATA[7:0] or DATA[15:8] on the AD6905 Memory Interface. For 8-bit reads and writes, the unused byte will be driven with the last latched value. Since the DATA[15:0] pads contain bus holders, there will be no transition on tri-stating.

TIMING CHARACTERISTICS

Read→Write and Write→Read, One Wait State

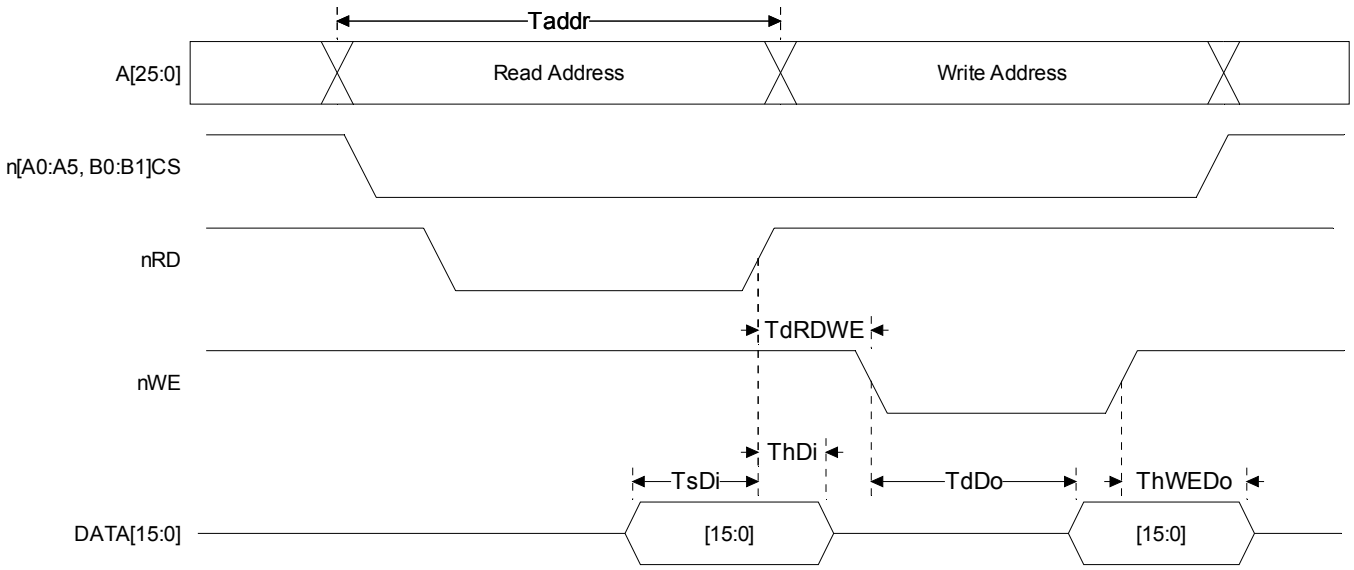


Figure 18: Read → Write Turnaround, One Wait State

TIMING CHARACTERISTICS

8 Half-Word (16-bit) Page Access

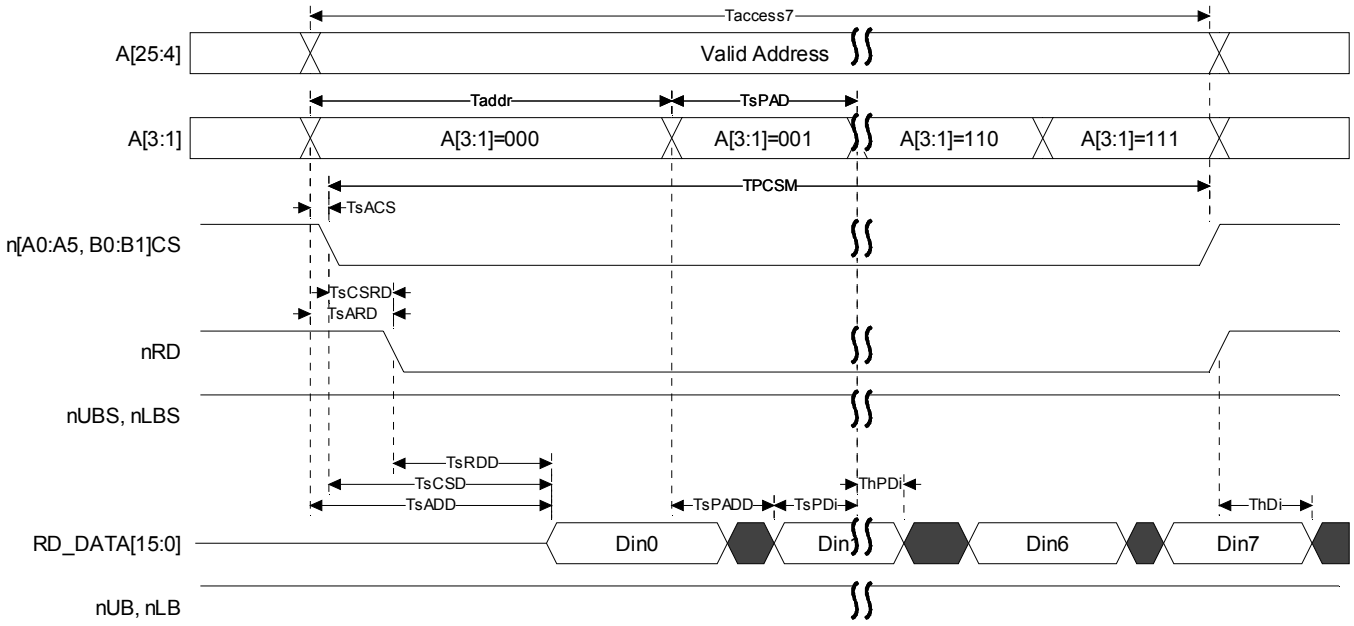


Figure 19: 8 Half-Word (16-bit) Asynchronous Page Mode Read

NOTE: The timing shown above assumes all accesses occur on the same page. The initial access of a new page always follows the timing shown for Q0.

TIMING CHARACTERISTICS

Synchronous Burst Read Access

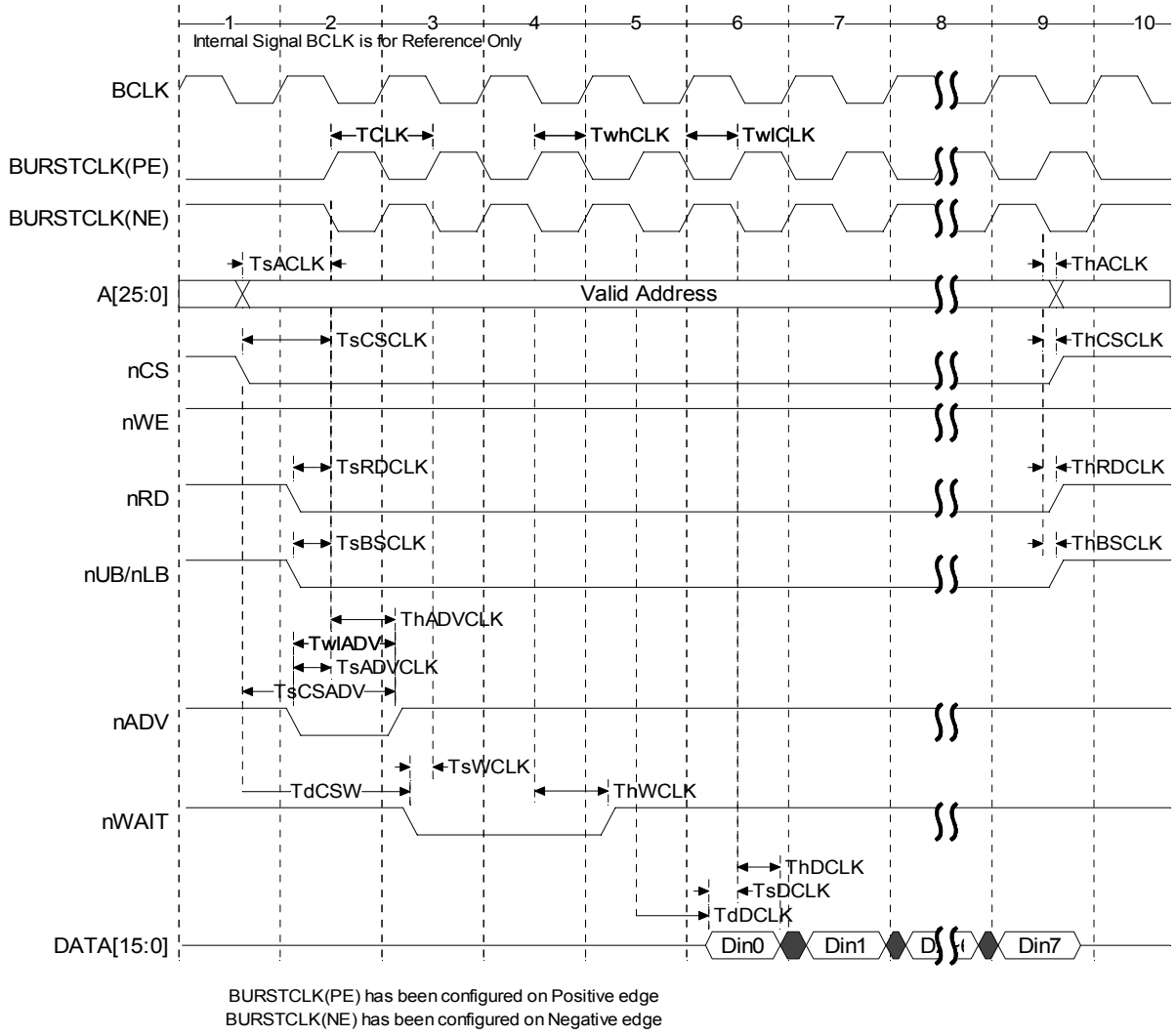


Figure 20: Synchronous Burst Read

TIMING CHARACTERISTICS

Synchronous Burst Write Access

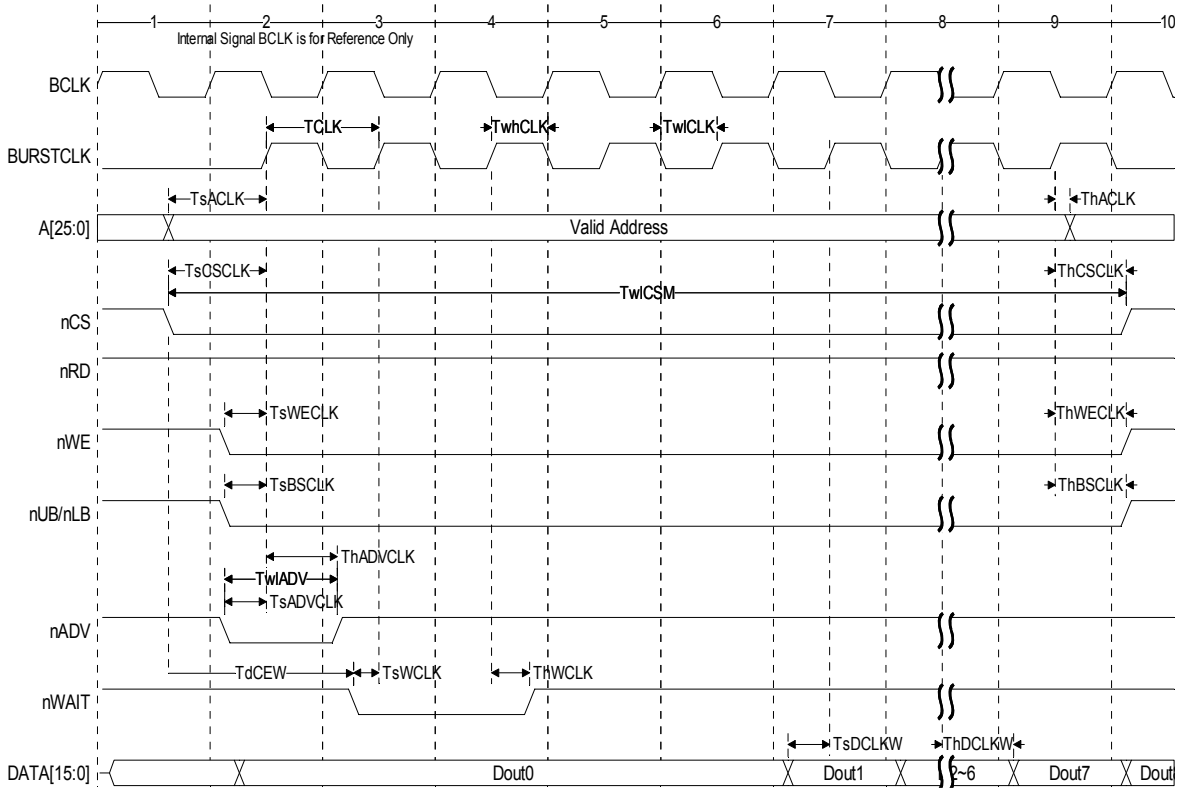


Figure 21: Synchronous Burst Write Access

TIMING CHARACTERISTICS

NAND Timing

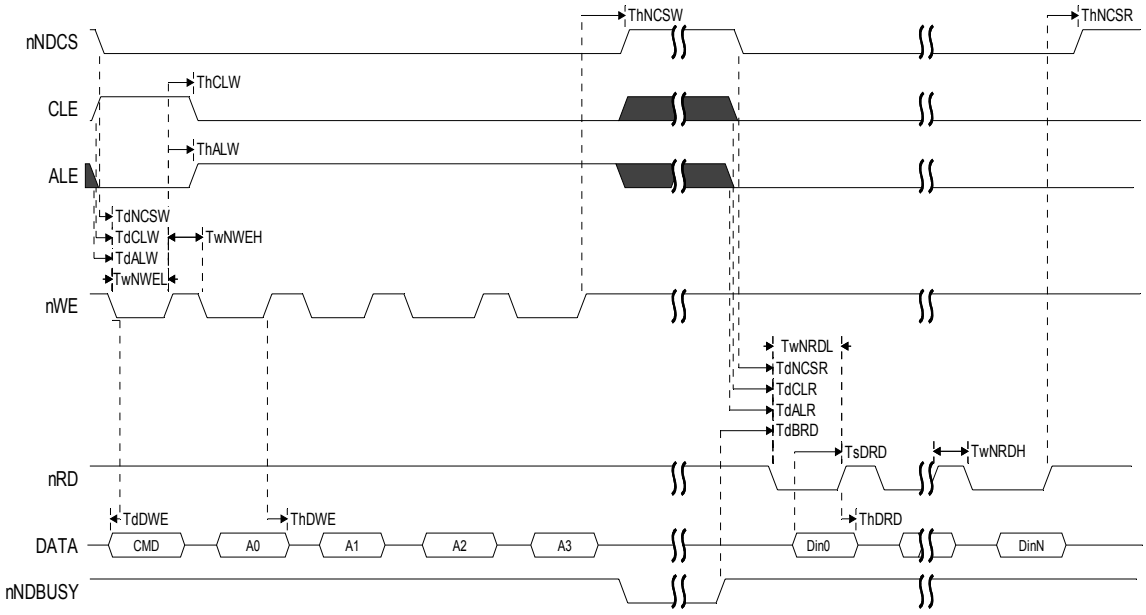


Figure 22: NAND Timing

Note: nNDBUSY is asynchronous and must be processed by software to begin a read cycle.

TIMING CHARACTERISTICS

SDRAM Read Timing

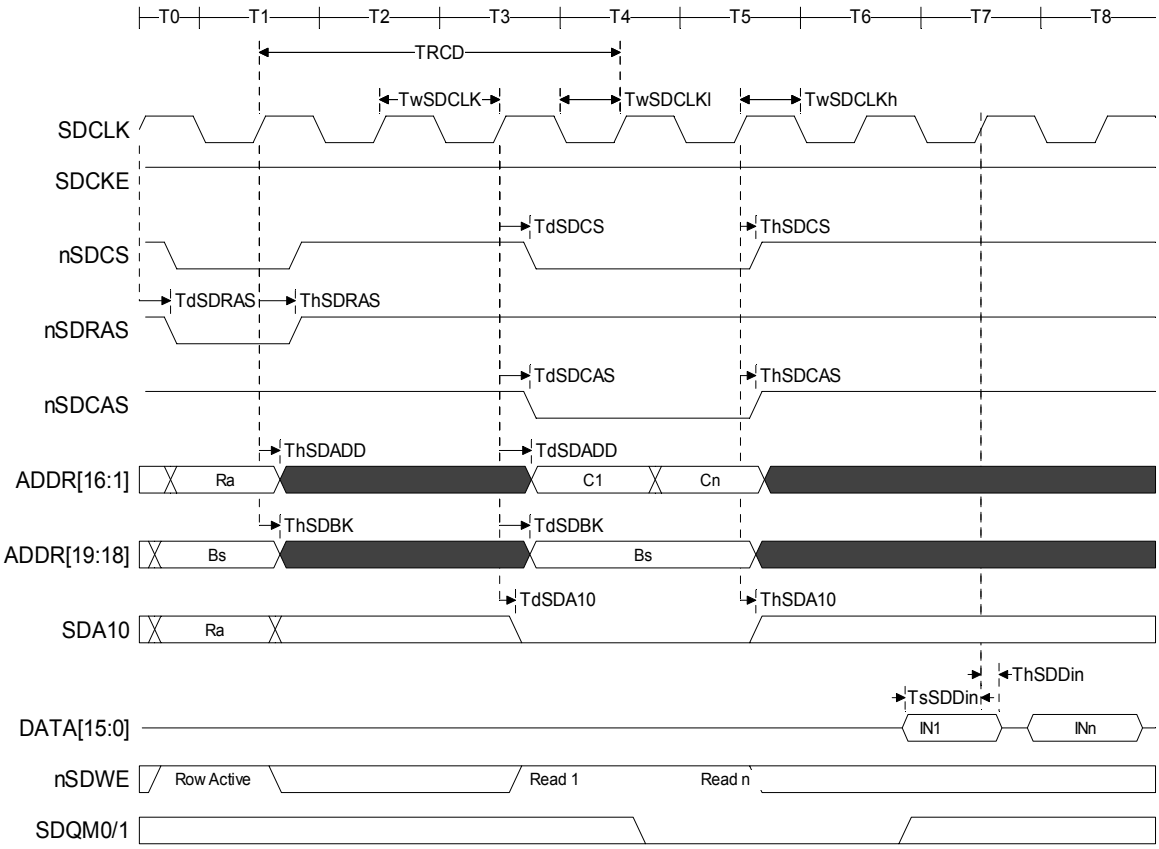


Figure 23: SDRAM Read Timing

TIMING CHARACTERISTICS

SDRAM Write Timing

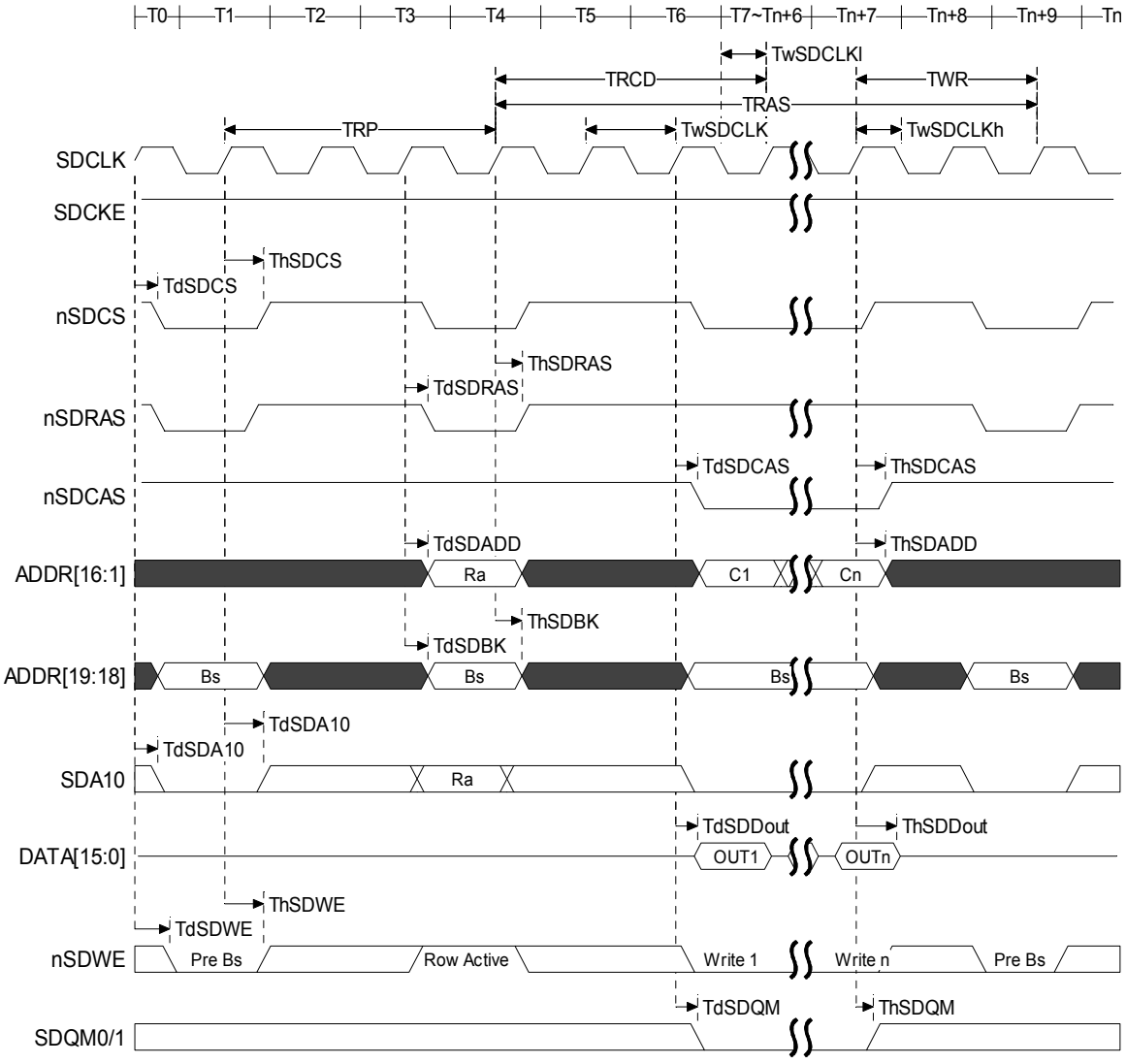


Figure 24: SDRAM Write Timing

TIMING CHARACTERISTICS

SDRAM Exit/Self-Refresh Timing

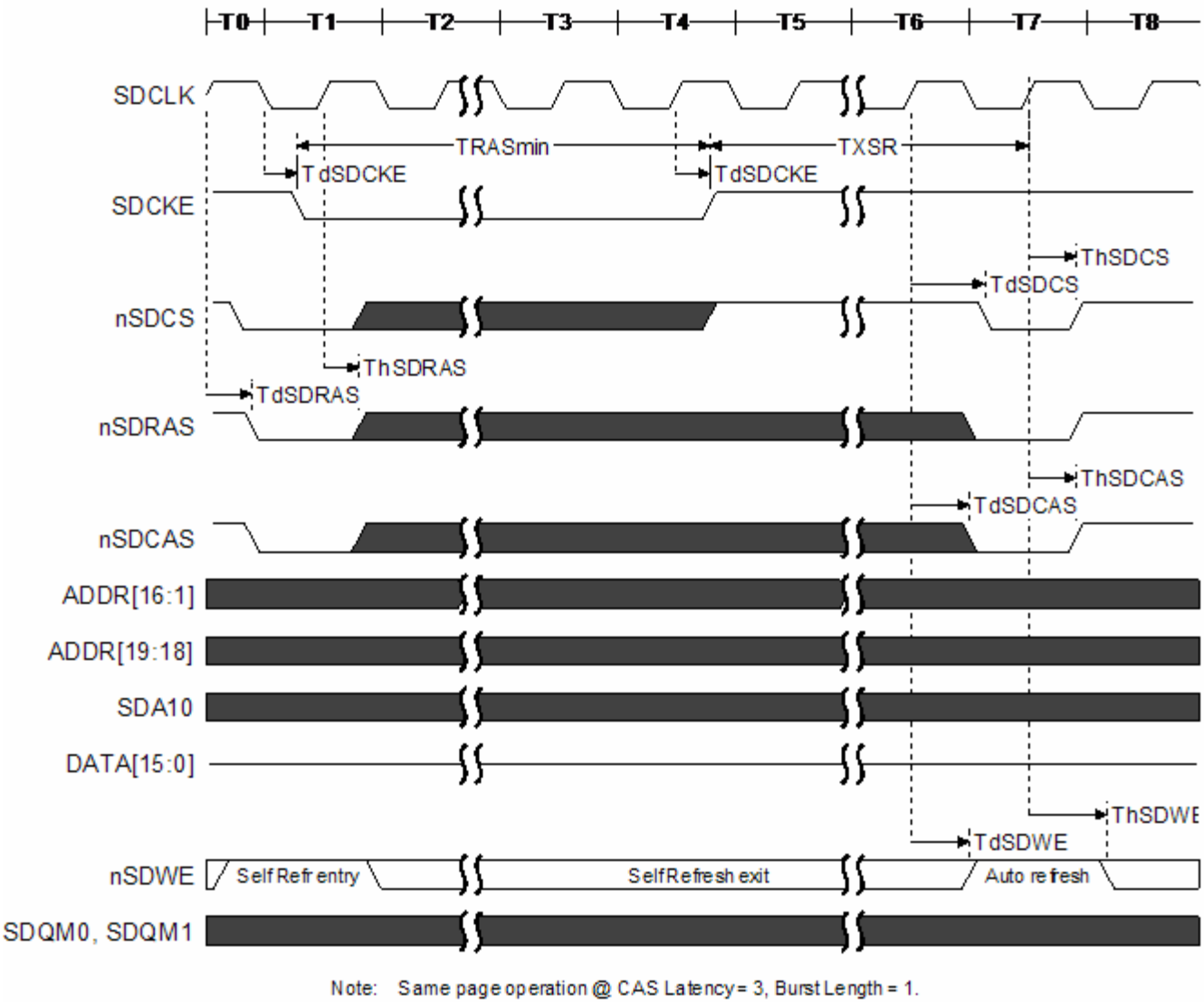


Figure 25: SDRAM Exit/Self-Refresh Timing

TIMING CHARACTERISTICS

EBUS2 Timing

Table 11: EBUS2 Timing

Parameters	Comments	Min	Typ	Max	Unit
TcycR	Display Access Cycle Time (Read)		(q+1)		
TcycW	Display Access Cycle Time (Write)		(p+1)		
TsRDDi	Read Data Setup to nRD	18			ns
ThRDDi	Read Data Hold to nRD	1			ns
TwlWE	nWE Width Low	p*Tclk – 1			ns
TwhWE	nWE Width High	p*Tclk – 1			ns
TwlRD	nRD Width Low	(q+0.5)*Tclk+1			ns
TwhRD	nRD Width High	(q+0.5)*Tclk – 4			ns
TsAWE	Address Setup to nWE	0.5*Tclk – 5			ns
TdWEDo	Write Data Delay to nWE			1	ns
TsCSWE	nCS Setup to nWE	0.5*Tclk – 5			ns
ThCSWE	nCS Hold from nWE	0.5*Tclk – 2.5			ns
ThWEDo	Write Data Hold to nWE	p*Tclk – 1.5			ns
TsARD	Address Setup to nRD	0.5*Tclk – 3			ns
TsCSRD	nCS Setup to nRD	0.5*Tclk – 3			ns

Note: ‘p’ and ‘q’ represent the number of wait states for read and write access, respectively

TIMING CHARACTERISTICS

CSPORT Interface

Table 12: CSPORT Timing

Parameter	Comments	Min	Typ	Max	Unit
Tclk	CLKOUT Clock Period		76.9		ns
TdFS	CSFS Delay from CLKOUT			10	ns
TwFS	CSFS Width	Tclk - 2		Tclk + 2	ns
TdDo	CSDO Output Delay			10	ns
TsDi	CSDI Input Setup	17			ns
ThDi	CSDI Input Hold	0			ns

The Data format consists of 10-bit Data (D[9:0]), followed by a 6-bit Address (A[5:0]). CSDO is driven off the CLKOUT rising edge, CSDI is sampled off the falling edge. During a read sequence the CSDO output is high.

The CSPORT automatically enables CLKOUT at the start of the transfer, which is halted low at the end of the transfer. CSDI data is sampled during TX if A[5:0] on the previous Tx was 0x1F.

CSDO and CSDI are invalid outside the active CSFS Frame Sync. CSFS is active one CLKOUT cycle before serial data transfer.

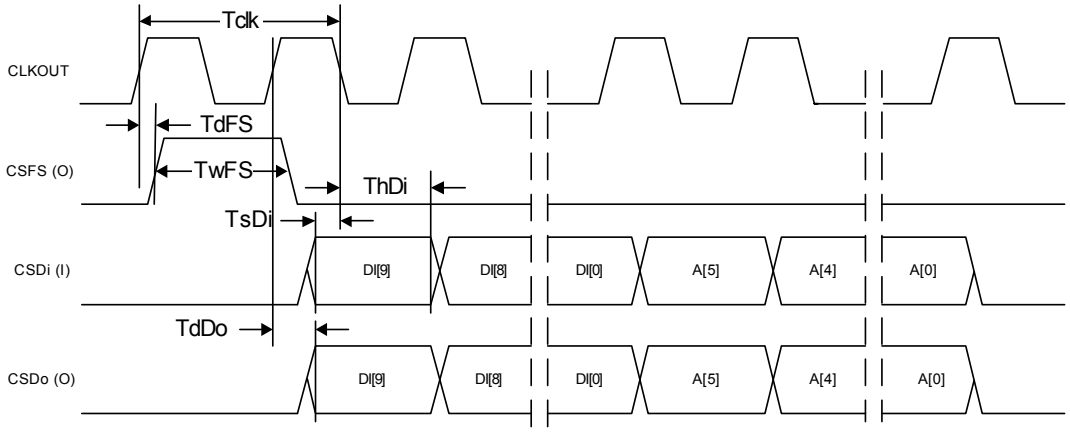


Figure 26: CSPORT Timing

TIMING CHARACTERISTICS

BSPORT Interface

Table 13: BSPORT Timing

Parameter	Comments	Min	Typ	Max	Unit
Tclk	BSCLK Clock Period		76.9		ns
TsIFS	BSIFS Setup	17			ns
ThIFS	BSIFS Hold	0			ns
TsDI	BSDI Input Setup	17			ns
ThDI	BSDI Input Hold	0			ns
TsOFS	BSOFS Input Setup	17			ns
ThOFS	BSOFS Input Hold	0			ns
TdDO	BSDO Output Delay			10	ns

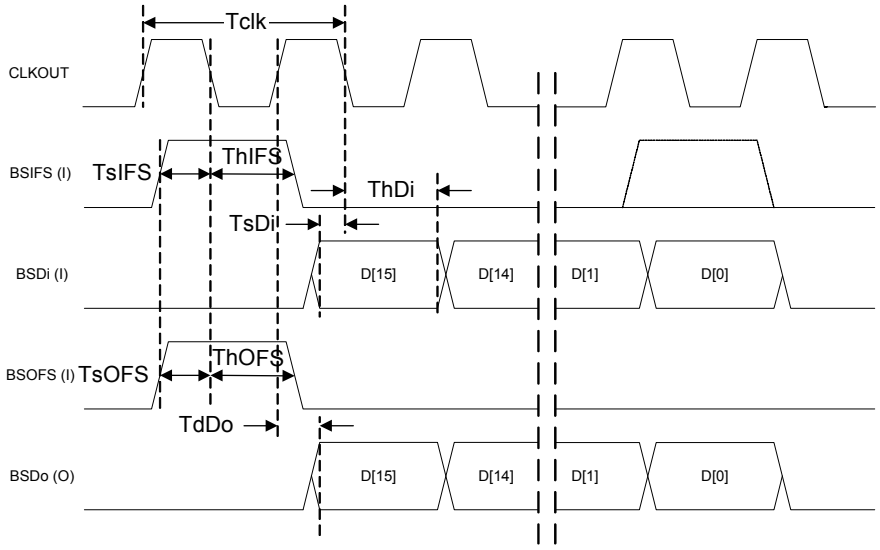


Figure 27: BSPORT Timing

TIMING CHARACTERISTICS

ASPORT Interface

Table 14: ASPORT Timing

Parameter	Comments	Min	Typ	Max	Unit
Tclk	ASCLK Clock Period		76.9		ns
TsFS	ASFS Setup	17			ns
ThFS	ASFS Hold	0			ns
TsDI	ASDI Input Setup	17			ns
ThDI	ASDI Input Hold	0			ns
TdDO	ASDO Output Delay			10	ns

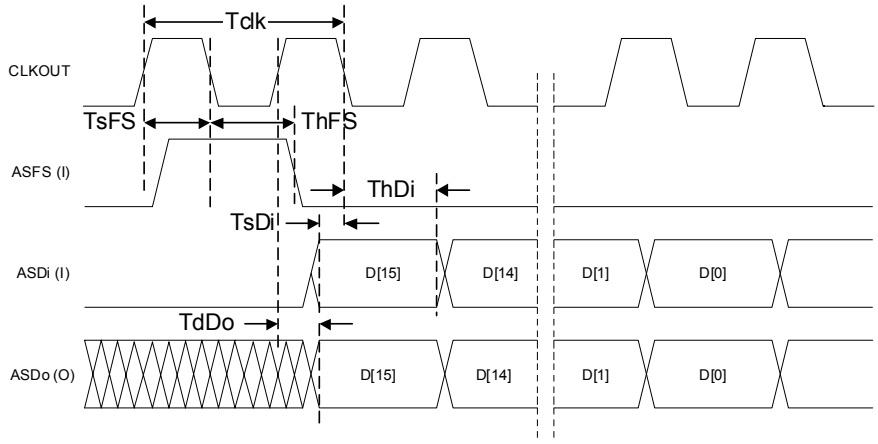


Figure 28: ASPORT Timing

TIMING CHARACTERISTICS

WSPORT Interface

Table 15: WSPORT Timing

Parameter	Comments	Min	Typ	Max	Unit
Tclk	UCLK Clock Period		32.5		ns
TsWDDx	WDDI, WDDQ Input Setup	0			ns
ThWDDx	WDDI, WDDQ Input Hold	1			ns
TdWUDx	WUDI, WUDQ Output Delay			17	ns

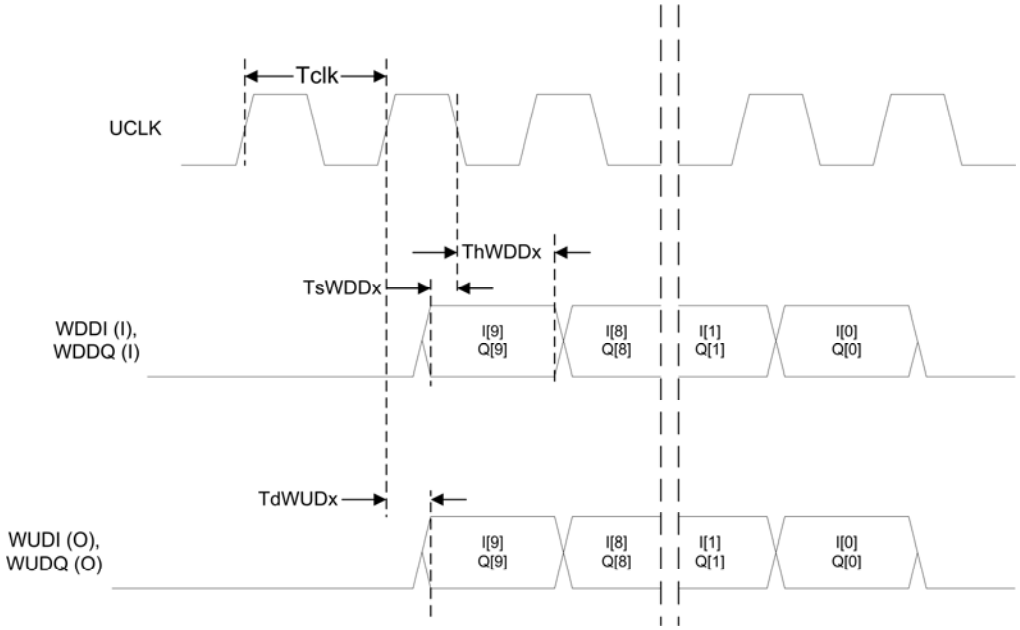


Figure 29: WSPORT Timing

TIMING CHARACTERISTICS

Table 16: AC Characteristics

Parameter	Symbols	Min	Typ	Max	Unit	Notes
Rise Time – Full Speed USB	Tr	4		20	ns	10% to 90%
Fall Time – Full Speed USB	Tf	4		20	ns	10% to 90%
Rise/Fall Matching	Tr/Tf	90		111	%	

Table 17: USB DC Characteristics

Parameter	Symbols	Min	Typ	Max	Unit	Notes
Differential Output Crossover Voltage	Vcrs	1.3		2.0	V	
Driver Output Resistance [1]	Zdrv		10		Ω	

Notes:
[1] In order to comply with the USB 2.0 specification, external series resistors of 27 Ω +/-1% are recommended for both D+ and D-.

The USB characteristic values are guaranteed by design, not tested in production.

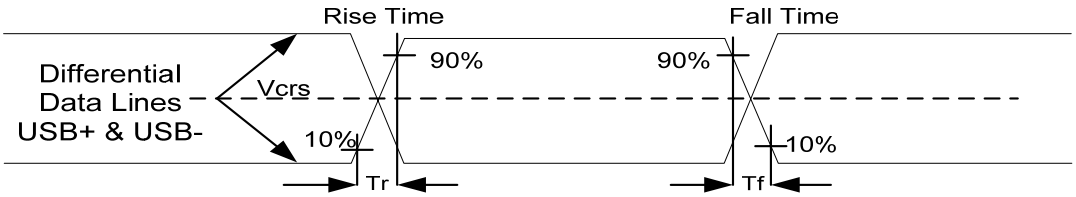


Figure 30: USB Interface Timing Waveforms – USB D+ and D-

TIMING CHARACTERISTICS

Parallel Port Interface (PPI)

Table 18: PPI Timing

Parameter	Comments	Min	Typ	Max	Unit
T_{CLK}	PPI_CLK Clock Period	30.77			ns
Ts_{VS}	PPI_VSYNC Setup	1			ns
Th_{VS}	PPI_VSYNC Hold	1			ns
Ts_{HS}	PPI_HSYNC Setup	1			ns
Th_{HS}	PPI_HSYNC Hold	1			ns
Ts_{PD}	PPI_Data Setup	1			ns
Th_{PD}	PPI_Data Hold	3			ns

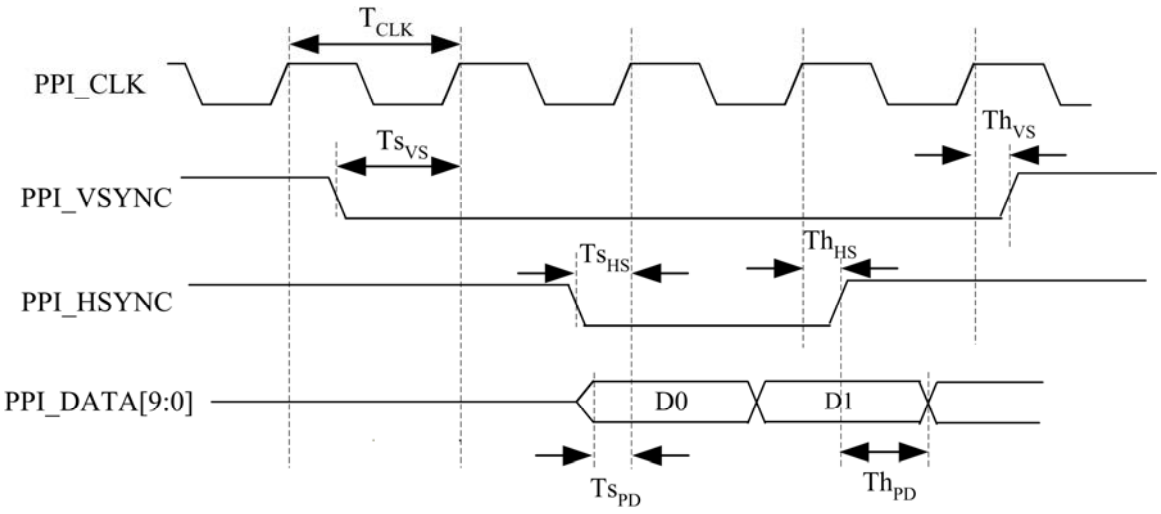


Figure 31: PPI Timing

TIMING CHARACTERISTICS

JTAG Test Interface

Table 19: JTAG Port Timing

Parameter	Comments	Min	Max	Unit
TsTCK	TCK Clock Period	250		ns
TsTMS	TMS Setup	15		ns
ThTMS	TMS Hold	15		ns
TsTDI	TDI Setup	15		ns
ThTDI	TDI Hold	15		ns
TdTDO	TDO Output Delay		10	ns

Note: JTAG Port Timing measurements are Guaranteed by Design

The same timing applies to the JTAG signals for both the dedicated JTAG port and the mapping onto the USC port. TDO does not go tri-state when run through the USC.

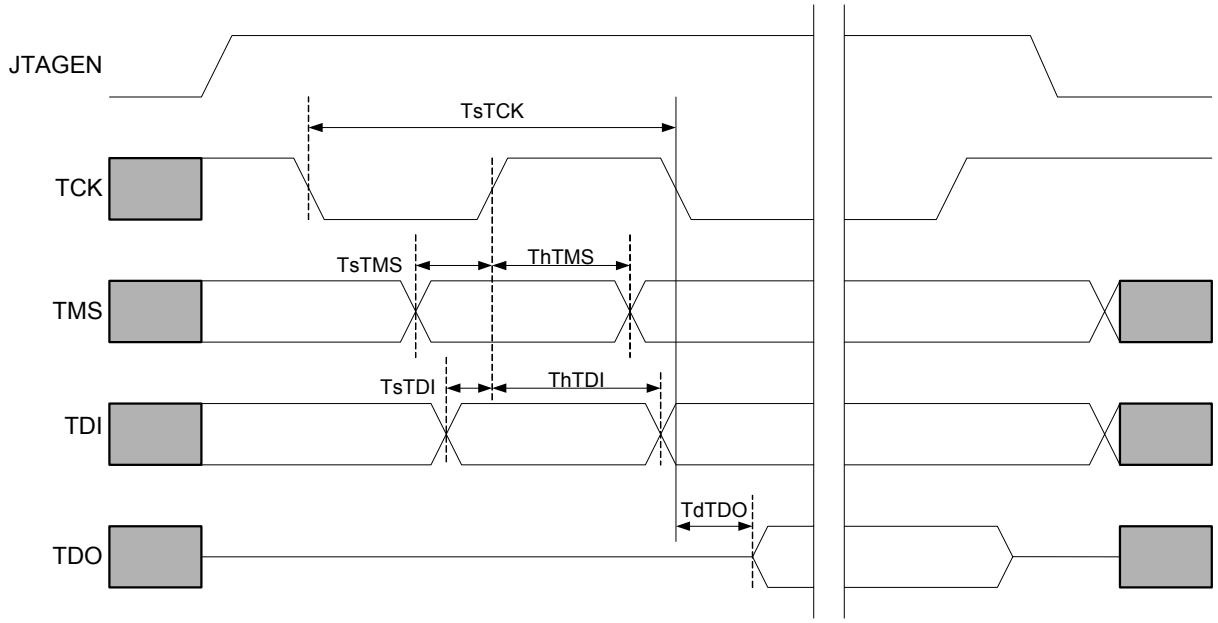
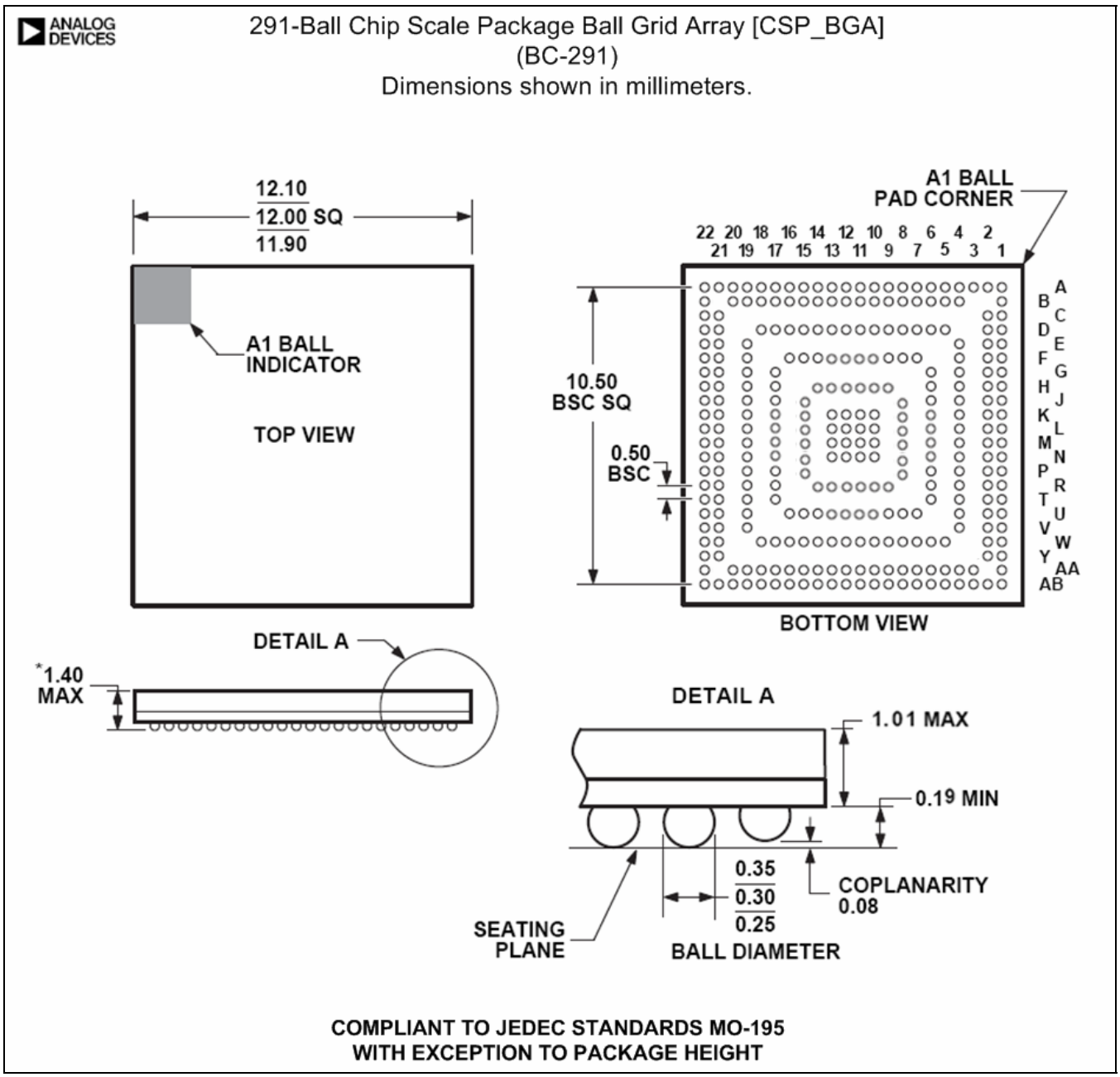


Figure 32: JTAG Port Timing

The gray areas show alternative signal function states.

PACKAGING

Package Outline



Package Signal Assignments

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
A1	GND	B1	nWE	C1	nADV	D1	nA0CS
A2	TESTMODE	B2	*Not Populated*	C2	nWAIT	D2	BURSTCLK
A3	nLWR_LBS	B3	*Not Populated*	C3	*Not Populated*	D3	*Not Populated*
A4	nRD	B4	nHWR_UBS	C4	*Not Populated*	D4	*Not Populated*
A5	DATA[1]	B5	DATA[0]	C5	*Not Populated*	D5	ADD[6]
A6	DATA[3]	B6	DATA[2]	C6	*Not Populated*	D6	ADD[8]
A7	DATA[5]	B7	DATA[4]	C7	*Not Populated*	D7	ADD[10]
A8	DATA[7]	B8	DATA[6]	C8	*Not Populated*	D8	ADD[12]
A9	DATA[9]	B9	DATA[8]	C9	*Not Populated*	D9	ADD[14]
A10	DATA[11]	B10	DATA[10]	C10	*Not Populated*	D10	ADD[16]
A11	DATA[13]	B11	DATA[12]	C11	*Not Populated*	D11	ADD[18]
A12	DATA[14]	B12	DATA[15]	C12	*Not Populated*	D12	ADD[20]
A13	GPIO_24	B13	GND	C13	*Not Populated*	D13	ADD[22]
A14	GND	B14	CLKIN	C14	*Not Populated*	D14	ADD[23]
A15	VPLL	B15	VRTC	C15	*Not Populated*	D15	GPIO_32
A16	OSCOUT	B16	GND	C16	*Not Populated*	D16	ASFS
A17	OSCIN	B17	GND	C17	*Not Populated*	D17	BSDI
A18	PWRON	B18	ASDI	C18	*Not Populated*	D18	CSFS
A19	BSIFS	B19	BSOFS	C19	*Not Populated*	D19	*Not Populated*
A20	CSDO	B20	CSDI	C20	*Not Populated*	D20	*Not Populated*
A21	CLKOUT	B21	*Not Populated*	C21	GPIO_63	D21	GPIO_57
A22	GND	B22	GPIO_76	C22	GPIO_62	D22	USB_DP

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
E1	nA2CS	F1	GPIO_51	G1	nRESET	H1	nSDCAS
E2	nA1CS	F2	GPIO_49	G2	GPIO_53	H2	nSDRAS
E3	*Not Populated*	F3	*Not Populated*	G3	*Not Populated*	H3	*Not Populated*
E4	ADD[5]	F4	ADD[3]	G4	ADD[1]	H4	nA3CS
E5	*Not Populated*	F5	*Not Populated*	G5	*Not Populated*	H5	*Not Populated*
E6	*Not Populated*	F6	*Not Populated*	G6	ADD[4]	H6	ADD[2]
E7	*Not Populated*	F7	ADD[7]	G7	*Not Populated*	H7	*Not Populated*
E8	*Not Populated*	F8	ADD[9]	G8	*Not Populated*	H8	*Not Populated*
E9	*Not Populated*	F9	ADD[11]	G9	*Not Populated*	H9	VMEM
E10	*Not Populated*	F10	ADD[13]	G10	*Not Populated*	H10	VMEM
E11	*Not Populated*	F11	ADD[15]	G11	*Not Populated*	H11	VCORE
E12	*Not Populated*	F12	ADD[17]	G12	*Not Populated*	H12	VCORE
E13	*Not Populated*	F13	ADD[19]	G13	*Not Populated*	H13	VCORE
E14	*Not Populated*	F14	ADD[21]	G14	*Not Populated*	H14	VINT1

E15	*Not Populated*	F15	ASDO	G15	*Not Populated*	H15	*Not Populated*
E16	*Not Populated*	F16	BSDO	G16	*Not Populated*	H16	*Not Populated*
E17	*Not Populated*	F17	*Not Populated*	G17	CLKOUT_GATE	H17	USB_ID
E18	*Not Populated*	F18	*Not Populated*	G18	*Not Populated*	H18	*Not Populated*
E19	GPIO_58	F19	USB_VBUS	G19	GND	H19	VUSB
E20	*Not Populated*	F20	*Not Populated*	G20	*Not Populated*	H20	*Not Populated*
E21	MC_DAT[1]	F21	MC_DAT[2]	G21	GPIO_124	H21	WUDQ
E22	USB_DM	F22	MC_CLK	G22	GPIO_123	H22	UCLK

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
J1	nSDCS	K1	SCLKOUT	L1	GPIO_0	M1	GPIO_2
J2	nSDWE	K2	SDA10	L2	nNDWP	M2	GPIO_3
J3	*Not Populated*	K3	*Not Populated*	L3	*Not Populated*	M3	*Not Populated*
J4	GPIO_52	K4	GPIO_54	L4	nNDCS	M4	GPIO_1
J5	*Not Populated*	K5	*Not Populated*	L5	*Not Populated*	M5	*Not Populated*
J6	ADD[0]	K6	GPIO_50	L6	SCKE	M6	nNDBUSY
J7	*Not Populated*	K7	*Not Populated*	L7	*Not Populated*	M7	*Not Populated*
J8	VMEM	K8	VMEM	L8	VCORE	M8	VCORE
J9	*Not Populated*	K9	*Not Populated*	L9	*Not Populated*	M9	*Not Populated*
J10	*Not Populated*	K10	GND	L10	GND	M10	GND
J11	*Not Populated*	K11	GND	L11	GND	M11	GND
J12	*Not Populated*	K12	GND	L12	GND	M12	GND
J13	*Not Populated*	K13	GND	L13	GND	M13	GND
J14	*Not Populated*	K14	*Not Populated*	L14	*Not Populated*	M14	*Not Populated*
J15	VMMC	K15	VSIM	L15	VINT2	M15	VCORE
J16	*Not Populated*	K16	*Not Populated*	L16	*Not Populated*	M16	*Not Populated*
J17	MC_DAT[0]	K17	MC_DAT[3]	L17	GPIO_100	M17	VCPRO
J18	*Not Populated*	K18	*Not Populated*	L18	*Not Populated*	M18	*Not Populated*
J19	MC_CMD	K19	SIMCLK	L19	SIMDATAIO	M19	GND
J20	*Not Populated*	K20	*Not Populated*	L20	*Not Populated*	M20	*Not Populated*
J21	WUDI	K21	EB2_ADDR[6]	L21	EB2_ADDR[7]	M21	PPI_DATA[3]
J22	WDDQ	K22	WDDI	L22	PPI_DATA[0]	M22	PPI_DATA[1]

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
N1	GPIO_5	P1	GPIO_8	R1	GPIO_11	T1	GPIO_15
N2	GPIO_6	P2	GPIO_9	R2	GPIO_14	T2	JTAGEN
N3	*Not Populated*	P3	*Not Populated*	R3	*Not Populated*	T3	*Not Populated*
N4	GPIO_7	P4	GPIO_10	R4	GPIO_13	T4	GPIO_18
N5	*Not Populated*	P5	*Not Populated*	R5	*Not Populated*	T5	*Not Populated*
N6	GPIO_4	P6	GPIO_12	R6	GPIO_16	T6	GPIO_35
N7	*Not Populated*	P7	*Not Populated*	R7	*Not Populated*	T7	*Not Populated*

N8	VEXT	P8	VEXT	R8	*Not Populated*	T8	*Not Populated*
N9	*Not Populated*	P9	*Not Populated*	R9	VEXT	T9	*Not Populated*
N10	GND	P10	*Not Populated*	R10	VEXT	T10	*Not Populated*
N11	GND	P11	*Not Populated*	R11	VCORE	T11	*Not Populated*
N12	GND	P12	*Not Populated*	R12	VCORE	T12	*Not Populated*
N13	GND	P13	*Not Populated*	R13	VCORE	T13	*Not Populated*
N14	*Not Populated*	P14	*Not Populated*	R14	VVID	T14	*Not Populated*
N15	VCORE	P15	VVID	R15	*Not Populated*	T15	*Not Populated*
N16	*Not Populated*	P16	*Not Populated*	R16	*Not Populated*	T16	*Not Populated*
N17	EB2_nWE	P17	EB2_ADDR[1]	R17	EB2_ADDR[5]	T17	EB2_ADDR[11]
N18	*Not Populated*	P18	*Not Populated*	R18	*Not Populated*	T18	*Not Populated*
N19	VVID	P19	EB2_nRD	R19	EB2_ADDR[2]	T19	EB2_ADDR[3]
N20	*Not Populated*	P20	*Not Populated*	R20	*Not Populated*	T20	*Not Populated*
N21	PPI_DATA[2]	P21	EB2_ADDR[0]	R21	GPIO_155	T21	GPIO_153
N22	EB2_ADDR[9]	P22	EB2_ADDR[8]	R22	GPIO_156	T22	GPIO_154

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
U1	GPIO_17	V1	GPIO_20	W1	GPIO_22	Y1	GND
U2	GPIO_19	V2	GPIO_177	W2	GPIO_33	Y2	GPIO_34
U3	*Not Populated*	V3	*Not Populated*	W3	*Not Populated*	Y3	*Not Populated*
U4	GPIO_21	V4	VCPRO	W4	*Not Populated*	Y4	*Not Populated*
U5	*Not Populated*	V5	*Not Populated*	W5	GPIO_36	Y5	*Not Populated*
U6	*Not Populated*	V6	*Not Populated*	W6	GPIO_64	Y6	*Not Populated*
U7	GPIO_55	V7	*Not Populated*	W7	GPIO_66	Y7	*Not Populated*
U8	GPIO_65	V8	*Not Populated*	W8	GPIO_68	Y8	*Not Populated*
U9	GPIO_67	V9	*Not Populated*	W9	GPIO_86	Y9	*Not Populated*
U10	GPIO_74	V10	*Not Populated*	W10	GPIO_98	Y10	*Not Populated*
U11	GPIO_87	V11	*Not Populated*	W11	USC[4]	Y11	*Not Populated*
U12	USC[6]	V12	*Not Populated*	W12	USC[2]	Y12	*Not Populated*
U13	USC[0]	V13	*Not Populated*	W13	KEYPADROW[3]	Y13	*Not Populated*
U14	KEYPADROW[0]	V14	*Not Populated*	W14	KEYPADCOL[2]	Y14	*Not Populated*
U15	GPIO_173	V15	*Not Populated*	W15	KEYPADCOL[0]	Y15	*Not Populated*
U16	GPIO_175	V16	*Not Populated*	W16	GPIO_174	Y16	*Not Populated*
U17	*Not Populated*	V17	*Not Populated*	W17	EB2_nWAIT	Y17	*Not Populated*
U18	*Not Populated*	V18	*Not Populated*	W18	EB2_ADDR[12]	Y18	*Not Populated*
U19	EB2_ADDR[10]	V19	PPI_DATA[8]	W19	*Not Populated*	Y19	*Not Populated*
U20	*Not Populated*	V20	*Not Populated*	W20	*Not Populated*	Y20	*Not Populated*
U21	GPIO_152	V21	PPI_DATA[5]	W21	PPI_DATA[7]	Y21	PPI_CLK
U22	GPIO_167	V22	PPI_DATA[4]	W22	PPI_DATA[6]	Y22	PPI_DATA[9]

#	Pin Name	#	Pin Name
AA1	GND	AB1	GND
AA2	*Not Populated*	AB2	GPIO_37
AA3	GPIO_38	AB3	GPIO_56
AA4	GPIO_59	AB4	GPIO_60
AA5	GPIO_61	AB5	GPIO_69
AA6	GPIO_70	AB6	GPIO_71
AA7	GPIO_72	AB7	GPIO_73
AA8	GPIO_78	AB8	GPIO_85
AA9	GPIO_113	AB9	GPIO_99
AA10	USC[5]	AB10	USC[3]
AA11	USC[1]	AB11	CLKON
AA12	KEYPADROW[4]	AB12	KEYPADROW[2]
AA13	KEYPADROW[1]	AB13	KEYPADCOL[4]
AA14	KEYPADCOL[1]	AB14	KEYPADCOL[3]
AA15	GPIO_141	AB15	GPIO_172
AA16	GPIO_143	AB16	GPIO_142
AA17	GPIO_145	AB17	GPIO_144
AA18	GPIO_147	AB18	GPIO_146
AA19	GPIO_149	AB19	GPIO_148
AA20	GPIO_151	AB20	GPIO_150
AA21	*Not Populated*	AB21	PPI_HSYNC
AA22	PPI_VSYNC	AB22	GND