+3 V/+5 V, Dual, Serial Input 12-Bit DAC

AD7394

FEATURES

Micropower: 100 µA/DAC
0.1 µA typical power shutdown
Single-supply 2.7 V to 5.5 V operation
12-bit resolution
Serial interface with Schmitt trigger inputs

APPLICATIONS

Automotive output span voltage
Portable communications
Digitally controlled calibration
PC peripherals

FUNCTIONAL BLOCK DIAGRAM

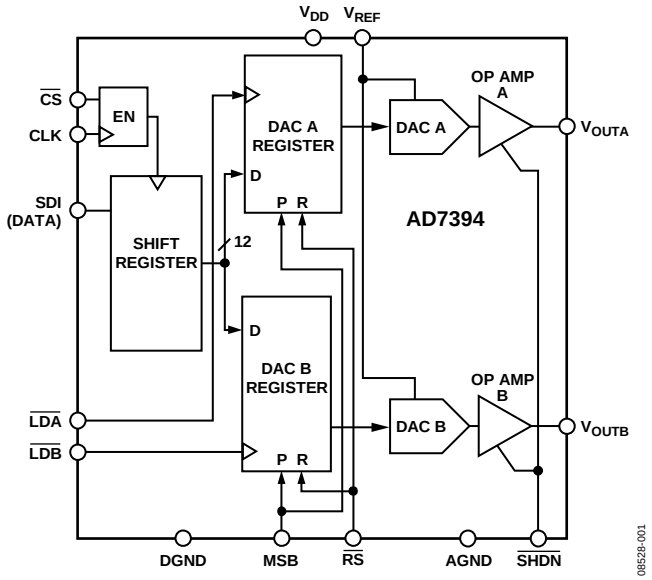

Figure 1.

GENERAL DESCRIPTION

The AD7394 is dual, 12-bit, voltage output digital-to-analog converter designed to operate from a single 3 V supply. Built using a CBCMOS process, this monolithic DAC offers the user low cost and ease-of-use in a single-supply 3 V system. Operation is guaranteed over the supply voltage range of 2.7 V to 5.5 V making this device ideal for battery-operated applications.

The full-scale output voltage is determined by the applied external reference input voltage, V_{REF}. The rail-to-rail V_{REF} input to V_{OUT} outputs allows for a full-scale voltage set equal to the positive supply, V_{DD}, or any value in between.

A doubled-buffered serial data interface offers high speed, microcontroller compatible inputs using the serial-data-in (SDI), clock (CLK), and load strobe ($\overline{LDA}$ and $\overline{LDB}$) pins. A chip-select ($\overline{CS}$) pin simplifies the connection of multiple DAC packages by enabling the clock input when active low. Additionally, an $\overline{RS}$ input sets the output to zero scale or to 1/2 scale based on the logic level applied to the MSB pin. The power shutdown pin, $\overline{SHDN}$, reduces power dissipation to nanoamp current levels. All digital inputs contain Schmitt-triggered logic levels to minimize power dissipation and prevent false triggering on the clock input.

The AD7394 is specified over the extended industrial (−40°C to +85°C) temperature range and is available in a low profile 1.75 mm height SOIC surface mount package.

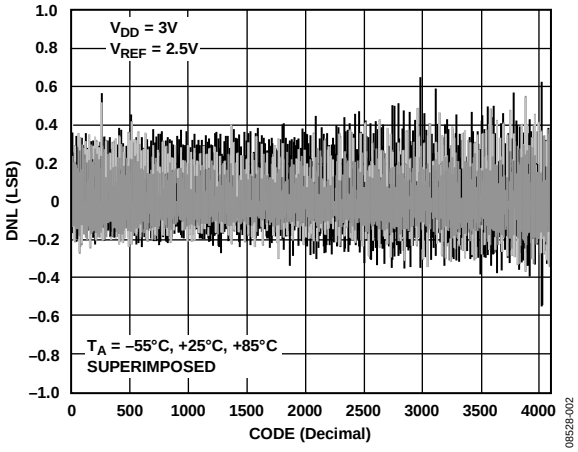

Figure 2. Differential Nonlinearity Error vs. Code

Rev. A

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TABLE OF CONTENTS

REVISION HISTORY

1/10—Rev. 0 to Rev. A

Updated Format ..... Universal
Removed AD7395 ..... Universal
Updated Outline Dimensions 18
Changes to Ordering Guide 19

4/98—Revision. 0: Initial Version

SPECIFICATIONS

AD7394 ELECTRICAL CHARACTERISTICS

@ $V_{REF\ IN}$ = 2.5 V, −40°C < T_A < +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	3 V ± 10%	5 V ± 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		12	12	Bits
Relative Accuracy[2]	INL	T_A = +25°C	±1.5	±1.5	LSB max
		T_A = −40°C, +85°C	±2.0	±2.0	LSB max
Differential Nonlinearity[2]	DNL	T_A = +25°C, monotonic	±0.9	±0.9	LSB max
		Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	4.0	4.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = +25°C, +85°C, data = FFF_H	±8	±8	mV max
		T_A = −40°C, data = FFF_H	±20	±20	mV max
Full-Scale Tempco[3]	TCV_{FS}		−30	−30	ppm/°C typ
REFERENCE INPUT					
$V_{REF\ IN}$ Range	V_{REF}		0/V_{DD}	0/V_{DD}	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (Source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	3	3	mA typ
Capacitive Load[3]	C_L	No oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD} − 0.6	4.0	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Clock Width High	t_{CH}		50	30	ns min
Clock Width Low	t_{CL}		50	30	ns min
Load Pulsewidth	t_{LDW}		30	20	ns min
Data Setup	t_{DS}		10	10	ns min
Data Hold	t_{DH}		30	15	ns min
Clear Pulsewidth	t_{CLRW}		15	15	ns min
Load Setup	t_{LD1}		30	15	ns min
Load Hold	t_{LD2}		40	20	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H	0.05	0.05	V/µs typ
Settling Time[6]	t_S	To ±0.1% of full scale	70	60	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800H to $7FF_H$	65	65	nV/s typ
Digital Feedthrough	Q				
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} +1 V p-p,	15	15	nV/s typ
		Data = 000_H, f = 100 kHz	−63	−63	dB typ

Parameter	Symbol	Conditions	3 V ± 10%	5 V ± 10%	Unit
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ± 1 LSB	2.7/5.5	2.7/5.5	V min/max
Shutdown Supply Current	I_{DD_SD}	$\overline{SHDN}$ = 0, V_{IL} = 0 V, no load	0.1/1.5	0.1/1.5	µA typ/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, no load	125/200	125/200	µA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, no load	600	1000	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

[1] One LSB = V_{REF}/4096 V for the 12-bit AD7394.
[2] The first two codes (000_H, 001_H) are excluded from the linearity error measurement.
[3] These parameters are guaranteed by design and not subject to production testing.
[4] Typicals represent average readings measured at 25°C.
[5] All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of +3 V) and timed from a voltage level of 1.6 V.
[6] The settling time specification does not apply for negative going transitions within the last three LSBs of ground.

Timing Diagrams

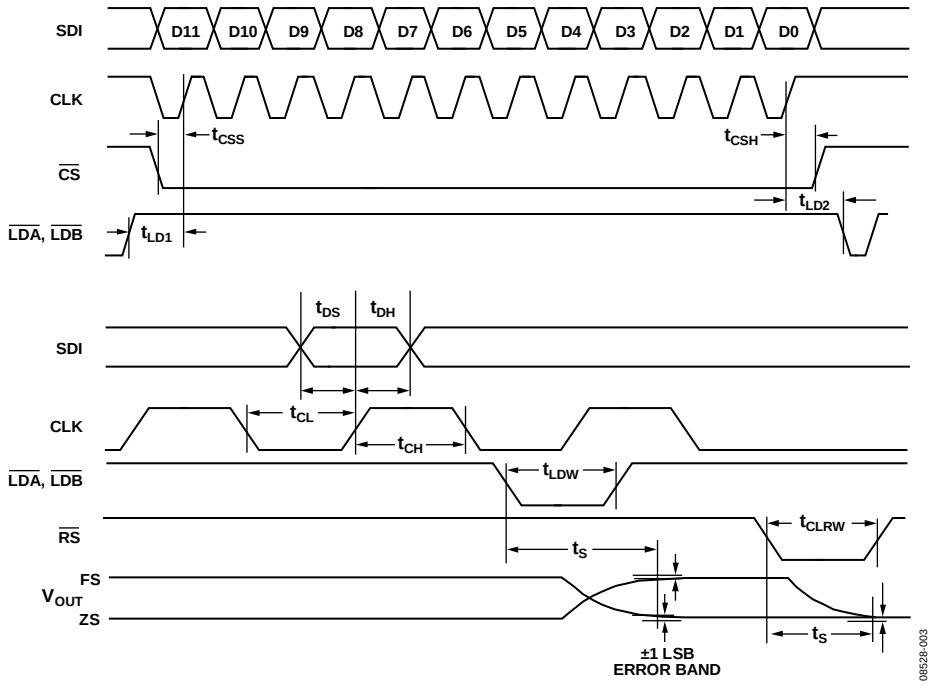


Figure 3.

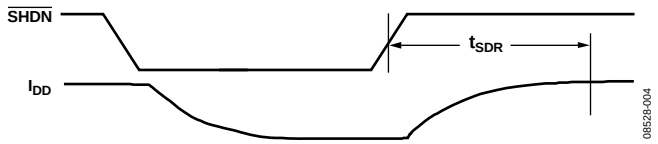


Figure 4.

Table 2. Control Logic Truth Table

$\overline{CS}$	CLK	$\overline{RS}$	MSB	$\overline{SHDN}$	$\overline{LDA}$/$\overline{LDB}$	Serial Shift Register Function	DAC Register Function
H	X	H	X	H	H	No effect	Latched
L	L	H	X	H	H	No effect	Latched
L	H	H	X	H	H	No effect	Latched
L	↑+	H	X	H	H	Shift-register-data advanced one bit	Latched
L	↑+	H	X	H	L	Shift-register-data advanced one bit	Transparent
L	H	H	X	H	L	No effect	Transparent
↑+[1]	L	H	X	H	H	No effect	Latched
H	X	H	X	H	↓–[2]	No effect	Updated with current shift register contents
H	X	H	X	H	L	No effect	Transparent
X	X	L	H	H	X	No effect	Loaded with 800_H
X	X	↑+	H	H	H	No effect	Latched with 800_H
X	X	L	L	H	X	No effect	Loaded with all zeros
X	X	↑+	L	H	H	No effect	Latched all zeros
X	X	X	X	L	X	No effect	No affect

[1] ↑+ positive logic transition; ↓– negative logic transition; X don't care.
[2] Do not clock in serial data while level sensitive inputs $\overline{LDA}$ or $\overline{LDB}$ are logic low.

Table 3. AD7394 Serial Input Register Data Format, Data Is Loaded in MSB-First Format

MSB											**LSB**
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD} to GND	–0.3 V to +7 V
V_{REF} to GND	–0.3 V to V_{DD}
Logic Inputs to GND	–0.3 V to +8 V
V_{OUT} to GND	–0.3 V to V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND	50 mA
Package Power Dissipation	$(T_J \text{ max} – T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}	
14-Lead SOIC Package (R-14)	158°C/W
Maximum Junction Temperature (T_J max)	150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature	
R-14 (Vapor Phase, 60 sec)	215°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

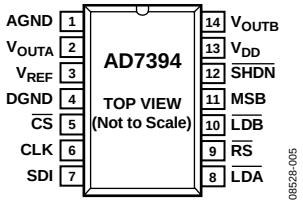


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AGND	Analog Ground.
2	V_{OUTA}	DAC A Voltage Output.
3	V_{REF}	DAC Reference Voltage Input Terminal. Establishes DAC full-scale output voltage. Pin can be tied to V_{DD} pin.
4	DGND	Digital Ground. Should be tied to analog GND.
5	$\overline{CS}$	Chip Select, Active Low Input. Disables shift register loading when high. Does not affect $\overline{LDA}$ or $\overline{LDB}$ operation.
6	CLK	Clock Input. Positive edge clocks data into shift register, MSB data bit first.
7	SDI	Serial Data Input. Input data loads directly into the shift register.
8	$\overline{LDA}$	Load DAC Register Strobe. Level sensitive active low. Transfers shift register data to DAC A register. Asynchronous active low input. See Table 2 for operation.
9	$\overline{RS}$	Resets DAC register to zero condition or half-scale, depending on MSB pin logic level. Asynchronous active low input.
10	$\overline{LDB}$	Load DAC Register Strobe. Level-sensitive active low. Transfers shift register data to DAC B register. Asynchronous active low input. See Table 2 for operation.
11	MSB	Digital Input. Logic High presets DAC registers to half-scale 800_H (sets MSB bit to one) when the $\overline{RS}$ pin is strobed; logic low clears all DAC registers to zero (000_H) when the $\overline{RS}$ pin is strobed.
12	$\overline{SHDN}$	Active Low Shutdown Control Input. Does not affect register contents as long as power is present on V_{DD}. New data can be loaded into the shift register and DAC register during shutdown. When device is powered up the most recent data loaded into the DAC register controls the DAC output.
13	V_{DD}	Positive Power Supply Input. Specified range of operation is 2.7 V to 5.5 V
14	V_{OUTB}	DAC B Voltage Output.

TYPICAL PERFORMANCE CHARACTERISTICS

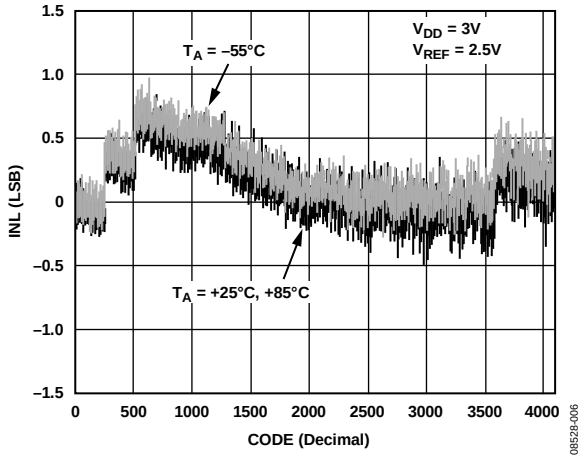


Figure 6. Integral Nonlinearity Error vs. Code

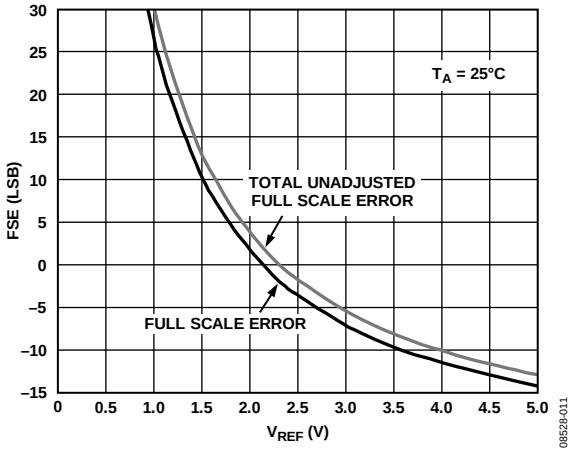


Figure 9. Full-Scale Error vs. V_{REF}

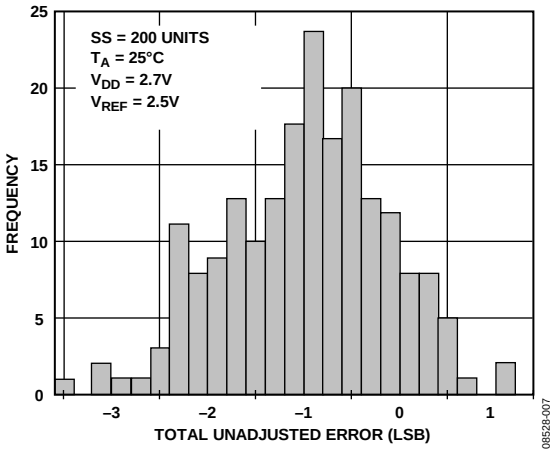


Figure 7. Total Unadjusted Error Histogram

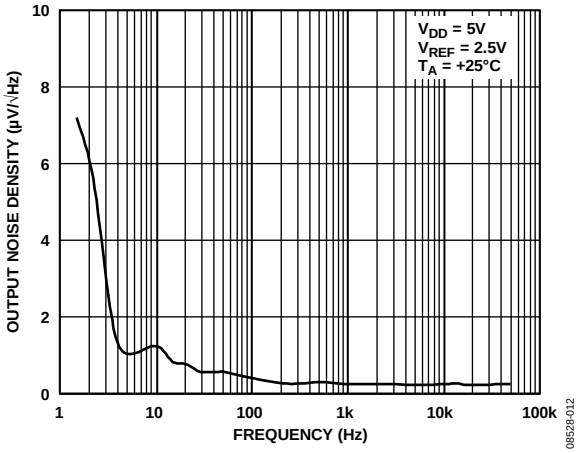


Figure 10. Output Noise Density vs. Frequency

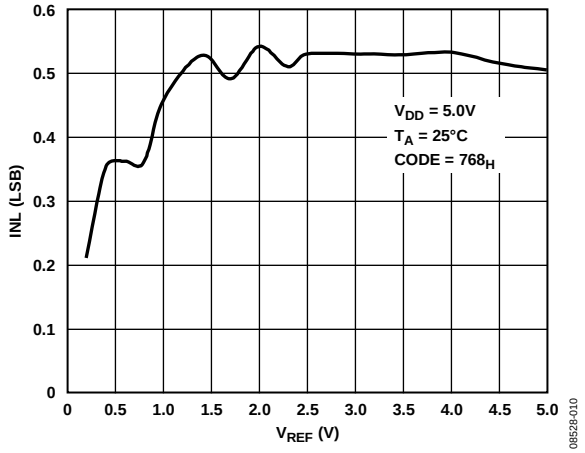


Figure 8. Integral Nonlinearity Error vs. V_{REF}

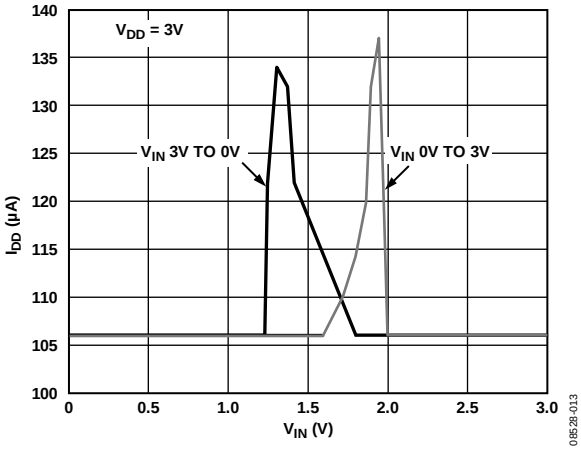


Figure 11. Supply Current vs. Logic Input Voltage

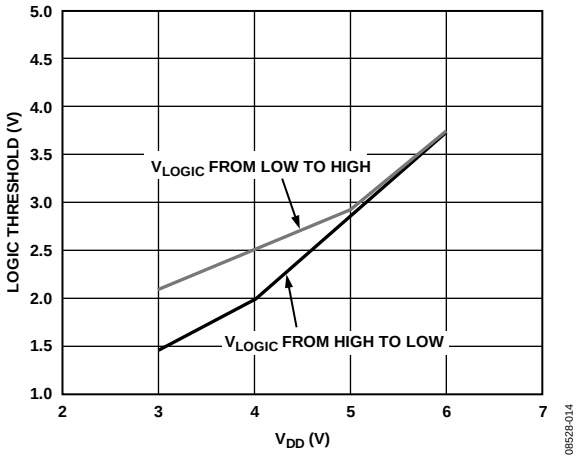


Figure 12. Logic Threshold vs. Supply Voltage

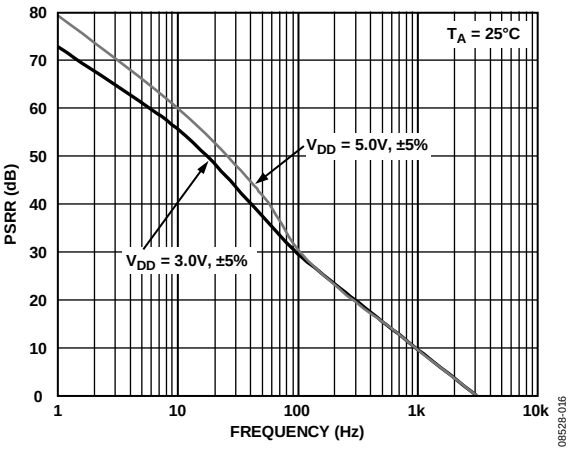


Figure 14. Power Supply Rejection vs. Frequency

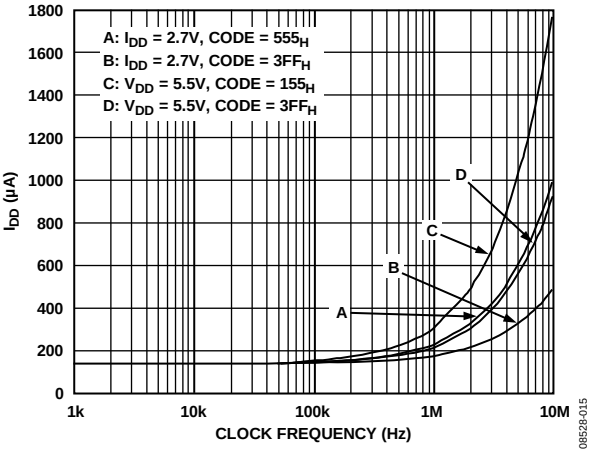


Figure 13. Supply Current vs. Clock Frequency

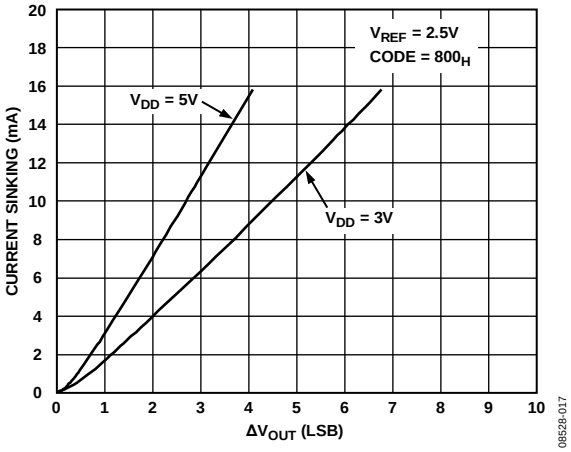


Figure 15. I_{OUT} Sink Current vs. ΔV_{OUT}

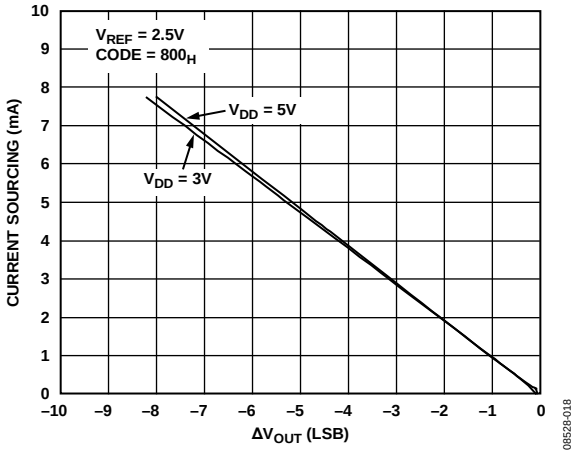


Figure 16. I_{OUT} Source Current vs. ΔV_{OUT}

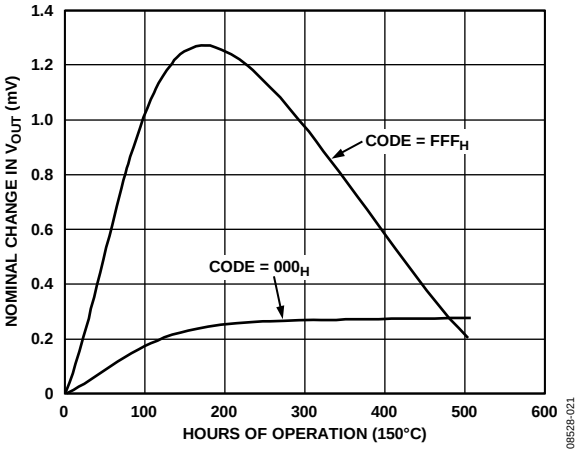


Figure 18. Long-Term Drift Accelerated by Burn-In

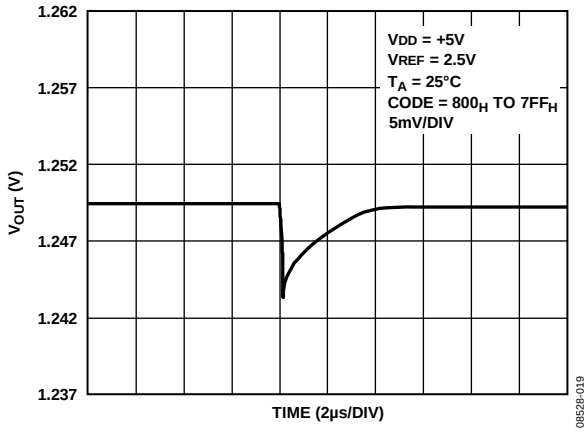


Figure 17. Midscale Transition Performance

THEORY OF OPERATION

The AD7394 is a pin compatible, dual, 12-bit digital-to-analog converter. This single-supply operation device consumes less than 200 microamps of current while operating from power supplies in the 2.7 V to 5.5 V range, making it ideal for battery-operated applications. The AD7394 contains a voltage-switched, 12-bit, laser trimmed digital-to-analog converter, rail-to-rail output op amps, two DAC registers, and a serial input shift register. The external reference input has constant input resistance independent of the digital code setting of the DAC. In addition, the reference input can be tied to the same supply voltage as V_{DD}, resulting in a maximum output voltage span of 0 to V_{DD}. The serial interface consists of a serial data input (SDI), clock ($\overline{CLK}$), a chip select pin ($\overline{CS}$), and two load DAC Register pins ($\overline{LDA}$ and $\overline{LDB}$). A reset ($\overline{RS}$) pin is available to reset the DAC register to zero scale or midscale, depending on the digital level applied to the MSB pin. This function is useful for power-on reset or system failure recovery to a known state. Additional power savings are accomplished by activating the $\overline{SHDN}$ pin resulting in a 1.5 mA maximum consumption sleep mode.

DAC SECTION

The voltage switched R-2R DAC generates an output voltage dependent on the external reference voltage connected to the REF pin according to the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N} \quad (1)$$

where:
D is the decimal data word loaded into the DAC register.
N is the number of bits of DAC resolution.

For the 12-bit AD7394 operating from a 5.0 V reference Equation 1 becomes:

$$V_{OUT} = \frac{5.0 \times D}{4096} \quad (3)$$

Using Equation 3 the AD7394 provides a nominal midscale voltage of 2.50 V for D = 2048, and a full-scale output of 4.998 V. The LSB step size is = 5.0 × 1/4096 = 0.0012 V.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. The op amp has a 60 μs typical settling time to 0.1% of full scale. There are slight differences in settling time for negative slewing signals vs. positive. Also, negative transition settling time to within the last 6 LSBs of zero volts has an extended settling time. The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 19 shows an equivalent output schematic of the rail-to-rail-amplifier with its N-channel pull-down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P-channel pull-up device that can source current to GND terminated loads.

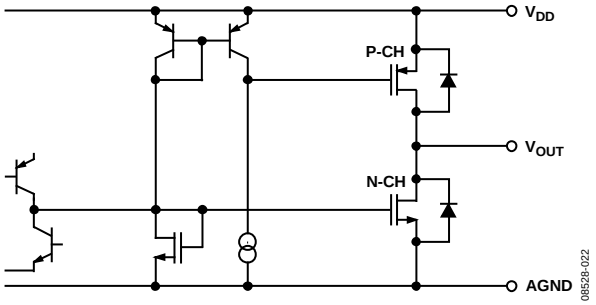


Figure 19. Equivalent Analog Output Circuit

The rail-to-rail output stage provides more than ±1 mA of output current. The N-channel output pull-down MOSFET shown in Figure 19 has a 35 Ω on resistance, which sets the sink current capability near ground. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 100 pF capacitive load driving capability.

REFERENCE INPUT

The reference input terminal has a constant input resistance independent of digital code, which results in reduced glitches on the external reference voltage source. The high 2.5 MΩ input resistance minimizes power dissipation within the AD7394 DAC. The V_{REF} input accepts input voltages ranging from ground to the positive supply voltage V_{DD}. One of the simplest applications, which saves an external reference voltage source, is connection of the V_{REF} terminal to the positive V_{DD} supply. This connection results in a rail-to-rail voltage output span maximizing the programmed range. The reference input accepts ac signals as long as they are kept within the supply voltage range, $0 < V_{REF} < V_{DD}$. The reference bandwidth and integral nonlinearity error performance are plotted in Figure 8. The ratiometric reference feature makes the AD7394 an ideal companion to ratiometric analog-to-digital converters such as the AD7896.

POWER SUPPLY

The very low power consumption of the AD7394 is a direct result of a circuit design optimizing the use of a CBCMOS process. By using the low power characteristics of CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors, excellent analog accuracy is achieved. One advantage of the rail-to-rail output amplifiers used in the AD7394 is the wide range of usable supply voltage. The part is fully specified and tested for operation from 2.7 V to 5.5 V.

POWER SUPPLY BYPASSING AND GROUNDING

Local supply bypassing consisting of a 10 µF tantalum electrolytic in parallel with a 0.1 µF ceramic capacitor is recommended in all applications (Figure 20).

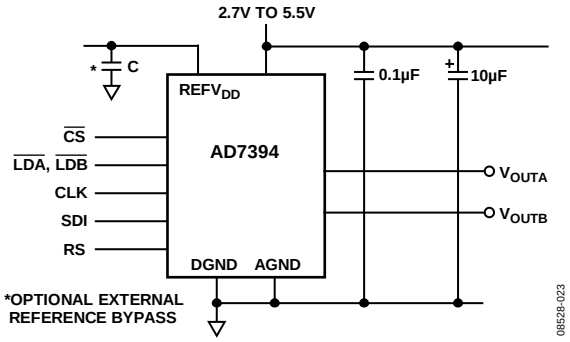


Figure 20. Recommended Supply Bypassing for the AD7394

INPUT LOGIC LEVELS

All digital inputs are protected with a Zener-type ESD protection structure (Figure 21) that allows logic input voltages to exceed the V_{DD} supply voltage. This feature can be useful if the user is driving one or more of the digital inputs with a 5 V CMOS logic input-voltage level while operating the AD7394 on a 3 V power supply. If this mode of interface is used, make sure that the V_{OL} of the 5 V CMOS meets the V_{IL} input requirement of the AD7394 operating at 3 V. See Figure 12 for a graph of digital logic input threshold vs. operating V_{DD} supply voltage.

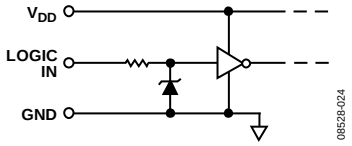


Figure 21. Equivalent Digital Input ESD Protection

To minimize power dissipation from input logic levels that are near the V_{IH} and V_{IL} logic input voltage specifications, a Schmitt trigger design was used that minimizes the input buffer current consumption compared to traditional CMOS input stages. Figure 11 is a plot of incremental input voltage vs. supply current showing that negligible current consumption takes place when logic levels are in their quiescent state. The normal crossover current still occurs during logic transitions. A secondary advantage of this Schmitt trigger is the prevention of false triggers that would occur with slow moving logic transitions when a standard CMOS logic interface or opto isolators are used. The logic inputs SDI, CLK, $\overline{CS}$, $\overline{LDA}$, $\overline{LDB}$, $\overline{RS}$, and $\overline{SHDN}$ all contain the Schmitt trigger circuits.

DIGITAL INTERFACE

The AD7394 has a serial data input. A functional block diagram of the digital section is shown in Figure 22, while Table 2 contains the truth table for the logic control inputs. Three pins control the serial data input register loading. Two additional pins determine which DAC receives the data loaded into the input shift register. Data at the SDI is clocked into the shift register on the rising edge of the CLK. Data is entered in the MSB-first format. The active low chip select ($\overline{CS}$) pin enables loading of data into the shift register from the SDI pin. Twelve clock pulses are required to load the 12-bit AD7390 DAC shift register. If additional bits are clocked into the shift register, for example, when a microcontroller sends two 8-bit bytes, the MSBs are ignored (Table 6). When $\overline{CS}$ returns to logic high, shift register loading is disabled. The load pins $\overline{LDA}$ and $\overline{LDB}$ control the flow of data from the shift register to the DAC register. After a new value is clocked into the serial-input register, it is transferred to the DAC register associated with its $\overline{LDA}$ or $\overline{LDB}$ logic control line. Note, if the user wants to load both DAC registers with the current contents of the shift register, both control lines $\overline{LDA}$ and $\overline{LDB}$ should be strobed together. The $\overline{LDA}$ and $\overline{LDB}$ pins are level-sensitive and should be returned to logic high prior to any new data being sent to the input shift register to avoid changing the DAC register values. See Table 2 for a complete set of conditions.

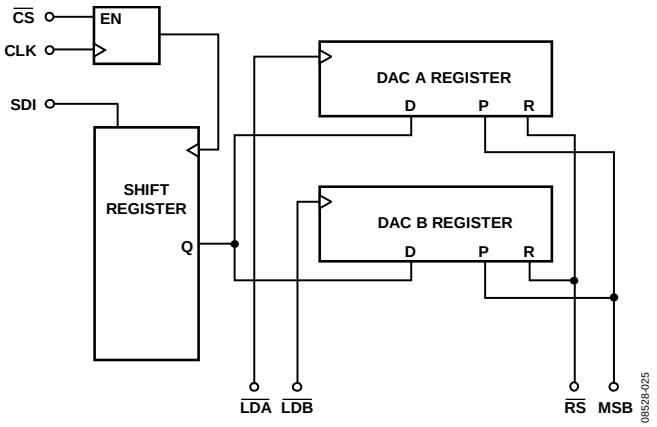


Figure 22. Equivalent Digital Interface Logic

RESET ($\overline{RS}$) PIN

Forcing the asynchronous $\overline{RS}$ pin low sets the DAC register to all zeros, or midscale, depending on the logic level applied to the MSB pin. When the MSB pin is set to logic high, both DAC registers are reset to midscale (that is, the DAC register's MSB bit is set to Logic 1 followed by all zeros). The reset function is useful for setting the DAC outputs to zero at power-up or after a power supply interruption. Test systems and motor controllers are two of many applications that benefit from powering up to a known state. The external reset pulse can be generated by the microprocessor's power-on reset signal, by an output from the microprocessor, or by an external resistor and capacitor. $\overline{RS}$ has a Schmitt trigger input, which results in a clean reset function when using external resistor/capacitor generated pulses. See Table 2 for more information.

Table 6. Typical Microcontroller Interface Formats[1]

MSB			BYTE 1				LSB	MSB			BYTE 0				LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

[1] D11 to D0: 12-bit AD7394 DAC data; X = don't care; the MSB of byte 1 is the first bit that is loaded into the SDI input.

POWER SHUTDOWN ($\overline{\text{SHDN}}$)

Maximum power savings can be achieved by using the power shutdown control function. This hardware activated feature is controlled by the active low input $\overline{\text{SHDN}}$ pin. This pin has a Schmitt trigger input, which helps to desensitize it to slowly changing inputs. By placing a logic low on this pin, the internal consumption of the device is reduced to nano amp levels, guaranteed to 1.5 µA maximum over the operating temperature range. When the AD7394 has been programmed into the power shutdown state, the present DAC register data is maintained as long as V_{DD} remains greater than 2.7 V. Once a wake-up command, $\overline{\text{SHDN}}$ = 1, is given, the DAC voltage outputs return to their previous values. It typically takes 80 microseconds for the output voltage to fully stabilize. In the shutdown state the DAC output amplifier exhibits an open circuit with a nominal output resistance of 500 kΩ to ground. If the power shutdown feature is not needed, tie the $\overline{\text{SHDN}}$ pin to the V_{DD} voltage thereby disabling this function.

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7394. As shown in Figure 23, the AD7394 has been designed to drive loads as low as 5 kΩ in parallel with 100 pF. The code table for this operation is shown in Table 7.

The circuit can be configured with an external reference plus power supply, or powered from a single dedicated regulator or reference depending on the application performance requirements.

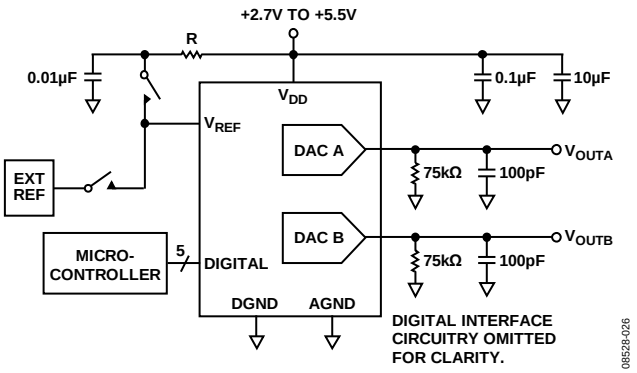
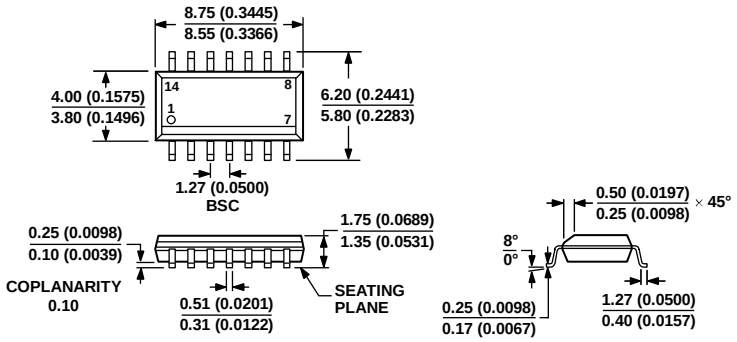


Figure 23. AD7394 Unipolar Output Operation

Table 7. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Output Voltage (V) [V_{REF} = 2.5 V]
FFF	4095	2.4994
801	2049	1.2506
800	2048	1.2500
7FF	2047	1.2494
000	0	0

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 24. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	Res (LSB)	Temperature Range	Package Description	Package Option
AD7394ARZ	12	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
AD7394ARZ-REEL7	12	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14

[1] The AD7394 contains 709 transistors. The die size measures 70 mil × 99 mil.
[2] Z = RoHS Compliant Part.

D08528-0-1/10(A)