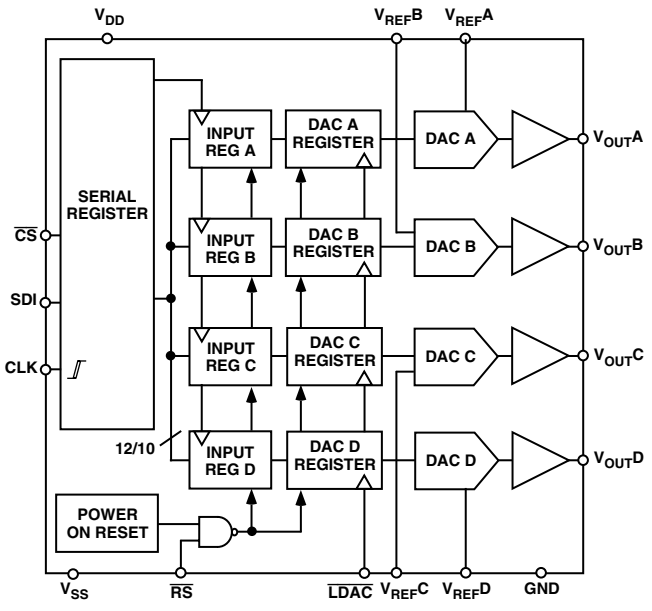
Quad, Serial-Input 12-Bit/10-Bit DACs

AD7398/AD7399

FEATURES
AD7398—12-Bit Resolution
AD7399—10-Bit Resolution
Programmable Power Shutdown
Single (3 V to 5 V) or Dual (±5 V) Supply Operation
3-Wire Serial SPI-Compatible Interface
Internal Power ON Reset
Double Buffered Registers for Simultaneous Multichannel DAC Update
Four Separate Rail-to-Rail Reference Inputs
Thin Profile TSSOP-16 Package Available
Low Tempco 1.5 ppm/°C

APPLICATIONS
Automotive Output Voltage Span
Portable Communications
Digitally Controlled Calibration
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7398/AD7399 family of quad, 12-bit/10-bit, voltage-output digital-to-analog converters is designed to operate from a single 3 V to 5 V or a dual ±5 V supply. Built with Analog's robust CBCMOS process, this monolithic DAC offers the user low cost, and ease-of-use in single or dual-supply systems.

The applied external reference V_{REF} determines the full-scale output voltage. Valid V_{REF} values include $V_{SS} < V_{REF} < V_{DD}$ that result in a wide selection of full-scale outputs. For multiplying applications ac inputs can be as large as ±5 V_P.

A doubled-buffered serial-data interface offers high-speed, 3-wire, SPI and microcontroller-compatible inputs using serial-data-in (SDI), clock (CLK), and a chip-select ($\overline{CS}$). A common level-sensitive load-DAC strobe ($\overline{LDAC}$) input allows simultaneous update of all DAC outputs from previously loaded Input Registers. Additionally, an internal power ON reset forces the output voltage to zero at system turn ON. An external asynchronous reset ($\overline{RS}$) also forces all registers to the zero code state. A programmable power-shutdown feature reduces power dissipation on unused DACs.

Both parts are offered in the same pinout to enable users to select the appropriate resolution for their application without redesigning the layout. For 8-bit resolution applications see the pin compatible AD7304 product.

The AD7398/AD7399 is specified over the extended industrial (–40°C to +125°C) temperature range. Parts are available in wide body SOIC-16 and ultracompact thin 1.1 mm TSSOP-16 packages.

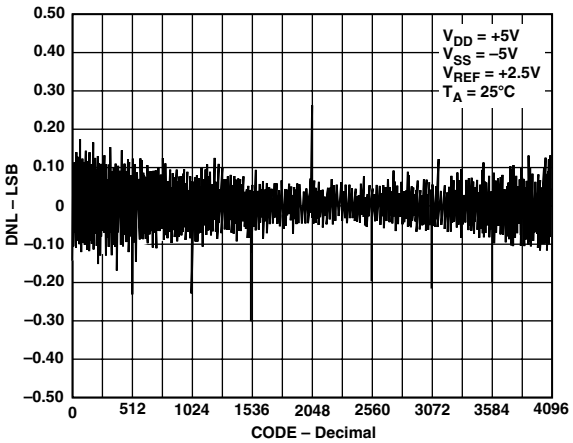


Figure 1. AD7398 DNL vs. Code (T_A = 25°C)

REV. 0

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AD7398/AD7399–SPECIFICATIONS

AD7398 12-BIT VOLTAGE OUTPUT DAC (@ V_{DD} = 5 V, V_{SS} = 0 V; or V_{DD} = +5 V, V_{SS} = –5 V, V_{REF} = +2.5 V, –40°C < T_A < +125°C, unless otherwise noted.)

Parameter	Symbol	Condition	3 V–5 V ± 10%	±5 V ± 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		12	12	Bits
Relative Accuracy[2]	INL		±1.5	±1.5	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	7	±2.5	mV max
Full-Scale Voltage Error	V_{FSE}	Data = FFF_H	±2.5	±2.5	mV max
Full-Scale Tempco[3]	TCV_{FS}		1.5	1.5	ppm/°C typ
REFERENCE INPUT					
V_{REF}IN Range[4]	V_{REF}		0/V_{DD}	V_{SS}/V_{DD}	V min/max
Input Resistance[5]	R_{REF}	Data = 555_H, Worst-Case	35	35	kΩ typ[6]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current	I_{OUT}	Data = 800_H, ΔV_{OUT} = 4 LSB	±5	±5	mA typ
Capacitive Load[3]	C_L	No Oscillation	200	400	pF max
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}	V_{DD} = 3 V	0.5		V max
		V_{DD} = 5 V	0.8	0.8	V max
Logic Input High Voltage	V_{IH}	CLK Only	80% V_{DD}	4.0	V min
			2.1–2.4	2.4	V min
Input Leakage Current	I_{IL}		1	1	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 7]					
Clock Frequency	f_{CLK}		11	16.6	MHz max
Clock Width High	t_{CH}		45	30	ns min
Clock Width Low	t_{CL}		45	30	ns min
$\overline{CS}$ to Clock Set Up	t_{CSS}		10	5	ns min
Clock to $\overline{CS}$ Hold	t_{CSH}		20	15	ns min
Load DAC Pulsewidth	t_{LDAC}		45	30	ns min
Data Setup	t_{DS}		15	10	ns min
Data Hold	t_{DH}		10	5	ns min
Load Setup to $\overline{CS}$	t_{LDS}		0	0	ns min
Load Hold to $\overline{CS}$	t_{LDH}		20	15	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H	2	2	V/µs typ
Settling Time[8]	t_S	To ±0.1% of Full Scale	6	6	µs typ
Shutdown Recovery	t_{SDR}		6	6	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	150	150	nVs typ
Digital Feedthrough	Q_{DF}		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} + 1 V p-p, Data = 000_H, f = 100 kHz	–63	–63	dB typ
SUPPLY CHARACTERISTICS					
Shutdown Supply Current	I_{DD_SD}	No Load	30/60	30/60	µA typ/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load	1.5/2.5	1.6/2.7	mA typ/max
Negative Supply Current	I_{SS}	V_{IL} = 0 V, No Load	1.5/2.5	1.6/2.7	mA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	5	16	mW typ
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

NOTES

[1]One LSB = V_{REF}/4096 V for the 12-bit AD7398.

[2]The first eight codes (000_H, 007_H) are excluded from the linearity error measurement in single supply operation.

[3]These parameters are guaranteed by design and not subject to production testing.

[4]When V_{REF} is connected to either the V_{DD} or the V_{SS} power supply the corresponding V_{OUT} voltage will program between ground and the supply voltage minus the offset voltage of the output buffer, which is the same as the V_{ZSE} error specification. See additional discussion in the Operation section of the data sheet.

[5]Input resistance is code-dependent.

[6]Typicals represent average readings measured at 25°C.

[7]All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

[8]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

AD7399 10-BIT VOLTAGE OUTPUT DAC

(@ V_{DD} = 5 V, V_{SS} = 0 V; or V_{DD} = +5 V, V_{SS} = –5 V, V_{REF} = +2.5 V, –40°C < T_A < +125°C, unless otherwise noted.)

Parameter	Symbol	Condition	3 V–5 V ± 10%	±5 V ± 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		10	10	Bits
Relative Accuracy[2]	INL		±1	±1	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	7	±4	mV max
Full-Scale Voltage Error	V_{FSE}	Data = $3FF_H$	±15	±15	mV max
Full-Scale Tempco[3]	TCV_{FS}		1.5	1.5	ppm/°C typ
REFERENCE INPUT					
V_{REF}IN Range[4]	V_{REF}		0/V_{DD}	V_{SS}/V_{DD}	V min/max
Input Resistance[5]	R_{REF}	Data = 155_H, Worst-Case	40	40	kΩ typ[6]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current	I_{OUT}	Data = 200_H, ΔV_{OUT} = 1 LSB		±5	mA typ
Capacitive Load[3]	C_L	No Oscillation	200	400	pF max
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}	V_{DD} = 3 V	0.5		V max
		V_{DD} = 5 V	0.8	0.8	V max
Logic Input High Voltage	V_{IH}	CLK Only	80% V_{DD}	4.0	V min
			2.1–2.4	2.4	V min
Input Leakage Current	I_{IL}		1	1	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 7]					
Clock Frequency	f_{CLK}		11	16.6	MHz max
Clock Width High	t_{CH}		45	30	ns min
Clock Width Low	t_{CL}		45	30	ns min
$\overline{CS}$ to Clock Set Up	t_{CSS}		10	5	ns min
Clock to $\overline{CS}$ Hold	t_{CSH}		20	15	ns min
Load DAC Pulsewidth	t_{LDAC}		45	30	ns min
Data Setup	t_{DS}		15	10	ns min
Data Hold	t_{DH}		10	5	ns min
Load Setup to $\overline{CS}$	t_{LDS}		0	0	ns min
Load Hold to $\overline{CS}$	t_{LDH}		20	15	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to $3FF_H$ to 000_H	2	2	V/µs typ
Settling Time[8]	t_S	To ±0.1% of Full Scale	6	6	µs typ
Shutdown Recovery	t_{SDR}		6	6	µs typ
DAC Glitch	Q	Code $1FF_H$ to 200_H to $1FF_H$	150	150	nVs typ
Digital Feedthrough	Q_{DF}		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} + 1 V p-p, Data = 000_H, f = 100 kHz	–63	–63	dB typ
SUPPLY CHARACTERISTICS					
Shutdown Supply Current	I_{DD_SD}	No Load	30/60	30/60	µA typ/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load	1.5/2.5	1.6/2.7	mA typ/max
Negative Supply Current	I_{SS}	V_{IL} = 0 V, No Load	1.5/2.5	1.6/2.7	mA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	5	16	mW typ
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

NOTES

[1]One LSB = V_{REF}/1024 V for the 10-bit AD7399.

[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement in single supply operation.

[3]These parameters are guaranteed by design and not subject to production testing.

[4]When V_{REF} is connected to either the V_{DD} or the V_{SS} power supply the corresponding V_{OUT} voltage will program between ground and the supply voltage minus the offset voltage of the output buffer, which is the same as the V_{ZSE} error specification. See additional discussion in the Operation section of the data sheet.

[5]Input resistance is code-dependent.

[6]Typicals represent average readings measured at 25°C.

[7]All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

[8]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . –0.3 V, +7 V
V_{SS} to GND . . . . . +0.3 V, –7 V
V_{REF} to GND . . . . . V_{SS}, V_{DD}
Logic Inputs to GND . . . . . –0.3 V, +8 V
V_{OUT} to GND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND . . . . . 50 mA
Thermal Resistance θ_{JA}
16-Lead SOIC Package (R-16) . . . . . 158°C/W
16-Lead Thin Shrink Surface Mount (RU-16) . . . 180°C/W
Maximum Junction Temperature (T_J Max) . . . . . 150°C
Package Power Dissipation . . . . . (T_J Max–T_A)/θ_{JA}
Operating Temperature Range . . . . . –40°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature
R-16 (Vapor Phase, 60 secs) . . . . . 215°C
RU-16 (Infrared, 15 secs) . . . . . 224°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Resolution (Bits)	Temperature Range	Package Description	Package Option	Container Quantity
AD7398BR	12	–40°C to +125°C	SOL-16	R-16	48
AD7398BR-REEL7	12	–40°C to +125°C	SOL-16	R-16	1,000
AD7398BRU-REEL7	12	–40°C to +125°C	TSSOP-16	RU-16	1,000
AD7399BR	10	–40°C to +125°C	SOL-16	R-16	48
AD7399BR-REEL7	10	–40°C to +125°C	SOL-16	R-16	1,000
AD7399BRU-REEL7	10	–40°C to +125°C	TSSOP-16	RU-16	1,000

The AD7398 contains 3254 transistors. The die size measures 108 mil × 144 millimeters.

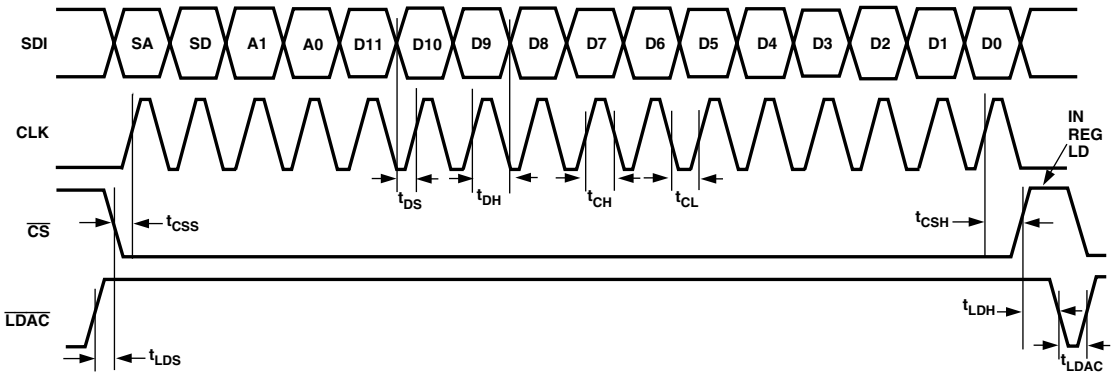


Figure 2. AD7398 Timing Diagram (AD7399 with SDI = 14 Bits Only)

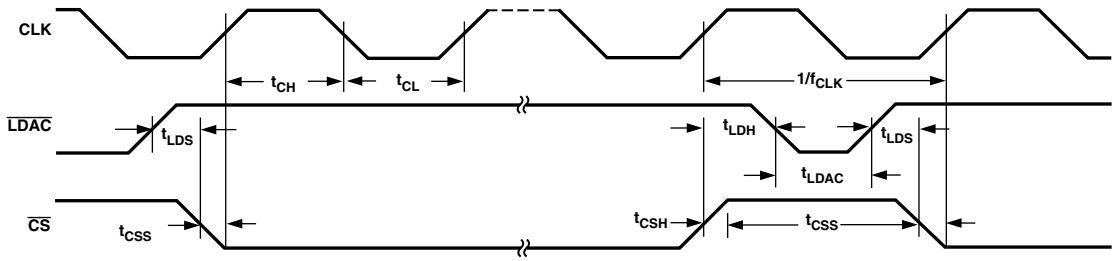
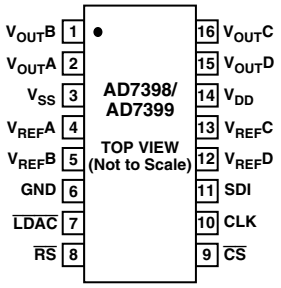


Figure 3. Continuous Clock Timing Diagram

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7398/AD7399 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$V_{OUT}B$	DAC B Voltage Output.
2	$V_{OUT}A$	DAC A Voltage Output.
3	V_{SS}	Negative Power Supply Input. Specified range of operation 0 V to –5.5 V.
4	$V_{REF}A$	DAC A Reference Voltage Input Terminal. Establishes DAC A full-scale output voltage. Pin can be tied to V_{DD} or V_{SS} pin.
5	$V_{REF}B$	DAC B Reference Voltage Input Terminal. Establishes DAC B full-scale output voltage. Pin can be tied to V_{DD} or V_{SS} pin.
6	GND	Ground Pin.
7	$\overline{LDAC}$	Load DAC Register Strobe, Level Sensitive Active Low. Transfers all Input Register data to DAC registers. Asynchronous active low input. See Control Logic Truth Table for operation.
8	$\overline{RS}$	Resets Input and DAC Registers to All Zero Codes. Shift Register contents unchanged.
9	$\overline{CS}$	Chip Select, Active Low Input. Disables shift register loading when high. Transfers Serial Register Data to the Input Register when $\overline{CS}$ returns High. Does not effect $\overline{LDAC}$ operation.
10	CLK	Schmitt Triggered Clock Input, Positive Edge Clocks Data into Shift Register.
11	SDI	Serial Data Input. Input data loads directly into the shift register.
12	$V_{REF}D$	DAC D Reference Voltage Input Terminal. Establishes DAC D full-scale output voltage. Pin can be tied to V_{DD} or V_{SS} pin.
13	$V_{REF}C$	DAC C Reference Voltage Input Terminal. Establishes DAC C full-scale output voltage. Pin can be tied to V_{DD} or V_{SS} pin.
14	V_{DD}	Positive Power Supply Input. Specified range of operation 3 V to 5 V ± 10%.
15	$V_{OUT}D$	DAC D Voltage Output.
16	$V_{OUT}C$	DAC C Voltage Output.

Table I. Control Logic Truth Table

$\overline{CS}$	CLK	$\overline{LDAC}$	Serial Shift Register Function	Input Register Function	DAC Register
H	X	H	No Effect	No Effect	No Effect
L	L	H	No Effect	No Effect	No Effect
L	↑+	H	Shift-Register-Data Advanced One Bit	Latched	Latched
L	H	H	No Effect	Latched	Latched
↑+	L/H	H	No Effect	Updated with SR Contents	Latched
H	X	L	No Effect	Latched	Transparent
H	X	↑+	No Effect	Latched	Latched

NOTES
1. ↑+ Positive logic transition; ↓– Negative logic transition; X Don't Care; SR shift register.
2. At power ON, both the Input Register and the DAC Register are loaded with all zeros.
3. During Power Shutdown, reprogramming of any internal registers can take place, but the output amplifiers will not produce the new values until the part is taken out of Shutdown mode.
4. $\overline{LDAC}$ input is a level-sensitive input that controls the four DAC registers.

Table II. AD7398 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format

	MSB															**LSB**
Bit Position	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
AD7398	SA	SD	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

NOTE
Bit positions B14 and B15 are power shutdown control Bits SD and SA. If SA is set to Logic 1, all DACs are placed in the power shutdown mode. If SD is set to Logic 1, the address decoded by Bits B12 and B13 (A0 and A1) determine the DAC channel that will be placed in the power shutdown state.

Table III. AD7399 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format

	MSB													**LSB**
Bit Position	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
AD7399	SA	SD	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

NOTE
Bit positions B12 and B13 are power shutdown control Bits SD and SA. If SA is set to Logic 1, all DACs are placed in the power shutdown mode. If SD is set to Logic 1, the address decoded by Bits B10 and B11 (A0 and A1) determine the DAC channel that will be placed in the power shutdown state.

Table IV. AD7398/AD7399 Address Decode Control

SA	SD	A1	A0	DAC Channel Affected
1	X	X	X	All DACs Shutdown
0	1	0	0	DAC A Shutdown
0	1	0	1	DAC B Shutdown
0	1	1	0	DAC C Shutdown
0	1	1	1	DAC D Shutdown
0	0	0	0	DAC A Input Register Decoded
0	0	0	1	DAC B Input Register Decoded
0	0	1	0	DAC C Input Register Decoded
0	0	1	1	DAC D Input Register Decoded

TERMINOLOGY

Relative Accuracy, INL

For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL versus code plot can be seen in TPC 1.

Differential Nonlinearity, DNL

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. TPC 3 illustrates a typical DNL versus code plot.

Zero-Scale Error, V_{ZSE}

Zero-scale error is a measure of the output voltage error from zero voltage when zero code is loaded to the DAC register.

Full-Scale Error, V_{FSE}

Full-scale error is a measure of the output voltage error from full-scale voltage when full-scale code is loaded to the DAC register.

Full-Scale Temperature Coefficient, TC_{VFS}

This is a measure of the change in full-scale error with a change in temperature. It is expressed in ppm/°C or mV/°C.

DAC Glitch Impulse, Q

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (midscale transition). A plot of the glitch impulse is shown in TPC 10.

Digital Feedthrough, Q_{DF}

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. $\overline{CS}$ is held high, while the CLK and SDI signals are toggled. It is specified in nV-s and is measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa. A typical plot of digital feedthrough is shown in TPC 11.

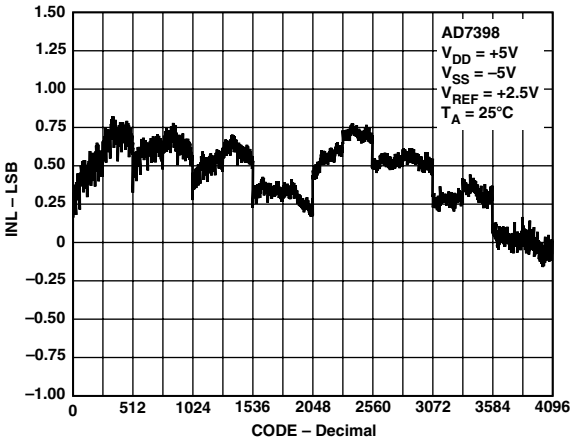
Power Supply Sensitivity, PSS

This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power supply sensitivity is quoted in terms of % change in output per % change in V_{DD} for full-scale output of the DAC. V_{DD} is varied by ±10%.

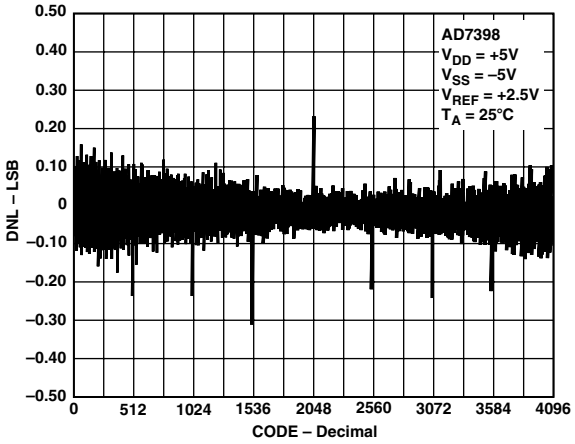
Reference Feedthrough, V_{OUT}/V_{REF}

This is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100 kHz, 1 V p-p is applied to V_{REF}. Reference feedthrough is expressed in dB or mV p-p.

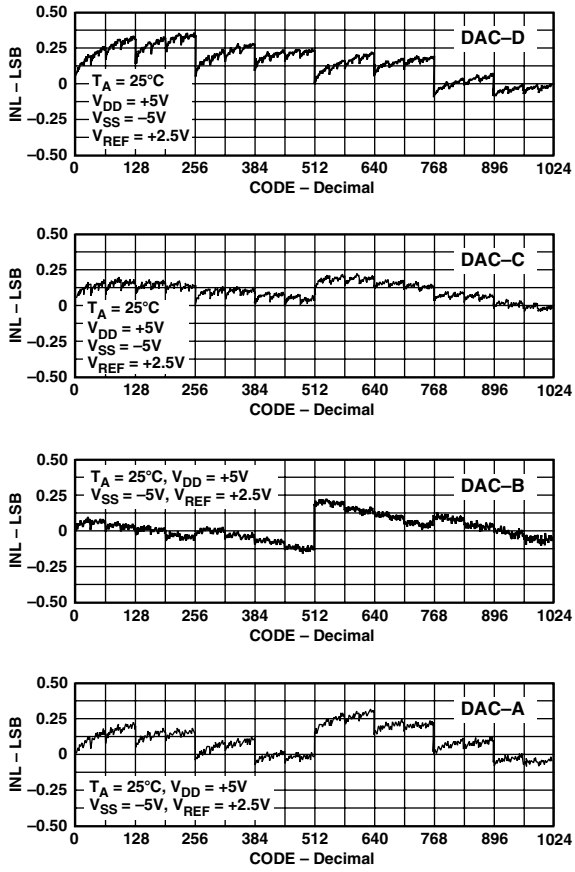
AD7398/AD7399–Typical Performance Characteristics



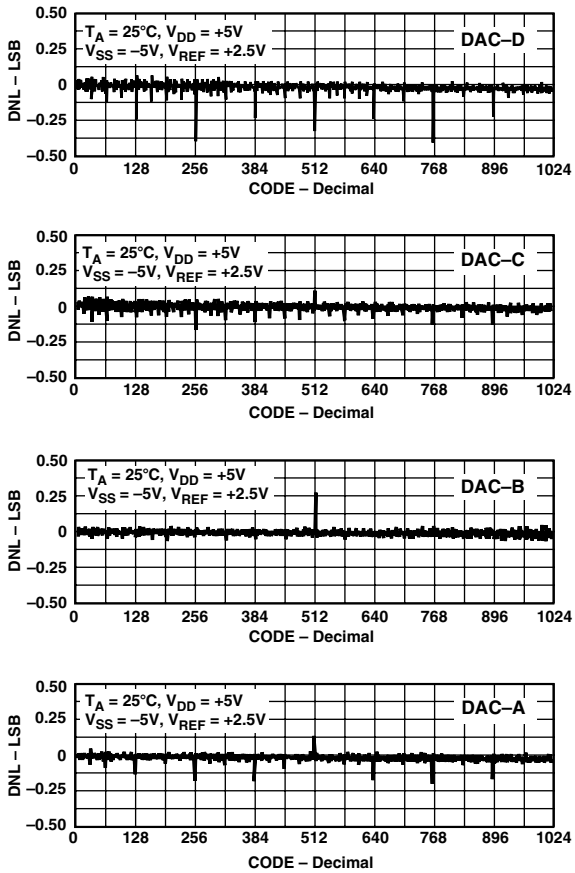
TPC 1. AD7398 INL vs. Code (T_A = 25°C)



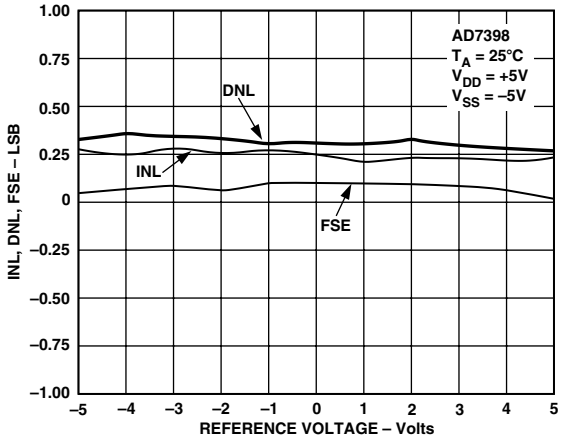
TPC 3. AD7398 DNL vs. Code (T_A = 25°C)



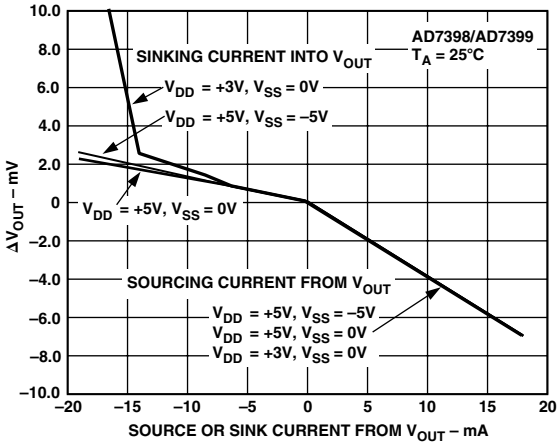
TPC 2. AD7399 INL vs. Code (T_A = 25°C)



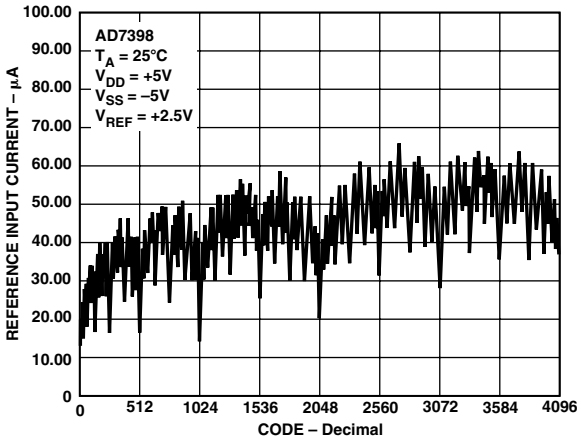
TPC 4. AD7399 DNL vs. Code (T_A = 25°C)



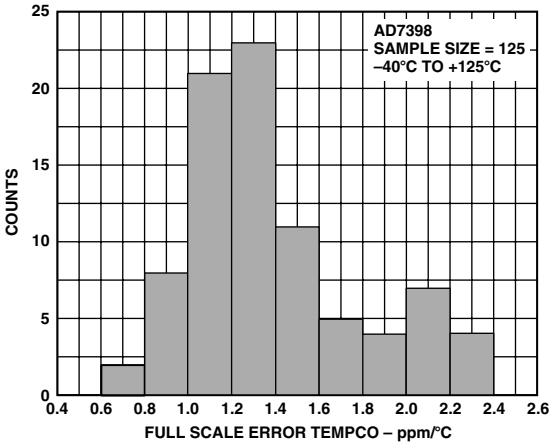
TPC 5. AD7398 INL, DNL, FSE vs. Reference Voltage



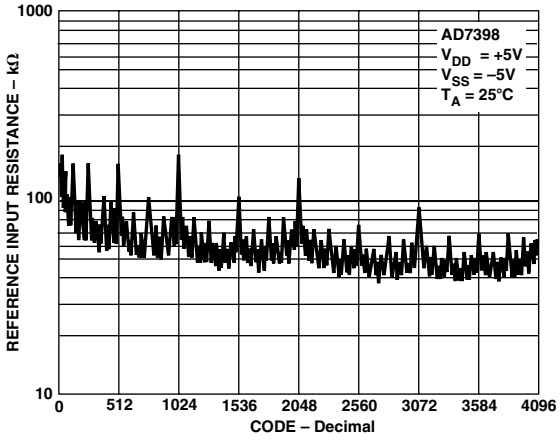
TPC 8. ΔV_{OUT} vs. Load Current



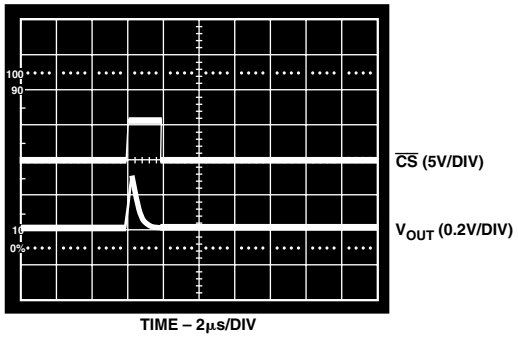
TPC 6. AD7398 Reference Input Current vs. Code



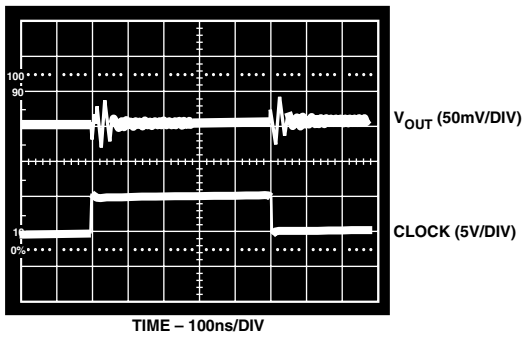
TPC 9. AD7398 Full-Scale Error Tempco



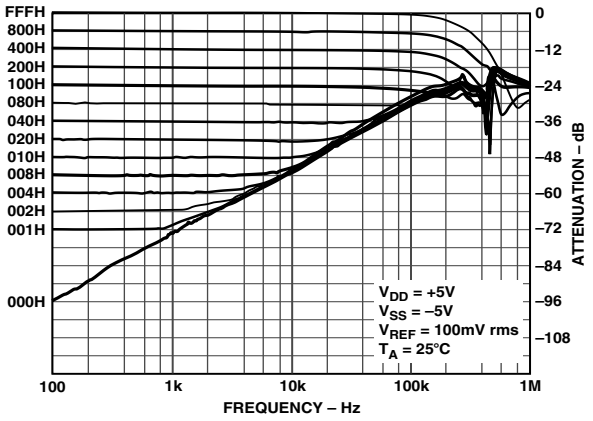
TPC 7. AD7398 Reference Input Resistance vs. Code



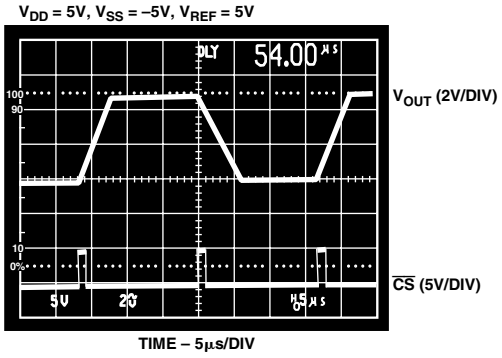
TPC 10. AD7398 Midscale Glitch



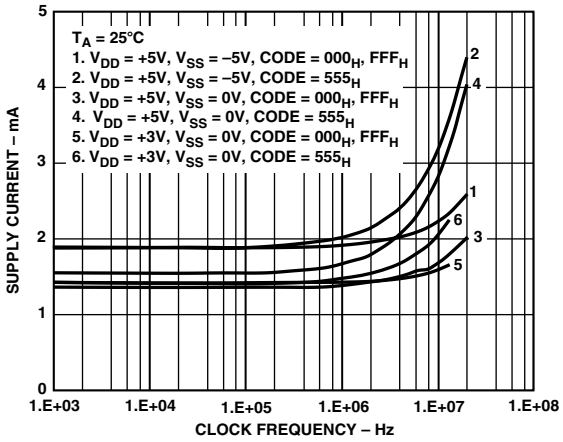
TPC 11. AD7398 Digital Feedthrough



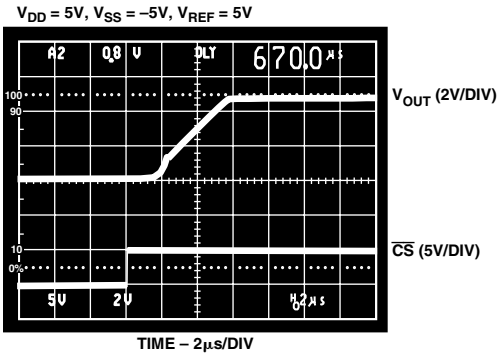
TPC 14. AD7398 Multiplying Gain vs. Frequency



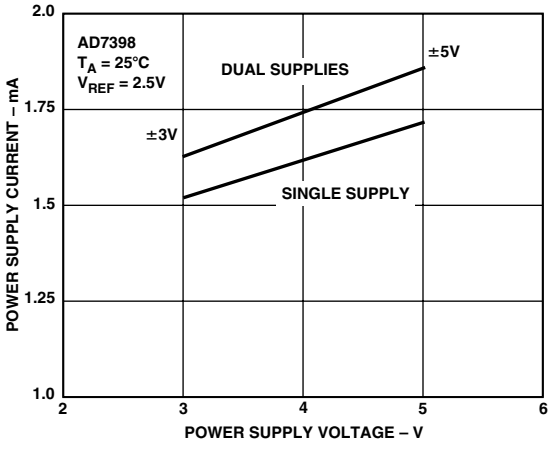
TPC 12. AD7398 Large Signal Settling Time



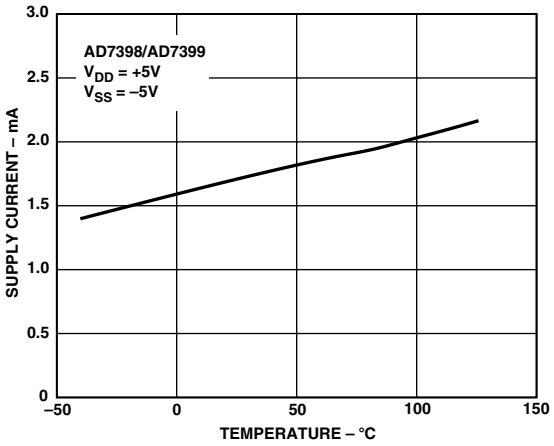
TPC 15. AD7398 Supply Current vs. Clock Frequency



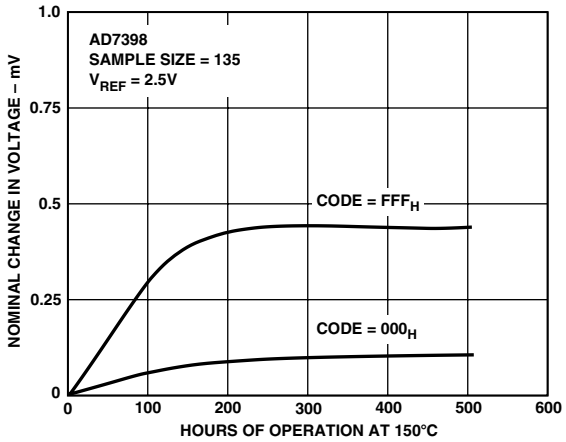
TPC 13. AD7398 Shutdown Recovery



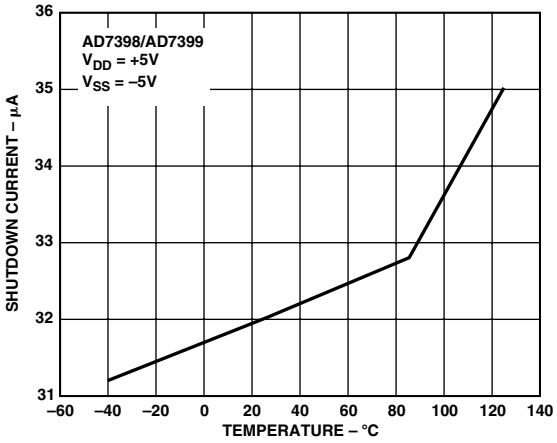
TPC 16. AD7398 Supply Current vs. Supply Voltage



TPC 17. Supply Current vs. Temperature



TPC 19. AD7398 Long-Term Drift



TPC 18. Shutdown Current vs. Temperature

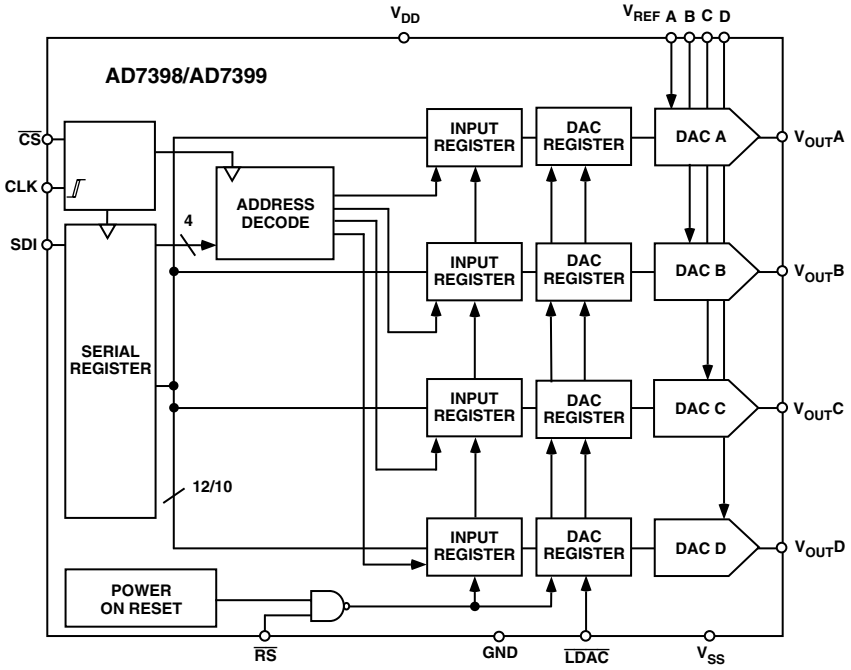


Figure 4. Simplified Block Diagram

CIRCUIT OPERATION

The AD7398 and AD7399 contain four, 12-bit and 10-bit, voltage-output, digital-to-analog converters respectively. Each DAC has its own independent multiplying reference input. Both AD7398/AD7399 use 3-wire SPI-compatible serial data interface, with an asynchronous $\overline{RS}$ pin for zero-scale reset. In addition, a $\overline{LDAC}$ strobe enables four channel simultaneous updates for hardware synchronized output voltage changes.

D/A Converter Section

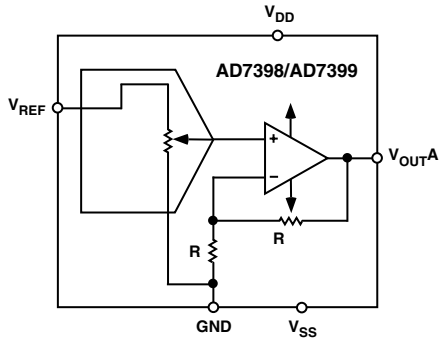


Figure 5. Simplified DAC Channel

DAC OPERATION

The internal R-2R ladder of the AD7398 and AD7399 operate in the voltage switching mode maintaining an output voltage that is the same polarity as the input reference voltage. A proprietary scaling technique is used to attenuate the input reference voltage in the DAC. The output buffer amplifies the internal DAC output to achieve a V_{REF} to V_{OUT} gain of unity.

The nominal DAC output voltage is determined by the externally applied V_{REF} and the digital data (D) as:

$$V_{OUT} = V_{REF} \times \frac{D}{4096} \quad \text{(For AD7398)} \tag{1}$$

$$V_{OUT} = V_{REF} \times \frac{D}{1024} \quad \text{(For AD7399)} \tag{2}$$

Where *D* is the 12-bit or 10-bit decimal equivalent of the data word. V_{REF} is the externally applied reference voltage.

In order to maintain good analog performance, bypass power supplies with 0.01 µF ceramic capacitors (mount them close to the supply pins) and 1 µF–10 µF Tantalum capacitors in parallel. In additions, clean power supplies with low ripple voltage capability should be used. Switching power supplies may be used for this application but beware of its higher ripple voltage and PSS frequency-dependent characteristics. It is also best to supply the AD7398/AD7399's power from the system's analog supply voltages. (Don't use the digital 5 V supply).

The reference input resistance is code dependent exhibiting worst case 35 kΩ for AD7398 when the DAC is loaded with alternating codes 010101010101. Similarly, the reference input resistance is 40 kΩ for AD7399 when the DAC is loaded with 0101010101.

OPERATION WITH V_{REF} EQUAL TO THE SUPPLY

The AD7398/AD7399 is designed to approach the full output voltage swing from ground to V_{DD} or V_{SS}. The maximum output swing is achieved when the corresponding V_{REF} input pin is tied to the same power supply. This power supply should be low noise and low ripple, preferably operated by a suitable reference voltage source such as ADR292 and REF02. The output swing

is limited by the internal buffer offset voltage and the output drive current capability of the output stage. One should at least budget the V_{ZSE} offset voltage as the closest the output voltage can get to either supply voltage under a no load condition. Under a loaded output, degrade the headroom by a factor of 2 mV per 1 mA of load current. Also note that the internal op amp has an offset voltage so that the first eight codes of AD7398 may not respond at either the supply voltage or at ground until the internal DAC voltage exceeds the output buffers offset voltage. Similarly, the first two codes of AD7399 should not be used.

POWER SUPPLY SEQUENCING

V_{DD}/V_{SS} of AD7398/AD7399 should be powered from the system analog supplies. In addition, V_{IN} of the external reference should also be coming from the same supply. Such practice will avoid a possible latch-up when the reference is powered on prior to V_{DD}/V_{SS}, or powered off subsequent to V_{DD}/V_{SS}. If V_{DD}/V_{SS} and V_{REF} are separate power sources, then ensure V_{DD}/V_{SS} is powered on before V_{REF} and powered off after V_{REF}. In addition, V_{REF} pins of the unused DACs should also be connected to GND or some power sources to ensure similar power-up/-down sequence.

PROGRAMMABLE POWER SHUTDOWN

The two MSBs of the serial input register, SA and SD, are used to program various shutdown modes. If SA is set to Logic 1, all DACs will be in shutdown mode. If SA = 0 and SD = 1, a corresponding DAC will be shut down addressed by Bits A0 and A1, See Tables II–IV.

WORST CASE ACCURACY

Assuming a perfect reference, the worst-case output voltage may be calculated from the following equation.

$$V_{OUT} = \frac{D}{2^N} \times (V_{REF} + V_{FSE}) + V_{ZSE} + INL \quad (3)$$

where

D = Decimal Code Loaded to DAC Ranges $0 \le D \le 2^N-1$
N = Number of Bits
V_{REF} = Applied Reference Voltage
V_{FSE} = Full-Scale Error in Volts
V_{ZSE} = Zero-Scale Error in Volts
INL = Integral Nonlinearity in Volts INL is 0 at Full Scale or Zero Scale

SERIAL DATA INTERFACE

The AD7398/AD7399 uses a 3-wire ($\overline{CS}$, SDI, CLK) SPI-compatible serial data interface. Serial data of the AD7398 and AD7399 is clocked into the serial input register in a 16-bit and 14-bit data-word format respectively. MSB bits are loaded first. Table II defines the 16 data-word bits for AD7398. Table III defines the 14 data-word bits for the AD7399. Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the Interface Timing specifications. Data can only be clocked in while the $\overline{CS}$ chip select pin is active low. For the AD7398, only the last 16 bits which are clocked into the serial register, will be interrogated when the $\overline{CS}$ pin returns to the logic high state, extra data bits are ignored. For the AD7399, only the last 14 bits, which are clocked into the serial register, will be interrogated when the $\overline{CS}$ pin returns to the logic high state. Since most microcontrollers' output serial data is in 8-bit bytes, two right-justified data bytes can be written to the AD7398 and AD7399. Keeping the $\overline{CS}$ line low between the first and second bytes transfer will result in a successful serial register update.

Once the data is properly aligned in the shift register, the positive edge of the $\overline{CS}$ initiates the transfer of new data to the target DAC register, determined by the decoding of address Bits A1 and A0. For the AD7398, Tables I, II, IV, and Figures 2 and 3 define the characteristics of the software serial interface. For the AD7399, Tables I, III, IV, and Figure 3 (with 14-bits exception) define the characteristics of the software serial interface. Figures 6 and 7 show the equivalent logic interface for the key digital control pins for AD7398 and AD7399.

An asynchronous $\overline{RS}$ provides hardware control reset to zero-code state over the preset function and DAC Register loading. If this function is not needed, the $\overline{RS}$ pin can be tied to logic high.

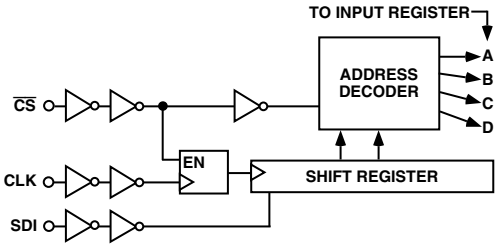


Figure 6. Equivalent Logic Interface

POWER-ON RESET

When the V_{DD} power supply is turned ON, an internal reset strobe forces all the Input and DAC registers to the zero-code state. The V_{DD} power supply should have a smooth positive ramp without drooping in order to have consistent results, especially in the region of V_{DD} = 1.5 V to 2.2 V. The V_{SS} supply has no effect on the power-on reset performance. The DAC register data will stay at zero until a valid serial register data load takes place.

ESD Protection Circuits

All logic input pins contain back-biased ESD protection Zeners connected to ground (GND) and V_{DD} as shown in Figure 7.

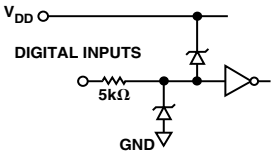


Figure 7. Equivalent ESD Protection Circuits

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7398/AD7399 is via a serial bus that uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a 3-wire interface consisting of a clock signal, a data signal and a synchronization signal. The AD7398/AD7399 requires a 16-bit/14-bit data word with data valid on the rising edge of CLK. The DAC update may be done automatically when all the data is clocked in, or it may be done under control of $\overline{LDAC}$.

ADSP-2101/ADSP-2103 to AD7398/AD7399 Interface

Figure 8 shows a serial interface between the AD7398/AD7399 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 is set to operate in the SPORT (Serial Port) transmit alternate framing mode. The ADSP-2101/ADSP-2103 is programmed through the SPORT control register and should be configured as follows: Internal Clock Operation, Active Low Framing, 16-Bit-Word Length. For the AD7398, transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. For the AD7399, the first two bits are don't care as the AD7399 will keep the last 14 bits. Similarly, transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. Because of the edge-triggered difference, an inverter is required at the SCLKs between the DSP and the DAC.

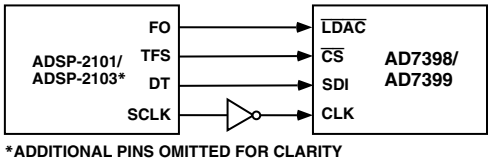


Figure 8. ADSP-2101/ADSP-2103 to AD7398/AD7399 Interface

68HC11 to AD7398/AD7399 Interface

Figure 9 shows a serial interface between the AD7398/AD7399 and the 68HC11 microcontroller. SCK of the 68HC11 drives the CLK of the DAC, while the MOSI output drives the serial data lines SDI. $\overline{CS}$ signal is driven from one of the port lines. The 68HC11 is configured for master mode; MSTR = 1, CPOL = 0, and CPHA = 0. Data appearing on the MOSI output is valid on the rising edge of SCK.

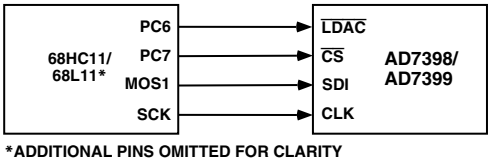


Figure 9. 68HC11/68L11 to AD7398/AD7399 Interface

MICROWIRE to AD7398/AD7399 Interface

Figure 10 shows an interface between the AD7398/AD7399 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and into the AD7398/AD7399 on the rising edge of the serial clock. No glue logic is required as the DAC clocks data into the input shift register on the rising edge.

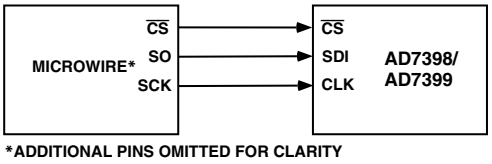


Figure 10. MICROWIRE to AD7398/AD7399 Interface

80C51/80L51 to AD7398/AD7399 Interface

A serial interface between the AD7398/AD7399 and the 80C51/80L51 microcontroller is shown in Figure 11. TxD of the microcontroller drives the CLK of the AD7398/AD7399, while RxD drives the serial data line of the DAC. P3.3 is a bit programmable pin on the serial port which is used to drive $\overline{CS}$.

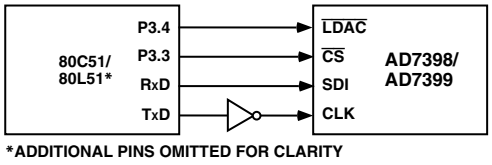


Figure 11. 80C51/80L51 to AD7398/AD7399 Interface

Note that the 80C51/80L51 provides the LSB first, while the AD7398/AD7399 expect the MSB of the 16-bit/14-bit word first. Care should be taken to ensure the transmit routine takes this into account. It can usually be done through software by shifting out and accumulating the bits in the correct order before inputting to the DAC. In addition, 80C51 outputs two byte words/16 bits data, thus for AD7399, the first two bits, after rearrangement, should be Don't Care as they will be dropped from the AD7399's 14-bit word.

When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is valid on the falling edge of TxD, so the clock must be inverted as the DAC clocks data into the input shift register on the rising edge of the serial clock. The 80C51/80L51 transmits its data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. As AD7399 requires a 14-bit word, P3.3 (or any one of the other programmable bits) is the $\overline{CS}$ input signal to the DAC, so P3.3 should be brought low at the beginning of the 16-bit write cycle 2×8 bit words, and held low until the 16-bit 2×8 cycle is completed. After that, P3.3 is brought high again and the new data loads to the DAC. Again, the first two bits, after rearranging, should be don't care. $\overline{LDAC}$ on the AD7398/AD7399 may also be controlled by the 80C51/80L51 serial port output by using another bit-programmable pin, P3.4.

APPLICATIONS

STAIRCASE WINDOWS COMPARATOR

Many applications need to determine whether voltage levels are within predetermined limits. Some requirements are for non-overlapping windows and others for overlapping windows. Both circuit configurations are shown in Figures 12 and 13 respectively.

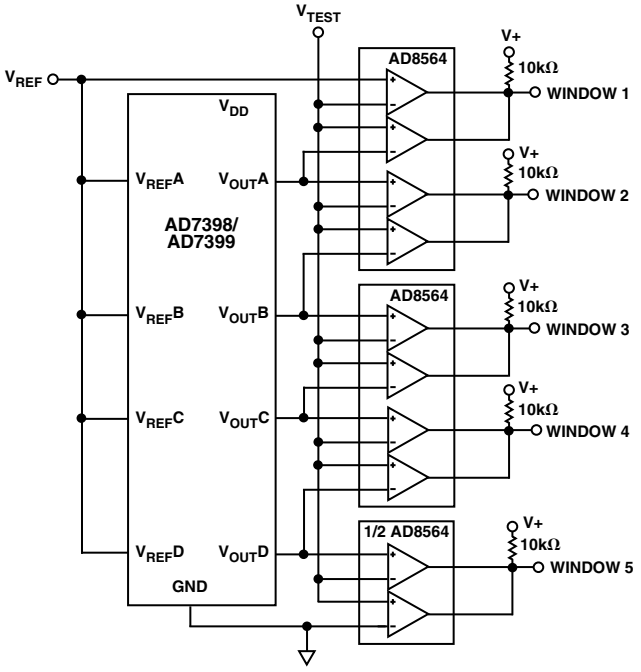


Figure 12. Nonoverlapping Windows Comparator

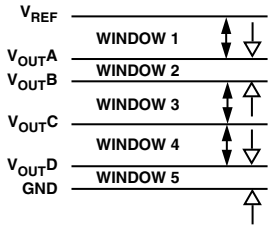


Figure 13. Nonoverlapping Windows Range

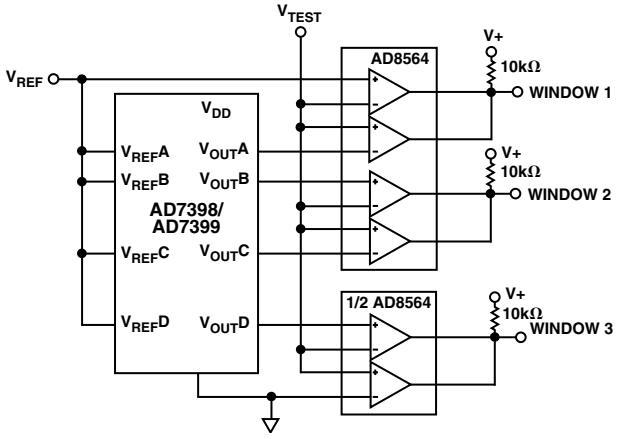


Figure 14. Overlapping Windows Comparator

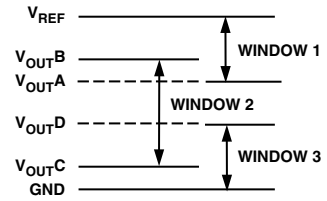


Figure 15. Overlapping Windows Range

The nonoverlapping circuit employs one AD7398/AD7399 and ten comparators to achieve five voltage windows. These windows range between V_{REF} and analog ground as shown in Figure 13. Similarly, the overlapping circuit employs six comparators to achieve three overlapping windows, Figure 15.

PROGRAMMABLE DAC REFERENCE VOLTAGE

With AD7398/AD7399's flexibility, one of the internal DACs can be used to control a common programmable V_{REFX} for the rest of the DACs.

The circuit configuration is shown in Figure 16. The relationship of V_{REFX} to V_{REF} is dependent upon the digital code and the ratio of R1 and R2, and is given by:

$$V_{REFX} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) - V_{REFX} \times \frac{D}{2^N} \times \frac{R2}{R1} \quad (5)$$

$$V_{REFX} = \frac{V_{REF} \times \left(1 + \frac{R2}{R1}\right)}{\left(1 + \frac{D}{2^N} \times \frac{R2}{R1}\right)} \quad (6)$$

Where D = Decimal Equivalent of Input Code
N = Number of Bits
V_{REF} = Applied External Reference
V_{REFX} = Reference Voltage for DAC A to D

Table V. V_{REFX} vs. R1 and R2

R1, R2	Digital Code	V_{REFX}
R1 = R2	0000 0000 0000	2 V_{REF}
R1 = R2	1000 0000 0000	1.3 V_{REF}
R1 = R2	1111 1111 1111	V_{REF}
R1 = 3R2	0000 0000 0000	4 V_{REF}
R1 = 3R2	1000 0000 0000	1.6 V_{REF}
R1 = 3R2	1111 1111 1111	V_{REF}

The accuracy of V_{REFX} will be affected by the quality of R1 and R2 and therefore, tight tolerance low tempco thin film resistors should be used.

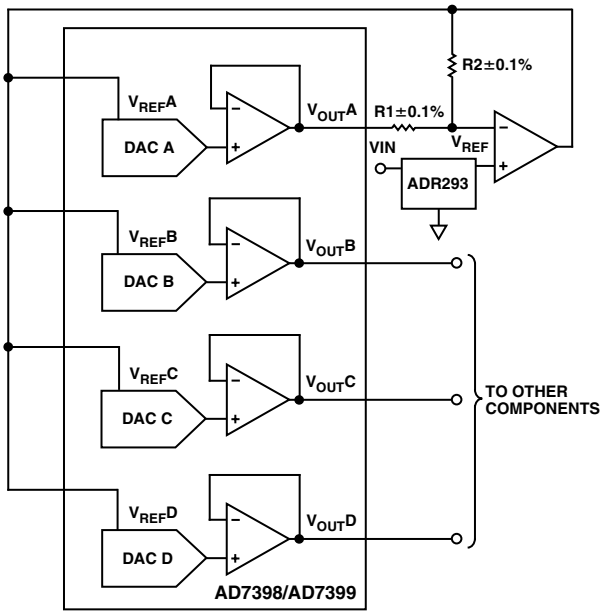
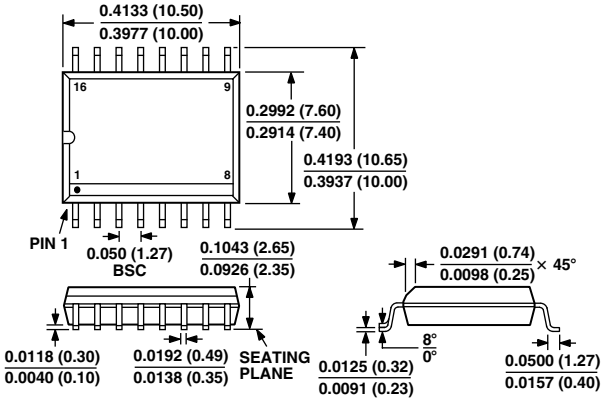


Figure 16. Programmable DAC Reference

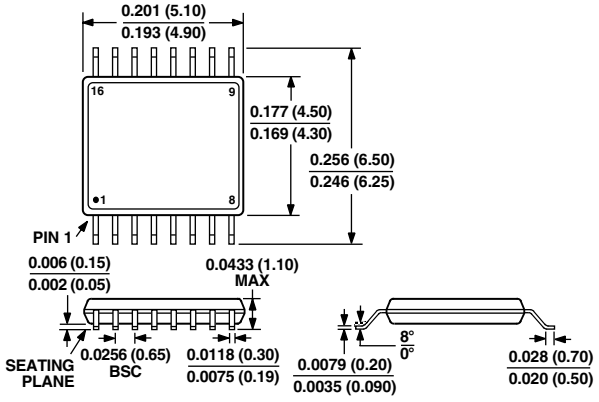
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Wide SOIC (R-16)



16-Lead TSSOP (RU-16)



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