Differential Input, 100kSPS, 12-Bit ADC in 8-lead SOT-23

Preliminary Technical Data — AD7456

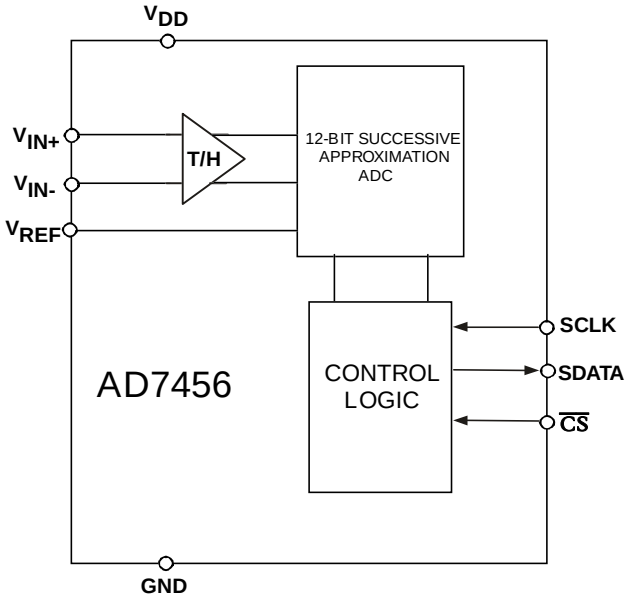
FEATURES

Specified for V_{DD} of 3 V and 5 V
Very Low Power:
TBD mW typ at 100kSPS with 3 V Supplies
TBD mW typ at 100kSPS with 5 V Supplies
Fully Differential Analog Input
Wide Input Bandwidth:
70dB SINAD at 20kHz Input Frequency
No Pipeline Delays
Serial Interface - SPI™/QSPI™/MICROWIRE™/ DSP Compatible
Automatic Power-Down Mode
8 Pin SOT-23 and µSOIC Package

APPLICATIONS

Transducer Interface
Battery Powered Systems
Data Acquisition Systems
Portable Instrumentation
Motor Control
Communications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7456 is a 12-bit, low power, successive-approximation (SAR) analog-to-digital converter that features a fully differential analog input. This part operates from a single 3 V or 5 V power supply and features throughput rates up to 100kSPS.

The part contains a low-noise, wide bandwidth, differential track and hold amplifier (T/H) which can handle input frequencies in excess of 1MHz with the -3dB point being 20MHz typically. The reference voltage is applied externally to the V_{REF} pin and can be varied from 100 mV to 3.5 V depending on the power supply and what suits the application. The value of the reference voltage determines the common mode voltage range of the part. With this truly differential input structure and variable reference input, the user can select a variety of input ranges and bias points.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock allowing the device to interface with Microprocessors or DSPs. The device is powered up on the falling edge of $\overline{CS}$ and a conversion is initiated on the rising edge of $\overline{CS}$, where the analog input is sampled. Once a conversion is complete, the device automatically enters a power down mode to reduce power dissipation between conversions.

The SAR architecture of this part ensures that there are no pipeline delays.

PRODUCT HIGHLIGHTS

1. Operation with either 3 V or 5 V power supplies.
2. Low Power Consumption.
   With a 3V supply, the AD7456 offer TBDmW typ power consumption for 100kSPS throughput.
3. Fully Differential Analog Input.
4. Variable Voltage Reference Input.
5. No Pipeline Delay.
6. Accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.
7. 8-lead SOT-23 package.
8. ENOB > 8 bits typically with 100mV reference.

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SPI and QSPI are trademarks of Motorola, Inc.

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AD7456 - SPECIFICATIONS[1]

(V_{DD} = 2.7V to 3.6V, f_{SCLK} = 12MHz, f_S = 100kHz, V_{REF} = 2.0 V; F_{IN} = 20kHz; V_{DD} = 4.75V to 5.25V, f_{SCLK} = 12MHz, f_S = 100kHz, V_{REF} = 2.5 V; F_{IN} = 20kHz; V_{CM}[3] = V_{REF}; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Test Conditions/Comments	B Version[1]	Unit
DYNAMIC PERFORMANCE			
Signal to (Noise + Distortion) (SINAD)[2]	V_{DD} = 5V	70	dB min
	V_{DD} = 3V	68	dB min
Total Harmonic Distortion (THD)[2]	V_{DD} = 5V, -80dB typ	-75	dB max
	V_{DD} = 3V, -78dB typ	-73	dB max
Peak Harmonic or Spurious Noise[2]	V_{DD} = 5V, -82dB typ	-75	dB max
	V_{DD} = 3V, -80dB typ	-73	dB max
Intermodulation Distortion (IMD)[2]			
Second Order Terms		-85	dB typ
Third Order Terms		-85	dB typ
Aperture Delay[2]		10	ns typ
Aperture Jitter[2]		50	ps typ
Full Power Bandwidth[2]	@ -3 dB	20	MHz typ
	@ -0.1 dB	2.5	MHz typ
DC ACCURACY			
Resolution		12	Bits
Integral Nonlinearity (INL)[2]		±1	LSB max
Differential Nonlinearity (DNL)[2]	Guaranteed No Missed Codes to 12 Bits.	±1	LSB max
Zero Code Error[2]	V_{DD} = 5V	±3	LSB max
	V_{DD} = 3V	±6	LSB max
Positive Gain Error[2]	V_{DD} = 5V	±3	LSB max
	V_{DD} = 3V	±6	LSB max
Negative Gain Error[2]	V_{DD} = 5V	±3	LSB max
	V_{DD} = 3V	±6	LSB max
ANALOG INPUT			
Full Scale Input Span	2 x V_{REF}[4]	V_{IN+} - V_{IN-}	V
Absolute Input Voltage			
V_{IN+}	V_{CM} = V_{REF}	V_{CM}[3] ± V_{REF}/2	V
V_{IN-}	V_{CM} = V_{REF}	V_{CM}[3] ± V_{REF}/2	V
DC Leakage Current		±1	µA max
Input Capacitance	When in Track	20	pF typ
	When in Hold	6	pF typ
REFERENCE INPUT			
V_{REF} Input Voltage	V_{DD} = 5 V (±1% tolerance for specified performance)	2.5[5]	V
	V_{DD} = 3 V (±1% tolerance for specified performance)	2.0[6]	V
DC Leakage Current		±1	µA max
V_{REF} Input Capacitance		15	pF typ
LOGIC INPUTS			
Input High Voltage, V_{INH}		2.4	V min
Input Low Voltage, V_{INL}		0.8	V max
Input Current, I_{IN}	Typically 10nA, V_{IN} = 0VorV_{DD}	±1	µA max
Input Capacitance, C_{IN}[7]		10	pF max
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} = 5V; I_{SOURCE} = 200µA	2.8	V min
	V_{DD} = 3V; I_{SOURCE} = 200µA	2.4	V min
Output Low Voltage, V_{OL}	I_{SINK} =200µA	0.4	V max
Floating-State Leakage Current		±1	µA max
Floating-State Output Capacitance[7]		10	pF max
Output Coding		Two's Complement	

AD7456 - SPECIFICATIONS AD7456

Parameter	Test Conditions/Comments	B Version[1]	Units	
CONVERSION RATE				
Conversion Time	1.33µs with a 12MHz SCLK	16	SCLK cycles	
Track/Hold Acquisition Time[2]	Sine Wave Input	TBD	ns max	
	Step Input	TBD	ns max	
Throughput Rate[9]		100	kSPS max	
POWER REQUIREMENTS				
V_{DD}	Range: 3 V+20%/-10%; 5 V ± 5%	3/5	Vmin/max	
I_{DD}[10]				
Static	V_{DD} =3 V/5 V. SCLK On or Off	0.5	mA typ	
Operational	V_{DD} = 5 V.	TBD	mA max	
	V_{DD} = 3 V.	TBD	mA max	
Power Dissipation				
Operational	V_{DD} =5 V.	TBD	mW max	
	V_{DD} =3 V.	TBD	mW max	

NOTES

[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.

[2]See 'Terminology' section.

[3]Common Mode Voltage. The input signal can be centered on any choice of dc Common Mode Voltage as long as this value is in the range specified in Figures TBD.

[4]Because the input spans of V_{IN+} and V_{IN-} are both V_{REF}, and they are 180° out of phase, the differential voltage is 2 x V_{REF}.

[5]The AD7456 is functional with a reference input from100mV and for V_{DD} = 5V, the reference can range up to 3.5V (see 'Reference Section').

[6]The AD7456 is functional with a reference input from100mV and for V_{DD} = 3V, the reference range up to 2.2V (see 'Reference Section').

[7]Sample tested @ +25°C to ensure compliance.

[9]See 'Serial Interface Section'.

[10]Measured with a midscale DC input.

Specifications subject to change without notice.

AD7456

TIMING SPECIFICATIONS [1,2]

(V_{DD} = 2.7V to 3.6V, f_{SCLK} = 12MHz, f_S = 100kHz, V_{REF} = 2.0 V;
V_{DD} = 4.75V to 5.25V, f_{SCLK} = 12MHz, f_S = 100kHz, V_{REF} = 2.5 V;
V_{CM} [3] = V_{REF}; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} +3V	+5V	Units	Description
f_{SCLK} [4]	10	10	kHz min	
	12	12	MHz max	
$t_{CONVERT}$	16 x t_{SCLK}	16 x t_{SCLK}		t_{SCLK} = 1/f_{SCLK}
	1.33	1.33	µs max	12MHz f_{SCLK}
$t_{POWERUP}$	1.4	1.4	µs min	Power-Up Time
$t_{ACQUISITION}$	1.4	1.4	µs min	Acquisition Time
t_2	10	10	ns min	$\overline{CS}$ Rising Edge to SCLK Falling Edge Setup Time
t_3 [5]	20	20	ns max	Delay from $\overline{CS}$ Rising Edge Until SDATA 3-State Disabled
t_4 [5]	40	40	ns max	Data Access Time After SCLK Falling Edge
t_5	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK High Pulse Width
t_6	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK Low Pulse Width
t_7	10	10	ns min	SCLK Edge to Data Valid Hold Time
t_8 [6]	10	10	ns min	SCLK Falling Edge to SDATA 3-State Enabled
	35	35	ns max	SCLK Falling Edge to SDATA 3-State Enabled
t_{SLEEP}	20	20	ns min	Time spent in Power Down

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts.

[2]See Figure 1, Figure 2 and the 'Serial Interface' section.

[3]Common Mode Voltage.

[4]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[5]Measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.8 V or 2.4 V with V_{DD} = 5 V and time for an output to cross 0.4 V or 2.0 V for V_{DD} = 3 V.

[6]t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

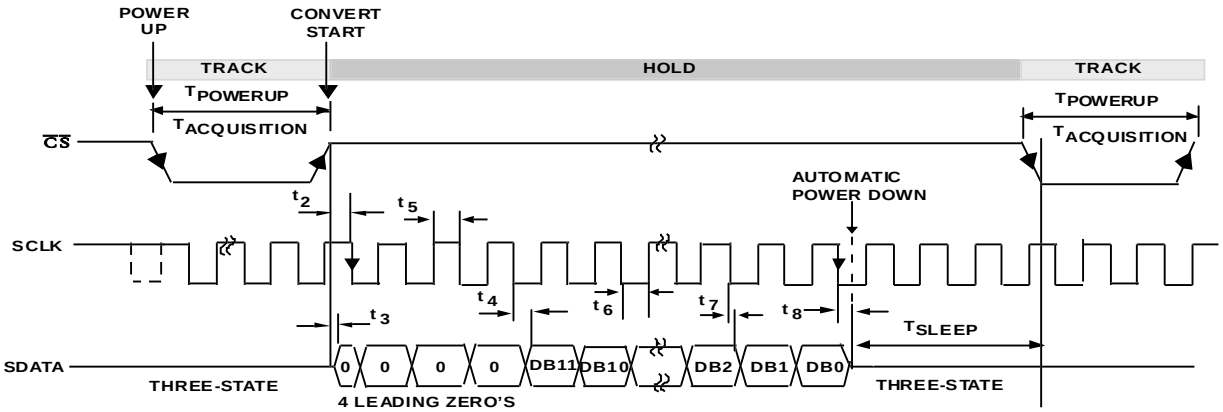


Figure 1. AD7456 Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... -0.3 V to +7 V
V_{IN+} to GND ..... –0.3 V to V_{DD} + 0.3 V
V_{IN-} to GND ..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND ..... -0.3 V to +7 V
Digital Output Voltage to GND . -0.3 V to V_{DD} + 0.3 V
V_{REF} to GND ..... -0.3 V to V_{DD} +0.3 V
Input Current to Any Pin Except Supplies[2] .... ±10mA
Operating Temperature Range
Commercial (A, B Version) ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
θ_{JA} Thermal Impedance .....205.9°C/W (µSOIC)
211.5°C/W (SOT-23)
θ_{JC} Thermal Impedance ..... 43.74°C/W (µSOIC)
91.99°C/W (SOT-23)
Lead Temperature, Soldering
Vapor Phase (60 secs) ..... +215°C
Infared (15 secs) ..... +220°C
ESD 3.5kV

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

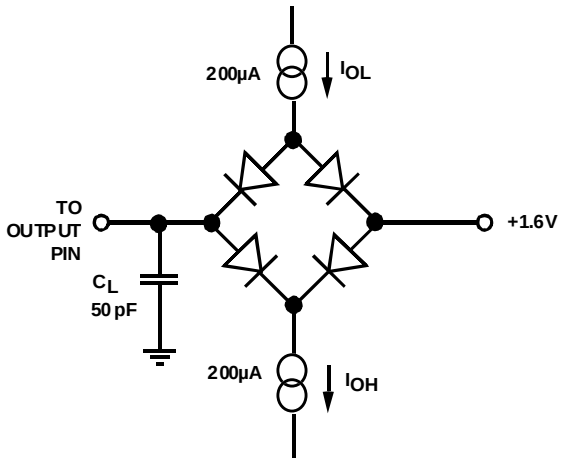


Figure 3. Load Circuit for Digital Output Timing Specifications

ORDERING GUIDE

Model	Range	Linearity Error (LSB)[1]	Package Option[4]	Branding Information
AD7456BRT	-40°C to +85°C	±1 LSB	RT-8	TBD
AD7456BRM	-40°C to +85°C	±1 LSB	RM-8	TBD
TBD	Evaluation Board			
EVAL-CONTROL BRD2[3]	Controller Board			

NOTES
[1]Linearity error here refers to Integral Non-linearity Error.
[2]This can be used as a stand-alone evaluation board or in conjunction with the EVALUATION BOARD CONTROLLER for evaluation/demonstration purposes.
[3]EVALUATION BOARD CONTROLLER. This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete Evaluation Kit, you will need to order the ADC evaluation board i.e. TBD, the EVAL-CONTROL BRD2 and a 12V AC transformer. See the TBD technote for more information.
[4]S0 = SOIC; RM = µSOIC

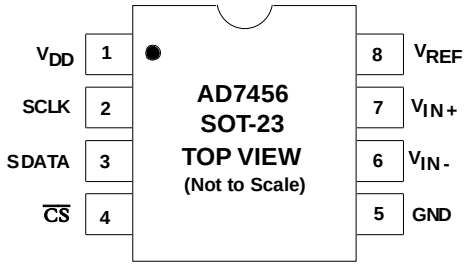
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7456 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

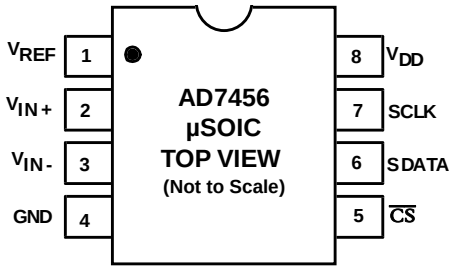
PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
V_{REF}	Reference Input for the AD7456. An external reference must be applied to this input. For a 5 V power supply, the reference is 2.5 V (±1%) and for a 3 V power supply, the reference is 2V (±1%) for specified performance. This pin should be decoupled to GND with a capacitor of at least 0.1µF. See the 'Reference Section' for more details.
V_{IN+}	Positive Terminal for Differential Analog Input.
V_{IN-}	Negative Terminal for Differential Analog Input.
GND	Analog Ground. Ground reference point for all circuitry on the AD7456. All analog input signals and any external reference signal should be referred to this GND voltage.
$\overline{CS}$	Chip Select. This input provides the dual function of powering up the device and initiating a conversion on the AD7456.
SDATA	Serial Data. Logic Output. The conversion result from the AD7456 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream of the AD7456 consists of four leading zeros followed by the 12 bits of conversion data which is provided MSB first. The output coding is two's complement.
SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process.
V_{DD}	Power Supply Input. V_{DD} is 3 V (+20%/-10%) or 5 V (±5%). This supply should be decoupled to GND with a 0.1µF Capacitor and a 10µF Tantalum Capacitor.

PIN CONFIGURATION 8-LEAD SOT-23



PIN CONFIGURATION µSOIC



TERMINOLOGY

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB,

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7450, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7456 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Aperture Delay
This is the amount of time from the leading edge of the sampling clock until the ADC actually takes the sample.

Aperture Jitter
This is the sample to sample variation in the effective point in time at which the actual sample is taken.

Full Power Bandwidth
The full power bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1dB or 3dB for a full scale input.

Common Mode Rejection Ratio (CMRR)
The Common Mode Rejection Ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200mV p-p sine wave applied to the Common Mode Voltage of V_{IN+} and V_{IN-} of frequency fs:

CMRR (dB) = 10log(Pf/Pfs)

Pf is the power at the frequncy f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

Integral Nonlinearity (INL)
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero Code Error
This is the deviation of the midscale code transition (111...111 to 000...000) from the ideal V_{IN+}-V_{IN-} (i.e., 0LSB).

Positive Gain Error
This is the deviation of the last code transition (011...110 to 011...111) from the ideal V_{IN+}-V_{IN-} (i.e., +V_{REF} - 1LSB), after the Zero Code Error has been adjusted out.

Negative Gain Error
This is the deviation of the first code transition (100...000 to 100...001) from the ideal V_{IN+}-V_{IN-} (i.e., -V_{REF} + 1LSB), after the Zero Code Error has been adjusted out.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode on the 13th SCLK rising edge (see the "Serial Interface Section"). The track/hold acquisition time is the minimum time required for the track and hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

Power Supply Rejection Ratio (PSRR)
The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200mV p-p sine wave applied to the ADC V_{DD} supply of frequency fs. The frequency of this input varies from 1kHz to 1MHz.

PSRR (dB) = 10 log (Pf/Pfs)

Pf is the power at frequency f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

SERIAL INTERFACE

Figure 1 shows a detailed timing diagram for the serial interface of the AD7456. The serial clock provides the conversion clock and also controls the transfer of data from the AD7456 during conversion.

The falling edge of $\overline{CS}$ powers the part up and also puts the track and hold into track. The power up time is 1.4µsec minimum and in this time, the device also acquires the analog input signal. $\overline{CS}$ must remain low for the duration of power up. The rising edge of $\overline{CS}$ initiates the conversion process, puts the track and hold into hold mode and takes the serial data bus out of three-state. The conversion will require 16 SCLK cycles to complete.

On the 16th SCLK falling edge, after the time t_8, the serial data bus will go back into three-state, and the device will automatically enter full power down. It will remain powered down until the next falling edge of $\overline{CS}$.

If the falling edge of $\overline{CS}$ occurs before the 16 bits of conversion data have been clocked out of the device, the conversion will be aborted, SDATA will go back into three-state and the track and hold will go back into track; thus the part will sample the analog input. On the next rising edge of $\overline{CS}$, a normal conversion will be initiated and the device will automatically powerdown at the end of the conversion as before.

The conversion result from the AD7456 is provided on the SDATA output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream of the AD7456 consists of four leading zeros followed by the 12 bits of conversion data which is provided MSB first. The output coding is two's complement.

16 serial clock cycles are therefore required to perform a conversion and to access data from the AD7456. A rising edge on $\overline{CS}$ provides the first leading zero to be read in by the micro-controller or DSP. The remaining data is then clocked out on the subsequent SCLK falling edges beginning with the second leading zero. Thus the first falling clock edge on the serial clock after $\overline{CS}$ has gone high provides the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge.