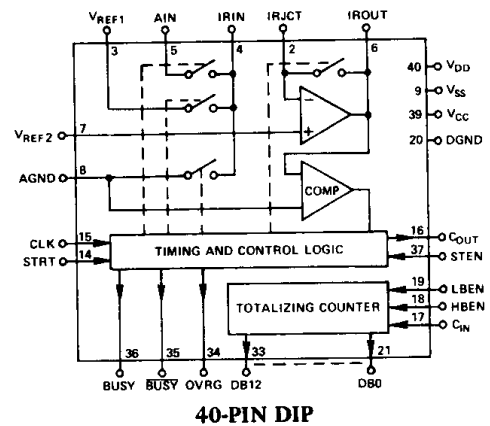


**FEATURES**

- Resolution: 13 Bits, 2's Complement
- Relative Accuracy:  $\pm 1/2$ LSB
- "Quad Slope" Precision
  - Gain Drift: 1ppm/ $^{\circ}$ C
  - Offset Drift: 1ppm/ $^{\circ}$ C
- Microprocessor Compatible
- Ratiometric
- Overrange Flag
- Very Low Power Dissipation
- TTL/CMOS Compatible
- CMOS Monolithic Construction

**AD7550 FUNCTIONAL BLOCK DIAGRAM**



**GENERAL DESCRIPTION**

The AD7550 is a 13-bit (2's complement) monolithic CMOS analog-to-digital converter on a 118 x 125 mil die packaged in a 40-pin ceramic DIP. Outstanding accuracy and stability (1ppm/ $^{\circ}$ C) is obtained due to its revolutionary integrating technique, called "Quad Slope" (Analog Devices patent No. 3872466). This conversion consists of four slopes of integration as opposed to the traditional dual slope and provides much higher precision.

The AD7550 parallel output data lines have three-state logic and are microprocessor compatible through the use of two enable lines which control the lower eight LSB's (low byte enable) and the five MBS's (high byte enable). An overrange flag is also available which together with the BUSY and  $\overline{\text{BUSY}}$  flags can be interrogated through the STATUS ENABLE providing easy microprocessor interface.

The AD7550 conversion time is about 40ms with a 1MHz clock. Clock can be externally controlled or internally generated by simply connecting a capacitor to the clock pin. A positive start pulse can be self-generated by having a capacitor on the start pin or can be externally applied.

**PACKAGE IDENTIFICATION<sup>1</sup>**

Suffix "D" – Ceramic DIP (D40A)

**NOTE**

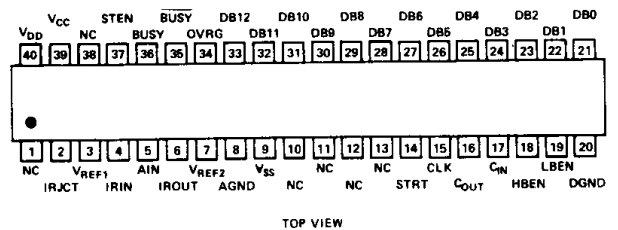
<sup>1</sup> See Section 19 for package outline information.

For most applications, the AD7550 needs only three resistors, one capacitor, and a reference voltage since the integrating amplifier, comparator, switches and digital logic are all on the CMOS chip.

A wide range of power supply voltages ( $\pm 5$ V to  $\pm 12$ V) with minuscule current requirements make the AD7550 ideal for low power and/or battery operated applications. Selection of the logic ( $V_{CC}$ ) supply voltage (+5V to  $V_{DD}$ ) provides direct TTL or CMOS interface on the digital input/output lines.

The AD7550 uses a high density CMOS process featuring double layer metal and silicon nitride passivation to ensure high reliability and long-term stability.

**PIN CONFIGURATION**



# SPECIFICATIONS (V<sub>DD</sub> = +12V, V<sub>SS</sub> = -5V, V<sub>CC</sub> = +5V, V<sub>REF1</sub> = +4.25V unless otherwise noted)<sup>1</sup>

PARAMETER	TA = +25°C	OVER SPECIFIED TEMPERATURE RANGE	TEST CONDITIONS
<b>ACCURACY</b> Resolution Relative Accuracy Gain Error Gain Error Drift Offset Error Offset Error Drift	±1LSB max ±1LSB max 1ppm/°C typ ±0.5LSB max 1ppm/°C typ	13 Bits 2's Comp min ±1 LSB max	f <sub>CLK</sub> = 500kHz, R <sub>1</sub> = 1MΩ, C <sub>1</sub> = 0.01μF, IRJCT Voltage Adjusted to $\frac{V_{REF1}}{2} \pm 0.6\%$
<b>ANALOG INPUTS</b> AIN Input Resistance <sup>2</sup> V <sub>REF1</sub> Input Resistance <sup>2</sup> V <sub>REF2</sub> Leakage Current	R1MΩ min R1MΩ min 10pA typ		
<b>DIGITAL INPUTS</b> CIN, LBEN, HBEN, STEN V <sub>INL</sub> V <sub>INH</sub> V <sub>INL</sub> V <sub>INH</sub> I <sub>INL</sub> , I <sub>INH</sub>	+0.8V max +2.4V min +1.2V max +10.8V min 5nA typ	+0.8V max +2.4V min +1.2V max +10.8V min	V <sub>CC</sub> = +5V V <sub>CC</sub> = +12V
<b>START</b> V <sub>INL</sub> V <sub>INH</sub> I <sub>INL</sub> I <sub>INH</sub>	+0.8V max +3.0V min -1μA typ +150μA typ	+0.8V max +3.0V min	V <sub>CC</sub> = +5V to V <sub>DD</sub> V <sub>CC</sub> = +5V to V <sub>DD</sub> , BUSY = Low V <sub>CC</sub> = +5V to V <sub>DD</sub> , BUSY = High
<b>CLOCK</b> V <sub>INL</sub> V <sub>INH</sub> V <sub>INL</sub> V <sub>INH</sub> I <sub>INL</sub> I <sub>INH</sub>	+0.8V max +3V min +1.2V max +10.8V min -100μA typ +100μA typ	+0.8V max +3V min +1.2V max +10.8V min	V <sub>CC</sub> = +5V V <sub>CC</sub> = +12V V <sub>IN</sub> = V <sub>INL</sub> ; V <sub>CC</sub> = +5V to +12V V <sub>IN</sub> = V <sub>INH</sub> ; V <sub>CC</sub> = +5V to +12V
<b>DIGITAL OUTPUTS</b> V <sub>OUTL</sub> V <sub>OUTH</sub> V <sub>OUTL</sub> V <sub>OUTH</sub> Capacitance (Floating State) (OVRG, BUSY, $\overline{BUSY}$ , and DB0-DB12) I <sub>LKG</sub> (Floating State) (OVRG, BUSY, $\overline{BUSY}$ , and DB0-DB12)	+0.5V max +2.4V min +1.2V max +10.8V min 5pF typ ±5nA typ	+0.8V max +2.4V min +1.2V max +10.8V min	V <sub>CC</sub> = +5V, I <sub>SINK</sub> = 1.6mA V <sub>CC</sub> = +5V, I <sub>SOURCE</sub> = 40μA V <sub>CC</sub> = +12V, I <sub>SINK</sub> = 1.6mA V <sub>CC</sub> = +12V, I <sub>SOURCE</sub> = 0.6mA V <sub>CC</sub> = +5V to +12V V <sub>OUT</sub> = 0V and V <sub>CC</sub>
<b>DYNAMIC PERFORMANCE</b> Conversion Time STEN, HBEN, LBEN Propagation Delay t <sub>ON</sub> , t <sub>OFF</sub> External STRT Pulse Duration	90ms typ 40ms typ 250ns typ, 500ns max 800ns min		V <sub>IN</sub> (CLK) = 0 to +3V, f <sub>CLK</sub> = 500kHz V <sub>IN</sub> (CLK) = 0 to +3V, f <sub>CLK</sub> = 1MHz V <sub>IN</sub> (STEN, HBEN, LBEN) 0 to +3V V <sub>IN</sub> (STRT) = 0 to +3V
<b>POWER SUPPLIES</b> V <sub>DD</sub> Range V <sub>SS</sub> Range V <sub>CC</sub> Range I <sub>DD</sub> I <sub>SS</sub> I <sub>CC</sub>	+10V min, +12V max -5V min, -12V max +5V min, V <sub>DD</sub> max 0.6mA typ, 2mA max 0.3mA typ, 2mA max 0.06mA typ, 2mA max		f <sub>CLK</sub> = 1MHz

## NOTES

<sup>1</sup> Full Scale Voltage = ±V<sub>REF1</sub> ÷ 2.125. For V<sub>REF1</sub> = +4.25V, FS voltage is ±2.000V.

<sup>2</sup> The equivalent input circuit is the integrator resistor R<sub>1</sub> (1MΩ min, 10MΩ max) in series with a voltage source  $\frac{V_{REF1}}{2}$ , (see Figure 1). Specifications subject to change without notice.

**ORDERING INFORMATION**

Model	Temperature Range	Package
AD7550BD	-25°C to +85°C	Ceramic

**CAUTION:**

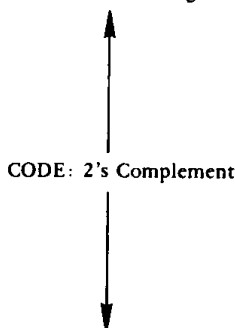
1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.
2.  $V_{CC}$  should never exceed  $V_{DD}$  by more than 0.4V, especially during power ON or OFF sequencing.

**ABSOLUTE MAXIMUM RATINGS**

$V_{DD}$ to AGND	0V, +14V
$V_{DD}$ to DGND	0V, +14V
$V_{SS}$ to AGND	0V, -14V
$V_{SS}$ to DGND	0V, -14V
AGND to DGND	0V, +14V
$V_{CC}$ to DGND	.0V, $V_{DD}$
$V_{REF1}$	$V_{SS}$ , $V_{DD}$
$V_{REF2}$	AGND, $V_{DD}$
AIN	$V_{SS}$ , $V_{DD}$
IRIN	$V_{SS}$ , $V_{DD}$
IRJCT	AGND, $V_{DD}$
IROUT	$V_{SS}$ , $V_{DD}$
Digital Input Voltage	
HBEN, LBEN, STEN, $C_{IN}$	DGND, (DGND +27V)
CLK, START	DGND, $V_{DD}$
Digital Output Voltage	
DB0-DB12, OVRG, BUSY, $\overline{BUSY}$ , $C_{OUT}$	DGND, $V_{CC}$
Power Dissipation (Package)	
Up to +50°C	.1000mW
Derates above +50°C by	.10mW/°C
Storage Temperature	-65°C to +150°C
Operating Temperature	-25°C to +85°C

## PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	NC	No Connection
2	IRJCT	IntegratoR JunCTion. Summing junction (negative input) of integrating amplifier.
3	V <sub>REF1</sub>	Voltage REFerence Input
4	IRIN	IntegratoR INput. External integrator input R is connected between IRJCT and IRIN.
5	AIN	Analog INput. Unknown analog input voltage to be measured. Fullscale AIN equals V <sub>REF</sub> /2.125.
6	IROUT	IntegratoR OUTput. External integrating capacitor C <sub>1</sub> is connected between IROUT and IRJCT.
7	V <sub>REF2</sub>	Voltage REFerence ÷ 2 Input
8	AGND	Analog GrouND
9	V <sub>SS</sub>	Negative Supply (-5V to -12V)
10	NC	No Connection
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	STRT	STaRT Conversion. When STRT goes to a Logic "1," the AD7550's digital logic is set up and BUSY is latched "high." When STRT returns "low," conversion begins in synchronization with CLK. Reinitiating STRT during conversion causes a conversion restart. STRT can be driven from an external logic source or can be programmed for continuous conversion by connecting an external capacitor between STRT and DGND. An externally applied STRT command must be a positive pulse of at least 800 nanoseconds to ensure proper set-up of the AD7550 logic.
15	CLK	CLock Input. The CLK can be driven from external logic, or can be programmed for internal oscillation by connecting an external capacitor between CLK and DGND.
16	C <sub>OUT</sub>	Count OUT provides a number (N) of gated clock pulses given by: $N = \left[ \frac{A_{IN}}{V_{REF1}} \cdot 2.125 + 1 \right] \cdot 4096$
17	C <sub>IN</sub>	Count IN is the input to the output counter. 2's complement binary data appears on the DB0 through DB12 output lines (if the HBEN and LBEN enable lines are "high") if C <sub>OUT</sub> is connected to C <sub>IN</sub> .
18	HBEN	High Byte ENable is the three-state logic enable input for the DB8-DB12 data outputs. When HBEN is low, the DB8-DB12 outputs are floating. When HBEN is "high," digital data appears on the data lines.
19	LBEN	Low Byte ENable is the three-state logic enable for DB0-DB7. When LBEN is "low," DB0-DB7 are floating. When "high," digital data appears on the data lines.
20	DGND	Digital GrouND is the ground return for all digital logic and the comparator.
21	DB0	Data Bit 0 (least significant bit)
22	DB1	
23	DB2	
24	DB3	
25	DB4	
26	DB5	
27	DB6	
28	DB7	
29	DB8	
30	DB9	
31	DB10	
32	DB11	
33	DB12	Data Bit 12 (most significant bit)
34	OVRG	OVeRRange indicates a Logic "1" if AIN exceeds plus or minus full scale by at least 1/2 LSB. OVRG is a three-state output and floats until STEN is addressed with a Logic "1".
35	$\overline{BUSY}$	Not BUSY. $\overline{BUSY}$ indicates whether conversion is complete or in progress. $\overline{BUSY}$ is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, $\overline{BUSY}$ will indicate either a "1" (conversion complete) or a "0" (conversion in progress).
36	BUSY	BUSY indicates conversion status. BUSY is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, BUSY indicates a "0" (conversion complete) or a "1" (conversion in progress).
37	STEN	STatus ENable is the three-state control input for BUSY, $\overline{BUSY}$ , and OVRG.
38	NC	No Connection
39	V <sub>CC</sub>	Logic Supply. Digital inputs and outputs are TTL compatible if V <sub>CC</sub> = +5V, CMOS compatible for V <sub>CC</sub> = +10V to V <sub>DD</sub> .
40	V <sub>DD</sub>	Positive Supply +10V to +12V.



# PRINCIPLES OF OPERATION

## BASIC OPERATION

The essence of the quad slope technique is best explained through Figures 1 and 2.

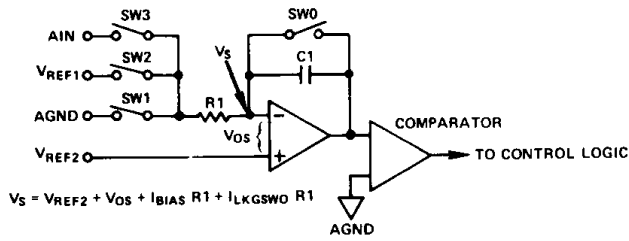


Figure 1. Quad Slope Integrator Circuit

The inputs AGND (analog ground), VREF1 and AIN (analog input) are applied in sequence to an integrator (Figure 1), creating four slopes (phases 1 through 4, Figure 2) at the integrator output. Voltage VS is ideally equal to  $\frac{V_{REF1}}{2}$ , but if not, will create an error count "n" that will be minimized by the "quad-slope" conversion process. VREF1 and VREF2 must be positive voltages.

The equivalent integrator input voltages and their integration times are shown in Table I.

TABLE I.  
INTEGRATOR EQUIVALENT INPUT VOLTAGES  
AND INTEGRATION TIMES

Phase	Input Voltage	Integration Time
1	AGND - VS	$t_1 = K_1 t$
2	VREF1 - VS	$t_2 = (K_1 + n)t$
3	AIN - VS	$t_3 = (2K_1 - n)t$
4	VREF1 - VS	$t_4 = (K_3 - 2K_1 + n - 2N)t$

NOTE: Ideally  $V_S = V_{REF2} = 1/2 V_{REF1}$

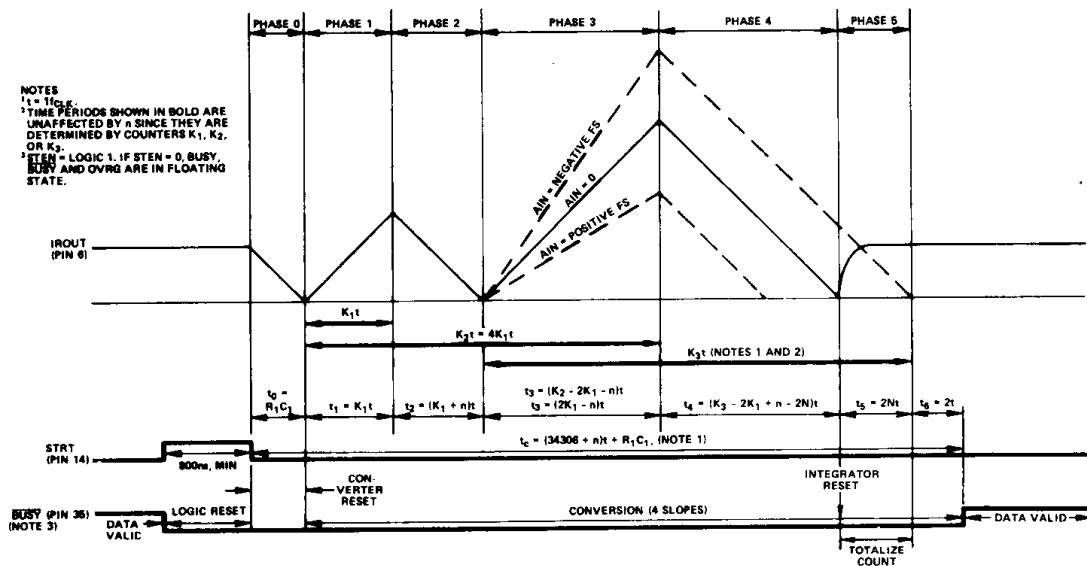


Figure 2. Quad Slope Timing Diagram

where:

$t$  = The CLK period

$n$  = System error count

$K_1$  = A fixed count equal to 4352 counts

$K_2$  = A fixed count equal to 17408 counts ( $K_2 = 4K_1$ )

$K_3$  = A fixed count equal to 25600 counts

$N$  = Digital output count corresponding to the analog input voltage, AIN

### PHASE 0

After the start pulse is applied, switch SW2 is closed (all other switches open) and the integrator output is ramped to comparator zero crossing. Phase 0 can be considered the reset phase of the converter, and always has a duration  $t_0 = R_1 C_1$  (integrator time constant). Upon zero crossing, counters  $K_1$  and  $K_2$  are started, switch SW2 is opened and SW1 is closed.

### PHASE 1

Phase 1 integrates (AGND - VS) for a fixed period of time (by counter  $K_1$ ) equal to  $t_1 = K_1 t$ . At the end of phase 1, switch SW1 is opened and SW2 is closed.

### PHASE 2

The integrator input is switched to (VREF1 - VS) and the output ramps down until zero crossing is achieved. The integration time  $t_2 = (K_1 + n)t$  includes the error count "n" due to offsets, etc. At the end of phase 2, switch SW2 is opened, SW3 is closed, and a third counter ( $K_3$ ) is started.

### PHASE 3

Phase 3 integrates the analog input (AIN - VS) until counter  $K_2$  counts  $4K_1 t$ . At this time SW3 is opened and SW2 is closed again.

### PHASE 4

Phase 4 integrates (VREF1 - VS) and the comparator output ramps down until zero crossing once again is achieved. Since the comparator always approaches zero crossing from the same slope, propagation delay is constant and hysteresis effect is eliminated.

The time  $t_5$  between the phase 4 zero crossing and the termination of counter  $K_3$  is considered equal to  $2N$  counts.  $N$ , the number of counts at the  $C_{OUT}$  terminal, is obtained by a divide-by-two counter stage. This reduces "jitter" effect. Barring third (and higher) order effects, it can be proven that:

$$N = \underbrace{\left( \frac{A_{IN}}{V_{REF1}} - 1 \right) \cdot 2K_1 + \frac{K_3}{2}}_{\text{ideal transfer function}} + \underbrace{\left( \frac{A_{IN}}{V_{REF1}} - 1 \right) \cdot \left[ \frac{AGND}{V_{REF1}} (1 + 2\alpha) - \alpha^2 \right] \cdot 2K_1}_{\text{error term}} \quad (\text{EQN 1})$$

where:

$$\alpha = \frac{2V_S - V_{REF1}}{V_{REF1}}$$

The ideal case assumes:

$$AGND = 0V$$

$$V_S = \frac{V_{REF1}}{2}, \text{ therefore } \alpha = 0$$

Then (EQN 1) simplifies to:

$$N = \frac{A_{IN}}{V_{REF1}} \cdot 8704 + 4096 \quad (\text{EQN 2})$$

or

$$N = \frac{A_{IN}}{V_{FS}} \cdot 4096 + 4096 \quad (\text{EQN 3})$$

where:

$$V_{FS} = \text{full scale input voltage} = \frac{V_{REF1}}{2.125}$$

The parallel output (DB0-DB12) of the AD7550 represents the number  $N$  in binary 2's complement coding when the  $C_{OUT}$  pin is connected to the  $C_{IN}$  pin (see Table II).

TABLE II  
OUTPUT CODING (Bipolar 2's Complement)

Analog Input (Note 1)	N (Note 2)	Parallel Digital Output (Note 3)									
		OVRG	DB12								
+Ovrerrange	-	1	0	1111	1111	1111	1111	1111	1111	1111	1111
+VFS (1-2 <sup>-12</sup> )	8191	0	0	1111	1111	1111	1111	1111	1111	1111	1111
+VFS (2 <sup>-12</sup> )	4097	0	0	0000	0000	0000	0000	0000	0000	0000	0001
0	4096	0	0	0000	0000	0000	0000	0000	0000	0000	0000
-VFS (2 <sup>-12</sup> )	4095	0	1	1111	1111	1111	1111	1111	1111	1111	1111
-VFS	0	0	1	0000	0000	0000	0000	0000	0000	0000	0000
-Ovrerrange	-	1	1	0000	0000	0000	0000	0000	0000	0000	0000

Notes

1  $V_{FS} = \frac{V_{REF1}}{2.125}$

2 N = number of counts at  $C_{OUT}$  pin

3  $C_{OUT}$  strapped to  $C_{IN}$ ; LBEN, HBEN and STEN = Logic 1

### ERROR ANALYSIS

Equation 1 shows that only  $\alpha$  and  $AGND$  generate error terms. Their impact can be analyzed as follows:

Case 1:  $AGND = 0, \alpha \neq 0$

Error sources such as capacitor-leakage ( $I_L$ ) and op amp offset ( $e$ ) cause  $\alpha$  to be different from zero.

Under this condition,

$$\alpha = \frac{2(e + I_L R_1)}{V_{REF1}}$$

where  $I_L R_1$  is the equivalent error voltage generated by leakage  $I_L$ .

The evaluation of this error term is best demonstrated through the following example:

Assume:

$$e = 5mV, I_L = 5nA, R_1 = 1M\Omega \text{ and } V_{REF1} = 4.25V.$$

Then:

$$\alpha = 4.7 \times 10^{-3}$$

and:

$$N = \left[ \frac{A_{IN}}{V_{REF1}} - 1 \right] \times 8704 + 12800 - \underbrace{\left[ \frac{A_{IN}}{V_{REF1}} - 1 \right] \times 22.1 \times 10^{-6} \times 8704}_{\text{error term } N_e}$$

Therefore, the error count  $N_e$  is as follows:

$$\text{For } A_{IN} = -V_{FS}: N_e = 0.28 \text{ counts} = 0.28\text{LSB}$$

$$A_{IN} = 0: N_e = 0.19 \text{ counts} = 0.19\text{LSB}$$

$$A_{IN} = +V_{FS}: N_e = 0.09 \text{ counts} = 0.09\text{LSB}$$

The above example shows the strong reduction of the circuit errors because of the  $\alpha^2$  term in (EQN 1). Another consequence of this effect is that  $N_e$  is always positive, regardless of the polarity of the circuit errors.

Case 2:  $AGND \neq 0, \alpha = 0$

When  $AGND$  is different from the signal ground, then this error will come through on a first-order basis. Indeed:

$$N = \left[ \frac{A_{IN}}{V_{REF1}} - 1 \right] \cdot 8704 + 12800 + \underbrace{\left[ \frac{A_{IN}}{V_{REF1}} - 1 \right] \cdot \frac{AGND}{V_{REF1}}}_{\text{error term } N_e}$$

The following example demonstrates the impact of  $AGND$ .

Let  $AGND = 1mV$  and  $V_{REF1} = 4.25V$ .

For  $A_{IN} = -V_{FS}$ , then  $N_e = 3.01$  counts

$A_{IN} = 0$ , then  $N_e = 2.05$  counts

$A_{IN} = +V_{FS}$ , then  $N_e = 1.08$  counts

Therefore, ground loops should be minimized because a  $330\mu V$  difference between  $AGND$  and signal ground will cause 1 count (1 LSB) of error when the analog input is at minus full scale. An optimized ground system is shown in Figure 7.

## OPERATING GUIDELINES

The following steps, in conjunction with Figure 3, explain the calculations of the component values required for proper operation.

### 1. DETERMINATION OF $V_{REF1}$

When the full scale voltage requirement ( $V_{FS}$ ) has been ascertained, the reference voltage can be calculated by:

$$V_{REF1} = 2.125 (V_{FS})$$

$V_{REF1}$  must be positive for proper operation.

### 2. SELECTION OF $C_3$ (INTERNAL CLOCK OPERATION)

For internal clock operation, connect capacitor  $C_3$  to the clock pin as shown in Figure 3. The clock frequency versus capacitor  $C_3$  is shown in Figure 4.

The clock frequency must be limited to 1.3MHz for proper operation.

### 3. SELECTION OF INTEGRATOR COMPONENTS ( $R_1$ AND $C_1$ )

To ensure that the integrator's output doesn't saturate to its bound ( $V_{DD}$ ) during the phase (3) integration cycle, the integrator time constant ( $R_1 C_1$ ) should be approximately equal to:

$$\pi = R_1 C_1 = \frac{V_{REF1} (9 \times 10^3)}{f_{CLK} (V_{DD} - 4V)}$$

The integrator components  $R_1$  and  $C_1$  can be selected by referring to Figure 5 and/or Figure 6. Figure 5 plots the time constant ( $R_1 C_1$ ) versus clock frequency for different reference voltages. Figure 6 is a direct plot of the required  $C_1$  versus  $f_{CLK}$  for  $R_1$  values of  $1M\Omega$  and  $10M\Omega$ .

$R_1$  can be a standard 10% resistor, but must be selected between  $1M\Omega$  to  $10M\Omega$ .

The integrating capacitor " $C_1$ " must be a low leakage, low dielectric absorption type such as teflon, polystyrene or polypropylene. To minimize noise, the outside foil of  $C_1$  must be connected to  $IR_{OUT}$ .

### 4. CONVERSION TIME

As shown in Figure 2, the conversion time is independent of the analog input voltage  $A_{IN}$ , and is given by:

$$t_{convert} = t_{STRT} + \frac{34306}{f_{CLK}} + R_1 C_1$$

where:

$t_{STRT}$  = STRT pulse duration  
 $R_1 C_1$  = Integrator Time Constant  
 $f_{CLK}$  = CLK Frequency

For example, if  $V_{EEF1} = 4.25V$ ,  $R_1 = 1M\Omega$ ,  $C_1 = 4,000pF$  and  $CLK = 1MHz$ , the conversion time (not including  $t_{STRT}$ , which is normally only microseconds in duration) is approximately 40 milliseconds.

### 5. EXTERNAL OR AUTO STRT OPERATION

The STRT pin can be driven externally, or with the addition of  $C_2$ , made to self-start.

The size of  $C_2$  determines the length of time from end of conversion until a new conversion is initiated. This is the "data valid" time and is given by:

$$t_{DAV} \approx (1.7 \times 10^6 \Omega) C_2 + 20\mu s$$

When first applying power to the AD7550, a 0V to  $V_{DD}$  positive pulse (power up restart) is required at the STRT terminal to initiate auto STRT operation.

### 6. INITIAL CALIBRATION

Trim  $R_4$  (Figure 3) so that pin 2 ( $IR_{JCT}$ ) equals  $1/2 V_{REF1} \pm 0.6\%$ . When measuring the voltage on  $IR_{JCT}$ , apply a Logic "1" to the STRT terminal.

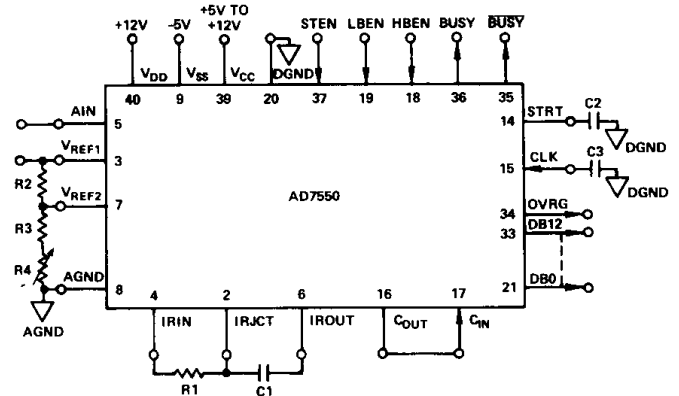


Figure 3. Operation Diagram

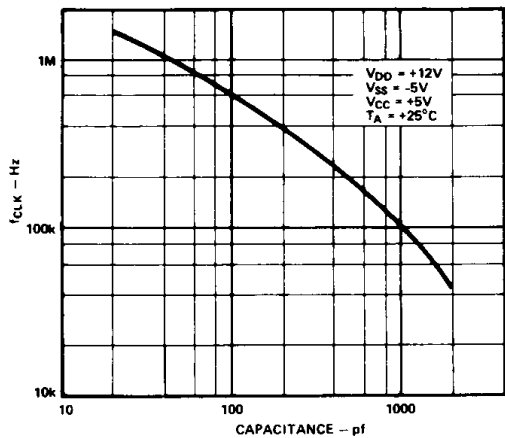


Figure 4.  $f_{CLK}$  vs.  $C_3$

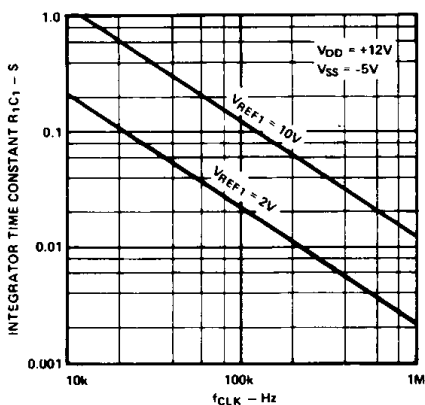


Figure 5. Integrator Time Constant ( $R_1C_1$ ) vs.  $f_{CLK}$  for Different Reference Voltages

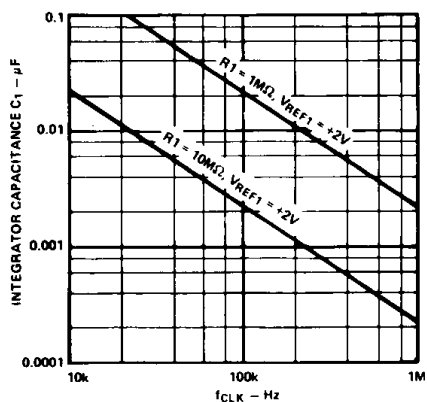


Figure 6. Integrator Capacitance ( $C_1$ ) vs.  $f_{CLK}$  for Different Integrator Resistances ( $R_1$ )

#### APPLICATION HINTS

When operating at  $f_{CLK}$  greater than 500kHz, the following steps are recommended to minimize errors due to noise coupling (see Figure 7).

1. Decouple AIN (pin 5),  $V_{REF1}$  (pin 3) and  $V_{REF2}$  (pin 7) through  $0.01\mu F$  to signal ground.
2. Signal ground must be located as close to pin 8 (AGND) as possible.
3. Keep the lead lengths of  $R_1$  and  $C_1$  toward pin 2 (IRJCT) as short as possible. In addition, both components should lie over the analog ground plane. If  $C_1$  has an outside foil, connect it to pin 6 (IROUT), not pin 2.
4. Hold the data bit enables (HBEN, LBEN) in the 0 state during conversion. This is easily accomplished by tying STEN to the 1 state and driving HBEN and LBEN with BUSY. This prevents the DB0 through DB12 outputs from coupling noise into the integrator during the phase 1–4 active integration periods.

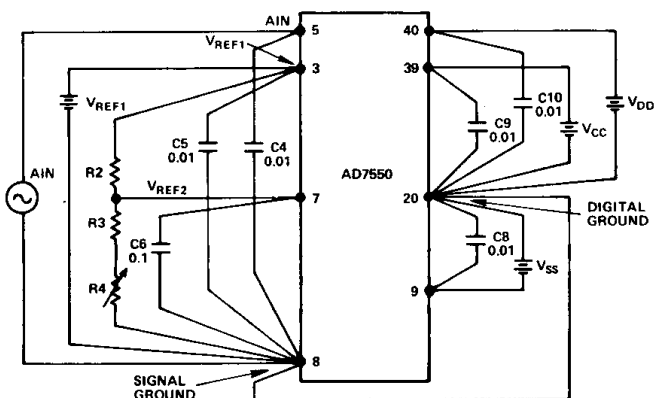


Figure 7. Ground System