ANALOG DEVICES

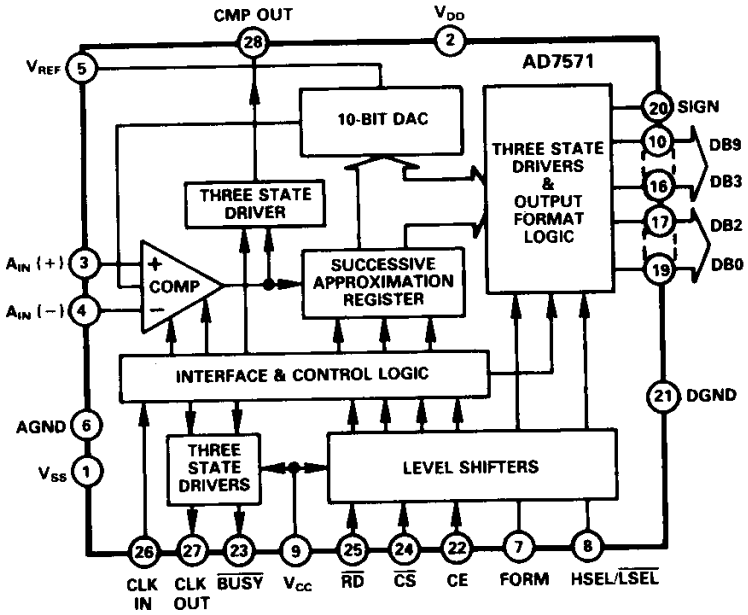
CMOS μP-Compatible 10-Bit Plus Sign ADC

AD7571

FEATURES

- 10-Bit Plus Sign Resolution
- No Missed Codes Over Full Temperature Range
- Conversion Time 80μs
- Differential Analog Voltage Inputs, ±10V Range
- Serial and Parallel Data Outputs
- Easy Interface to Most Microprocessors
- Internal Clock Oscillator
- Single Supply Operation for Positive-Only Signals
- Monolithic Construction

AD7571 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7571 is a high speed, low cost 10-bit plus sign CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 80μs. The device is designed for easy microprocessor interface allowing full parallel or double byte reading over three-state outputs. Conversion results are also available in serial form allowing opto-isolated operation using as few as two wires for the interconnect.

A new differential analog input configuration is used in the AD7571, increasing the common-mode rejection performance and allowing the analog zero input voltage to be offset from true analog ground. Analog input voltage range is ±10V using a single positive reference. With positive-only input signals the AD7571 can be operated from a single positive power supply.

PRODUCT HIGHLIGHTS

1. Pin Programmable Data Output Formats
   The output format for the 10-bits plus sign data is pin programmable allowing full parallel, two byte (left justified) and serial output formats.
2. Proven Control Logic
   The AD7571 control logic is similar to that used in the highly successful AD7574. This allows the AD7571 to be operated as a memory mapped input device interfacing to the μP via the control lines $\overline{CS}$ (chip select) and $\overline{RD}$ ($\overline{READ}$/WRITE).
3. All Active Components on Chip
   The addition of a few passive support components makes the AD7571 a complete 10-bit plus sign converter requiring only a reference voltage and power supply(ies). An on chip clock is also provided but the device can run from an external clock if required.
4. Differential Analog Inputs
   The analog input voltage can be unipolar or bipolar with an input range of ±10V. The differential input allows asymmetric input voltage ranges to be easily accommodated.
5. Single Supply Operation
   The AD7571 may be operated with a single positive supply if the input signal range is always positive with respect to AGND.

PACKAGE IDENTIFICATION

Suffix "N" – Plastic DIP (N28A)
Suffix "Q" – Cerdip (Q28A)
Suffix "D" – Ceramic DIP (D28B)

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, V_{CC} = +5V, V_{REF} = +5.12V, f_{CLK} = 550kHz External, Bipolar Configuration. All specifications T_{min} to T_{max} unless otherwise noted)

Parameter	AD7571JN[1]	AD7571KN	AD7571AQ	AD7571BQ	AD7571SD	AD7571TD	Units	Conditions/Comments
ACCURACY[2]								
Resolution	10 bits plus sign	*	*	*	*	*		
Relative Accuracy	±1	±3/4	*	**	*	**	LSB max	
Zero Input Reading	±000H	*	*	*	*	*	Hex	Full Scale Reading is ±3FFH
Roll-Over Error	±2	±1	*	**	*	**	LSB max	Difference in reading for equal positive and negative inputs near full scale
Minimum Resolution for which no Missing Codes are Guaranteed,	10 bits plus sign	*	*	*	*	*		
Full Scale Error (Gain Error)								
+25°C	±4	±3	*	**	*	**	LSB max	
T_{min} to T_{max}	±5	±4	*	**	*	**	LSB max	
Offset Errors								
Positive Differential Input	−3/4; +2	−3/4; +1	*	**	*	**	LSB max	
Negative Differential Input	−3/4; +2	−3/4; +1	*	**	*	**	LSB max	
Sign Bit Offset Error								
+25°C	±1	±1/2	*	**	*	**	LSB max	
T_{min} to T_{max}	±1	±1	*	**	*	**	LSB max	
Offset Error TC	±5	*	*	*	*	*	ppm/°C typ	
Sign Bit Offset TC	±5	*	*	*	*	*	ppm/°C typ	
Full Scale Error TC (Gain Error TC)	±5	*	*	*	*	*	ppm/°C typ	
POWER SUPPLY REJECTION								
V_{DD} Only	1	*	*	*	*	*	LSB max	14.25≤V_{DD}≤15.75V
V_{SS} Only	0.1	*	*	*	*	*	LSB max	−15.75≤V_{SS}≤−14.25V
V_{DD} and V_{SS} Together	1	*	*	*	*	*	LSB max	Same Limits as Above. Worst Case Combination.
ANALOG INPUTS								
Analog Input Range	±10.24	*	*	*	*	*	V	Full Scale with V_{REF} = +5.12V
Analog dc Input Impedance, $A_{IN}(+)$, $A_{IN}(-)$	10	*	*	*	*	*	MΩ min	
Input Common Mode Voltage	±10	*	*	*	*	*	V	
Common Mode Rejection	0.1	*	*	*	*	*	LSB/V typ	
REFERENCE INPUT								
V_{REF} (for specified performance)	+5.12	*	*	*	*	*	V	±5%
V_{REF} Range[3]	+1 to +6	*	*	*	*	*	V	Degraded transfer accuracy
I_{REF}, Input Reference Current	1.5	*	*	*	*	*	mA max	V_{REF} = +5.12V
LOGIC INPUTS								
FORM (pin 7), HSEL/LSEL (pin 8), CE (pin 22), CS (pin 24), RD (pin 25)								
V_{IL} Input Low Voltage	+0.8	*	*	*	*	*	V max	V_{CC} = +5V
	+1.5	*	*	*	*	*	V max	V_{CC} = +15V
V_{IH} Input High Voltage	+2.4	*	*	*	*	*	V min	V_{CC} = +5V
	+13.5	*	*	*	*	*	V min	V_{CC} = +15V
I_{IN} Input Current +25°C	1	*	*	*	*	*	μA max	V_{IN} = 0V or V_{CC}
T_{min} to T_{max}	10	*	*	*	*	*	μA max	V_{IN} = 0V or V_{CC}
C_{IN} Input Capacitance[4]	8	*	*	*	*	*	pF max	
CLK IN (Pin 26)								
V_{IL} Input Low Voltage	+1.5	*	*	*	*	*	V max	
V_{IH} Input High Voltage	+13.5	*	*	*	*	*	V min	
I_{IL} Input Low Current	10	*	*	*	*	*	μA max	
I_{IH} Input High Current	3	*	*	*	*	*	mA max	
LOGIC OUTPUTS								
DB9 to DB0 (pins 10-19), SIGN (pin 20), BUSY (pin 23), CLK OUT (pin 27), CMP OUT (pin 28)								
V_{OH} Output High Voltage	+4.0	*	*	*	*	*	V min	V_{CC} = +5V, I_{SOURCE} = 40μA
	+13.5	*	*	*	*	*	V min	V_{CC} = +15V, I_{SOURCE} = 100μA
V_{OL} Output Low Voltage	+0.4	*	*	*	*	*	V max	V_{CC} = +5V, I_{SINK} = 1.6mA
	+1.5	*	*	*	*	*	V max	V_{CC} = +15V, I_{SINK} = 2mA
Floating State Leakage Current (DB9–DB0, BUSY, CLK OUT, CMP OUT)	±10	*	*	*	*	*	μA max	
Floating State Output Capacitance[4]	7	*	*	*	*	*	pF max	
POWER REQUIREMENTS								
V_{DD}	+11.4 to +16.5	*	*	*	*	*	V	
V_{SS}	−11.4 to −16.5	*	*	*	*	*	V[4]	
V_{CC}	+4.5 to V_{DD}	*	*	*	*	*	V	
I_{DD} +25°C	7.5	*	*	*	*	*	mA max	
T_{min} to T_{max}	9.75	*	*	*	*	*	mA max	
T_{min} to T_{max}	5.0	*	*	*	*	*	mA typ	
I_{SS}	10	*	*	*	*	*	μA typ	
I_{CC}	50	*	*	*	*	*	μA typ	
	200	*	*	*	*	*	μA max	V_{IN} = 0V or V_{CC}
	0.5	*	*	*	*	*	mA typ	
	1.0	*	*	*	*	*	mA max	V_{IN} = V_{IL} or V_{IH}

NOTES

[1]Temperature Range as follows: AD7571JN, KN; 0 to +70°C
AD7571AQ, BQ; −25°C to +85°C
AD7571SD, TD; −55°C to +125°C

[2]The analog input voltage at either AIN+ or AIN− must not exceed the V_{DD} or V_{SS} supply voltages. However, with only positive analog input signals, the AD7571 may be operated with V_{SS} = 0V. All relevant specifications in the above table will apply in this unipolar configuration.

[3]Typical value, not guaranteed or subject to test.

[4]Guaranteed but not tested.

*Specifications same as AD7571JN.

**Specifications same as AD7571KN.

Specifications subject to change without notice.

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, V_{CC} = +5V, f_{CLK} = 550kHz. External unless otherwise noted)

Parameter		Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, A & B Grades)	Limit at T_{min}, T_{max} (S & T Grades)	Units	Conditions/ Comments
STATIC RAM INTERFACE MODE		(See Figure 5)				
t_{CS}	$\overline{CS}$ Pulse Width Requirement	100	130	150	ns min	Start Conversion Only
t_{BSR}	$\overline{BUSY}$ to $\overline{RD}$ Setup Time	0	0	0	ns min	
t_{BSCS}	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0	0	0	ns min	
t_{SELS}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Setup Time	0	0	0	ns min	
t_{RD}	$\overline{RD}$ Pulse Width	t_{RAD}	t_{RAD}	t_{RAD}	ns min	$t_{RD} \geq t_{RAD}$
t_{CBPD}	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	150	190	220	ns typ	$\overline{BUSY}$ Load = 20pF
		210	250	300	ns max	
		175	220	250	ns typ	$\overline{BUSY}$ Load = 100pF
		240	300	340	ns max	
t_{RAD}	Data Access Time	300	360	390	ns typ	Bus Load = 20pF
		430	510	550	ns max	
		460	540	600	ns typ	Bus Load = 100pF
		680	800	900	ns max	
t_{RHD}	Data Hold Time	300	330	360	ns typ	
		200	220	260	ns min	
		400	450	480	ns max	
t_{RHCS}	$\overline{CS}$ to $\overline{RD}$ Hold Time	200	350	500	ns max	
t_{SELH}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Hold Time	0	0	0	ns min	
t_{RESET}	Reset Time Requirement	0.5	0.6	0.8	µs min	
$t_{CONVERT}$	Conversion Time Using Internal Clock Oscillator	See Typical Data of Figure 14.				f_{CLK} = 550kHz
$t_{CONVERT}$	Conversion Time Using External Clock	80	80	80	µs max	See Figure 15.
ROM INTERFACE MODE		(See Figure 8.)				
t_{RD}	$\overline{RD}$ Pulse Width Requirement	Same as t_{RD} in RAM mode.				
t_{SELS}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Setup Time	Same as RAM mode.				
t_{SELH}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Hold Time	Same as RAM mode.				
t_{RAD}	Data Access Time	Same as RAM mode.				
t_{RHD}	Data Hold Time	Same as RAM mode.				
t_{WBPD}	$\overline{RD}$ High to $\overline{BUSY}$ Propagation Delay	0.5	0.7	0.8	µs typ	$\overline{BUSY}$ Load = 20pF
		0.9	1.0	1.4	µs max	
$t_{CONVERT}$	Conversion Time Using Internal Clock Oscillator	Add t_{WBPD} to Typical Data Shown in Figure 14.				
SLOW-MEMORY INTERFACE MODE		(See Figure 11).				
t_{CBPD}	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	Same as RAM mode.				
t_{RAD}	Data Access Time	40	60	70	ns typ	Bus Load = 20pF
		70	100	120	ns max	
		180	230	280	ns typ	Bus Load = 100pF
		300	370	420	ns max	
t_{RHD}	Data Hold Time	Same as RAM mode.				
t_{SELS}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Setup Time	Same as RAM mode.				
t_{SELH}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Hold Time	Same as RAM mode.				
t_{RESET}	Reset Time Requirement	Same as RAM mode.				
$t_{CONVERT}$	Conversion Time	Same as RAM mode.				
SERIAL DATA OUTPUT		(Applies to all Three Modes, see Figures 5, 8 and 11).				
t_{CEL}	CE to Low Impedance Outputs ($\overline{BUSY}$, CLK OUT, CMP OUT)	60	100	120	ns max	Low Impedance to DGND or V_{CC}
t_{CEH}	CE to High Impedance Outputs ($\overline{BUSY}$, CLK OUT, CMP OUT)	60	100	120	ns max	High Impedance to DGND or V_{CC}
t_{CBPD}	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	Same as RAM mode.				
t_{WBPD}	$\overline{RD}$ HIGH to $\overline{BUSY}$ Propagation Delay	Same as ROM mode.				
t_{SDS}	Serial Data to CLK OUT Setup Time	20	20	20	ns min	
t_{SDH}	Serial Data to CLK OUT Hold Time	500	500	500	ns min	

NOTE
All specified control signals are measured with $t_r = t_f$ = 20ns (10% to 90%) for +5V logic and timed from a voltage level of +1.6V. Data is timed from V_{IH}, V_{IL} or V_{OH}, V_{OL}. Sample tested at +25°C to ensure conformance.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
V_{CC} to DGND	0V, V_{DD} +0.4
V_{SS} to AGND	0V, −17V
V_{SS} to DGND	0V, −17V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND (pins 7, 8, 22, 24, 25)	−0.3V, V_{CC}
CLK IN Input Voltage (pin 26) to DGND	−0.3V, V_{DD}
Digital Output Voltage to DGND (pins 10-20, 23, 27, 28)	−0.3V, V_{CC}
V_{REF} to AGND	−0.3V, V_{DD}
AIN (+), AIN (−) to AGND	V_{SS}, V_{DD}

Operating Temperature Range	
JN, KN	0 to +70°C
AQ, BQ	−25°C to +85°C
SD, TD	−55°C to +125°C
Storage Temperature	+65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package)	
To +75°C	1,000mW
Derates above +75°C	10mW/°C

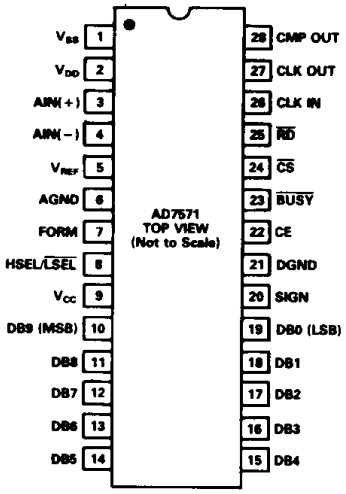
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing. See diode protection in Figure 16.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION



TERMINOLOGY AND DEFINITIONS

LEAST SIGNIFICANT BIT (LSB)

An ADC with 10-bits plus sign resolution can resolve 1 part in 2^{10} of either positive or negative full scale. For the AD7571 with ±10.24V full scale one LSB is 10.0mV.

RELATIVE ACCURACY

Relative accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the device's measured first LSB transition point and the measured full scale transition point. For the purpose of specifying the relative accuracy of a 10-bit plus sign ADC, the AD7571 is treated as two separate unipolar ADCs with the transfer characteristics for both positive and negative differential inputs measured independently.

DIFFERENTIAL NONLINEARITY (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a non-zero width. Since all grades of the AD7571 guarantee no missing codes to 10-bits plus sign resolution, all 1024 codes plus sign bit (i.e., total of 2048 codes) must be present over the entire operating temperature ranges.

OFFSET ERRORS

Positive Differential Inputs: A measure of the difference between the ideal (+1LSB) and the actual differential analog input level required to produce the first positive LSB code transition (000 . . . 00 to 000 . . . 01), see Figure 1.

Negative Differential Inputs: A measure of the difference between the ideal (−1LSB) and the actual differential input level required to produce the first negative LSB code transition (100 . . . 00 to 100 . . . 01).

ORDERING INFORMATION

Relative Accuracy (T_{min} to T_{max})	Temperature Range and Package: Plastic (N28A) 0 to +70°C	Cerdip[1] (Q28A) −25°C to +85°C	Side-Brazed Ceramic (D28B) −55°C to +125°C
±1LSB	AD7571JN	AD7571AQ	AD7571SD
±1/2LSB	AD7571KN	AD7571BQ	AD7571TD

NOTES

[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

See Section 19 for package outline information.

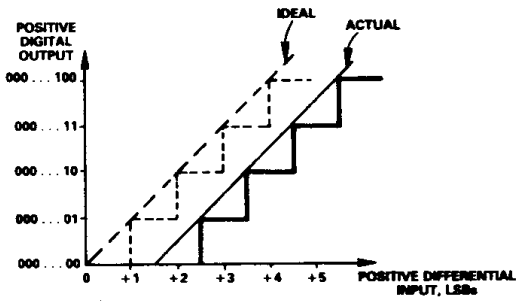


Figure 1. ADC Transfer Characteristics for Positive Differential Input with Offset Error of +1 1/2 LSBs

SIGN BIT OFFSET ERROR

Ideally occurring at 0V input, the sign bit transition may shift by up to ±1/2LSB for the AD7571 K/B/T grades and by ±1LSB for J/A/S grades. However, since all grades of the AD7571 are guaranteed to have no missed codes over their entire temperature ranges, the sign bit transition will always occur before the first LSB transitions occur.

The magnitude and polarity of offset errors depends on the clock frequency and V_{DD} power supply used to operate the AD7571. See Figure 2 and Figure 3.

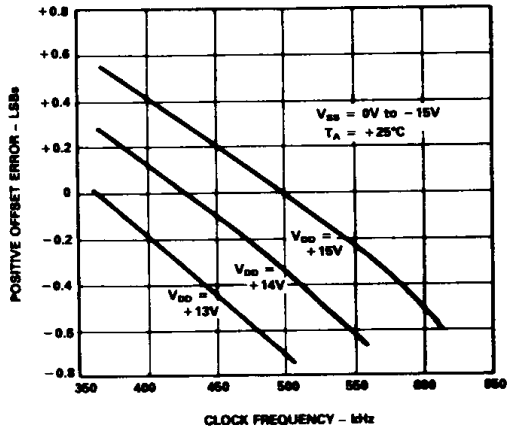


Figure 2. Typical Positive Offset Error vs. Clock Frequency for Different Supply Voltages

FULL SCALE ERROR (GAIN ERROR)

The gain of a unipolar ADC is defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation of the actual span from the ideal span of FS–2LSBs. In the AD7571 both positive and negative differential input ADC transfer characteristics exhibit the same magnitude and direction of gain error. This correspondence also extends to the gain error drift performance over temperature.

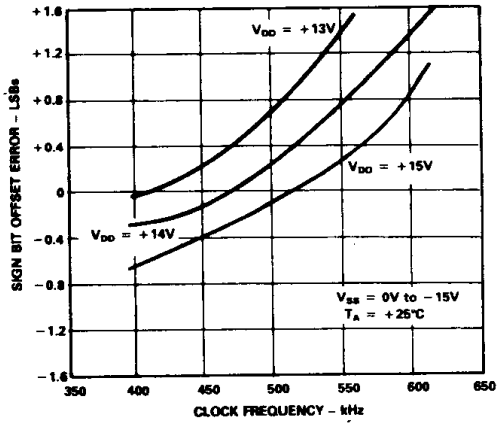


Figure 3. Typical Sign Bit Offset Error vs. Clock Frequency for Different Supply Voltages

ZERO INPUT READING

Digital output which results when AIN (+) = AIN (−).

ROLL-OVER ERROR

This is the difference in digital output, i.e., reading, for equal positive and negative inputs near full scale.

POWER SUPPLY REJECTION

A measure of the maximum change in the full scale range of the AD7571 resulting from a change in supply voltage.

INPUT COMMON MODE VOLTAGE

For the AD7571, the voltage at both inputs can be raised above (or lowered below) analog ground potential. The common mode voltage represents the voltage range over which this is allowed. However, the maximum possible differential input signal range will be directly affected by this common mode voltage signal. Table I shows the analog input signal range with a common mode voltage of +6V.

Note that the supply voltage V_{SS} must be at least as negative as the most negative analog input applied to the AD7571.

AIN(+), Volts	AIN(−), Volts	Differential Input, Volts	Output Code										
			Sign	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
+6	+6	0	0	0	0	0	0	0	0	0	0	0	0
+6.01	+6	+0.01	0	0	0	0	0	0	0	0	0	0	1
+10.24	+6	+4.24	0	0	1	1	0	1	0	1	0	0	0
+5.99	+6	−0.01	1	0	0	0	0	0	0	0	0	0	1
−4.24	+6	−10.24	1	1	1	1	1	1	1	1	1	1	1
+6	+6.01	−0.01	1	0	0	0	0	0	0	0	0	0	1
+6	+10.24	−4.24	1	0	1	1	0	1	0	1	0	0	0
+6	+5.99	+0.01	0	0	0	0	0	0	0	0	0	0	1
+6	−4.24	+10.24	0	1	1	1	1	1	1	1	1	1	1

Table I. Realizable Output Codes vs. Analog Inputs with a Common Mode Voltage of +6V. Note that All Error Sources are Assumed to be Zero and V_{REF} = +5.12V.

ANALOG INPUT RANGE

With V_{REF} = +5.12V the maximum analog input voltage range is ±10.24V. The digital output data is related to the reference and differential input voltages by the following expression:

$$DATA = \frac{AIN(+) - AIN(-)}{2V_{REF}} \times 1024$$

The sign of this data is determined by the sign of AIN (+) – AIN (–).

The negative supply (V_{SS}) must be equal to or more negative than the most negative analog input signal applied to AIN+ or AIN– (pins 3 and 4).

BIPOLAR TRANSFER CHARACTERSTIC

The ideal composite transfer characteristic for the AD7571 is shown in Figure 4. The sign bit transition which ideally occurs at 0V analog input is not shown for ease of illustration.

The first LSB transition points are mirror images of each other. The effect of non-zero offset errors is to either broaden or narrow the zero code widths. The effect of non-zero Gain Error is to pivot the composite transfer characteristic around the 0V origin.

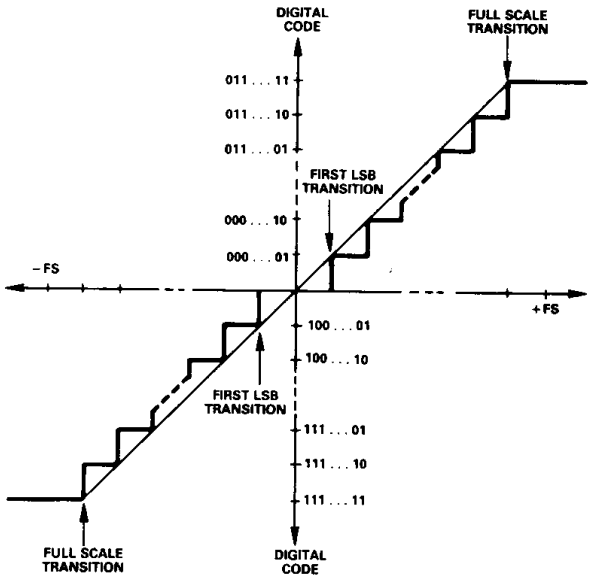


Figure 4. Composite AD7571 Transfer Characteristic

PIN	MNEMONIC	DESCRIPTION
1	V_{SS}	Negative supply 0V to – 15V. V_{SS} must be equal to or more negative than the most negative analog input voltage. With positive only input signals AD7571 may be operated with V_{SS} = 0V.
2	V_{DD}	Positive supply, +15V.
3	AIN +	Positive differential input.
4	AIN –	Negative differential input.
5	V_{REF}	Voltage reference input. The AD7571 is specified with V_{REF} = +5.12V.
6	AGND	Analog ground.
7	FORM	Data format select. See pin 8 description.
8	HSEL/$\overline{LSEL}$	HIGH BYTE/$\overline{LOW\ BYTE}$ select. Used in conjunction with FORM (pin 7) to select the data output format.

FORM	HSEL/$\overline{LSEL}$	DATA OUTPUT FORMAT	ACTIVE OUTPUT PINS
0	X	SIGN + 10-BIT PARALLEL	PIN 20 (SIGN) & PINS 10–19 (DB9–DB0)
1	0	LOW BYTE (3LSBs)	PINS 17, 18 & 19 DB2, DB1 & DB0)
1	1	HIGH BYTE (SIGN + 7MSBs)	PIN 20 (SIGN) & PINS 10–16 (DB9–DB3)

PIN	MNEMONIC	DESCRIPTION
		X = "Don't care" state.
9	V_{CC}	Logic Supply. For V_{CC} = +5V digital inputs and outputs are TTL compatible. For V_{CC} = V_{DD} digital inputs and outputs are CMOS compatible.
10–19	DB9–DB0	DATA OUTPUT. Three state output. DB9 = MSB.
20	SIGN	SIGN BIT OUTPUT. Three state output. Sign = AIN(+) – AIN(–) and is a logic zero for positive differential inputs and logic one for negative differential inputs.
21	DGND	Digital Ground.
22	CE	CHIP ENABLE. This is an enabling signal for the AD7571. CE = 1: Normal device operation. CE = 0: All outputs are placed in high impedance state, $\overline{CS}$ and $\overline{RD}$ input activity is ignored. Conversion results, if they have not previously been read, are stored internally and can be read when device returns to normal operation.
23	$\overline{BUSY}$	$\overline{BUSY}$ indicates conversion status. Three-state output. $\overline{BUSY}$ is low during conversion. $\overline{BUSY}$ is placed into a high impedance state when CE = 0.
24	$\overline{CS}$	$\overline{CHIP\ SELECT}$. Decoded device address, used with $\overline{RD}$ (pin 25) to control conversion sequences (see operating modes).
25	$\overline{RD}$	$\overline{READ/WRITE}$ control. Used with $\overline{CS}$ (pin 24) to control conversion sequences (see operating modes).
26	CLK IN	CLOCK INPUT for internal/external clock operation. Internal: Connect R_{CLK} and C_{CLK} timing components. See Figure 21 and Figure 22. External: Connect external clock via three-state buffer (see Figure 23). See section entitled "Internal/External clock".
27	CLK OUT	CLOCK OUTPUT. Three-state output. Used in conjunction with CMP OUT (pin 28) for serial data transfer. During a conversion CLK OUT frequency is CLK IN frequency divided by 4 otherwise CLK OUT is held at a logic HIGH. CLK OUT is placed into a high impedance state when CE = 0.
28	CMP OUT	COMPARATOR OUTPUT. Three-state output is used in conjunction with CLK OUT (pin 27) for serial data transfer. Output occurs during conversion and data is valid on rising edges of CLK OUT. Format is SIGN, MSB . . . . . LSB. CMP OUT is placed into a high impedance state when CE = 0.

Table II. Pin Function Description

FUNCTIONAL DESCRIPTION

The AD7571 uses the successive approximation technique to generate 10-bit plus sign conversion data. A block diagram of the device is shown previously. The comparator is a sampled data type comparator providing true differential analog inputs to allow conversion of both positive and negative input signals with a single positive reference. The comparator output drives the successive approximation register, which in turn, controls the output of the 10-bit thin-film R-2R D/A converter.

The control logic has been designed to allow easy interface to most microprocessors. Conversion start and data read are under the control of two input signals, $\overline{CS}$ ($\overline{CHIP\ SELECT}$) and $\overline{RD}$ ($\overline{READ}$/WRITE). Their timing determines the AD7571 operating mode (see Operating Modes Section). Upon receipt of a start command, $\overline{BUSY}$ goes low indicating conversion is in progress. The first decision made by the comparator concerns the sign of the differential input voltage AIN (+) – AIN (–). Based on the result of the sign decision, the comparator and its control logic then proceeds to successively approximate the differential input voltage by making differential voltage comparisons between AIN (+) – AIN (–) and the DAC output voltage V_{DAC} – AGND. Note that all comparator decisions are available at CMP OUT (pin 28) allowing serial data interfacing. To avoid misinterpretation of the serial data stream, a synchronizing signal (providing 11 rising edges) is available on CLK OUT (pin 27). Comparator output data is guaranteed valid on the rising edge of this synchronizing signal (see Operating Modes Section).

When the conversion is complete $\overline{BUSY}$ returns HIGH indicating the successive approximation register contains a valid representation of the differential analog input. This data can now be read out via the three-state data outputs. To allow easy interfacing to both 8-bit and 16-bit microprocessors, the data output format is controlled by FORM (pin 7) and HSEL/$\overline{LSEL}$ (pin 8) to provide sign plus 10-bits in parallel (one READ operation) or 3 lower bits followed by sign plus 7 upper bits (two READ operations). The internal successive approximation register is always reset after a sign plus 10-bit or sign plus 7-bit read operation (see Data Output Formats Section).

The CE input (CHIP ENABLE, pin 22) is an enabling signal for the AD7571. When CE is HIGH, normal device operation as outlined above occurs. When CE is LOW, all outputs are placed in the high impedance state and $\overline{CS}$ and $\overline{RD}$ activity is ignored. This device enabling signal allows a number of AD7571 to share common data and control lines in either serial or parallel data transfer configurations.

DATA OUTPUT FORMATS

The AD7571 has three possible data output formats, one serial and two parallel. Serial data is only available while a conversion is in progress. Parallel data, being the contents of the Successive Approximation Register, can be read before a conversion starts (ROM Mode) or after a conversion finishes (RAM and SLOW MEMORY Modes). Parallel data cannot be read during a conversion since control inputs $\overline{CS}$ and $\overline{RD}$ are ignored while $\overline{BUSY}$ is LOW.

SERIAL DATA OUTPUT FORMAT

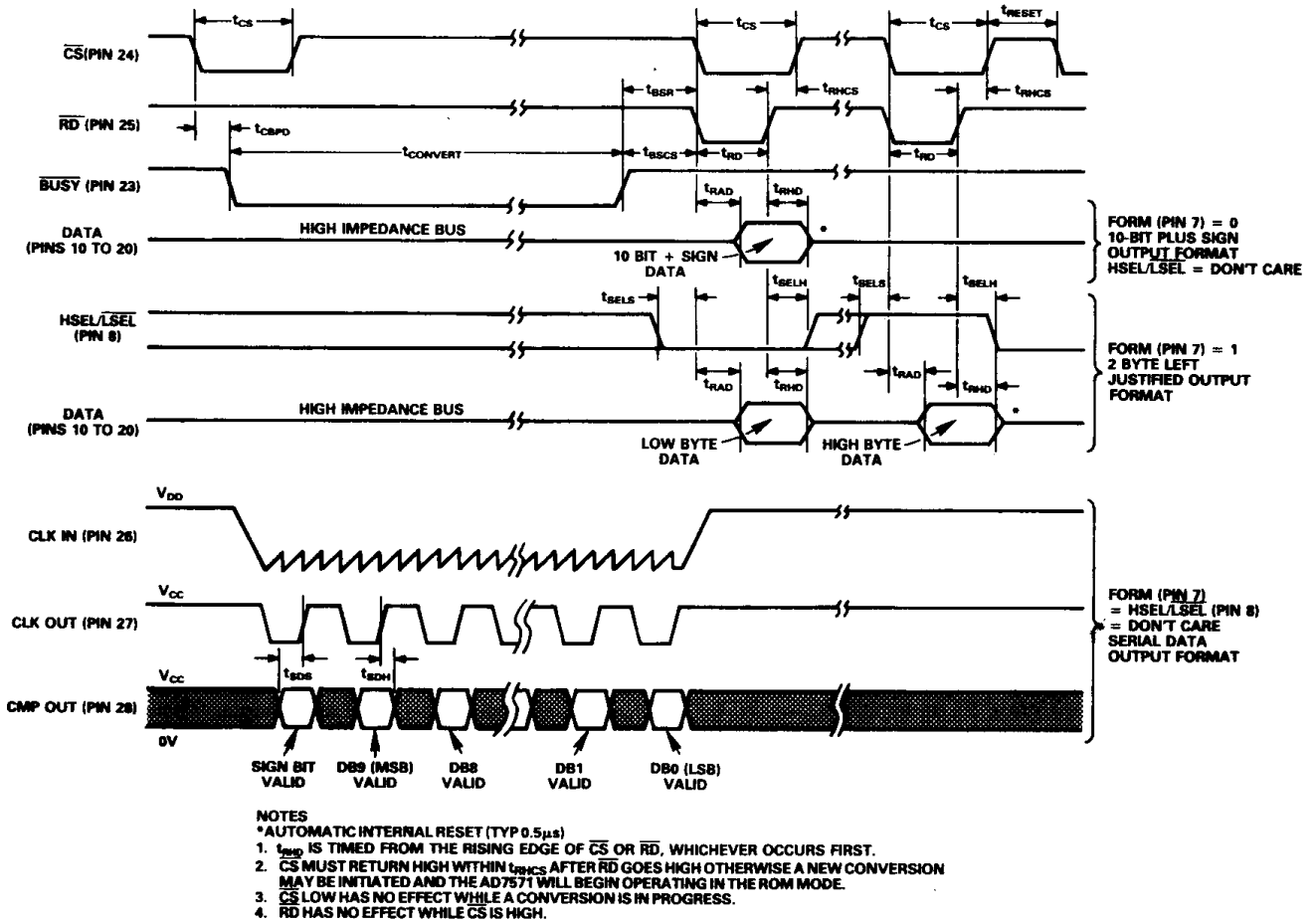
The output of the comparator is available at CMP OUT (COMPARATOR OUTPUT, pin 28). To avoid misinterpretation of this serial output data stream, a synchronizing signal is made available at CLK OUT (CLOCK OUT, pin 27). Serial output data is valid on the rising edge of this synchronizing signal, 11 rising edges in total. The format of this output data is SIGN, DB9, DB8 . . . . . DB0. When a conversion is not taking place the CMP OUT output will continue to register activity but the CLK OUT output will be held at a logic HIGH. The CLK OUT frequency is synchronized to the converter's input clock frequency present on CLK IN (CLOCK INPUT, pin 26), but is divided by 4. Both CLK OUT and CMP OUT are placed in the high impedance state when the CE input (CHIP ENABLE, pin 22) is taken LOW. This feature allows numerous AD7571s to send digital data to a microprocessor using as few as three wires for the interconnect. Both CLK OUT and CMP OUT can drive one low power TTL load.

10-BITS PLUS SIGN FORMAT

This parallel format allows the AD7571 to interface directly to 12- and 16-bit microprocessors. It is also the more useful format in non-microprocessor based applications. This data can only be read once since an automatic internal reset occurs whenever the $\overline{RD}$ input returns HIGH regardless of the operating mode (STATIC RAM, ROM or SLOW MEMORY). This format is selected by holding the FORM input (DATA FORMAT SELECT, pin 7) at a logic LOW. When the FORM input is LOW, the Low Byte/High Byte select input (HSEL/$\overline{LSEL}$, pin 8) is ignored.

2 BYTE LEFT-JUSTIFIED FORMAT

This format has been included to allow direct interfacing to 8-bit microprocessors. The data is broken into two bytes, sign plus upper 7 bits as one byte, and lower 3 bits as the second byte. To configure a left-justified 8-bit output data bus, DB2 should be connected to SIGN, DB1 to DB9 and DB0 to DB8. This is shown in the typical circuits such as Figure 12. Two READ operations are thus required to obtain the full 10-bits plus sign data. The byte select input (HSEL/$\overline{LSEL}$) is used to select which byte of data is placed on the data bus during the next data READ operation. This input can be connected to the microprocessor's lowest address line A0, thus giving the AD7571 two effective memory addresses, one for high byte conversion data, and one for low byte conversion data. If the full 10-bits plus sign data is required, then the two bytes must be read in an ordered sequence of low byte first then high byte. This sequence is required because an automatic internal reset occurs when $\overline{RD}$ returns HIGH after reading the sign plus 7 bits of data. Reading the low byte does not cause the internal reset to occur. In applications where only sign plus 7-bit resolution is required this can be obtained by one READ operation. The conversion time is not altered as the AD7571 always completes a full 10-bits plus sign conversion regardless of the output data format requirements.



NOTES
*AUTOMATIC INTERNAL RESET (TYP 0.5μs)
1. t_{RHD} IS TIMED FROM THE RISING EDGE OF $\overline{CS}$ OR $\overline{RD}$, WHICHEVER OCCURS FIRST.
2. $\overline{CS}$ MUST RETURN HIGH WITHIN t_{RHCS} AFTER $\overline{RD}$ GOES HIGH OTHERWISE A NEW CONVERSION MAY BE INITIATED AND THE AD7571 WILL BEGIN OPERATING IN THE ROM MODE.
3. $\overline{CS}$ LOW HAS NO EFFECT WHILE A CONVERSION IS IN PROGRESS.
4. $\overline{RD}$ HAS NO EFFECT WHILE $\overline{CS}$ IS HIGH.

Figure 5. AD7571 Static RAM Mode Timing Diagram

OPERATING MODES

The AD7571 has been designed to interface with microprocessors as a memory mapped peripheral device. As such, its control logic allows it to mimic such standard memory systems as static RAM, ROM or SLOW MEMORY.

STATIC RAM MODE

In this mode, the AD7571 is controlled by microprocessor READ and WRITE instructions and offers complete control over the converter operation. A single WRITE instruction to the AD7571 assigned memory address commands the A/D to start a conversion and 80μs later, depending on the data format decision, either one or two READ instructions retrieves the conversion result. To operate in this mode, the AD7571 must be connected so that executing a WRITE instruction to the AD7571 address pulls the $\overline{CS}$ input LOW while $\overline{RD}$ remains HIGH. Executing a READ instruction to the AD7571 address(es) must cause both $\overline{CS}$ and $\overline{RD}$ inputs to be pulled LOW for the duration of the READ instruction. $\overline{BUSY}$ must have returned HIGH before a data READ is attempted, i.e., delay from conversion start to data READ must be at least as great as the AD7571 conversion time. Figure 5 shows the timing diagram for all output data formats. Figures 6 and 7 show typical hookup examples to 8-bit and 16-bit microprocessors respectively.

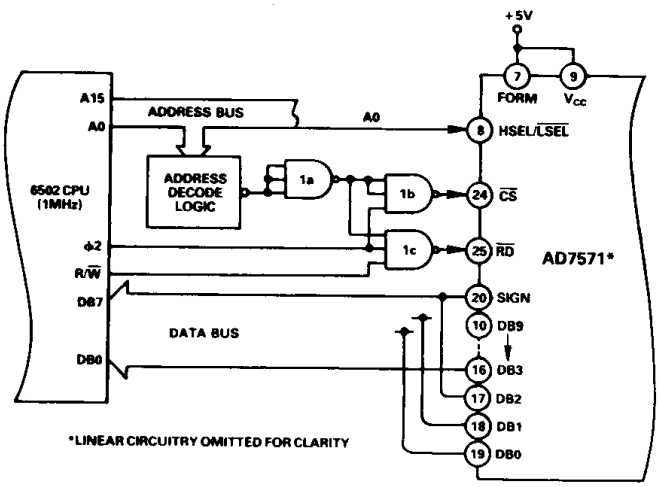


Figure 6. AD7571 to 6502 Interface, Static RAM Mode

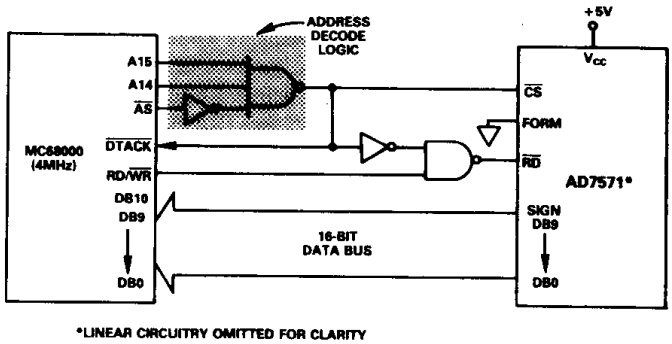


Figure 7. AD7571 to MC68000, Static RAM Mode

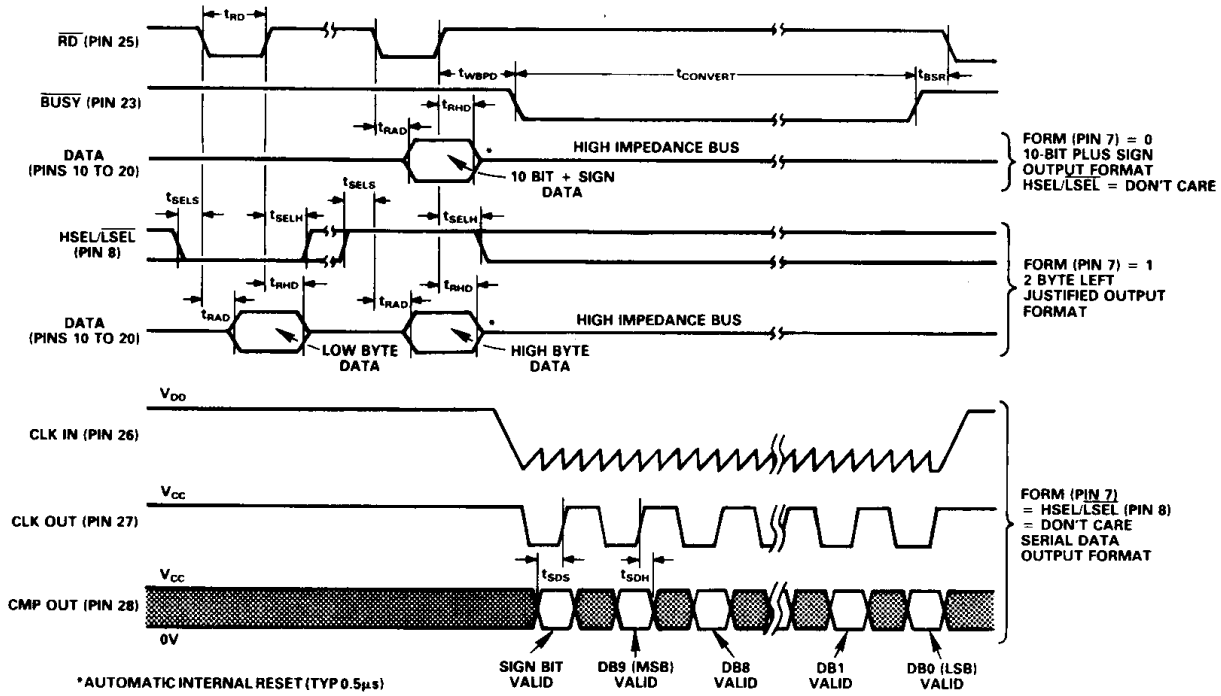


Figure 8. AD7571 ROM Mode Timing Diagram

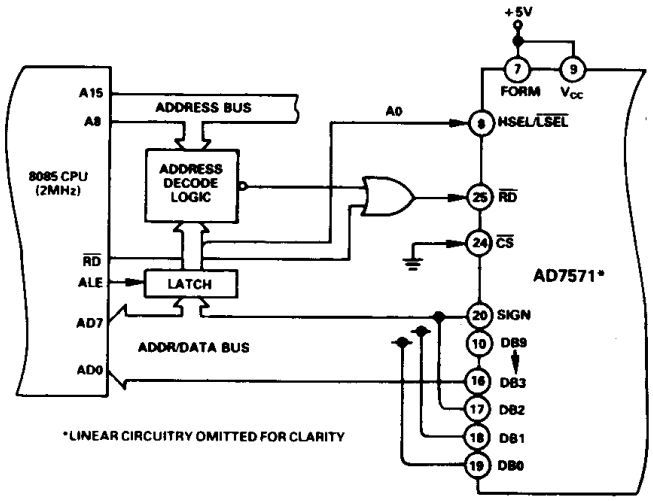


Figure 9. AD7571 to 8085 Interface, ROM Mode

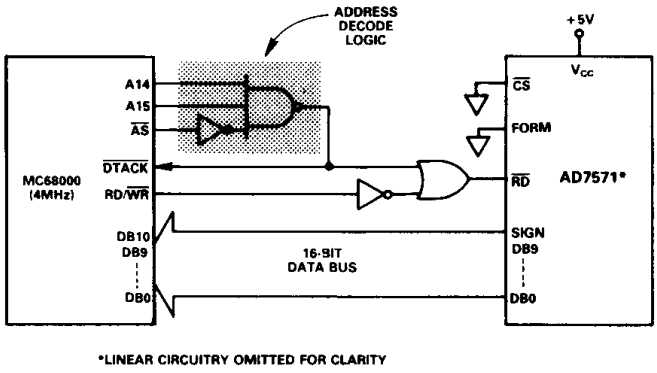


Figure 10. AD7571 to MC68000, ROM Mode

ROM MODE

This is the simplest method of interfacing the AD7571 to any microprocessor. Only READ instructions with a minimal amount of interface logic control the device's operation. This mode has the disadvantage that the time reference for the A/D conversion data is not well defined since the data read is the result of the previous conversion. This means that the time reference for the data sample will depend on when the previous READ operation finished. In applications where this uncertainty creates problems it can be eliminated by executing two complete READ operations separated by a software delay. To operate in this mode the $\overline{CS}$ input must be held LOW continuously and the $\overline{RD}$ input only pulled LOW when a READ instruction to the AD7571 memory address (es) is executed. A timing diagram is shown in Figure 8 and typical hookup examples to 8-bit and 16-bit microprocessors are shown respectively in Figures 9 and 10.

SLOW MEMORY MODE

In this mode, the normal A/D conversion time is treated as if it were the long access time of a slow memory device. It simplifies the software and can be used with any microprocessor which can be forced into a WAIT state for at least the duration of a conversion (e.g., Z80, 8085A). To operate in this mode, the AD7571 should be connected so that executing a memory READ instruction to its address causes both $\overline{CS}$ and $\overline{RD}$ inputs to be pulled low. $\overline{BUSY}$ subsequently goes LOW indicating a conversion start. Since $\overline{BUSY}$ is connected to the microprocessor READY input, the microprocessor is forced into a wait state thus suspending execution of the READ instruction. When $\overline{BUSY}$ returns HIGH (conversion finished), the microprocessor is released from the wait state to read the conversion data placed on the data bus by the AD7571. Many microprocessors test the condition of the READY/WAIT input shortly after the start of an instruction cycle. For this reason, the timing of the AD7571 and its associated address decode logic must be such that $\overline{BUSY}$ goes LOW early enough in the processor instruction cycle for the READY/WAIT input to be effective in forcing the processor into a WAIT state. In applications where the processor's memory READ/WRITE signal is not available early enough in the machine cycle for it to be used to enable or disable the address decode logic, the system software must be such that a WRITE operation to the AD7571 address(es) is never attempted, otherwise a bus conflict may occur between processor and AD7571.

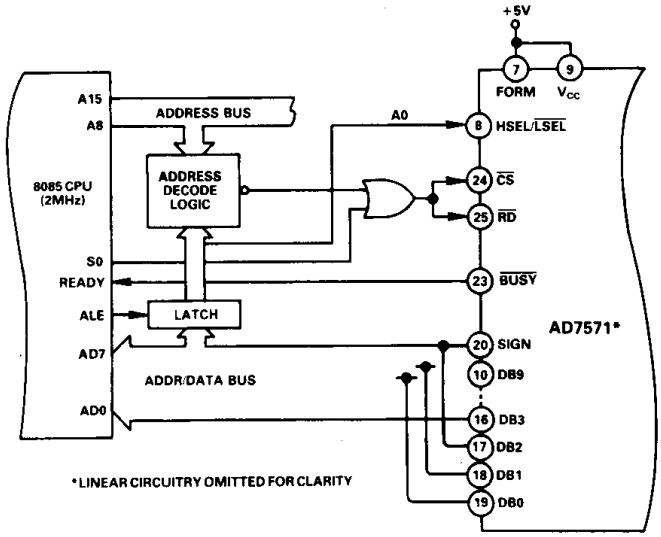


Figure 12. AD7571 to 8085 Interface Slow Memory Mode

A timing diagram for this mode is shown in Figure 11. A typical hookup example to the 8085A is shown in Figure 12.

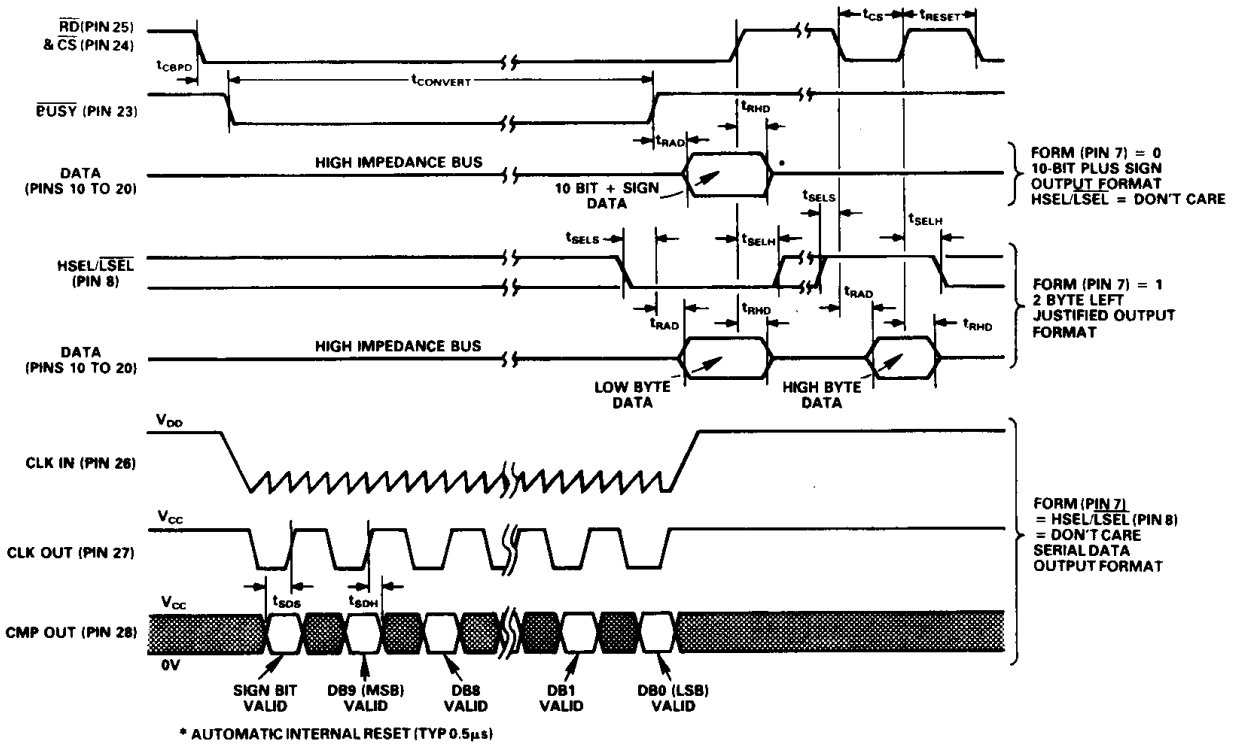


Figure 11. AD7571 Slow Memory Mode Timing Diagram

INTERNAL/EXTERNAL CLOCK

The AD7571 can be used with either its own internal asynchronous clock or with an externally applied clock. Whichever clock source is used, a single conversion ($\overline{BUSY}$ = LOW) lasts for 44 input clock cycles. Internal logic propagation delays add less than 0.5µs to this time.

INTERNAL CLOCK

A simplified equivalent circuit for the AD7571 internal clock circuitry is shown in Figure 13.

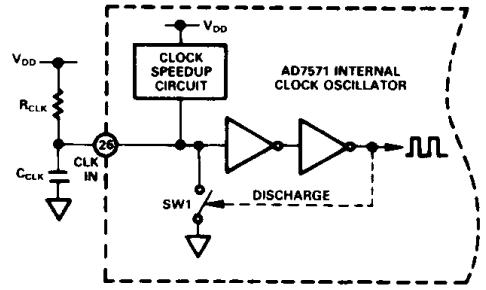


Figure 13. Simplified AD7571 Internal Clock Circuit

Clock pulses are generated by the action of an external capacitor C_{CLK} charging through an external resistor R_{CLK} and discharging through switch SW1. The clock speedup circuit acts to shorten the last clock period of a conversion. When a conversion is complete, the internal clock stops operation. However, in addition to conversion the internal clock also controls the automatic internal reset. For this reset operation, the internal clock runs for one cycle. Reset occurrences are indicated by asterisks in Figures 5, 8 and 11.

Nominal conversion times versus temperature for different R_{CLK} and C_{CLK} combinations are shown in Figure 14. The internal clock is useful in that it provides a convenient clock source for the AD7571. Due to process variations the actual operating frequency for a given R_{CLK} and C_{CLK} combination can vary from device to device by up to 10%. For this reason Analog Devices recommends using an external clock in the following situations.

1. Applications requiring a conversion time which is within 10% of 80μs, the minimum conversion time for specified accuracy. (A 550kHz clock frequency gives an 80μs conversion time.)
2. Applications where software constraints on time cannot accommodate time differences which may occur due to unit to unit clock frequency variations or temperature variations.

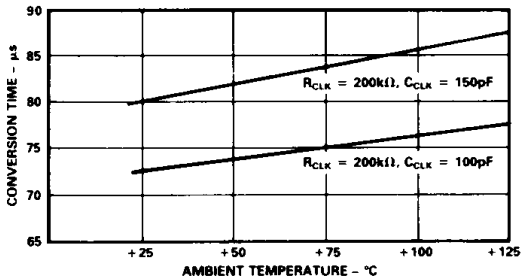


Figure 14. Typical Conversion Times vs. Temperature for Different R_{CLK} and C_{CLK}

EXTERNAL CLOCK

Due to the automatic internal reset cycle of the AD7571 the external clock source used to drive the CLK IN input must be capable of three-state operation. Figure 15 shows how the external clock (TTL compatible) should be connected. The $\overline{BUSY}$ output of the AD7571 controls the three-state enable input of a CD40109B three-state buffer. R1 is used as a pullup resistor and can be any value between 6kΩ and 100kΩ. The reset timing is still performed by the converter's internal logic and does not require an external clock pulse. The CD40109B also functions as a low-to-high voltage level shifter since the CLK IN input is not TTL compatible.

If a high level clock is already available, then an MC14503B three-state buffer can be used. The mark/space ratio of the external clock can vary from 70/30 to 30/70.

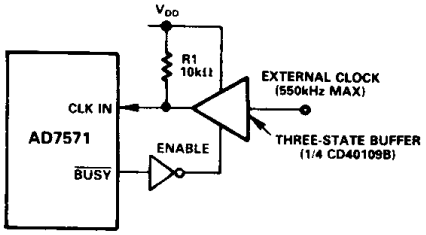


Figure 15. External Clock Connection

The AD7571 can be used with an external clock when configured in either the STATIC RAM or SLOW MEMORY modes, but is not recommended in the ROM mode. This is because the internal reset timing in this mode occurs after a conversion start command but before $\overline{BUSY}$ goes LOW (t_{WBPD} of Figure 8). With an external clock, it is possible for the comparator to have insufficient settling time before making the SIGN decision.

Timing constraints for external clock operation are as follows:

STATIC RAM MODE: When initiating a conversion, $\overline{CS}$ should go LOW on a negative clock edge to provide optimum settling time for the MSB.

SLOW MEMORY MODE: When initiating a conversion, $\overline{CS}$ and $\overline{RD}$ should go LOW on a negative clock edge to provide optimum settling time for the MSB.

10

APPLICATION HINTS

1. INPUT CURRENT: Due to the internal comparator switching action, displacement currents will flow at the analog inputs. The magnitude and polarity of these displacement currents will depend upon the differential analog input voltage levels.

   The effect of placing bypass capacitors at the analog inputs is to integrate the transient currents over the switching cycle. This causes a dc current to flow through any output resistance of the analog signal sources, thereby causing an input error. This dc current has a maximum value under conditions of continuous conversions with an input clock frequency of 550kHz and a differential input voltage of 10.24V. Under these conditions the dc current is a maximum of approximately 25μA. Therefore, to ensure that the input error will remain less than 1/4LSB, bypass capacitors should not be used at either the analog inputs or the V_{REF} input for source resistances greater than 100Ω. Where bypass capacitors are not used, large values of source resistance will not cause errors as the transient input currents have reduced to zero by the time data is accepted from the comparator. If it is necessary to filter the incoming analog signals through a low pass filter, use a passive RC low pass filter with series R < 100Ω or else an active RC low pass filter. If input bypass capacitors are necessary for noise filtering and high source resistance is unavoidable, the input error can be compensated for by a full scale adjustment while the given source resistance and bypass capacitor are in place.

2. NOISE: The leads to the analog inputs (pins 3 and 4) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible a twisted pair transmission line between source and ADC is recommended. The twisted pair keeps induced noise (due to capacitive and inductive coupling) to a minimum. Also any potential difference in grounds between signal source and ADC appears as a common mode voltage to the ADC's differential inputs. In general, the source resistance should be kept below 2kΩ. Large values of bypass capacitors will eliminate this system noise pickup, but will also introduce input scaling errors as outlined in the previous section.
3. PROPER LAYOUT: Layout for a printed circuit board should ensure that digital and analog signal lines are kept separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. Both analog inputs and the reference input should be screened by AGND. A single point analog ground which is separate from the logic ground system should be established at or near the AD7571. This single point analog ground subsystem should be connected to the digital ground system by a single-track connection only. Any reference bypass capacitors, analog input filter capacitors or input signal shielding should be returned to the analog ground point.

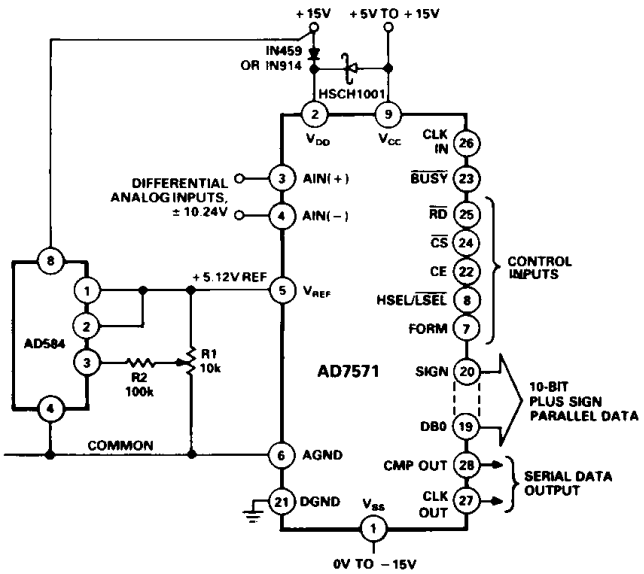


Figure 16. AD7571 Operational Diagram (see Table I for Pin Function Description)

4. OFFSET ERROR: For either positive or negative differential inputs, the procedure for adjusting the input offset error to zero is similar. The circuit for zero offset adjust is shown connected to the AIN(−) input which is assumed to be at some common mode voltage V_{CM}. For positive differential inputs the AIN(+) input is forced to V_{CM} +10mV (V_{CM} + 1LSB) while the potentiometer is adjusted until the ADC output code flickers between 000 . . . . 00 and 000 . . . . 01. For negative differential inputs the AIN(+) input is forced to V_{CM} − 10mV (V_{CM} − 1LSB) while the potentiometer is adjusted until the ADC output code flickers between 100 . . . . 00 and 100 . . . . 01.

   In applications where the differential input voltage can swing both positive and negative no offset adjust is required since the offset errors for both positive and negative differential inputs are already mirror images of each other due to the architecture of the AD7571.

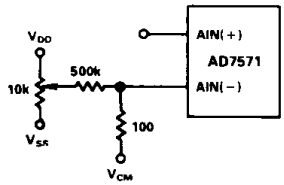


Figure 17. Zero Offset Adjust Circuit

5. FULL-SCALE ADJUST: The full-scale adjustment is made by applying a positive or negative differential input voltage to the analog inputs which is 1LSB down from the required positive or negative analog full scale range. The magnitude of the reference voltage V_{REF} is then adjusted until the ADC output code flickers between 011 . . . . 10 and 011 . . . . 11 for a positive differential input or between 111 . . . . 10 and 111 . . . . 11 for a negative differential input.
6. SUPPLY SEQUENCING: Do not allow V_{CC} to exceed V_{DD}. In cases where V_{CC} could exceed V_{DD}, the diode protection scheme shown in Figure 16 is recommended.