4-Channel DAS with 16-Bit, Bipolar Input, Simultaneous Sampling ADC

Data Sheet

AD7605-4

FEATURES

- 4 simultaneously sampled inputs
- True bipolar analog input ranges: ±10 V (maximum), ±5 V (maximum)
- Single 5 V analog supply and 2.5 V to 5 V V_{DRIVE} (nominal)
- Fully integrated data acquisition solution
  - Analog input clamp protection
  - Input buffer with 1 MΩ analog input impedance
  - Second-order antialiasing analog filter
  - On-chip accurate reference and reference buffer
  - 16-bit ADC with 300 kSPS on all channels
- Flexible parallel/serial interface
  - Serial peripheral interface (SPI)/QSPI/MICROWIRE/DSP compatible
- Performance
  - 7 kV ESD rating on analog input pins
  - Standby mode: 25 mW (typical)
- 64-lead LQFP package

APPLICATIONS

- Power line monitoring and protection systems
- Multiphase motor control
- Instrumentation and control systems
- Multiaxis positioning systems
- Data acquisition systems (DAS)

GENERAL DESCRIPTION

The AD7605-4[1] is a 4-channel, 16-bit, simultaneous sampling, analog-to-digital data acquisition system (DAS). The device contains analog input clamp protection, a second-order antialiasing filter, a track-and-hold amplifier, a 16-bit charge redistribution successive approximation analog-to-digital converter (ADC), a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces.

The AD7605-4 operates from a single 5 V supply and can accommodate ±10 V and ±5 V true bipolar input signals while sampling at throughput rates of up to 300 kSPS for all channels. The input clamp protection circuitry can tolerate voltages up to ±16.5 V. The AD7605-4 has 1 MΩ analog input impedance, regardless of sampling frequency. The single-supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies.

The AD7605-4 is SPI, QSPI™, MICROWIRE™, and digital signal processor (DSP) compatible.

Table 1. High Resolution, Bipolar Input, Simultaneous Sampling DAS Solutions

Resolution (Bits)	Single-Ended Inputs	True Differential Inputs	No. of Simultaneous Sampling Channels
18	AD7608	AD7609	8
16	AD7606		8
	AD7606-6		6
	AD7606-4		4
	AD7605-4		4
14	AD7607		8

FUNCTIONAL BLOCK DIAGRAM

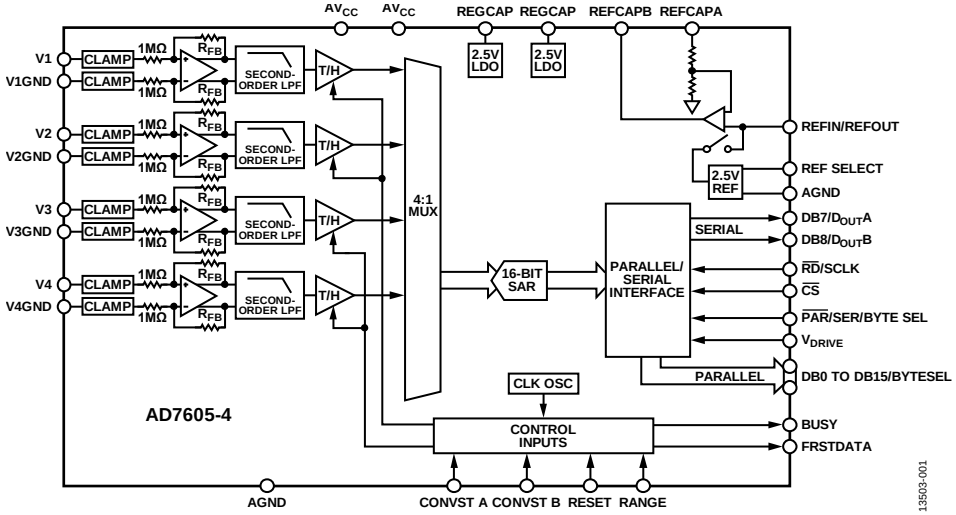

Figure 1.

[1] Protected by U.S. Patent No. 8,072,360 B2.

Rev. 0 Document Feedback

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7605-4 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1091: Configuring the AD7606/AD7607 for Slow Supply Ramp Conditions

Data Sheet

- AD7605-4: 4-Channel DAS with 16-Bit, Bipolar Input, Simultaneous Sampling ADC Data Sheet

User Guides

- UG-851: Evaluating the AD7606/AD7606-6/AD7606-4/AD7607/AD7608 and AD7605-4 16-Bit Simultaneous Sampling, 8-/6-/4-Channel, SAR ADC

SOFTWARE AND SYSTEMS REQUIREMENTS

- CED1Z FPGA Project for AD7606 with Nios driver

TOOLS AND SIMULATIONS

- AD7605-4 IBIS Model

REFERENCE DESIGNS

- CN0148

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7605-4 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7605-4 EngineerZone Discussions.

SAMPLE AND BUY

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DOCUMENT FEEDBACK

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REVISION HISTORY

9/2016—Revision 0: Initial Version

SPECIFICATIONS

V_{REF} = 2.5 V external/internal, AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V, f_{SAMPLE} = 300 kSPS, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	f_{IN} = 1 kHz sine wave, unless otherwise noted				
Signal-to-Noise Ratio (SNR)	±10 V range	86.5	90		dB
	±5 V range	86	89		dB
Signal-to-(Noise + Distortion) (SINAD) Ratio	±10 V range	86.5	90		dB
	±5 V range	86	89		dB
Dynamic Range	±10 V range		90.5		dB
	±5 V range		90		dB
Total Harmonic Distortion (THD)			−107	−95	dB
Spurious-Free Dynamic Range (SFDR)			−108		dB
Intermodulation Distortion (IMD)	fa = 1 kHz, fb = 1.1 kHz				
Second-Order Terms			−110		dB
Third-Order Terms			−106		dB
Channel-to-Channel Isolation	f_{IN} on unselected channels up to 160 kHz		−95		dB
ANALOG INPUT FILTER					
Full Power Bandwidth	−3 dB, ±10 V range		23		kHz
	−3 dB, ±5 V range		15		kHz
	−0.1 dB, ±10 V range		10		kHz
	−0.1 dB, ±5 V range		5		kHz
$t_{GROUP\ DELAY}$	±10 V range		11		µs
	±5 V range		15		µs
DC ACCURACY					
Resolution	No missing codes	16			Bits
Differential Nonlinearity			±0.5	±0.99	LSB[1]
Integral Nonlinearity			±0.5	±2	LSB
Total Unadjusted Error (TUE)	±10 V range		±6		LSB
	±5 V range		±12		LSB
Positive Full-Scale (PFS) Error	External reference		±8	±32	LSB
	Internal reference		±8		LSB
Drift	External reference		±2		ppm/°C
	Internal reference		±7		ppm/°C
Matching	±10 V range		5	32	LSB
	±5 V range		16	40	LSB
Bipolar Zero Code Error	±10 V range		±1	±6	LSB
	±5 V range		±3	±12	LSB
Drift	±10 V range		10		µV/°C
	±5 V range		5		µV/°C
Matching	±10 V range		1	8	LSB
	±5 V range		6	22	LSB
Negative Full-Scale (NFS) Error	External reference		±8	±32	LSB
	Internal reference		±8		LSB
Drift	External reference		±4		ppm/°C
	Internal reference		±8		ppm/°C
Matching	±10 V range		5	32	LSB
	±5 V range		16	40	LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT					
Input Voltage Range	RANGE = 1			±10	V
	RANGE = 0			±5	V
Analog Input Current	Input voltage (V_{IN}) = 10 V		9		μA
	V_{IN} = 5 V		2.5		μA
Input Capacitance			5		pF
Input Impedance			1		MΩ
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range		2.475	2.5	2.525	V
DC Leakage Current				±1	μA
Input Capacitance	REF SELECT = 1		7.5		pF
Reference Output Voltage	REFIN/REFOUT		2.49 to 2.505		V
Reference Temperature Coefficient			±10		ppm/°C
LOGIC INPUTS					
Input Voltage					
High (V_{INH})		0.7 × V_{DRIVE}			V
Low (V_{INL})				0.3 × V_{DRIVE}	V
Input Current (I_{IN})				±2	μA
Input Capacitance (C_{IN})			5		pF
LOGIC OUTPUTS					
Output Voltage					
High (V_{OH})	I_{SOURCE} = 100 μA	V_{DRIVE} − 0.2			V
Low (V_{OL})	I_{SINK} = 100 μA			0.2	V
Floating State					
Leakage Current			±1	±20	μA
Output Capacitance			5		pF
Output Coding	Twos complement		16		Bits
CONVERSION RATE					
Conversion Time	All four channels included		2		μs
Track-and-Hold Acquisition Time			1		μs
Throughput Rate	Per channel, all four channels included		300		kSPS
POWER REQUIREMENTS					
AV_{CC}		4.75	5	5.25	V
V_{DRIVE}	2.5 V to 5 V nominal	2.3		5.25	V
Total Current, I_{TOTAL}	Digital inputs = 0 V or V_{DRIVE}				
Normal Mode					
Static			10	12	mA
Operational	f_{SAMPLE} = 300 kSPS		12	15.2	mA
Standby Mode			5	8	mA
Shutdown Mode			2	6	μA
Power Dissipation					
Normal Mode					
Static			52	61	mW
Operational	f_{SAMPLE} = 300 kSPS		71	80	mW
Standby Mode			25	42	mW
Shutdown Mode			10	31.5	μW

[1] LSB means least significant bit. With a ±5 V input range, 1 LSB = 152.58 μV. With a ±10 V input range, 1 LSB = 305.175 μV.

TIMING SPECIFICATIONS

AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V, V_{REF} = 2.5 V external reference/internal reference, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Note that throughout this data sheet, multifunction pins, such as $\overline{RD}$/SCLK, are referred to either by the entire pin name or by a single function of the pin, for example, $\overline{RD}$, when only that function is relevant.

Table 3.

Parameter	$V_{INL} = 0.1 \times V_{DRIVE}$ and $V_{INH} = 0.9 \times V_{DRIVE}$ Logic Input Levels			$V_{INL} = 0.3 \times V_{DRIVE}$ and $V_{INH} = 0.7 \times V_{DRIVE}$ Logic Input Levels			Unit	Description
	Min	Typ	Max	Min	Typ	Max		
PARALLEL/SERIAL/BYTE MODE								See Figure 2 and Figure 3
t_{CYCLE}	3.33			3.33			µs	1/throughput rate, parallel mode, reading during or after conversion; or serial mode: V_{DRIVE} = 3.3 V to 5.25 V, reading during a conversion using $D_{OUT}A$ and $D_{OUT}B$ lines
t_{CONV}		2	2.08		2	2.08	µs	Conversion time
$t_{WAKE-UP\ STANDBY}$			100			100	µs	$\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from standby mode; not shown in Figure 2 or Figure 3
$t_{WAKE-UP\ SHUTDOWN}$								Not shown in Figure 2 or Figure 3
Internal Reference			30			30	ms	$\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from shutdown mode
External Reference			13			13	ms	$\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from shutdown mode
t_{RESET}	50			50			ns	RESET high pulse width
t_1			40			45	ns	CONVST x high to BUSY high
t_2	25			25			ns	Minimum CONVST x low pulse
t_3	25			25			ns	Minimum CONVST x high pulse
t_4	0			0			ns	BUSY falling edge to $\overline{CS}$ falling edge setup time
t_5			0.5			0.5	ms	Maximum delay allowed between CONVST A and CONVST B rising edges
t_6			25			25	ns	Maximum time between last $\overline{CS}$ rising edge and BUSY falling edge
t_7	25			25			ns	Minimum delay between RESET low to CONVST x high
PARALLEL/BYTE READ OPERATION								See Figure 4, Figure 5, and Figure 7
t_8	0			0			ns	$\overline{CS}$ to $\overline{RD}$ setup time
t_9	0			0			ns	$\overline{CS}$ to $\overline{RD}$ hold time
t_{10}								$\overline{RD}$ low pulse width
	16			19			ns	V_{DRIVE} above 4.75 V
	21			24			ns	V_{DRIVE} above 3.3 V
	25			30			ns	V_{DRIVE} above 2.7 V
	32			37			ns	V_{DRIVE} above 2.3 V
t_{11}	15			15			ns	$\overline{RD}$ high pulse width
t_{12}	22			22			ns	$\overline{CS}$ high pulse width; $\overline{CS}$ and $\overline{RD}$ linked
t_{13}								Delay from $\overline{CS}$ until DB15 to DB0 three-state disabled
			16			19	ns	V_{DRIVE} above 4.75 V
			20			24	ns	V_{DRIVE} above 3.3 V
			25			30	ns	V_{DRIVE} above 2.7 V
			30			37	ns	V_{DRIVE} above 2.3 V
t_{14}								Data access time after $\overline{RD}$ falling edge
			16			19	ns	V_{DRIVE} above 4.75 V
			21			24	ns	V_{DRIVE} above 3.3 V
			25			30	ns	V_{DRIVE} above 2.7 V
			32			37	ns	V_{DRIVE} above 2.3 V

Parameter	$V_{INL} = 0.1 \times V_{DRIVE}$ and $V_{INH} = 0.9 \times V_{DRIVE}$ Logic Input Levels			$V_{INL} = 0.3 \times V_{DRIVE}$ and $V_{INH} = 0.7 \times V_{DRIVE}$ Logic Input Levels			Unit	Description
	Min	Typ	Max	Min	Typ	Max		
t_{15}	6			6			ns	Data hold time after $\overline{RD}$ falling edge
t_{16}	6			6			ns	$\overline{CS}$ to DB15 to DB0 hold time
t_{17}			22			22	ns	Delay from $\overline{CS}$ rising edge to DB15 to DB0 three-state enabled
SERIAL READ OPERATION								See Figure 6
f_{SCLK}								Frequency of serial read clock
			23.5			20	MHz	V_{DRIVE} above 4.75 V
			17			15	MHz	V_{DRIVE} above 3.3 V
			14.5			12.5	MHz	V_{DRIVE} above 2.7 V
			11.5			10	MHz	V_{DRIVE} above 2.3 V
t_{18}								Delay from $\overline{CS}$ until $D_{OUT}A/D_{OUT}B$ three-state disabled/delay from $\overline{CS}$ until MSB valid
			15			18	ns	V_{DRIVE} above 4.75 V
			20			23	ns	V_{DRIVE} above 3.3 V
			30			35	ns	V_{DRIVE} = 2.3 V to 2.7 V
t_{19}								Data access time after SCLK rising edge
			17			20	ns	V_{DRIVE} above 4.75 V
			23			26	ns	V_{DRIVE} above 3.3 V
			27			32	ns	V_{DRIVE} above 2.7 V
			34			39	ns	V_{DRIVE} above 2.3 V
t_{20}	$0.4 \times t_{SCLK}$			$0.4 \times t_{SCLK}$			ns	SCLK low pulse width
t_{21}	$0.4 \times t_{SCLK}$			$0.4 \times t_{SCLK}$			ns	SCLK high pulse width
t_{22}	7			7			ns	SCLK rising edge to $D_{OUT}A/D_{OUT}B$ valid hold time
t_{23}			22			22	ns	$\overline{CS}$ rising edge to $D_{OUT}A/D_{OUT}B$ three-state enabled
FRSTDATA OPERATION								See Figure 4 and Figure 7
t_{24}								Delay from $\overline{CS}$ falling edge until FRSTDATA three-state disabled
			15			18	ns	V_{DRIVE} above 4.75 V
			20			23	ns	V_{DRIVE} above 3.3 V
			25			30	ns	V_{DRIVE} above 2.7 V
			30			35	ns	V_{DRIVE} above 2.3 V
t_{25}								Delay from $\overline{CS}$ falling edge until FRSTDATA high, serial mode
			15			18	ns	V_{DRIVE} above 4.75 V
			20			23	ns	V_{DRIVE} above 3.3 V
			25			30	ns	V_{DRIVE} above 2.7 V
			30			35	ns	V_{DRIVE} above 2.3 V
t_{26}								Delay from $\overline{RD}$ falling edge to FRSTDATA high
			16			19	ns	V_{DRIVE} above 4.75 V
			20			23	ns	V_{DRIVE} above 3.3 V
			25			30	ns	V_{DRIVE} above 2.7 V
			30			35	ns	V_{DRIVE} above 2.3 V
t_{27}								Delay from $\overline{RD}$ falling edge to FRSTDATA low
			19			22	ns	V_{DRIVE} = 3.3 V to 5.25V
			24			29	ns	V_{DRIVE} = 2.3 V to 2.7V
t_{28}								Delay from 16th SCLK falling edge to FRSTDATA low
			17			20	ns	V_{DRIVE} = 3.3 V to 5.25V
			22			27	ns	V_{DRIVE} = 2.3 V to 2.7V
t_{29}			24			29	ns	$\overline{CS}$ rising edge until FRSTDATA three-state enabled

Timing Diagrams

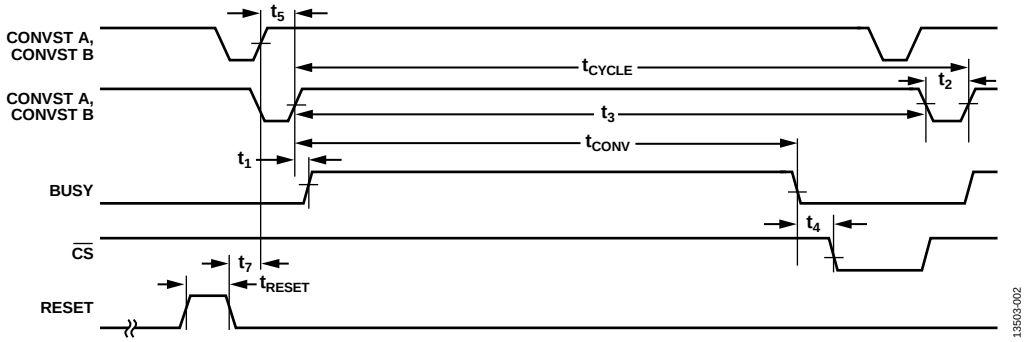


Figure 2. CONVST x Timing—Reading After a Conversion

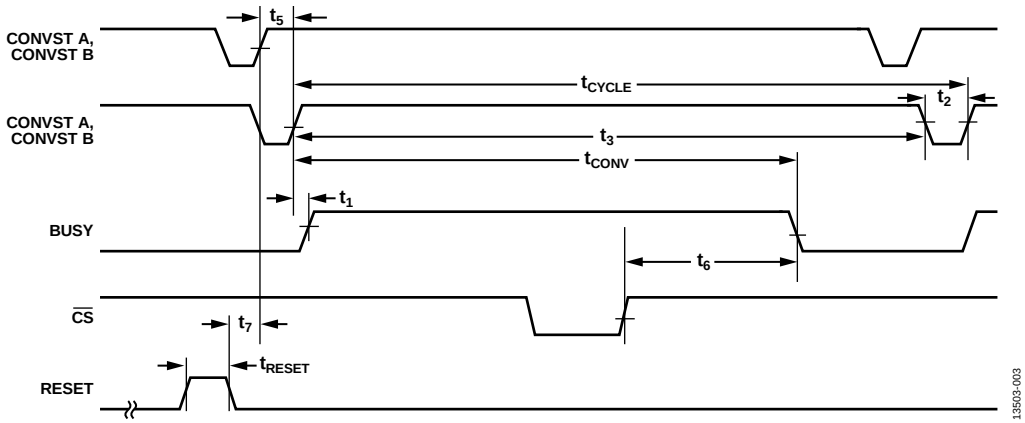


Figure 3. CONVST x Timing—Reading During a Conversion

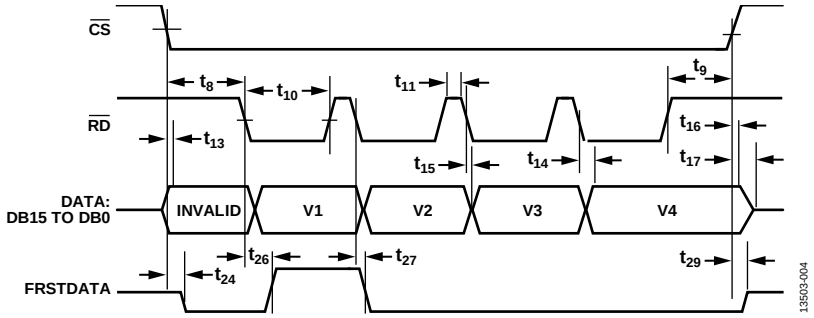


Figure 4. Parallel Mode, Separate $\overline{CS}$ and $\overline{RD}$ Pulses

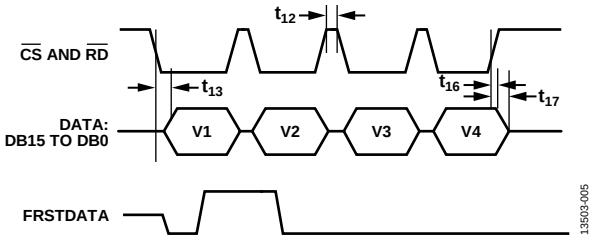


Figure 5. $\overline{CS}$ and $\overline{RD}$, Linked Parallel Mode

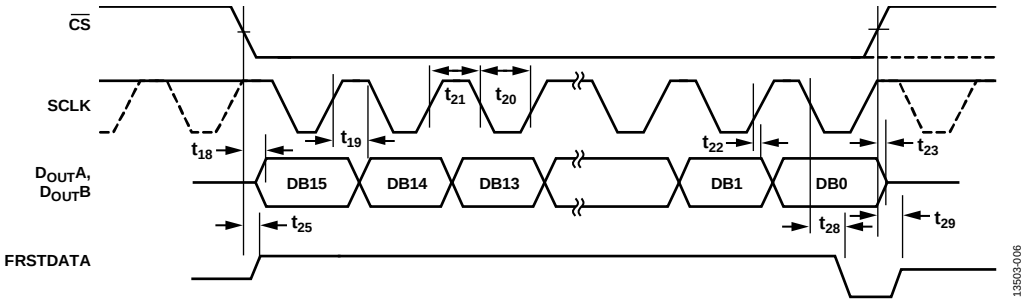


Figure 6. Serial Read Operation

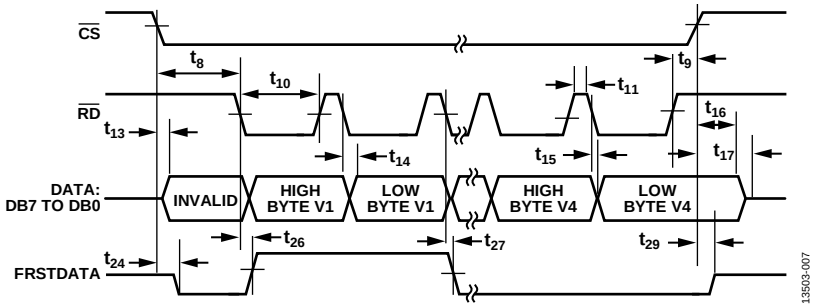


Figure 7. Parallel Byte Mode Read Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
AV_{CC} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to AV_{CC} + 0.3 V
Analog Input Voltage to AGND[1]	±16.5 V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN/REFOUT to AGND	−0.3 V to AV_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb/Sn Temperature, Soldering	
Reflow (10 sec to 30 sec)	240 (+0)°C
Pb-Free Temperature, Soldering Reflow	260 (+0)°C
ESD	
All Pins Except Analog Inputs	2 kV
Analog Input Pins Only	7 kV

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance, measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
ST-64-2	45.5	9.5	°C/W

[1] The thermal resistance specifications are based on the device being mounted to a JEDEC 2P2S compliant, 4-layer PCB, as per JEDEC Standard JESD51-7.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

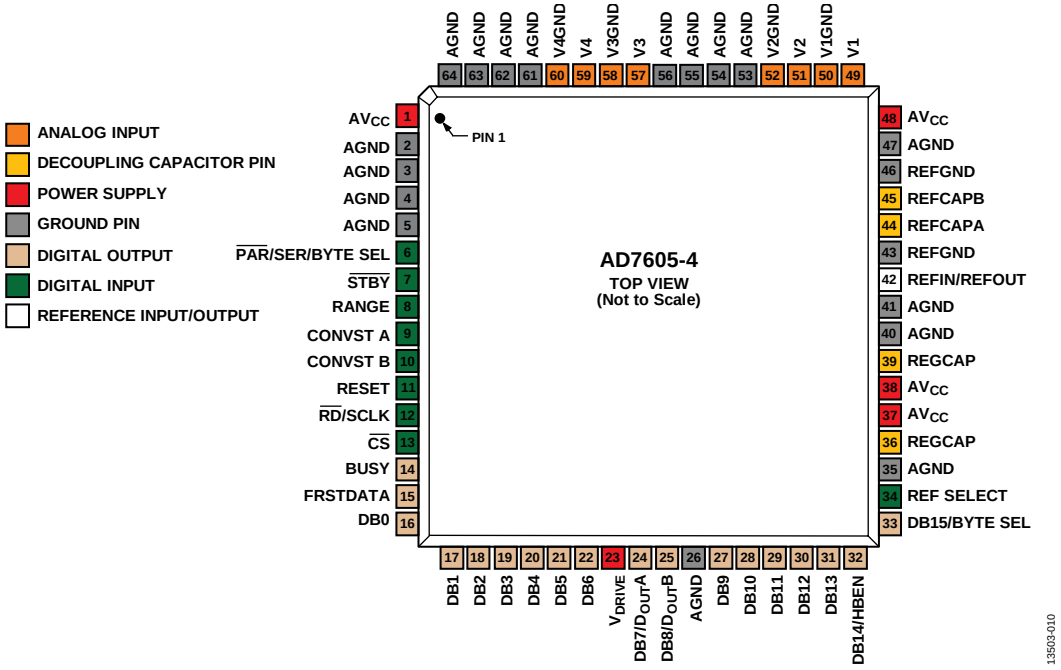


Figure 8. Pin Configuration

Table 6. Pin Function Descriptions[1]

Pin No.	Type[2]	Mnemonic	Description
1, 37, 38, 48	P	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. Decouple these supply pins to AGND.
2, 3, 4, 5, 26, 35, 40, 41, 47	GND	AGND	Analog Ground. These pins are the ground reference points for all analog circuitry on the AD7605-4. Refer all analog input signals and external reference signals to these pins. Connect all AGND pins to the AGND plane of a system.
6	DI	$\overline{PAR}$/SER/ BYTE SEL	Parallel Interface Selection Input ($\overline{PAR}$). This pin is a logic input. If this pin is tied to a logic low, the parallel interface is selected. Parallel byte interface mode is selected when this pin is logic high and DB15/BYTE SEL is logic high (see Table 8). Serial Interface Selection Input (SER). If this pin is tied to a logic high, the serial interface is selected. In serial mode, the $\overline{RD}$/SCLK pin functions as the serial clock input. The DB7/D_{OUT}A pin and the DB8/D_{OUT}B pin function as serial data outputs. When the serial interface is selected, tie the parallel output data bit pins (Pin 16 to Pin 22, and Pin 27 to Pin 33) to ground. Parallel Byte Interface Selection Input (BYTE SEL). In byte mode, DB15/BYTE SEL, in conjunction with $\overline{PAR}$/SER/BYTE SEL, selects the parallel byte mode of operation (see Table 8). DB14/HBEN functions as the high byte enable (HBEN) pin. DB7 to DB0 transfer the 16-bit conversion results in two $\overline{RD}$/SCLK operations, with DB0 as the LSB of the data transfers.
7	DI	$\overline{STBY}$	Standby Mode Input. This pin places the AD7605-4 into one of two power-down modes: standby mode or shutdown mode. The power-down mode entered depends on the state of the RANGE pin, as shown in Table 7. When in standby mode, all circuitry, except the on-chip reference, regulators, and regulator buffers, is powered down. When in shutdown mode, all circuitry is powered down.
8	DI	RANGE	Analog Input Range Selection. RANGE is a logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is ±10 V for all channels. If this pin is tied to a logic low, the analog input range is ±5 V for all channels. A logic change on this pin has an immediate effect on the analog input range. Changing this pin during a conversion is not recommended for fast throughput rate applications. See the Analog Input section for more information.

Pin No.	Type[2]	Mnemonic	Description
9	DI	CONVST A	Conversion Start Input A. CONVST A is a logic input. Use this logic input to initiate conversions on the analog input channels. For simultaneous sampling of all input channels, CONVST A and CONVST B can be shorted together, and a single convert start signal can be applied. Alternatively, CONVST A can be used to initiate simultaneous sampling of V1 and V2. When the CONVST A pin transitions from low to high, the front-end track-and-hold circuitry for the respective analog input is set to hold.
10	DI	CONVST B	Conversion Start Input B. CONVST B is a logic input. Use this logic input to initiate conversions on the analog input channels. For simultaneous sampling of all input channels, CONVST A and CONVST B can be shorted together, and a single convert start signal can be applied. CONVST B can be used to initiate simultaneous sampling on V3 and V4. When the CONVST B pin transitions from low to high, the front-end track-and-hold circuitry for the respective analog input is set to hold.
11	DI	RESET	Reset Input. When set to logic high, the rising edge of RESET resets the AD7605-4. The device receives a RESET pulse after power-up. The RESET high pulse is typically 50 ns wide. If a RESET pulse is applied during a conversion, the conversion is aborted. If a RESET pulse is applied during a read, the contents of the output registers reset to all zeros.
12	DI	$\overline{RD}$/SCLK	Parallel Data Read Control Input When the Parallel Interface Is Selected ($\overline{RD}$). When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the output bus is enabled. Serial Clock Input When the Serial Interface Is Selected (SCLK). In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{CS}$ falling edge takes the $D_{OUT}A$ and $D_{OUT}B$ data output lines out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the $D_{OUT}A$ and $D_{OUT}B$ serial data outputs. For more information, see the Conversion Control section.
13	DI	$\overline{CS}$	Chip Select. This active low logic input frames the data transfer. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the DB[15:0] output bus is enabled and the conversion result is output on the parallel data bus lines. In serial mode, $\overline{CS}$ frames the serial read transfer and clocks out the MSB of the serial output data.
14	DO	BUSY	Busy Output. This pin transitions to a logic high after both CONVST A and CONVST B rising edges and indicates that the conversion process has started. The BUSY output remains high until the conversion process for all channels is complete. The falling edge of the BUSY pin signals that the conversion data is being latched into the output data registers and is available to read after a period of time, t_4. Any data read while BUSY is high must be completed before the falling edge of BUSY occurs. Rising edges on CONVST A or CONVST B have no effect while the BUSY signal is high.
15	DO	FRSTDATA	Digital Output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on the parallel, byte, or serial interface. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. The falling edge of $\overline{CS}$ takes FRSTDATA out of three-state. In parallel mode, the falling edge of $\overline{RD}$ corresponding to the result of V1, then sets the FRSTDATA pin high, indicating that the result from V1 is available on the output data bus. The FRSTDATA output returns to a logic low following the next falling edge of $\overline{RD}$. In serial mode, FRSTDATA goes high on the falling edge of $\overline{CS}$ because this clocks out the MSB of V1 on $D_{OUT}A$. FRSTDATA returns low on the 16th SCLK falling edge after the $\overline{CS}$ falling edge. See the Conversion Control section for more details.
16 to 22	DO	DB0 to DB6	Parallel Output Data Bits, DB0 to DB6. When $\overline{PAR}$/SER/BYTE SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB6 to DB0 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, tie these pins to AGND. When operating in parallel byte interface mode, DB7 to DB0 outputs the 16-bit conversion result in two $\overline{RD}$ operations. DB7 (Pin 24) is the MSB; DB0 is the LSB.
23	P	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin, 2.3 V to 5.25 V, determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface (that is, DSP and field-programmable gate array (FPGA)).
24	DO	DB7/$D_{OUT}A$	Parallel Output Data Bit 7 (DB7). When $\overline{PAR}$/SER/BYTE SEL = 0, this pins acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin outputs DB7 of the conversion result. Serial Interface Data Output Pin ($D_{OUT}A$). When $\overline{PAR}$/SER/BYTE SEL = 1, this pin functions as $D_{OUT}A$ and outputs serial conversion data (see the Conversion Control section for more details). When operating in parallel byte mode, DB7 is the MSB of the byte.
25	DO	DB8/$D_{OUT}B$	Parallel Output Data Bit 8 (DB8). When $\overline{PAR}$/SER/BYTE SEL = 0, this pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin outputs DB8 of the conversion result. Serial Interface Data Output Pin ($D_{OUT}B$). When $\overline{PAR}$/SER/BYTE SEL = 1, this pin functions as $D_{OUT}B$ and outputs serial conversion data (see the Conversion Control section for more details).
27 to 31	DO	DB9 to DB13	Parallel Output Data Bits, DB9 to DB13. When $\overline{PAR}$/SER/BYTE SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB13 to DB9 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, tie these pins to AGND.

Pin No.	Type[2]	Mnemonic	Description
32	DO/DI	DB14/ HBEN	Parallel Output Data Bit 14 (DB14). When $\overline{PAR}$/ SER/BYTE SEL = 0, this pin acts as a three-state parallel digital output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin outputs DB14 of the conversion result. High Byte Enable (HBEN). When $\overline{PAR}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1, the AD7605-4 operates in parallel byte interface mode. In parallel byte mode, the HBEN pin selects whether the most significant byte (MSB) or the least significant byte (LSB) of the conversion result is output first. When HBEN = 1, the MSB is output first, followed by the LSB. When HBEN = 0, the LSB is output first, followed by the MSB. In serial mode, tie this pin to AGND.
33	DO/DI	DB15/ BYTE SEL	Parallel Output Data Bit 15 (DB15). When $\overline{PAR}$/SER/BYTE SEL = 0, this pin acts as a three-state parallel digital output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin outputs DB15 of the conversion result. Parallel Byte Mode Select (BYTE SEL). When $\overline{PAR}$/SER/BYTE SEL = 1, the BYTE SEL pin selects between serial interface mode and parallel byte interface mode (see Table 8). When $\overline{PAR}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 0, the AD7605-4 operates in serial interface mode. When $\overline{PAR}$/ SER/BYTE SEL = 1 and DB15/BYTE SEL = 1, the AD7605-4 operates in parallel byte interface mode.
34	DI	REF SELECT	Internal/External Reference Selection Input. REF SELECT is a logic input. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
36, 39	CAP	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple these output pins separately to AGND using a 1 µF capacitor. The voltage on these pins is in the range of 2.5 V to 2.7 V.
42	REF	REFIN/ REFOUT	Reference Input (REFIN)/Reference Output (REFOUT). The on-chip reference of 2.5 V is available on this pin for external use if the REF SELECT pin is set to logic high. Alternatively, the internal reference can be disabled by setting the REF SELECT pin to logic low, and an external reference of 2.5 V can be applied to this input (see the Internal/External Reference section). Decoupling is required on this pin for both the internal and external reference options. Apply a 10 µF capacitor from this pin to ground close to the REFGND pins.
43, 46	GND	REFGND	Reference Ground Pins. Connect these pins to AGND.
44, 45	CAP	REFCAPA, REFCAPB	Reference Buffer Output Force/Sense Pins. These pins must be connected together and decoupled to AGND using a low effective series resistance (ESR), 10 µF ceramic capacitor. The voltage on these pins is typically 4.5 V.
49	AI	V1	Analog Input 1. This pin is a single-ended analog input. The analog input range of this channel is determined by the RANGE pin.
50, 52	AI GND	V1GND, V2GND	Analog Input Ground Pin 1 and Pin 2. These pins correspond to Analog Input Pin V1 and Analog Input Pin V2. Connect all analog input ground pins to the AGND plane of a system.
51	AI	V2	Analog Input 2. This pin is a single-ended analog input. The analog input range of this channel is determined by the RANGE pin.
53, 54, 55, 56	GND	AGND	Analog Ground. These pins are the ground reference points for all analog circuitry on the AD7605-4. Refer all analog input signals and external reference signals to these pins. Connect all the AGND pins to the AGND plane of a system.
57	AI	V3	Analog Input 3. This pin is a single-ended analog input. The analog input range of this channel is determined by the RANGE pin.
58	AI GND	V3GND	Analog Input Ground Pin 3. Connect all analog input ground pins to the AGND plane of a system.
59	AI	V4	Analog Input 4. This pin is a single-ended analog input.
60	AI GND	V4GND	Analog Input Ground Pin 4. Connect all analog input ground pins to the AGND plane of a system.
61, 62, 63, 64	AGND	AGND	Analog Ground. These pins are the ground reference points for all analog circuitry on the AD7605-4. Refer all analog input signals and external reference signals to these pins. Connect all the analog ground pins to the AGND plane of a system.

[1] Note that throughout this data sheet, multifunction pins, such as $\overline{RD}$/SCLK, are referred to either by the entire pin name or by a single function of the pin, for example, $\overline{RD}$, when only that function is relevant.
[2] P is power supply, DI is digital input, DO is digital output, REF is reference input/output, CAP is decoupling capacitor pin, AI is analog input, and GND is ground.

TYPICAL PERFORMANCE CHARACTERISTICS

AV_{CC} = 5 V, V_{DRIVE} = 5 V, ±10 V range, internal reference, T_A = 25°C, unless otherwise noted.

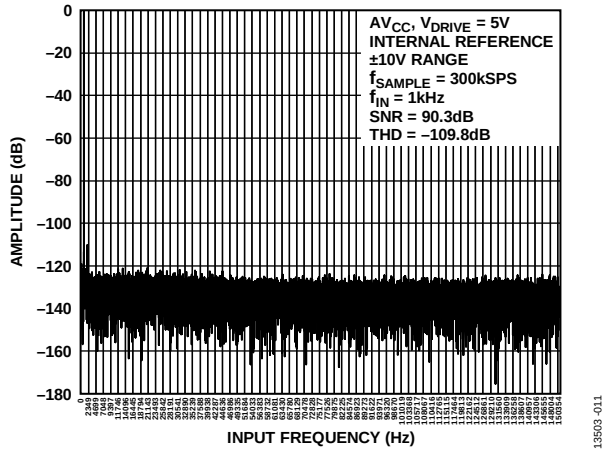


Figure 9. FFT Plot, ±10 V Range

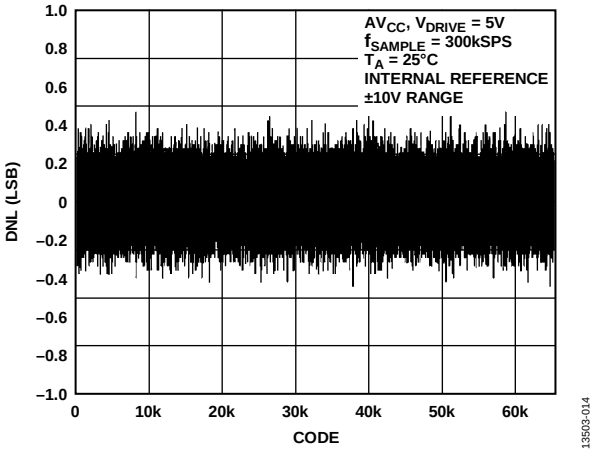


Figure 12. Typical DNL, ±10 V Range

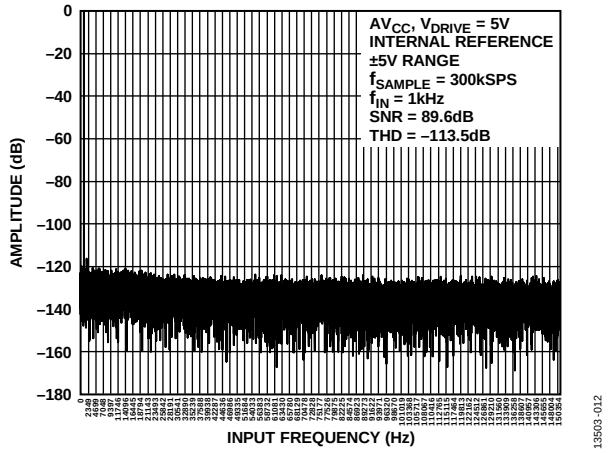


Figure 10. FFT Plot, ±5 V Range

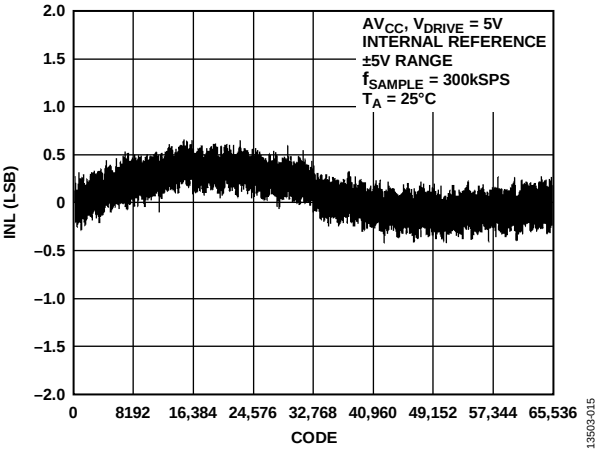


Figure 13. Typical INL, ±5 V Range

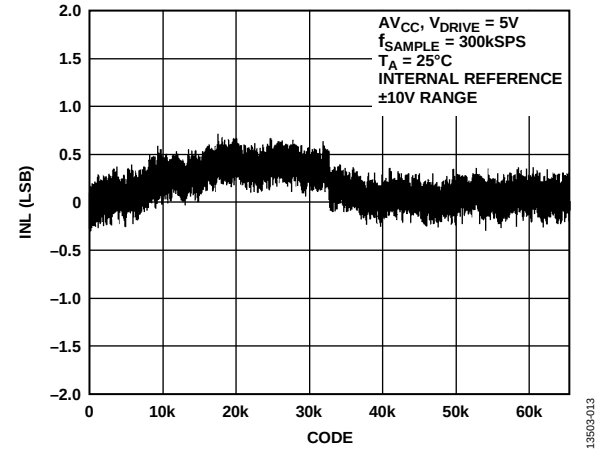


Figure 11. Typical INL, ±10 V Range

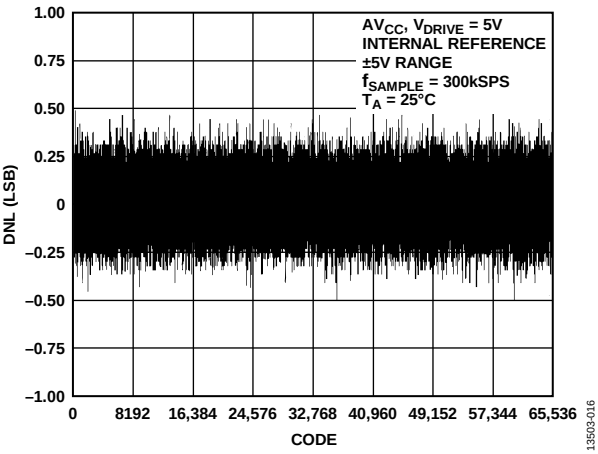


Figure 14. Typical DNL, ±5 V Range

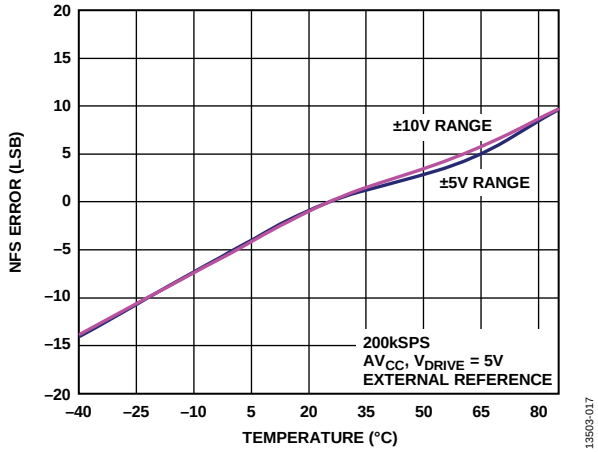


Figure 15. NFS Error vs. Temperature

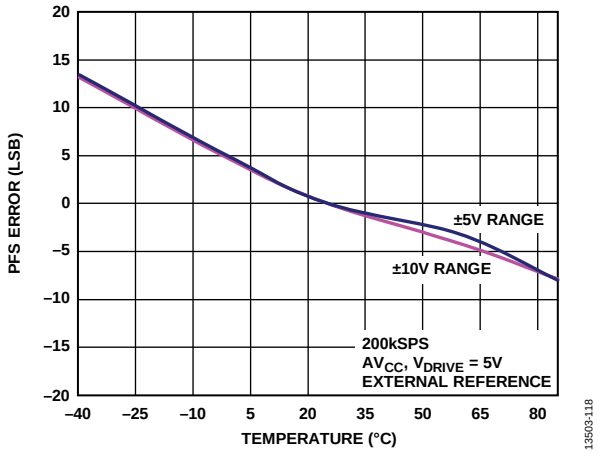


Figure 16. PFS Error vs. Temperature

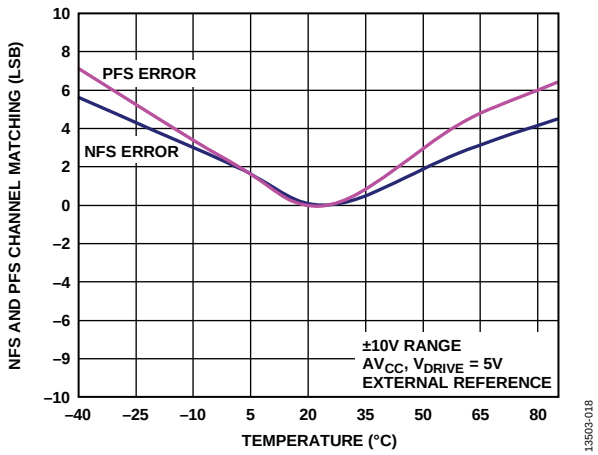


Figure 17. NFS and PFS Error Matching

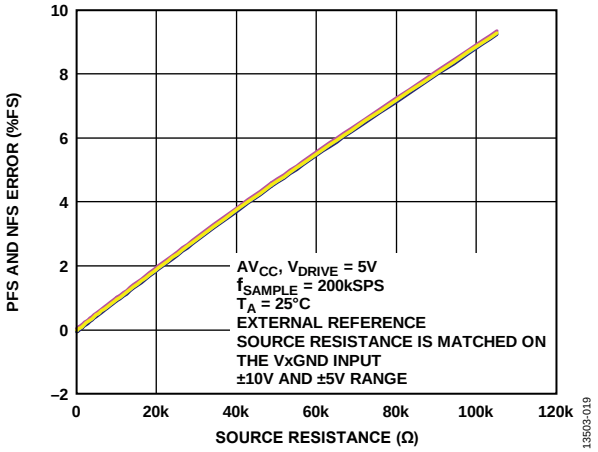


Figure 18. PFS and NFS Error vs. Source Resistance

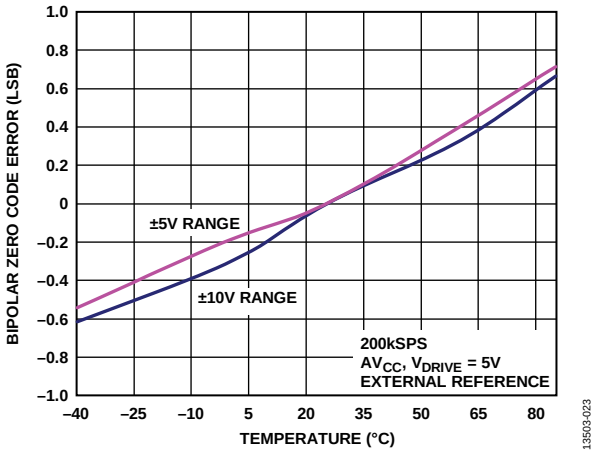


Figure 19. Bipolar Zero Code Error vs. Temperature

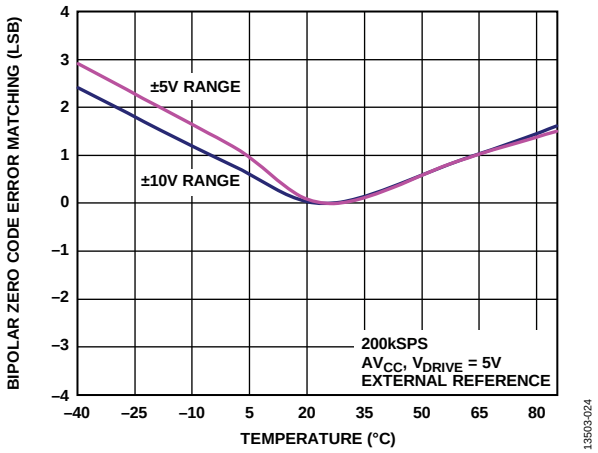


Figure 20. Bipolar Zero Code Error Matching Between Channels

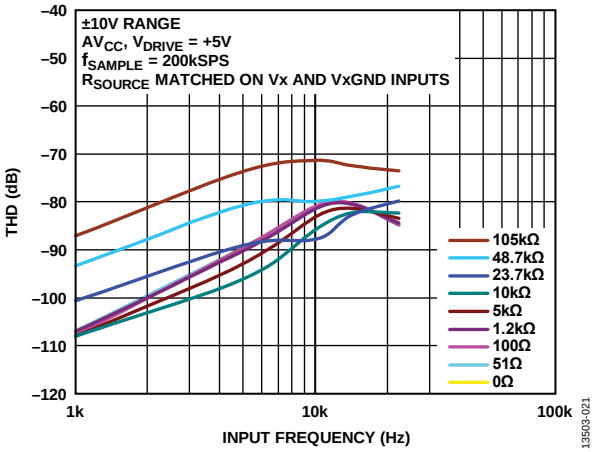


Figure 21. THD vs. Input Frequency for Various Source Impedances, ±10 V Range

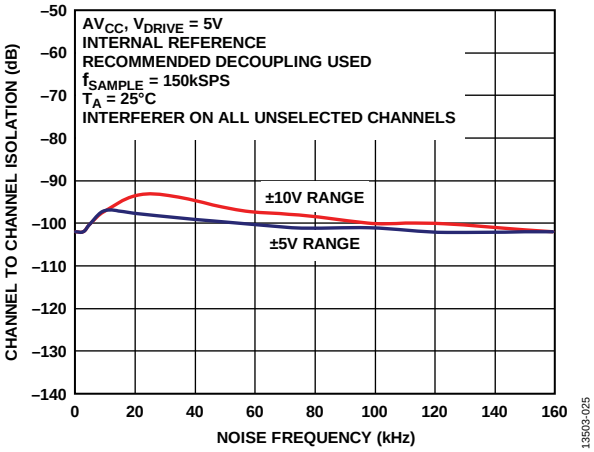


Figure 23. Channel to Channel Isolation

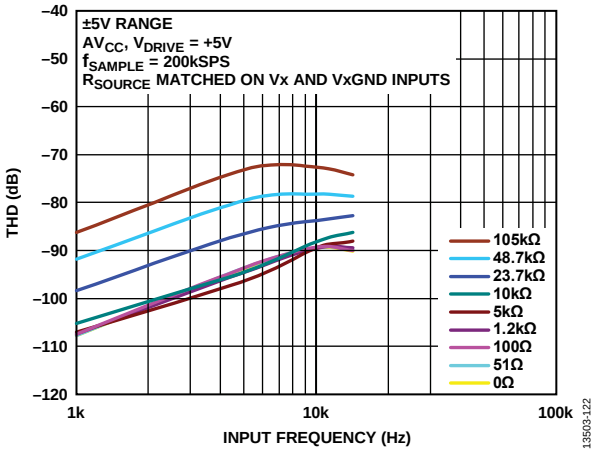


Figure 22. THD vs. Input Frequency for Various Source Impedances, ±5 V Range

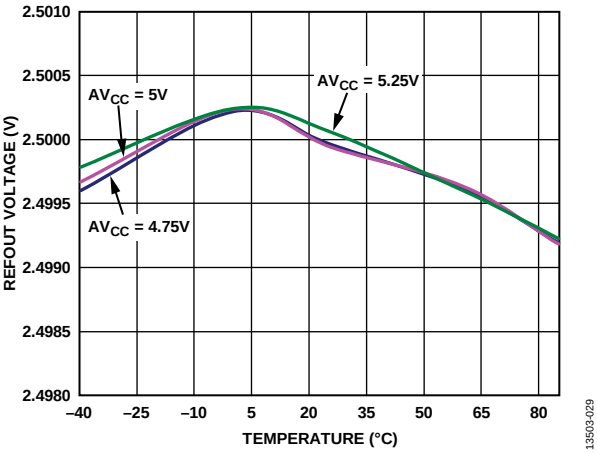


Figure 24. REFOUT Voltage vs. Temperature for Different Supply Voltages

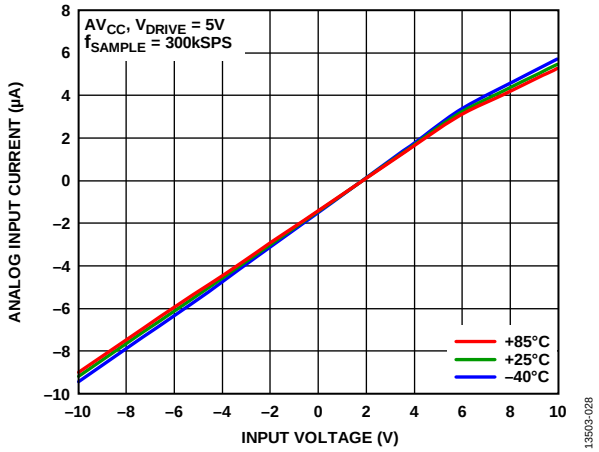


Figure 25. Analog Input Current vs. Input Voltage for Various Temperatures

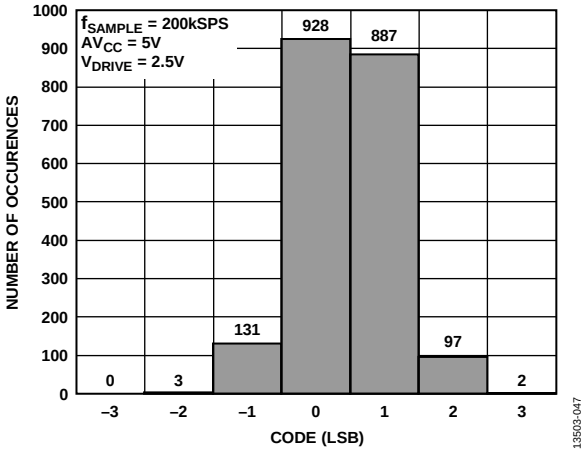


Figure 27. Histogram of Codes (Six Codes)

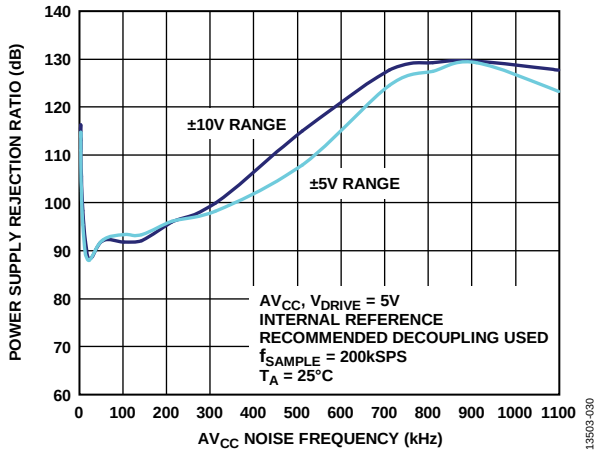


Figure 26. Power Supply Rejection Ratio (PSRR)

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, at ½ LSB below the first code transition; and full scale, at ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error
Bipolar zero code error is the deviation of the midscale transition (all 1s to all 0s) from the ideal, which is 0 V − ½ LSB.

Bipolar Zero Code Error Matching
Bipolar zero code error matching is the absolute difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error
Positive full-scale error is the deviation of the actual last code transition from the ideal last code transition (10 V − 1½ LSB (9.99954) and 5 V − 1½ LSB (4.99977)) after bipolar zero code error is adjusted out. The positive full-scale error includes the contribution from the internal reference buffer.

Positive Full-Scale Error Matching
Positive full-scale error matching is the absolute difference in positive full-scale error between any two input channels.

Negative Full-Scale Error
Negative full-scale error is the deviation of the first code transition from the ideal first code transition (−10 V + ½ LSB (−9.99984) and −5 V + ½ LSB (−4.99992)) after the bipolar zero code error is adjusted out. The negative full-scale error includes the contribution from the internal reference buffer.

Negative Full-Scale Error Match
Negative full-scale error match is the absolute difference in negative full-scale error between any two input channels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$, excluding dc).

The ratio depends on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise.

The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Thus, for a 16-bit converter, the ideal signal-to-(noise + distortion) is 98 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the harmonics to the fundamental. For the AD7605-4, it is defined as

$$THD\ (\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + V_8^2 + V_9^2}}{V_1}$$

where:
V_2 to V_9 are the rms amplitudes of the second through ninth harmonics.
V_1 is the rms amplitude of the fundamental.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3. Intermodulation distortion terms are those for which neither m nor n is equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels (dB).

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The PSRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the ADC's V_{DD} and V_{SS} supplies of Frequency f_S.

$$PSRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is equal to the power at Frequency f in the ADC output.
Pf_S is equal to the power at Frequency f_S coupled onto the AV_{CC} supply.

Channel to Channel Isolation
Channel to channel isolation is a measure of the level of crosstalk between all input channels. It is measured by applying a full-scale sine wave signal, up to 160 kHz, to all unselected input channels and then determining the degree to which the signal attenuates in the selected channel with a 1 kHz sine wave signal applied (see Figure 23).

THEORY OF OPERATION

Note that throughout this data sheet, multifunction pins, such as $\overline{RD}$/SCLK, are referred to either by the entire pin name or by a single function of the pin, for example, $\overline{RD}$, when only that function is relevant.

CONVERTER DETAILS

The AD7605-4 is a data acquisition system that employs a high speed, low power, charge redistribution, successive approximation register (SAR) ADC and allows the simultaneous sampling of four analog input channels. The analog inputs on the AD7605-4 can accept true bipolar input signals. The RANGE pin selects either ±10 V or ±5 V as the input range. The AD7605-4 operates from a single 5 V supply.

The AD7605-4 contains input clamp protection, input signal scaling amplifiers, a second-order anti-aliasing filter, track-and-hold amplifiers, an on-chip reference, reference buffers, a high speed ADC, a digital filter, and high speed parallel and serial interfaces. Sampling on the AD7605-4 is controlled using the CONVST x signals.

ANALOG INPUT

Analog Input Ranges

The AD7605-4 can handle true bipolar, single-ended input voltages. The logic level on the RANGE pin determines the analog input range of all analog input channels. If this pin is tied to a logic high, the analog input range is ±10 V for all channels. If this pin is tied to a logic low, the analog input range is ±5 V for all channels. A logic change on this pin has an immediate effect on the analog input range; however, there is typically a settling time of approximately 80 µs, in addition to the normal acquisition time requirement. The recommended practice is to hardwire the RANGE pin according to the desired input range for the system signals.

During normal operation, keep the applied analog input voltage within the analog input range selected via the RANGE pin. A RESET pulse must be applied after power up to ensure the analog input channels are configured for the range selected.

When in one of the two power-down modes, it is recommended to tie the analog inputs to AGND. The overvoltage clamp protection is designed to protect against transient overvoltage conditions only; do not keep the clamp protection circuitry active for extended periods (see the Analog Input Clamp Protection section).

Analog Input Impedance

The analog input impedance of the AD7605-4 is 1 MΩ. This fixed input impedance does not vary with sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7605-4, allowing direct connection to the source or sensor. With the need for a driver amplifier eliminated, bipolar supplies (which are often a source of noise in a system) can be removed from the signal chain.

Analog Input Clamp Protection

Figure 28 shows the analog input structure of the AD7605-4. Each analog input contains clamp protection circuitry. Despite single 5 V supply operation, this analog input clamp protection allows an input overvoltage of up to ±16.5 V.

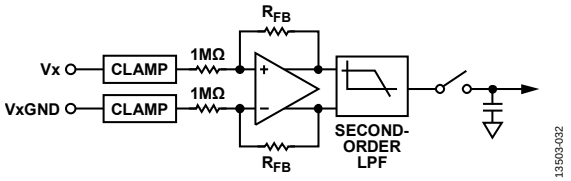


Figure 28. Analog Input Circuitry

Figure 29 shows the input clamp current vs. the source voltage characteristic of the clamp circuit. For input voltages of up to ±16.5 V, no current flows in the clamp circuit. For input voltages greater than ±16.5 V, the AD7605-4 clamp circuitry turns on.

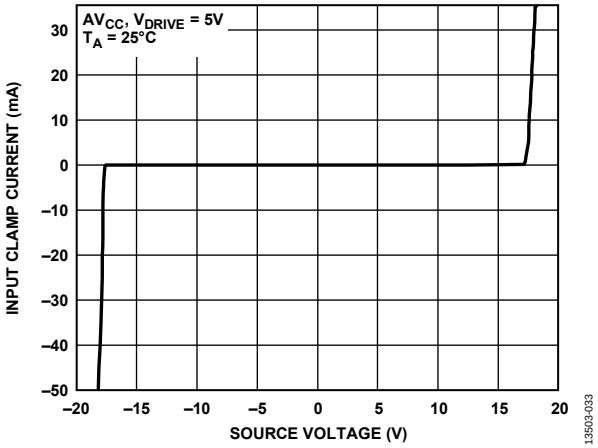


Figure 29. Input Protection Clamp Profile

Place a series resistor on the analog input channels to limit the current to ±10 mA for input voltages greater than ±16.5 V. In an application where there is a series resistance on an analog input channel, Vx, a corresponding resistance is required on the analog input ground channel, VxGND (see Figure 30). If there is no corresponding resistor on the VxGND channel, an offset error occurs on that channel. It is recommended that the input overvoltage clamp protection circuitry be used to protect the AD7605-4 against transient overvoltage events. It is not recommended to leave the AD7605-4 in a condition where the clamp protection circuitry is active in normal or power-down conditions for extended periods because doing so may degrade the bipolar zero code error performance of the AD7605-4.

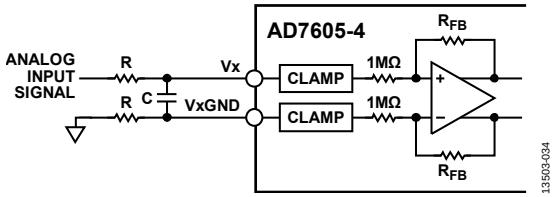
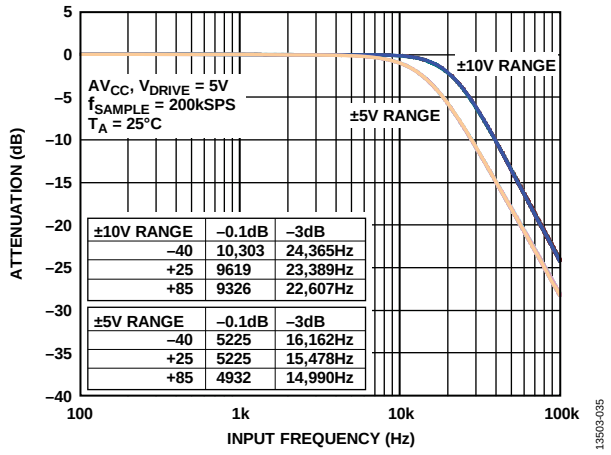


Figure 30. Input Resistance Matching on the Analog Input of the AD7605-4

Analog Input Antialiasing Filter

An analog antialiasing filter (a second-order Butterworth) is also provided on the AD7605-4. Figure 31 and Figure 32 show the frequency and phase response, respectively, of the analog antialiasing filter. In the ±5 V range, the −3 dB frequency is typically about 15 kHz. In the ±10 V range, the −3 dB frequency is typically about 23 kHz.



±10V RANGE	−0.1dB	−3dB
−40	10,303	24,365Hz
+25	9619	23,389Hz
+85	9326	22,607Hz

±5V RANGE	−0.1dB	−3dB
−40	5225	16,162Hz
+25	5225	15,478Hz
+85	4932	14,990Hz

Figure 31. Analog Antialiasing Filter Frequency Response

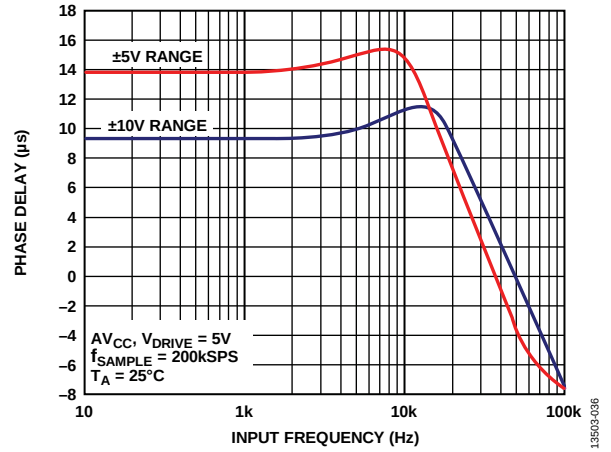


Figure 32. Analog Antialias Filter Phase Response

Track-and-Hold Amplifiers

The track-and-hold amplifiers on the AD7605-4 allow the ADC to accurately acquire an input sine wave of full-scale amplitude to 16-bit resolution. The track-and-hold amplifiers sample their respective inputs simultaneously on the rising edge of CONVST x.

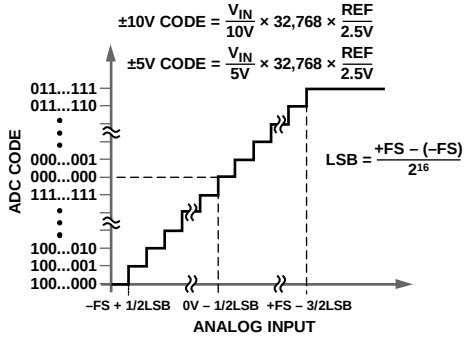
The aperture time for the track-and-hold (that is, the delay time between the external CONVST x signal and the track-and-hold actually going into hold) is well matched, by design, across all track-and-holds on one device and from device to device. This matching allows more than one AD7605-4 device to be sampled simultaneously in a system.

The end of the conversion process across all channels is indicated by the falling edge of BUSY; it is at this point that the track-and-holds return to track mode, and the acquisition time for the next set of conversions begins.

The conversion clock for the device is internally generated, and the conversion time for all channels is 2 µs on the AD7605-4. The BUSY signal returns low after all four conversions are completed, to indicate the end of the conversion process. On the falling edge of BUSY, the track-and-hold amplifiers return to track mode. New data can be read from the output register via the parallel interface, parallel byte interface, or serial interface after BUSY goes low; or, alternatively, data from the previous conversion can be read while BUSY is high. Reading data from the AD7605-4 while a conversion is in progress has little effect on performance and allows a faster throughput to be achieved. In parallel mode at V_{DRIVE} > 3.3 V, the SNR is reduced by ~1.5 dB when reading during a conversion.

ADC TRANSFER FUNCTION

The output coding of the AD7605-4 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB and 3/2 LSB. The LSB size is FSR/65,536 for the AD7605-4. The ideal transfer characteristic for the AD7605-4 is shown in Figure 33.



	+FS	MIDSCALE	−FS	LSB
±10V RANGE	+10V	0V	−10V	305µV
±5V RANGE	+5V	0V	−5V	152µV

Figure 33. Transfer Characteristics

The LSB size is dependent on the analog input range selected.

INTERNAL/EXTERNAL REFERENCE

The AD7605-4 contains an on-chip 2.5 V band gap reference. The REFIN/REFOUT pin allows access to the 2.5 V reference that generates the on-chip 4.5 V reference internally, or it allows an external reference of 2.5 V to be applied to the AD7605-4. An externally applied reference of 2.5 V is also amplified to 4.5 V, using the internal buffer. This 4.5 V buffered reference is the reference used by the SAR ADC.

The REF SELECT pin is a logic input pin that allows the user to select between the internal reference and an external reference. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. The internal reference buffer is always enabled. After a reset, the AD7605-4 operates in the reference mode selected by the REF SELECT pin. Decoupling is required on the REFIN/REFOUT pin for both the internal and external reference options. A 10 µF ceramic capacitor is required on the REFIN/REFOUT pin.

The AD7605-4 contains a reference buffer configured to amplify the REFIN/REFOUT voltage to 4.5 V, as shown in Figure 34. The REFCAPA and REFCAPB pins must be shorted together externally, and a ceramic capacitor of 10 µF applied to REFGND, to ensure that the reference buffer is in closed-loop operation. The reference voltage available at the REFIN/REFOUT pin is 2.5 V.

When the AD7605-4 is configured in external reference mode, the REFIN/REFOUT pin is a high input impedance pin. For applications using multiple devices, the following configurations are recommended, depending on the application requirements.

External Reference Mode

One ADR421 external reference can be used to drive the REFIN/REFOUT pins of all AD7605-4 devices (see Figure 35). In this configuration, decouple each REFIN/REFOUT pin of the AD7605-4 with at least a 100 nF decoupling capacitor.

Internal Reference Mode

Use one AD7605-4 device, configured to operate in the internal reference mode, to drive the remaining AD7605-4 devices, which are configured to operate in external reference mode (see Figure 36). Decouple the REFIN/REFOUT pin of the AD7605-4 that is configured in internal reference mode, using a 10 µF ceramic decoupling capacitor. For the other AD7605-4 devices, configured in external reference mode, use at least a 100 nF decoupling capacitor on their REFIN/REFOUT pins.

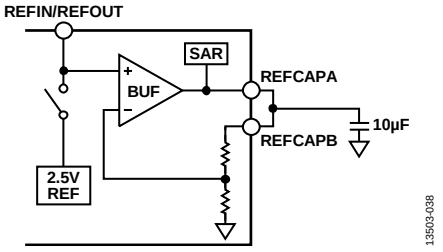


Figure 34. Reference Circuitry

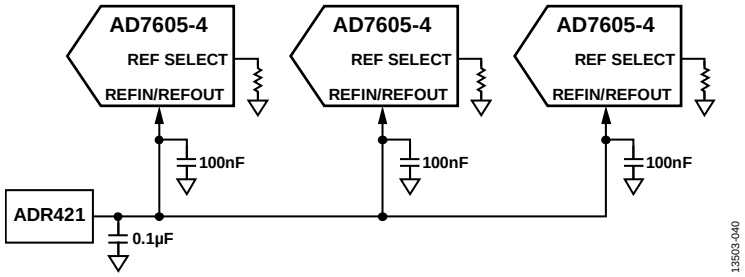


Figure 35. Single External Reference Driving Multiple AD7605-4 REFIN/RFOUT Pins

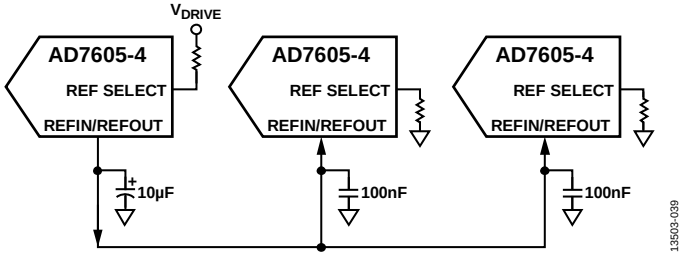


Figure 36. Internal Reference Driving Multiple AD7605-4 REFIN/REFOUT Pins

TYPICAL CONNECTION DIAGRAM

Figure 37 shows the typical connection diagram for the AD7605-4. There are four AV_{CC} supply pins on the device. Decouple each of the four pins using a 100 nF capacitor at each supply pin and a 10 µF capacitor at the supply source. The AD7605-4 can operate with the internal reference or an externally applied reference. In this configuration, the AD7605-4 is configured to operate with the internal reference. When using a single AD7605-4 device on the board, decouple the REFIN/REFOUT pin with a 10 µF capacitor. Refer to the Internal/External Reference section when using an application with multiple AD7605-4 devices. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 µF ceramic capacitor.

The V_{DRIVE} supply is connected to the same supply as the processor. The V_{DRIVE} voltage controls the voltage value of the output logic signals. For layout, decoupling, and grounding hints, see the Layout Guidelines section.

After supplies are applied to the AD7605-4, apply a reset to ensure that the device is configured for the correct mode of operation.

POWER-DOWN MODES

Two power-down modes are available on the AD7605-4: standby mode and shutdown mode. The $\overline{STBY}$ pin controls whether the AD7605-4 is in normal mode or in one of the two power-down modes.

The power-down mode is selected through the state of the RANGE pin when the $\overline{STBY}$ pin is low. Table 7 shows the configurations required to choose the desired power-down mode. When the AD7605-4 is placed in standby mode, the current consumption is 8 mA maximum and the power-up time is approximately 100 µs because the capacitor on the REFCAPA and REFCAPB pins must charge up. In standby mode, the on-chip reference and regulators remain powered up, and the amplifiers and ADC core are powered down.

When the AD7605-4 is placed in shutdown mode, the current consumption is 6 µA maximum and power-up time is approximately 13 ms (external reference mode). In shutdown mode, all circuitry is powered down. When the AD7605-4 is powered up from shutdown mode, a RESET signal must be applied to the AD7605-4 after the required power-up time has elapsed.

Table 7. Power-Down Mode Selection

Power-Down Mode	$\overline{STBY}$ Setting	RANGE Setting
Standby	0	1
Shutdown	0	0

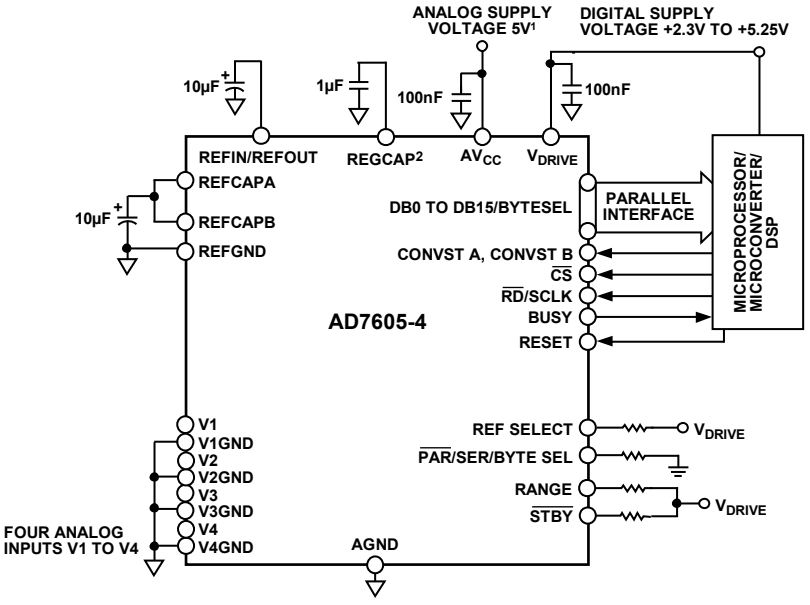


Figure 37. Typical Connection Diagram

CONVERSION CONTROL

Simultaneous Sampling on All Analog Input Channels

The AD7605-4 allows simultaneous sampling of all analog input channels. All channels are sampled simultaneously when both CONVST x pins (CONVST A, CONVST B) are tied together. A single CONVSTx signal is used to control both CONVST x inputs. The rising edge of this common CONVST x signal initiates simultaneous sampling on all analog input channels.

The AD7605-4 contains an on-chip oscillator that performs the conversions. The conversion time for all ADC channels is t_{CONV}. The BUSY signal indicates to the user when conversions are in progress, so when the rising edge of CONVST x is applied, BUSY goes logic high and transitions low at the end of the entire conversion process. The falling edge of the BUSY signal is used to place all track-and-hold amplifiers back into track mode. The falling edge of BUSY also indicates that the new data can now be read from the parallel bus (DB15 to DB0), the $D_{OUT}A$ and $D_{OUT}B$ serial data lines, or the parallel byte bus, DB7 to DB0.

Simultaneously Sampling Two Sets of Channels

The AD7605-4 also allows the analog input channels to be sampled simultaneously in two sets. This feature can be used in power line protection and measurement systems to compensate for phase differences introduced by potential transformers (PTs) and current transformers (CTs). In a 50 Hz system, simultaneous sampling allows up to 9° of phase compensation; and in a 60 Hz system, it allows up to 10° of phase compensation.

Simultaneous sampling is accomplished by pulsing the two CONVST x pins independently. CONVST A initiates simultaneous sampling of the first set of channels (V1 and V2); and CONVST B initiates simultaneous sampling on the second set of analog input channels (V3 and V4), as shown in Figure 38. On the rising edge of CONVST A, the track-and-hold amplifiers for the first set of channels are placed into hold mode. On the rising edge of CONVST B, the track-and-hold amplifiers for the second set of channels are placed into hold mode. The conversion process begins after both rising edges of CONVST x occur; therefore, BUSY goes high on the rising edge of the later CONVST x signal. In Table 3, t_5 indicates the maximum allowable time between the CONVST x sampling points.

There is no change to the data read process when using two separate CONVST x signals.

Connect all unused analog input channels to AGND. The results for any unused channels are still included in the data read because all channels are always converted.

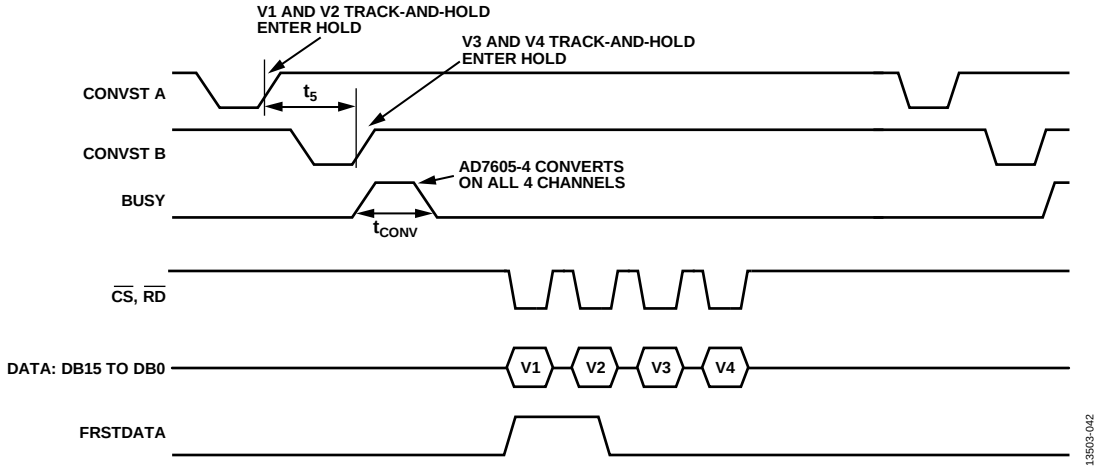


Figure 38. Simultaneous Sampling on Channel Sets While Using Independent CONVST A and CONVST B Signals—Parallel Mode

APPLICATIONS INFORMATION

The AD7605-4 provides three interface options: a parallel interface, a high speed serial interface, and a parallel byte interface. The required interface mode is selected via the $\overline{PAR}$/SER/BYTE SEL and DB15/BYTE SEL pins.

Table 8. Interface Mode Selection

$\overline{PAR}$/SER/BYTE SEL Setting	DB15/BYTE SEL Setting	Interface Mode
0	0	Parallel
1	0	Serial
1	1	Parallel byte

Operation of the interface modes is discussed in the following sections.

PARALLEL INTERFACE ($\overline{PAR}$/SER/BYTE SEL = 0)

Data can be read from the AD7605-4 via the parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals. To read the data over the parallel bus, tie the $\overline{PAR}$/SER/BYTE SEL pin low. The $\overline{CS}$ and $\overline{RD}$ input signals are internally gated to enable the conversion result onto the data bus. The data lines, DB15 to DB0, leave their high impedance state when both $\overline{CS}$ and $\overline{RD}$ are logic low.

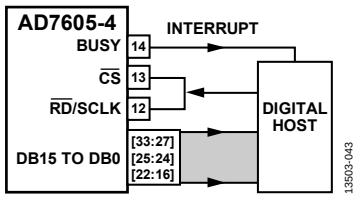


Figure 39. AD7605-4 Interface Diagram—One AD7605-4 Device Using the Parallel Bus, with $\overline{CS}$ and $\overline{RD}$/SCLK Shorted Together

The rising edge of the $\overline{CS}$ input signal three-states the bus, and the falling edge of the $\overline{CS}$ input signal takes the bus out of the high impedance state. $\overline{CS}$ is the control signal that enables the data lines; it is the function that allows multiple AD7605-4 devices to share the same parallel data bus.

The $\overline{CS}$ signal can be permanently tied low, and the $\overline{RD}$ signal can be used to access the conversion results as shown in Figure 4. A read operation of new data can take place after the BUSY signal goes low (see Figure 2); or, alternatively, a read operation of data from the previous conversion process can take place while BUSY is high (see Figure 3).

The $\overline{RD}$/SCLK pin is used to read data from the output conversion results register. Applying a sequence of $\overline{RD}$ pulses to the $\overline{RD}$/SCLK pin of the AD7605-4 clocks the conversion results out from each channel onto the parallel bus, DB15 to DB0, in ascending order. The first $\overline{RD}$ signal falling edge after BUSY goes low clocks out the conversion result from Channel V1. The next $\overline{RD}$ signal falling edge updates the bus with the V2 conversion result, and so on.

When the $\overline{RD}$ signal is logic low, it enables the data conversion result from each channel to be transferred to the digital host (DSP, FPGA).

When there is only one AD7605-4 device in a system/board and it does not share the parallel bus, data can be read using just one control signal from the digital host. The $\overline{CS}$ and $\overline{RD}$ signals can be tied together, as shown in Figure 5. In this case, the data bus comes out of three-state on the falling edge of the $\overline{CS}$/$\overline{RD}$ signal. The combined $\overline{CS}$ and $\overline{RD}$ signal allows the data to be clocked out of the AD7605-4 and to be read by the digital host. In this case, $\overline{CS}$ frames the data transfer of each data channel.

PARALLEL BYTE ($\overline{PAR}$/SER/BYTE SEL = 1, DB15/BYTE SEL = 1)

Parallel byte interface mode operates much like the parallel interface mode, except that each channel conversion result is read out in two 8-bit transfers. Therefore, eight $\overline{RD}$ pulses are required to read all four conversion results from the AD7605-4. To configure the AD7605-4 to operate in parallel byte mode, tie the $\overline{PAR}$/SER/BYTE SEL and DB15/BYTE SEL pins to logic high (see Table 8). In parallel byte mode, DB7 to DB0 are used to transfer the data to the digital host. DB0 is the LSB of the data transfer, and DB7 is the MSB of the data transfer. In parallel byte mode, the DB14/HBEN pin functions as HBEN. When DB14/HBEN is tied to logic high, the most significant byte (MSB) of the conversion result is output first, followed by the LSB of the conversion result. When DB14/HBEN is tied to logic low, the LSB of the conversion result is output first, followed by the MSB of the conversion result. The FRSTDATA pin remains high until the entire 16 bits of the conversion result from V1 are read from the AD7605-4.

SERIAL INTERFACE ($\overline{PAR}$/SER/BYTE SEL = 1)

To read data back from the AD7605-4 over the serial interface, the $\overline{PAR}$/SER/BYTE SEL pin must be tied high. The $\overline{CS}$ and SCLK signals are used to transfer data from the AD7605-4. The AD7605-4 has two serial data output pins, $D_{OUT}A$ and $D_{OUT}B$. Data can be read back from the AD7605-4 using one or both of these $D_{OUT}x$ lines. For the AD7605-4, conversion results from Channel V1 and Channel V2 first appear on $D_{OUT}A$, and conversion results from Channels V3 and Channel V4 first appear on $D_{OUT}B$.

The $\overline{CS}$ falling edge takes the data output lines, $D_{OUT}A$ and $D_{OUT}B$, out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs, $D_{OUT}A$ and $D_{OUT}B$. The $\overline{CS}$ input can be held low for the entire serial read operation, or it can be pulsed to frame each channel read of 16 SCLK cycles. Figure 40 shows a read of four simultaneous conversion results using two $D_{OUT}x$ lines on the AD7605-4. In this case, a 32 SCLK transfer is used to access data from the AD7605-4, and $\overline{CS}$ is held low to frame all the 32 SCLK cycles.

Data can also be clocked out using just one $D_{OUT}x$ line, in which case it is recommended that $D_{OUT}A$ be used to access all conversion data because the channel data is output in ascending order. For the AD7605-4 to access all four conversion results on the $D_{OUT}A$ line, a total of 64 SCLK cycles is required. These 64 SCLK cycles can be framed by one $\overline{CS}$ signal, or each group of 16 SCLK cycles can be individually framed by the $\overline{CS}$ signal. The disadvantage of using just the one $D_{OUT}A$ line is that the throughput rate is reduced if reading occurs after conversion. Leave the unused $D_{OUT}B$ line unconnected in serial mode.

If $D_{OUT}B$ is used as the single data output line, the channel results are output in the following order: V3, V4, V1, and V2; however, the FRSTDATA indicator returns low after V3 is read on $D_{OUT}B$.

Figure 6 shows the timing diagram for reading one channel of data, framed by the $\overline{CS}$ signal, from the AD7605-4 in serial mode. The SCLK input signal provides the clock source for the serial read operation. The AD7605-4 can be accessed while the $\overline{CS}$ signal is held low.

The falling edge of $\overline{CS}$ takes the bus out of three-state and clocks out the MSB of the 16-bit conversion result. This MSB is valid on the first falling edge of the SCLK after the $\overline{CS}$ falling edge. The subsequent 15 data bits are clocked out of the AD7605-4 on the SCLK rising edge. Data is valid on the SCLK falling edge. To access each conversion result, 16 clock cycles must be provided to the AD7605-4.

The FRSTDATA output signal indicates when the first channel, V1, is being read back. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. In serial mode, the falling edge of $\overline{CS}$ takes FRSTDATA out of three-state and sets the FRSTDATA pin high, indicating that the result from V1 is available on the $D_{OUT}A$ output data line. The FRSTDATA output returns to a logic low following the 16th SCLK falling edge. If all channels are read on $D_{OUT}B$, the FRSTDATA output does not go high when V1 is being output on this serial data output pin. The FRSTDATA output goes high only when V1 is available on $D_{OUT}A$ (when V3 is available on $D_{OUT}B$ for the AD7605-4).

READING DURING CONVERSION

Data can be read from the AD7605-4 while BUSY is high and the conversions are in progress. Reading during conversions has little effect on the performance of the converter. A parallel read, parallel byte read, or serial read can be performed during conversions. Figure 3 shows the timing diagram for reading while BUSY is high in parallel or serial mode. Reading during conversions allows the full throughput rate to be achieved when using the serial interface with V_{DRIVE} greater than 4.75 V.

Data can be read from the AD7605-4 at any time other than on the falling edge of BUSY because the output data registers are updated with the new conversion data on the BUSY falling edge. Observe Time t_6, as outlined in Table 3, in this condition.

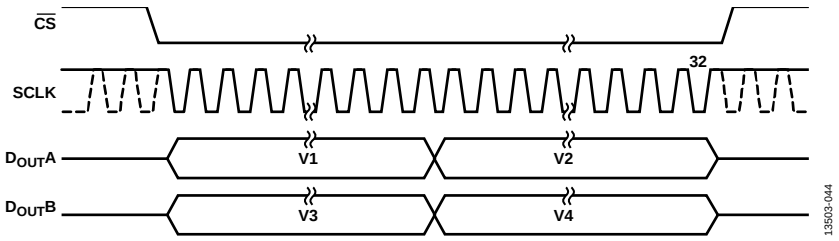


Figure 40. Serial Interface with Two $D_{OUT}x$ Lines

LAYOUT GUIDELINES

Design the PCB that houses the AD7605-4 so that the analog and digital sections are separated and confined to different areas of the board.

Use at least one ground plane. It can be common or split between the digital and analog sections. In the case of the split plane, join the digital and analog ground planes in only one place, preferably as close as possible to the AD7605-4.

If the AD7605-4 is in a system where multiple devices require analog to digital ground connections, make the connection at only one point: establish a star ground point as close as possible to the AD7605-4. Good connections must be made to the ground plane. Avoid sharing one connection for multiple ground pins. Use individual vias or multiple vias to the ground plane for each ground pin.

Avoid running digital lines under the devices because doing so couples noise onto the die. Allow the analog ground plane to run under the AD7605-4 to avoid noise coupling. Shield fast switching signals like CONVST A, CONVST B, or clocks with digital ground to avoid radiating noise to other sections of the board, and never run them near analog signal paths. Avoid crossover of digital and analog signals. Route traces on layers in close proximity on the board at right angles to each other to reduce the effect of feedthrough through the board.

For the power supply lines to the AV_{CC} and V_{DRIVE} pins on the AD7605-4, use as large a trace as possible to provide low impedance paths and to reduce the effect of glitches on the power supply lines. Where possible, use supply planes and make good connections between the AD7605-4 supply pins and the power tracks on the board. Use a single via or multiple vias for each supply pin.

Good decoupling is also important to lower the supply impedance presented to the AD7605-4 and to reduce the magnitude of the supply spikes. Place the decoupling capacitors close to (ideally, right up against) these pins and their corresponding ground pins. Place the decoupling capacitors for the REFIN/REFOUT pin and the REFCAPA and REFCAPB pins as close as possible to their respective AD7605-4 pins; and, where possible, place them on the same side of the board as the AD7605-4 device.

Figure 41 shows the recommended decoupling on the top layer of the AD7605-4 board. Figure 42 shows bottom layer decoupling, which is used for the four AV_{CC} pins and the V_{DRIVE} pin decoupling. Where the ceramic 100 nF capacitors for the AV_{CC} pins are placed close to their respective device pins, a single 100 nF capacitor can be shared between Pin 37 and Pin 38.

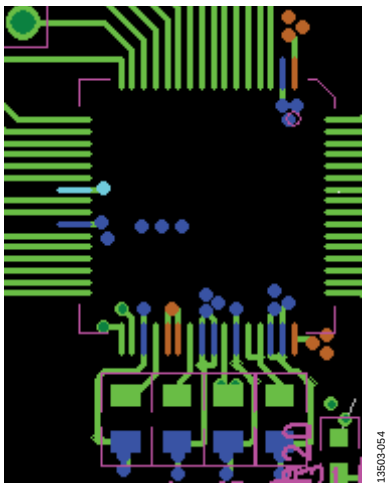


Figure 41. Top Layer Decoupling REFIN/REFOUT, REFCAPA, REFCAPB, and REGCAP Pins

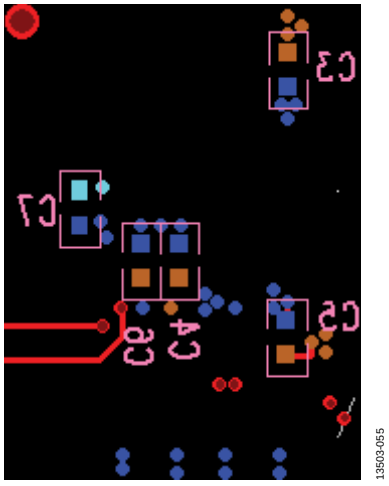


Figure 42. Bottom Layer Decoupling

To ensure good device to device performance matching in a system that contains multiple AD7605-4 devices, a symmetrical layout between the AD7605-4 devices is important.

Figure 43 shows a layout with two AD7605-4 devices. The AV_{CC} supply plane runs to the right of both devices, and the V_{DRIVE} supply track runs to the left of the two devices. The reference chip is positioned between the two devices, and the reference voltage track runs north to Pin 42 of U1 and south to Pin 42 of U2. A solid ground plane is used.

These symmetrical layout principles can also be applied to a system that contains more than two AD7605-4 devices. The AD7605-4 devices can be placed in a north to south direction, with the reference voltage located midway between the devices and the reference track running in the north to south direction, similar to Figure 43.

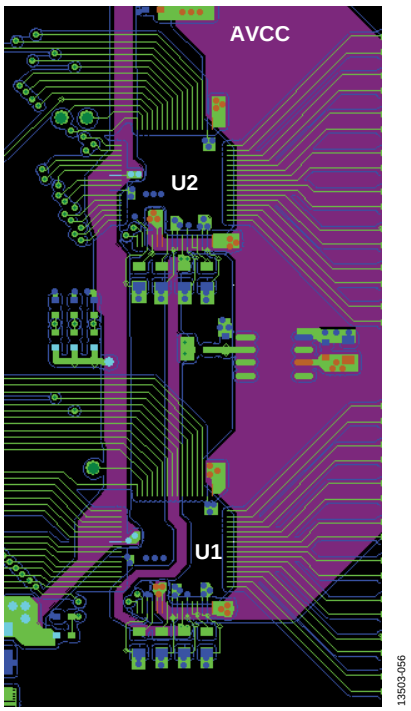
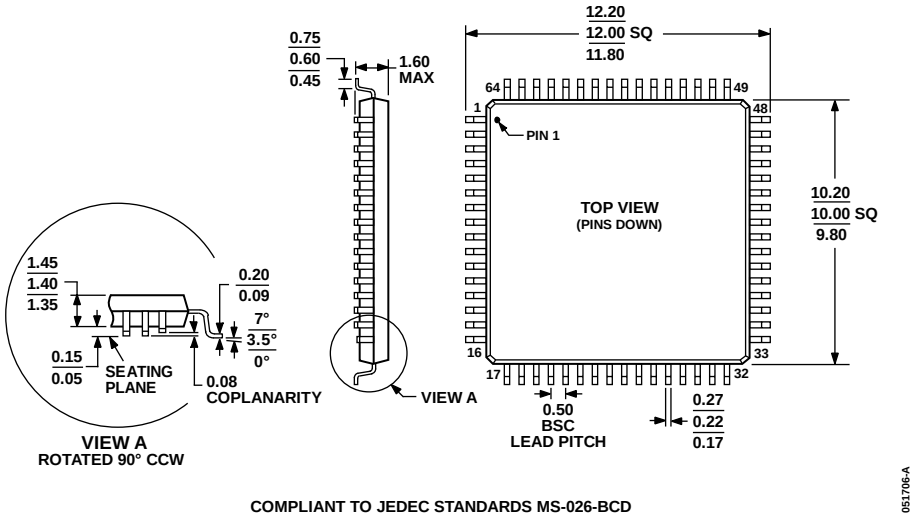


Figure 43. Layout for Multiple AD7605-4 Devices—Top Layer and Supply Plane Layer

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BCD

Figure 44. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD7605-4BSTZ	−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7605-4BSTZ-RL	−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
EVAL-AD7605-4SDZ		Evaluation Board	
EVAL-SDP-CB1Z		Controller Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD7605-4SDZ evaluation board requires the EVAL-SDP-CB1Z controller board to allow connection to a PC and full evaluation using the included evaluation software.