ANALOG DEVICES

16-Bit 100 kSPS Oversampling ADC

AD776

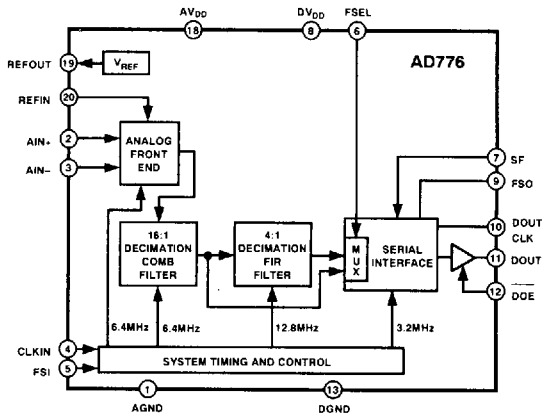
FEATURES

Monolithic 16-Bit Sigma-Delta ADC
Third-Order Noise Shaping
96 dB Dynamic Range
90 dB SNR
16-Bit 100 kHz Output from FIR Filter
12-Bit 400 kHz Output from Comb Filter
No Missing Codes
<0.001 dB In-Band Ripple

APPLICATIONS

Digital Audio Disk/Tape
Voice Bandwidth Communications
ADC Support for ADSP-21XX
High Accuracy Measurement Systems

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD776 is a 16-bit sigma-delta oversampled ADC, incorporating a 1-bit third-order modulator and digital decimation filter. An on-chip voltage reference circuit is also included.

The AD776 does not generally require the use of sample-hold circuits or complex antialiasing filters as a result of its sigma-delta architecture. The output is available both before and after the final Finite Impulse Response (FIR) decimation filter. This provides the flexibility of optimizing conversion speed or dynamic range: 12-bit/400 kHz (from the comb filter) or 16-bit/100 kHz (from the FIR filter). The serial port provides easy interface with a variety of standard processors including the ADSP-21XX.

The AD776 is specified for ac (or "dynamic") parameters such as SNR, THD and IMD which are important in signal processing and audio applications. Third order noise shaping is employed using 64 times oversampling to provide 90 dB SNR and −100 dB peak spurious component for signal bandwidths up to 45 kHz.

The AD776 operates from a single +5 V supply and typically consumes 350 mW during conversion. The device is packaged in 20-pin ceramic DIP (cerdip) and is offered in an industrial temperature grade (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Analog Front End. The analog input is differential providing increased signal swing, increased power supply rejection ratio, and reduced sensitivity to clock jitter. Since the input signal is oversampled by a factor of 64, a complex antialiasing filter is not needed.
2. Flexible Digital Interface. The AD776 has three output pins for the serial interface: 1) serial data out (DOUT), 2) frame sync out (FSO), and 3) serial clock out (DOUT CLOCK). The serial port can interface with general purpose DSPs such as the ADSP-21XX, TMS320XX, and DSP56001/2 without additional "glue" logic.
3. Inherently Self-Sampling. The AD776 needs no external sample-and-hold amplifier to capture and freeze the analog input while the conversion takes place.
4. Speed/Performance Options. In addition to the standard 16-bit resolution at 100 kHz, the output of the comb filter can be accessed to provide 12-bit resolution at 400 kHz.

AD776—SPECIFICATIONS (T_{MIN} to T_{MAX}; AV_{DD}, DV_{DD} = +5 V, FIR filter output mode unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	16			Bits
TEMPERATURE RANGE	−40		+85	°C
TOTAL HARMONIC DISTORTION (THD)[1, 2, 3]	−80	−83		dB
	0.01	0.003		%
SIGNAL-TO-NOISE RATIO (SNR)[1, 2], f_S = 48 ksps	88	90		dB
Signal to Noise Ratio (SNR)[1, 2], f_S = 100 ksps		86		dB
Comb Filter Mode, CLKIN = 12.8 MHz		72		dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−100		dB
INTERMODULATION DISTORTION (IMD)[4]				
2nd Order Products		−102		dB
3rd Order Products		−98		dB
VOLTAGE REFERENCE OUTPUT (V_{REF})	(AV_{DD} × 0.4) − 4%	AV_{DD} × 0.4 V	(AV_{DD} × 0.4) + 4%	V
MAXIMUM ANALOG INPUT RANGE[5]		2 × V_{REF} − 0.5		V p–p
MAXIMUM INPUT SIGNAL[6]		±0.5 V_{REF}		V p–p
DC ACCURACY[1]				
Differential Nonlinearity		±0.5		LSB
INL		2		LSB
Gain Error		1.0		%
Midscale Error		0.5		%
DIGITAL FILTER CHARACTERISTICS				
Passband Ripple		0.001		dB
Stopband Attenuation		−96		dB
POWER SUPPLY REQUIREMENTS[7]				
Analog Supply Voltage (AV_{DD})	4.5	5.0	5.5	V
Digital Supply Voltage (DV_{DD})	4.5		AV_{DD}	V
Analog Supply Current		20		mA
Digital Supply Current		20		mA
Power Consumption[8]		300	400	mW
Power Supply Rejection[9]		70		dB

DIGITAL SPECIFICATIONS

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
I_{IH}	High Level Input Current	V_{IH} = V_{DD}		1		μA
I_{IL}	Low Level Input Current	V_{IL} = 0 V		1		μA
C_{IN}	Input Capacitance			10		pF
I_Z	Hi-Z Input Current for SDO				10	μA
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.4 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.0 mA			0.5	V

NOTES
[1]At +25°C.
[2]Analog Input = 1.2 V rms @ 10 kHz, $V_{COMMON\ MODE}$ = 2.5 V, CLKIN = 6.4 MHz.
[3]THD performance can be improved, depending upon the application, by making slight adjustments to the dc common mode voltage at the analog inputs.
[4]IMD measured at f_s = 48 kHz and using 61.6 Hz and 986.4 Hz as the input tones (sum of the two peaks added to be −3 dB FS).
[5]Applied differentially between AIN+ and AIN−.
[6]The input signal may be centered at any choice of dc offset voltage as long as peak values are bounded by the Maximum Analog Input Range value. Performance may be improved by reducing the maximum input signal by 3 dB. For nominal operation, 2.5 V dc offset is recommended.
[7]The AD776 may be operated from a single +5 V supply.
[8]AV_{DD}, DV_{DD} = 5.5 V; f = 12.8 MHz; T_A = +85°C.
[9]With external voltage reference.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (AV_{DD}, DV_{DD} = +5 V ± 10%, T_{MIN} to T_{MAX}) — see Figures 14 through 18.

Symbol	Parameter	Min	Max	Units
f	Clock in Frequency	1	12.8	MHz
t_{CLK}	Clock in Period (= 1/f)	78	1000	ns
t_D	Duty Cycle	0.475 t_{CLK}	0.525 t_{CLK}	ns
t_{CL}	Clock LOW	37	41	ns[1]
		475	525	ns[2]
t_{CH}	Clock HIGH	37	41	ns[1]
		475	525	ns[2]
t_R	Rise Time	5		ns
t_F	Fall Time	5		ns
t_{FSS}	Frame Sync Input Setup Time	20	78	ns
t_{FSH}	Frame Sync Input Hold Time	20	−[3]	ns
t_{FSIL}	Frame Sync Input LOW	2		t_{CLK}
t_{DOD}	Data Output Clock Delay	25	75	ns
t_{DOP}	Data Output Clock Period	156		ns[1, 4]
			312	ns[1, 5]
t_{FSOSC}	FSO Setup Time Before CLKIN	130		ns[5]
t_{FSOHC}	FSO Hold Time After CLKIN	130		ns[5]
t_{FSOSD}	FSO Setup Time Before DOUT CLK	110		ns[5]
t_{FSOHD}	FSO HIGH to DOUT CLK Rising Edge	110		ns[5]
t_{IO}	FSI to FSO Delay	1		t_{CLK}[4]
		5		t_{CLK}[5]
t_{DSU}	Data Output Setup Time	40		ns[4]
		130		ns[5]
t_{DH}	Data Output Hold Time	40		ns[4]
		130		ns[5]
t_{DD}	Data Delay Time	0	20	ns
t_{DF}	Data Float Time	0	20	ns

NOTES
[1]CLKIN = 12.8 MHz.
[2]CLKIN = 1 MHz.
[3]FSI must be deasserted for at least two CLKIN periods prior to being asserted.
[4]Comb Filter mode.
[5]FIR Filter mode.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

AV_{DD} to AGND . . . . . −0.3 V to +7.0 V
DV_{DD} to DGND . . . . . −0.3 V to +7.0 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . −0.3 V to DV_{DD}
Analog Inputs to AGND . . . . . −0.3 V to AV_{DD}
REFIN to AGND . . . . . −0.3 V to +2.5 V
Soldering (10 sec) . . . . . +300°C
Storage Temperature . . . . . −55°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

The AD776 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD776 has been classified as a Category 1 Device.

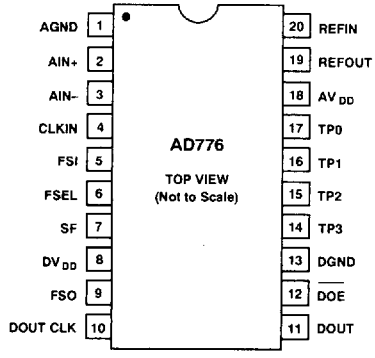
Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD precaution, refer to Analog Devices' *ESD Prevention Manual*.

AD776 PIN DESCRIPTION

Symbol	Pin Number	Type	Name and Function
AGND	1		Analog Ground. Return current for analog front end. No internal connection to DGND.
AIN+	2	I	Analog Signal Input. Noninverting terminal.
AIN−	3	I	Analog Signal Input. Inverting terminal.
CLKIN	4	I	Clock In. This TTL compatible input accepts clock frequencies in the range of 1.0 MHz−12.8 MHz, with the output sample rate of the AD776 equal to CLKIN divided by 128 in FIR filter mode and 32 in comb filter mode.
FSI	5	I	Frame Sync Input. FSI is an optional control pin used to synchronize internal circuits and to start or reset the serial output data. If FSI is grounded, frame syncs will be automatically generated internally. When FSI is brought HIGH, serial data is presented at the output (DOUT−Pin 11). The purpose of FSI is to control externally the phasing of the A/D conversion process. FSI should be a periodic signal occurring every 16 DOUT CLK clock cycles in the 12-bit/400 kHz mode and every 32 DOUT CLK clock cycles in the 16-bit/ 100 kHz mode. When utilized, FSI must be synchronized to CLKIN as defined in the timing specification (see Figure 17). FSI allows multiple AD776s to be synchronized using a common frame sync source, requiring a common CLKIN signal.
FSEL	6	I	Filter Select. FSEL = "0" selects FIR output. FSEL = "1" selects comb filter output.
SF	7	I	Serial Format. Selects output format of DOUT and FSO when FSEL = "0." See Figures 14b and 15b.
DV_{DD}	8		+5 V ±10%. Digital Power Supply.
FSO	9	O	Frame Sync Output. Indicates beginning of serial data transmission on DOUT. See Timing Diagrams.
DOUT CLK	10	O	Serial Data Clock. See Figures 14a and 14b. In the FIR filter output mode (FSEL = 0), DOUT CLK is CLKIN divided by four; in the comb filter output mode (FSEL = 1), DOUT CLK is CLKIN divided by two.
DOUT	11	O	Data Output. Serial data is transmitted MSB first, twos complement format, once per FSO cycle with the data synchronous with DOUT CLK.
$\overline{DOE}$	12	I	Data Output Enable. Serial data (Pin 11) is an active output when $\overline{DOE}$ = "0." Serial data is three stated when $\overline{DOE}$ = "1."
DGND	13		Digital Ground. Return current for digital circuitry and pad drivers.
TP3, TP2, TP1, TP0	14, 15, 16, 17		Test Points. These pins must be connected to DGND.
AV_{DD}	18		+5 V ±10%. Analog Power Supply.
REFOUT	19	O	Internal Reference Output. Nominally +2 V with AV_{DD} = +5.0 V.
REFIN	20	I	Reference Input. +2 V maximum.

I = Input
O = Output

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD776AQ	−40°C to +85°C	20-Pin Cerdip	Q-20

*For outline information see Package Information section.

TOTAL HARMONIC DISTORTION
Total Harmonic Distortion (THD) is the ratio of the rms sum of the harmonic components to the rms value of a full-scale input signal and is expressed in percent (%) or decibels (dB).

SIGNAL-TO-NOISE RATIO (SNR)
Signal-to-Noise Ratio (SNR) is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the passband.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa± nfb, where m, n = 0, 1, 2, 3. . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa+fb) and (fa−fb), and the third order terms are (2fa+fb), (2fa−fb), (fa+2fb) and (fa−2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the IMD products are normalized to a 0 dB input signal.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are one LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for an ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the most negative code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the most positive code transition. INL is the worst-case deviation of a code center average from the straight line.

GAIN ERROR
The last transition should ideally occur at an analog value 1.5 LSB below the nominal full scale. The gain error is the deviation of the actual difference between the first and last code transition from the ideal difference between the first and last code transition.

MIDSCALE ERROR
Midscale error is the difference between the ideal midscale analog input voltage and the actual voltage producing the midscale output code.

PASSBAND
The passband is the region of the frequency spectrum unaffected by the attenuation of the decimation filter. In the case of the AD776, the passband is a function of the CLKIN frequency (see Table I).

PASSBAND RIPPLE
Passband ripple is defined as the variation in the amplitude response of the converter for input signal frequencies within the passband.

STOPBAND
The stopband is the region of the frequency spectrum in which the amplitude response is fully attenuated by the digital filter. In the case of the AD776, the stopband is a function of the CLKIN frequency (see Table I).

STOPBAND ATTENUATION
Stopband attenuation is defined to be the amount by which spectral components in the stopband are attenuated by the digital filter relative to the full-scale input range of the converter.

POWER SUPPLY REJECTION
DC variations in the power supply voltage will affect the midscale transition point, resulting in offset error. Power supply rejection is the maximum change in the midscale transition point due to a change in power-supply voltage from the nominal value. Additionally, there is another power supply variation to consider. AC ripple on the power supplies can couple noise into the ADC, resulting in degradation of dynamic performance.

GENERAL OVERVIEW
The AD776 is a single supply (+5 V) ADC providing simple analog and digital interface requirements. A minimal number of external connections are required to achieve the specified performance:

1. POWER
2. GROUNDS
3. CLOCKING
4. INPUT BUFFER CIRCUIT

These points will be further explored in the Application Information section.

THEORY OF OPERATION
The AD776 differs from traditional multi-bit ADCs through its use of sigma-delta conversion architecture. A 1-bit analog-to-digital conversion is performed at a very high rate, which redistributes quantization noise to beyond the frequency band of interest (see Figure 1). The frequency band of interest is denoted by f_C, and f_S is the sample frequency; $f_S/2$ is the expanded noise spectrum resulting from oversampling. The total noise energy remains constant, but by spreading it over a wider spectrum, the amount in the frequency band of interest is reduced. Noise shaping, performed by the modulator, attenuates noise in the signal passband and pushes out the noise energy into the higher frequency range (Figure 2). The oversampled signal is presented to the digital filter circuitry for:

- sophisticated averaging (filtering).
- removing high frequency noise (quantization noise removal).
- reducing sampling rate (decimation).

The resulting output data stream is presented in a format equivalent to a traditional ADC at a much reduced output sample rate.

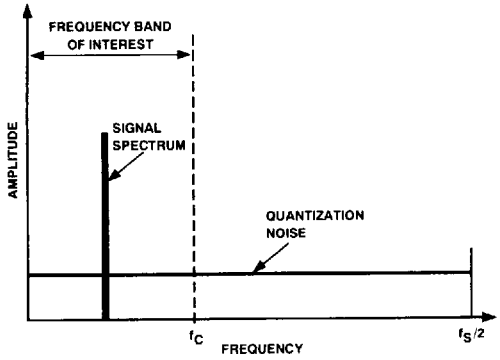


Figure 1. Noise Spectrum from Oversampling

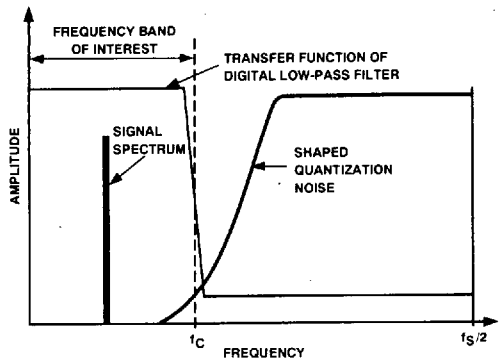


Figure 2. Noise Shaping

Figure 3 provides a block diagram of the various sections of the AD776. The Analog Front End is comprised of three differential switched-capacitor linear integrators which perform the noise-shaping function. Digital filter complexity of the AD776 is reduced by performing the filtering and decimation in two stages. The first section contains a 16:1 decimating comb filter stage with the output presented to a 4:1 decimating low-pass/compensation FIR filter, resulting in a final decimation ratio of 64:1. The decimation function is described in detail in the DECIMATION paragraph. The output data is presented in twos complement, MSB first serial data format, providing serial communication to a host processor.

This interface uses three dedicated pins: serial data output (DOUT), frame sync output (FSO), and serial clock output (DOUT CLK). The serial interface format of operation is pin selectable. The timing diagrams for the serial interface are described in the **DIGITAL TIMING** section.

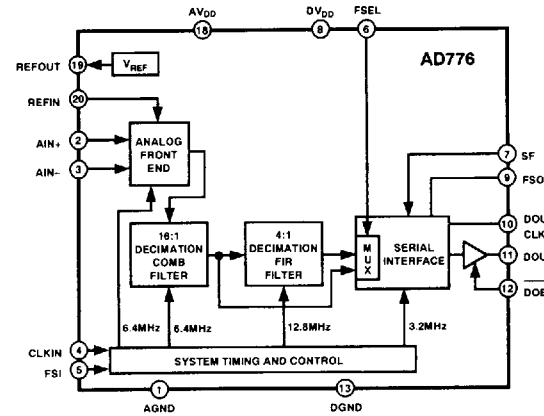


Figure 3. Block Diagram

ANALOG FRONT-END

The integrators of the third-order modulator front-end form a differential switched-capacitor network which results in increased signal swing, increased power supply rejection, and reduced sensitivity to clock jitter. Due to the nature of switched-capacitor circuits, the input impedance of AIN+, AIN−, and REFIN will vary with clock frequency. More information about these inputs is given in Table II and Table III.

The AD776 modulator is a third-order noise shaper which reduces quantization noise in the passband to the 16-bit level. The input signal is sampled at the rate of CLKIN/4. Since the input signal is oversampled by a factor of 64, a complex anti-aliasing filter is not needed; a single-pole RC filter will generally be sufficient. High quality polystyrene or NPO ceramic capacitors should be used for this filter.

DIGITAL FILTER OVERVIEW

The digital filters of the AD776 have two functions: high performance low-pass filtering and digital decimation. The shaped quantization noise from the output of the modulator is low-pass filtered to reduce the out-of-band noise components to a level which will not alias into the passband during the decimation process. Decimation then reduces the data rate to a manageable level.

DECIMATION

The comb filter performs the first-stage filtering of the analog front-end's quantized and noise-shaped output and decimates the input sample rate by a factor of 16:1. The z-domain transfer function for the comb filter is expressed by

$$H(z) = \frac{(1 - z^{-16})^4}{(1 - z^{-1})^4}$$

The frequency domain equivalent transfer function is

$$H(f) = \left[\frac{1}{16}\,\frac{sin\,(16\,\pi\,fT)}{sin\,(\pi\,fT)}\right]^4$$

where $T = 1/f_S$

f_S = the input sample rate for the Analog Front End (maximum 6.4 MHz).

The attenuation characteristics of the comb filter are shown in Figure 4. As illustrated, the frequency response in the passband region exhibits a nonflat behavior. In the 400 kHz mode, the output of the comb filter provides conversion data. The dynamic range is equivalent to approximately 72 dB, or 12 bits, in this mode. In the 16-bit/100 kHz mode, the comb filter serves as the input to the FIR filter. The FIR filter compensates for the passband roll-off of the comb filter and provides the final sharp cutoff required for stopband attenuation, removing the out-of-band noise components while partially serving as the system antialiasing filter.

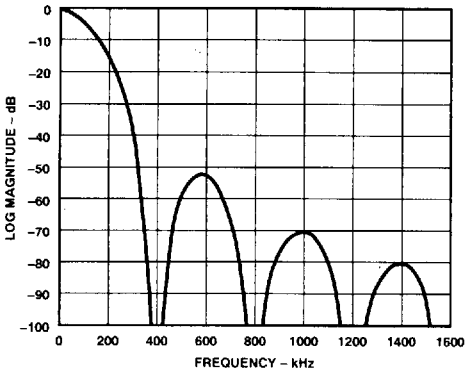


Figure 4. Comb Filter Response

Figure 5 illustrates the low-pass response of the FIR filter and Figure 6 shows the compensation function of the filter. The 255-tap FIR filter is low-pass with 9% transition-band, and with a CLKIN frequency of 12.8 MHz has a 45.5 kHz passband cutoff frequency, 50 kHz stopband frequency, 0.001 dB passband ripple, and a stopband ripple of −96 dB.

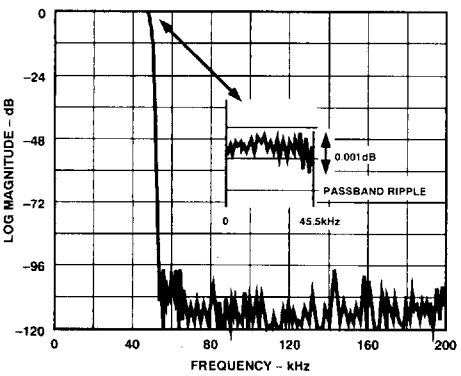


Figure 5. FIR Filter, Low-Pass Response

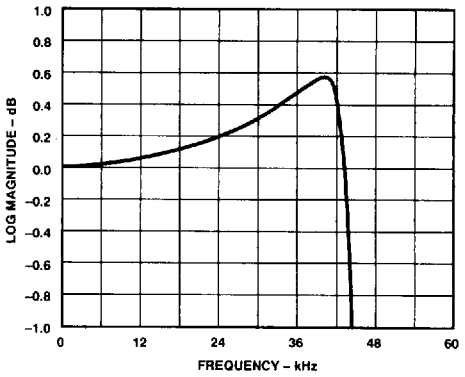


Figure 6. FIR Filter, Compensation Function

The passband and stopband frequencies of both the comb and FIR filters scale linearly with the CLKIN frequency, as shown in Table I.

Table I. FIR and Comb Filter Characteristics

CLKIN (MHz)	Passband (kHz)	Stopband (kHz)
12.8	45.5	50
12.288	43.7	48
11.2896	40.1	44.1
10.0	35.5	39.1
6.4	24.6	27.1

ANALOG INPUT

The input to the AD776, as previously described in the discussion of the analog front end, uses a switched-capacitor structure. As a result, the input impedance of AIN+ and AIN− will vary with clock frequency. Table II gives the typical analog input impedance for some common CLKIN frequencies. The input impedance is equal to $\approx 10^{12}/3f_{CLKIN}$, where f_{CLKIN} is the input clock rate.

Table II. Analog Input Impedance

Input Clock Rate (MHz)	Output Sample Rate (kHz) (FIR Filter Mode)	Analog Input Impedance (kΩ)
12.8	100	26
6.4	50	52
6.144	48	54.3
5.6448	44.1	59

The AD776 is designed to accept input signals of $(2 \times V_{REF})$ −0.5 V which can be centered at various dc offsets (common-mode inputs) as long as the signal peaks are bounded by +4.0 V and 0 V. Signal peaks outside this range will result in signal clipping and increased distortion products.

Capacitive coupling between the CLKIN and AIN pins can cause degradation to dynamic performance. Special care should be taken with respect to the layout of the clock and analog inputs.

In consideration of the dynamic characteristics of the analog input, an external op amp is generally required to provide a low impedance drive. Care should be taken with op amp selection; even with modest loading conditions, most available op amps do not meet the low distortion requirements necessary to match the performance capabilities of the AD776. The AD712 op amp is a good choice for low noise and low distortion.

SINGLE-ENDED INPUT CONFIGURATIONS

The differential input of the AD776 provides a choice of several different input connections. Figure 7 shows a simple configuration for a single-ended input. AIN− is nominally biased at +2.5 V by resistively dividing the −5 V power supply (AV_{DD}). Since the analog input impedance is a function of the input clock rate, determination of bias resistor values to achieve a particular bias voltage will vary with clock rate and AV_{DD}.

The circuit shown in Figure 7 is a low cost, minimal component solution, but may suffer from poor power supply rejection as noise present on the power supply could be coupled directly into the AIN− pin. An improved input circuit is shown in Figure 8, where the offset voltage is derived from the AD680 voltage reference. The AD680 has 40 μV/V line regulation which results in only a 20 μV error due to 10% supply fluctuation. This improves power supply rejection of AIN− input to approximately 88 dB.

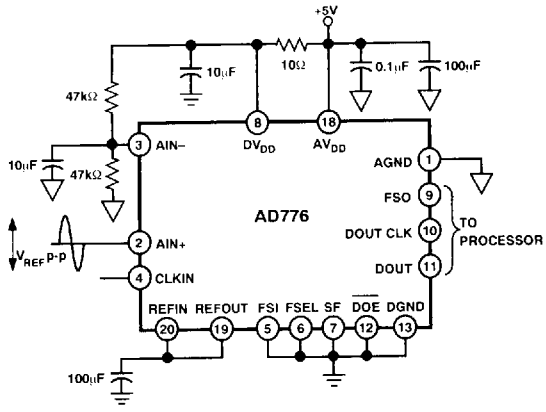


Figure 7. Simple Single-Ended Input Circuit

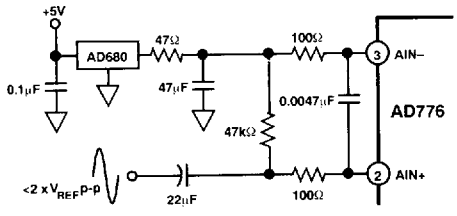


Figure 8. Single-Ended Input Circuit for Improved PSRR

For optimal performance in single-ended input applications, the circuit in Figure 9 may be used to convert the input to a differential signal.

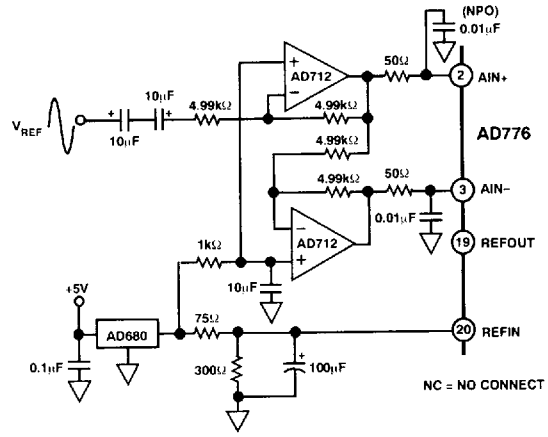


Figure 9. Single-Ended Input to Differential Circuit

REFERENCE INPUT

The AD776 has an on-chip 0.4 V_{DD} reference voltage circuit which can be used to drive REFIN, as shown in Figure 10. Alternately, an external voltage reference may be used to supply the required 2 V. REFIN exhibits characteristics similar to the Analog Input in that the input impedance is a function of the clock rate. This is illustrated in Table III. The minimum reference impedance is equal to $10^{12}/2.5\ f_{CLK}$, where f_{CLK} is the input clock rate.

Table III. Reference Input Impedance

Input Clock Rate (MHz)	Output Sample Rate (kHz)	Reference Input Impedance (kΩ min)
12.8	100	31.3
6.4	50	62.5
6.144	48	65.1
5.6448	44.1	70.9

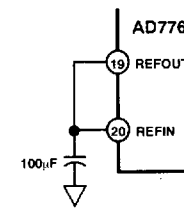


Figure 10. Simple Reference Voltage Circuit

While the internal reference will be adequate for most applications, power supply rejection and overall regulation may be improved through the use of an external reference. The process of selecting an external voltage reference should include consideration of drive capability, initial error, noise, and drift characteristics. A suitable choice would be the AD680 as shown in Figure 11.

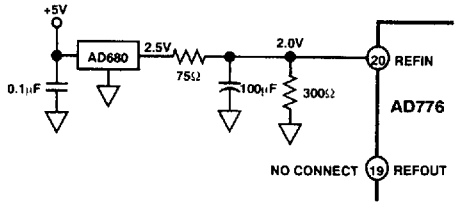


Figure 11. External Voltage Reference Circuit

MULTIPLEXING

The AD776 can also be used with an input multiplexer when the comb filter output is selected by setting FSEL = 1. If f_{CLK} = 12.8 MHz, the minimum multiplex intervals are (including the time to shift the data out from the serial interface):

15 μs (if the FSI and mux are perfectly synchronized)
17.5 μs (if the FSI and mux are not synchronized).

CLOCK GENERATION

With sigma-delta converters, it is critical that clock jitter be minimized in order to achieve optimal performance. Figure 12 illustrates a simple circuit used to derive a clock source for the AD776. An alternative would be to use an oscillator such as the CK1100 series from Cardinal Components (Montclair, NJ) or the F1100 from Fox Electronics. Compared with performance obtained with a typical crystal, use of an oscillator improves SNR by approximately 4 dB.

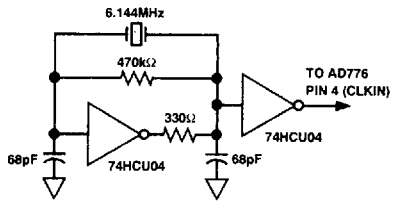


Figure 12. Basic Clock Circuit

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 20 LSBs at the 16 bit level for a 2 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals.

Analog and digital signals should not share a common return path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point at (or under) the part to minimize ground loops. This is preferred to interconnecting the grounds at the supplies.

Analog signals should be routed as far as possible from digital signals and should cross them, if at all, only at right angles. The AD776 may be treated as an analog component, with both AGND and DGND connected to a single analog ground plane. This helps to isolate the AD776 from large digital ground currents. For these reasons, the use of wire wrap circuit construction will not provide adequate performance; careful printed circuit board construction is preferred.

POWER SUPPLIES AND DECOUPLING

With high performance linear circuits, changes in the power supplies can produce undesired changes in the performance of the circuit. Optimally, well regulated power supplies with less than 1% ripple should be selected. The ac output impedance of a power supply is a complex function of frequency, but in general will increase with frequency. High frequency switching such as that encountered with digital circuitry requires fast transient currents which most power supplies cannot adequately provide. This results in voltage spikes on the supplies. To compensate for the finite ac output impedance of the supplies, it is necessary to store "reserves" of charge in bypass capacitors. These capacitors can effectively lower the ac impedance presented to the AD776 power inputs which in turn will significantly reduce the magnitude of the voltage spikes. Decoupling capacitors, typically 0.1 μF, should be placed as close as possible to each power supply pin of the AD776. It is essential that these capacitors be placed physically close to the AD776 to minimize the inductance of the PCB trace between the capacitor and the supply pin.

Additionally, it is beneficial to have large capacitors (>47 μF) located at the point where the power connects to the PCB with 10 μF capacitors located in the vicinity of the ADC to further reduce low frequency ripple.

The AD776 may be operated from a single +5 V supply. However, performance is optimized by using separate analog (AV_{DD}) and digital (DV_{DD}) supplies. Separate supplies enable isolation of digital noise from the analog circuitry. When separate supplies are used, AV_{DD} should be decoupled to analog ground (AGND) and DV_{DD} should be decoupled to digital ground (DGND) with decoupling capacitors.

When a single +5 V supply is used, the circuit shown in Figure 13 provides adequate decoupling.

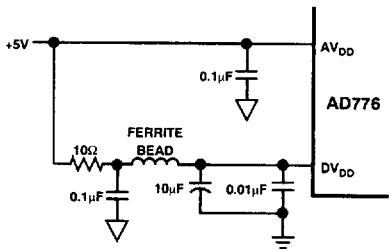


Figure 13. Single Supply Decoupling

DIGITAL TIMING

The CLKIN frequency and the choice of output filter mode (FIR or Comb) determine the output sample rate of the AD776. With FSEL LOW, the FIR filter output is selected and the output rate is equal to CLKIN divided by 128. When FSEL is HIGH, the Comb filter is selected and the output sample rate is equal to CLKIN divided by 32. The input sample rate (or modulator frequency) is always the CLKIN frequency divided by 2.

The flexible serial data output interface of the AD776 may be configured in one of three modes. MODE A and MODE B are used when the FIR filter output is desired. MODE C should be selected when output from the comb filter is used. Output data is always transmitted as 16-bit, twos complement, MSB first, serial words. In all modes, the FSI pin may be asserted to reset the serial data output and synchronize internal circuits. A $\overline{DOE}$ pin is available to place the DOUT pin in a high impedance state.

Configuring the appropriate timing mode is controlled by the FSEL and SF pins. The truth table is shown in Table IV.

Table IV. Timing Mode Truth Table

FSEL	SF	Output Mode
0	0	A
0	1	B
1	0	C

MODE A

The timing diagrams for MODE A are shown in Figures 14a and 14b. If MODE A is selected, an internal multiplexer routes serial data from the output of the FIR filter to the DOUT pin. The output sample rate is a function of the clock present at the CLKIN pin where:

$$Output\ Sample\ Rate = CLKIN/128$$

A continuous serial output clock, DOUT CLK, is available with the bit rate determined by:

$$DOUT\ CLK = CLKIN/4.$$

Serial data from the DOUT pin is valid on the falling edges of DOUT CLK. A framing signal, FSO, occurs with a period equal to the output sample rate (Figure 14b). The FSO signal is HIGH during the falling edge of DOUT CLK prior to the beginning of a new output data word.

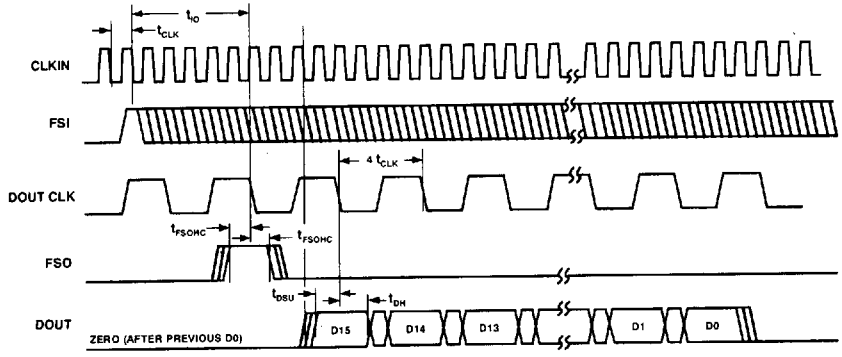


Figure 14a. Mode A Timing

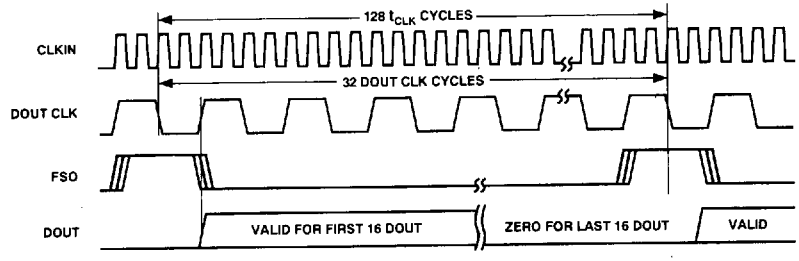


Figure 14b. Mode A Timing

MODE B

The timing diagrams for MODE B are shown in Figures 15a and 15b. If Mode B is selected, the internal multiplexer routes serial data from the output of the FIR filter to the DOUT pin similar to MODE A. The output sample rate is a function of the clock present at the CLKIN pin where:

Output Sample Rate = CLKIN/128.

A continuous serial output clock, DOUT CLK, is available with the bit rate determined by:

DOUT CLK = CLKIN/4.

Note that serial data present at the DOUT pin is valid on the rising edges of DOUT CLK. The framing signal, FSO, occurs with a period equal to the output sample rate. In MODE B, the FSO signal goes LOW at the beginning of the output data word and remains LOW until the entire word is transmitted.

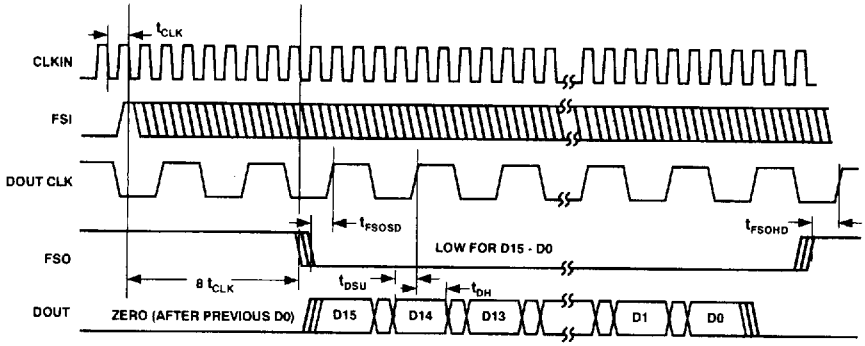


Figure 15a. Mode B Timing

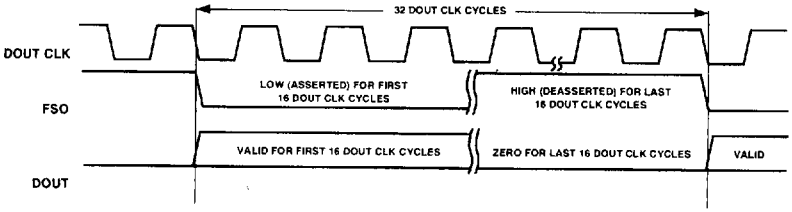


Figure 15b. Mode B Timing

MODE C

The timing diagrams for MODE C are shown in Figure 16. If Mode C is selected, the internal multiplexer routes serial data from the output of the COMB filter to the DOUT pin, bypassing the FIR filter. The output sample rate is a function of the clock present at the CLKIN pin where:

Output Sample Rate = CLKIN/32.

A continuous serial output clock, DOUT CLK, is available with the bit rate determined by:

DOUT CLK = CLKIN/2.

Serial output data is valid on the falling edges of DOUT CLK. The framing signal, FSO, occurs with a period equal to the output sample rate. The FSO signal is HIGH during the falling edge of DOUT CLK prior to transmission of the next output data word. Note that in MODE C, this is also when the LSB, (D0), of the previous data word is valid.

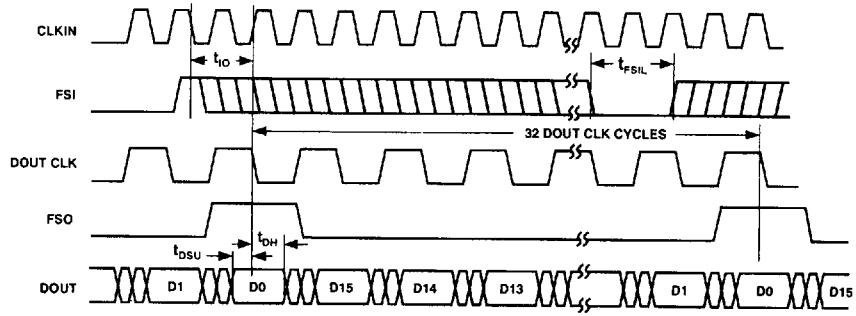


Figure 16. Mode C Timing

FSI Operation

A frame sync input is available to the user on the FSI pin to reset the serial data output and synchronize internal circuits.

Referring to Figure 17, the FSI pin is sampled on the falling edge of CLKIN. The FSI pin must adhere to several conditions depending on which mode is being used as follows:

FSI in MODE A, MODE B

1. FSI should be a periodic signal occurring every 32 DOUT CLK periods.
2. FSI must be deasserted for at least 2 CLKIN periods prior to being asserted.
3. FSI must be synchronized to CLKIN to meet the timing requirements outlined in Figure 17.

FSI in MODE C

1. FSI should be a periodic signal occurring every 16 DOUT CLK periods.
2. FSI must be deasserted for at least 2 CLKIN periods prior to being asserted.
3. FSI must be synchronized to CLKIN to meet the timing requirements outlined in Figure 17.

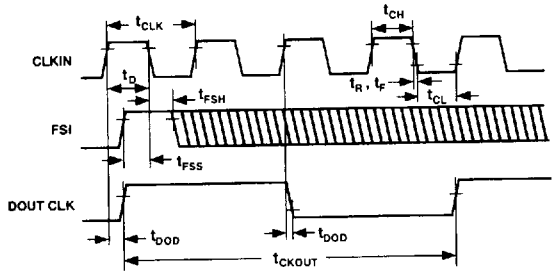


Figure 17. Frame Sync Input (FSI) Timing (FIR Filter Output Mode)

Synchronizing Two Channels

The FSI pin is useful when multiple AD776s are used together and must be synchronized. In such a case, a single pulse may be applied to FSI inputs of the converters. This causes the internal "state-machine" of the AD776 to be reset. Thus, the internal clocking for both the analog and digital circuitry of each individual converter is synchronized and in-phase. In the case of a single FSI pulse, it must still adhere to the timing outlined in Figure 17.

Three-Stating the DOUT Pin ($\overline{DOE}$)

In all modes DOUT may be three-stated using the $\overline{DOE}$ pin. Operation of the $\overline{DOE}$ input is shown in Figure 18. When the $\overline{DOE}$ input is HIGH, serial data will be present and active at the DOUT pin. When $\overline{DOE}$ is brought LOW, the DOUT pin is placed in a high-impedance state. $\overline{DOE}$ is completely asynchronous and independent of input and output clocks. DOUT loading will affect actual performance.

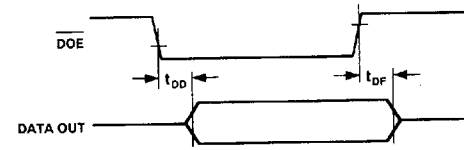


Figure 18. Data Output Timing

INTERFACING THE AD776

The AD776 is designed for ease of interface with a variety of popular processors. The following diagrams illustrate typical configurations:

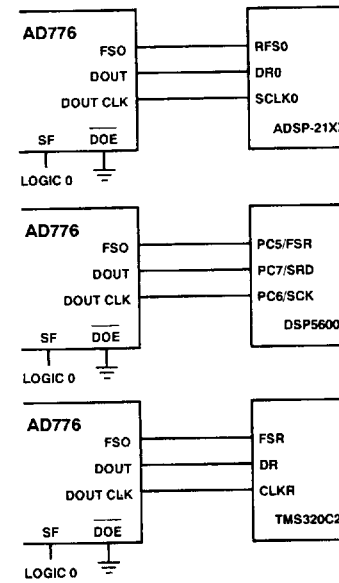


Figure 19.