Read Only, Pin Configured 24-Bit Σ-Δ ADC

AD7782

FEATURES

2-Channel, 24-Bit Σ-Δ ADC
- Pin Configurable (No Programmable Registers)
- Pin Selectable Input Channels
- Pin Programmable Input Ranges (±2.56 V or ±160 mV)

Fixed 19.79 Hz Update Rate
Simultaneous 50 Hz and 60 Hz Rejection
24-Bit No Missing Codes
18.5-Bit p-p Resolution (±2.56 V Range)
16.5-Bit p-p Resolution (±160 mV Range)

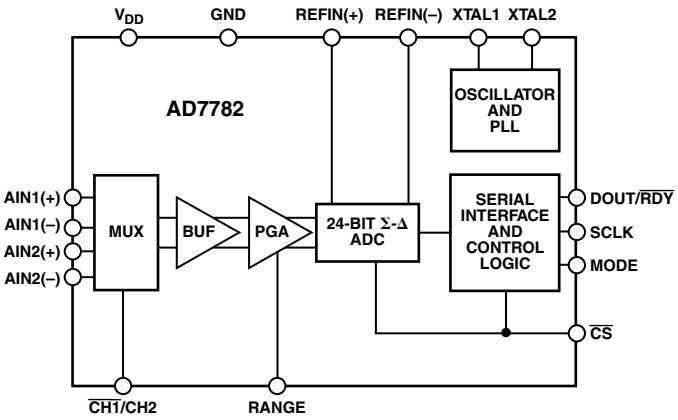
INTERFACE
Master or Slave Mode of Operation
Slave Mode
- 3-Wire Serial
- SPI™, QSPI™, MICROWIRE™, and DSP-Compatible
- Schmitt Trigger on SCLK

POWER
Specified for Single 3 V and 5 V Operation
Normal: 1.3 mA @ 3 V
Power-Down: 9 μA

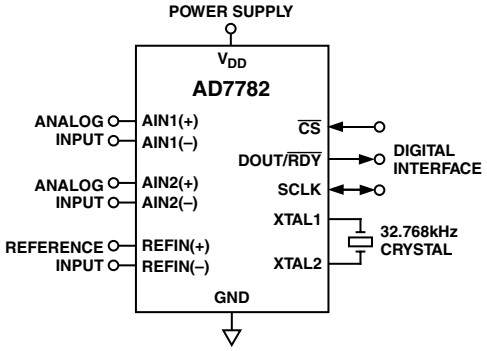
ON-CHIP FUNCTIONS
Rail-Rail Input Buffer and PGA

APPLICATIONS
Sensor Measurement
Industrial Process Control
Temperature Measurement
Pressure Measurements
Weigh Scales
Portable Instrumentation

FUNCTIONAL BLOCK DIAGRAM



BASIC CONNECTION DIAGRAM



GENERAL DESCRIPTION

The AD7782 is a complete analog front end for low-frequency measurement applications. The 24-bit sigma-delta ADC contains two fully differential analog input channels that can be configured with a gain of 1 or 16 allowing full-scale input signal ranges of ±2.56 V or ±160 mV from a +2.5 V differential reference input.

The AD7782 has an extremely simple, read-only digital interface which can be operated in master mode or slave mode. There are no on-chip registers to be programmed. The input signal range and input channel selection are configured using two external pins.

The device operates from a 32.768 kHz crystal with an on-chip PLL generating the required internal operating frequency. The output data rate from the part is fixed via the master clock at 19.79 Hz and provides simultaneous 50 Hz and 60 Hz rejection at this update rate. Eighteen-bit p-p resolution can be obtained at this update rate.

The part operates from a single 3 V or 5 V supply. When operating from 3 V supplies, the power dissipation for the part is 3.9 mW. The AD7782 is available in a 16-lead TSSOP package.

Another part in the AD778x family is the AD7783. It is similar to the AD7782 except it has two integrated current sources and only one differential input channel.

REV. A

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AD7782–SPECIFICATIONS (V_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V; REFIN(–) = GND; GND = 0 V; XTAL1/XTAL2 = 32.768 kHz Crystal; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	AD7782B	Unit	Test Conditions
ADC CHANNEL SPECIFICATION			
Output Update Rate	19.79	Hz nom	
ADC CHANNEL			
No Missing Codes[2]	24	Bits min	
Resolution	16	Bits p-p	±160 mV Range, RANGE = 0
	18	Bits p-p	±2.56 V Range, RANGE = 1
Output Noise	See Table I		
Integral Nonlinearity	±10	ppm of FSR max	Typically 2 ppm $FSR = \frac{2 \times 1.024\ REFIN}{Gain}$
Offset Error	±3	µV typ	AIN(+) = AIN(–) = 2.5 V
Offset Error Drift vs. Temperature	±10	nV/°C typ	
Full-Scale Error	±10	µV typ	V_{DD} = 3 V
Gain Drift vs. Temperature	±0.5	ppm/°C typ	
Power Supply Rejection (PSR)	100	dB typ	Input Range = ±160 mV, V_{IN} = 1/16 V
	85	dB typ	Input Range = ±2.56 V, V_{IN} = 1 V
ANALOG INPUTS			
Differential Input Voltage Ranges	±160	mV nom	RANGE = 0
	±2.56	V nom	RANGE = 1
ADC Range Matching	±2	µV typ	Input Voltage = 159 mV on Both Ranges
Absolute AIN Voltage Limits	GND + 100 mV	V min	
	V_{DD} – 100 mV	V max	
Analog Input Current[2]			
DC Input Current	±1	nA max	
DC Input Current Drift	±5	pA /°C typ	
Normal-Mode Rejection[2, 3]			
@ 50 Hz	60	dB min	50 Hz ± 1 Hz
@ 60 Hz	94	dB min	60 Hz ± 1 Hz
Common-Mode Rejection			Input Range = ±160 mV, V_{IN} = 1/16 V
@ DC	105	dB min	125 dB typ, 110 dB typ when Input Range = ±2.56 V
@ 50 Hz[2]	100	dB min	50 Hz ± 1 Hz
@ 60 Hz[2]	100	dB min	60 Hz ± 1 Hz
REFERENCE INPUT			
REFIN Voltage	2.5	V nom	REFIN = REFIN(+) – REFIN(–)
REFIN Voltage Range[2]	1	V min	
	V_{DD}	V max	
Absolute REFIN Voltage Limits[2]	GND – 30 mV	V min	
	V_{DD} + 30 mV	V max	
Average Reference Input Current	0.5	µA/V typ	
Average Reference Input Current Drift	±0.01	nA/V/°C typ	
Normal-Mode Rejection[2, 3]			
@ 50 Hz	60	dB min	50 Hz ± 1 Hz
@ 60 Hz	94	dB min	60 Hz ± 1 Hz
Common-Mode Rejection			Input Range = ±160 mV, V_{IN} = 1/16 V
@ DC	100	dB typ	
@ 50 Hz	110	dB typ	50 Hz ± 1 Hz
@ 60 Hz	110	dB typ	60 Hz ± 1 Hz
LOGIC INPUTS			
All Inputs Except SCLK and XTAL1[2]			
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	V_{DD} = 3 V or 5 V
SCLK Only (Schmitt-Triggered Input)[2]			
$V_{T(+)}$	1.4/2	V min/V max	V_{DD} = 5 V
$V_{T(-)}$	0.8/1.4	V min/V max	V_{DD} = 5 V
$V_{T(+)} - V_{T(-)}$	0.3/0.85	V min/V max	V_{DD} = 5 V
$V_{T(+)}$	0.95/2	V min/V max	V_{DD} = 3 V
$V_{T(-)}$	0.4/1.1	V min/V max	V_{DD} = 3 V
$V_{T(+)} - V_{T(-)}$	0.3/0.85	V min/V max	V_{DD} = 3 V

Parameter	AD7782B	Unit	Test Conditions
LOGIC INPUTS (continued)			
XTAL1 Only[2]			
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = 5 V
V_{INH}, Input High Voltage	3.5	V min	V_{DD} = 5 V
V_{INL}, Input Low Voltage	0.4	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage	2.5	V min	V_{DD} = 3 V
Input Currents	±1	μA max	V_{IN} = V_{DD}
	–70	μA max	V_{IN} = GND, Typically –40 μA at 5 V and –20 μA at 3 V
Input Capacitance	10	pF typ	All Digital Inputs
LOGIC OUTPUTS (Excluding XTAL2)			
V_{OH}, Output High Voltage[2]	V_{DD} – 0.6	V min	V_{DD} = 3 V, I_{SOURCE} = 100 μA
V_{OL}, Output Low Voltage[2]	0.4	V max	V_{DD} = 3 V, I_{SINK} = 100 μA
V_{OH}, Output High Voltage[2]	4	V min	V_{DD} = 5 V, I_{SOURCE} = 200 μA
V_{OL}, Output Low Voltage[2]	0.4	V max	V_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Leakage Current	±10	μA max	
Floating-State Output Capacitance	±10	pF typ	
Data Output Coding	Offset Binary		
START-UP TIME			
From Power-On	300	ms typ	
POWER REQUIREMENTS			
Power Supply Voltage			
V_{DD} – GND	2.7/3.6	V min/max	V_{DD} = 3 V nom
	4.75/5.25	V min/max	V_{DD} = 5 V nom
Power Supply Currents			
I_{DD} Current (Normal Mode)[4]	1.5	mA max	V_{DD} = 3 V, 1.3 mA typ
	1.7	mA max	V_{DD} = 5 V, 1.5 mA typ
I_{DD} (Power-Down Mode, $\overline{CS}$ = 1)	9	μA max	V_{DD} = 3 V, 6 μA typ
	24	μA max	V_{DD} = 5 V, 20 μA typ

NOTES
[1]Temperature Range –40°C to +85°C.
[2]Guaranteed by design and/or characterization data on production release.
[3]When a 28.8 kHz crystal is used, normal mode rejection is improved so that the rejection equals 75 dB at 50 ± 1 Hz and equals 66 dB at 60 ± 1 Hz.
[4]Normal Mode refers to the case where the ADC is running.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = 2.7 V to 3.6 V or V_{DD} = 4.75 V to 5.25 V; GND = 0 V; XTAL = 32.768 kHz; Input Logic 0 = 0 V, Logic 1 = V_{DD} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments
t_1	30.5176	µs typ	Crystal Oscillator Period
t_{ADC}	50.54	ms typ	19.79 Hz Update Rate
t_2	0	ns min	$\overline{CH1}$/CH2 Select to $\overline{CS}$ Setup Time
t_3	0	ns min	$\overline{CS}$ Falling Edge to DOUT Active
	60	ns max	V_{DD} = 4.75 V to 5.25 V
	80	ns max	V_{DD} = 2.7 V to 3.6 V
t_4	2 × t_{ADC}	ns typ	Channel Settling Time
t_5[3]	0	ns min	SCLK Active Edge to Data Valid Delay[4]
	60	ns max	V_{DD} = 4.75 V to 5.25 V
	80	ns max	V_{DD} = 2.7 V to 3.6 V
t_8[5]	10	ns min	Bus Relinquish Time after $\overline{CS}$ Inactive Edge
	80	ns max	
t_9	0	ns min	$\overline{CS}$ Rising Edge to SCLK Inactive Edge Hold Time
t_{10}	10	ns min	SCLK Inactive to DOUT High
	80	ns max	
Slave Mode Timing			
t_6	100	ns min	SCLK High Pulsewidth
t_7	100	ns min	SCLK Low Pulsewidth
Master Mode Timing			
t_6	$t_1/2$	µs typ	SCLK High Pulsewidth
t_7	$t_1/2$	µs typ	SCLK Low Pulsewidth
t_{11}	$t_1/2$	µs min	DOUT Low to First SCLK Active Edge[4]
	$3t_1/2$	µs max	

NOTES
[1]Sample tested during initial release to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[2]See Figure 2.
[3]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[4]SCLK active edge is falling edge of SCLK.
[5]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

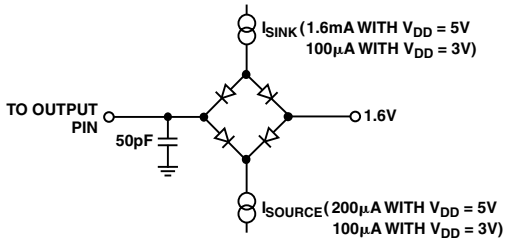


Figure 1. Load Circuit for Timing Characterization

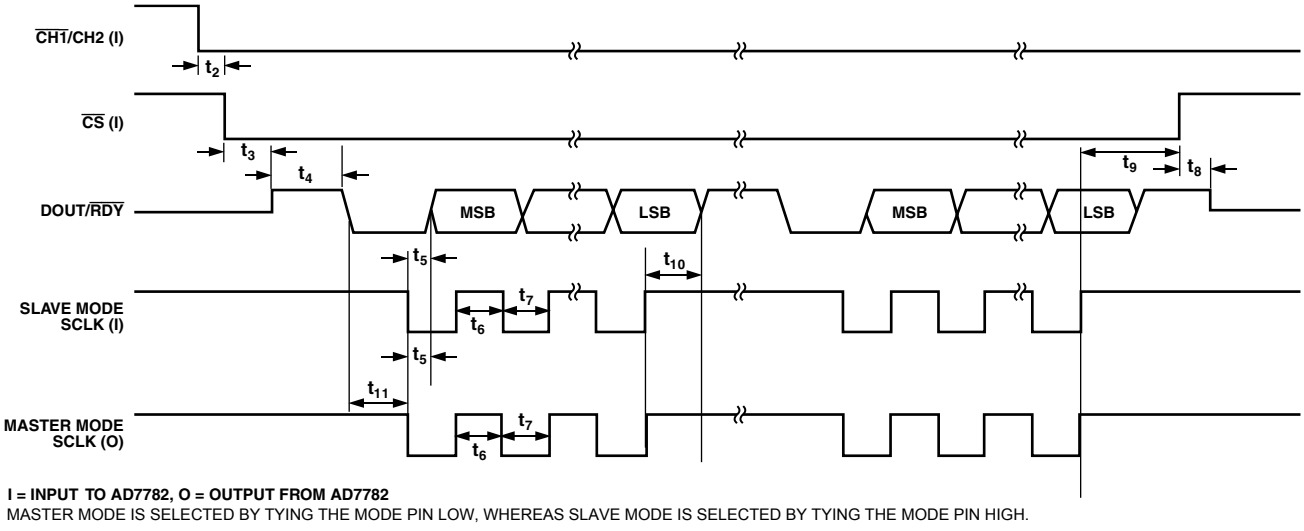


Figure 2. Slave/Master Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Analog Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Total AIN/REFIN Current (Indefinite) . . . . . 30 mA
Digital Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C

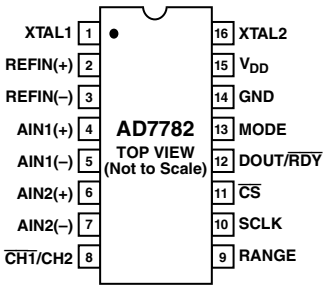
TSSOP Package
θ_{JA} Thermal Impedance . . . . . 97.9°C/W
θ_{JC} Thermal Impedance . . . . . 14°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7782 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

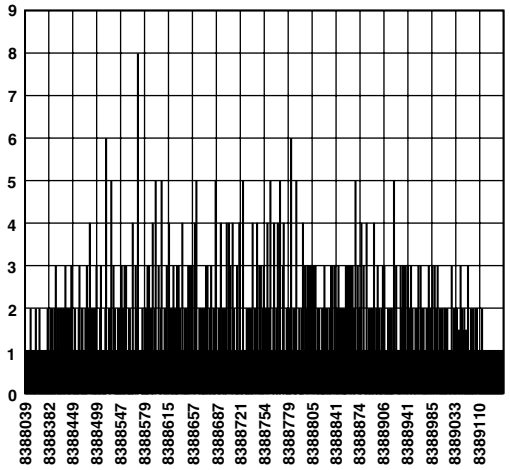
PIN CONFIGURATION



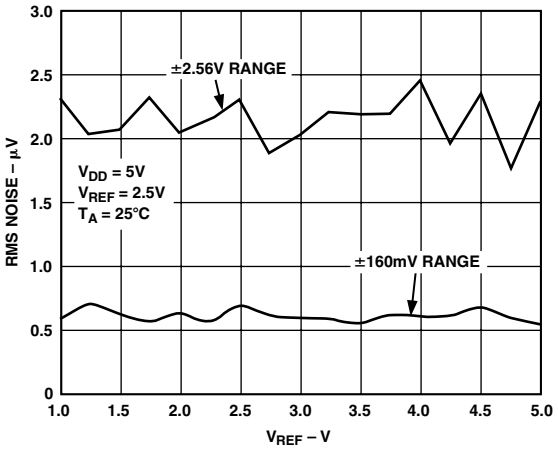
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	XTAL1	Input to the 32.768 kHz Crystal Oscillator Inverter.
2	REFIN(+)	Positive Reference Input. REFIN(+) can lie anywhere between V_{DD} and GND +1 V. The nominal reference voltage (REFIN(+) – REFIN(–)) is 2.5 V, but the part functions with a reference from 1 V to V_{DD}.
3	REFIN(–)	Negative Reference Input. This reference input can lie anywhere between GND and V_{DD} – 1 V.
4	AIN1(+)	Analog Input. AIN1(+) is the positive terminal of the fully-differential analog input pair AIN1(+)/AIN1(–).
5	AIN1(–)	Analog Input. AIN1(–) is the negative terminal of the fully-differential analog input pair AIN1(+)/AIN1(–).
6	AIN2(+)	Analog Input. AIN2(+) is the positive terminal of the fully-differential analog input pair AIN2(+)/AIN2(–).
7	AIN2(–)	Analog Input. AIN2(–) is the negative terminal of the fully-differential analog input pair AIN2(+)/AIN2(–).
8	$\overline{CH1}$/CH2	Channel Select, Logic Input. With $\overline{CH1}$/CH2 = 0, channel AIN1(+)/AIN1(–) is selected while the active channel is AIN2(+)/AIN2(–) when $\overline{CH1}$/CH2 = 1.
9	RANGE	Logic Input which configures the input range on the internal PGA. With RANGE = 0, the full-scale input range is ±160 mV while the full-scale input range equals ±2.56 V when RANGE = 1 for a +2.5 V Reference.
10	SCLK	Serial Clock Input/Output for Data Transfers from the ADC. When the device is operated in master mode, SCLK is an output with one SCLK period equal to one XTAL period. In slave mode, SCLK is generated by an external source. In slave mode, all the data can be transmitted on a continuous train of pulses. Alternatively, SCLK can be a noncontinuous clock with the information being transmitted from the AD7782 in smaller batches of data. SCLK is Schmitt triggered (slave mode) making the interface suitable for opto-isolated applications.
11	$\overline{CS}$	Chip Select Input. $\overline{CS}$ is an active low logic input used to select the AD7782. When $\overline{CS}$ is low, the PLL establishes lock and allows the AD7782 to initiate a conversion on the selected channel. When $\overline{CS}$ is high, the conversion is aborted, DOUT and SCLK are three-stated, the AD7782 enters standby mode and any conversion result in the output shift register is lost.
12	DOUT/$\overline{RDY}$	Serial Data Output/Data Ready Output. DOUT/$\overline{RDY}$ serves a dual purpose in this interface. When a conversion is initiated, DOUT/$\overline{RDY}$ goes high and remains high until the conversion is complete. DOUT/$\overline{RDY}$ will then return low to indicate that valid data is available to be read from the device. In slave mode, this acts as an interrupt to the processor indicating that valid data is available. If data is not read after a conversion, DOUT/$\overline{RDY}$ will go high before the next update occurs. In master mode, DOUT/$\overline{RDY}$ goes low for at least half an SCLK cycle before the device produces SCLKs. When SCLK becomes active, data is output on the DOUT/$\overline{RDY}$ pin. Data is output on the falling SCLK edge and is valid on the rising edge.
13	MODE	The MODE pin selects master or slave mode of operation. When MODE = 0, the AD7782 operates in master mode while the AD7782 is configured for slave mode when MODE = 1.
14	GND	Ground Reference Point for the AD7782.
15	V_{DD}	Supply Voltage, 3 V or 5 V Nominal.
16	XTAL2	Output from the 32.768 kHz Crystal Oscillator Inverter.

Typical Performance Characteristics



TPC 1. Noise Distribution Histogram



TPC 2. RMS Noise vs. Reference Input

ADC CIRCUIT INFORMATION

Overview

The AD7782 incorporates an analog multiplexer with a Σ-Δ ADC channel, on-chip programmable gain amplifier, and on-chip digital filtering intended for the measurement of wide dynamic range, low-frequency signals such as those in weigh-scale, strain-gage, pressure transducer, or temperature measurement applications.

This ADC input is buffered and can be programmed to have an input voltage range of ±160 mV or ±2.56 V. The input channels are configured as two fully differential inputs. Buffering the input channels means that the part can accommodate significant source impedances on the analog inputs and that R, C filtering (for noise rejection or RFI reduction) can be placed on the analog inputs if required. The device requires an external reference of +2.5 V nominal. Figure 3 shows the basic connections required to operate the part.

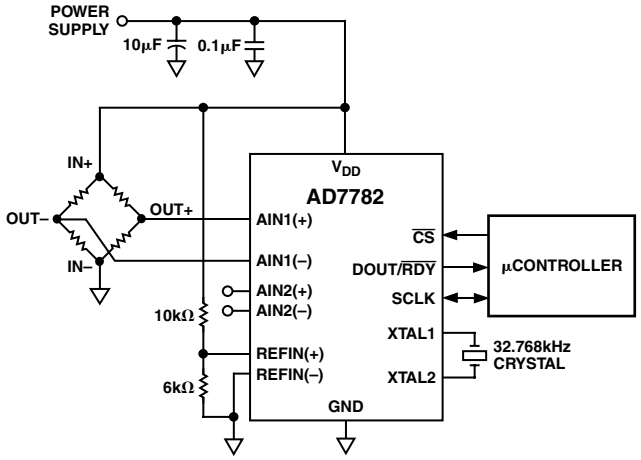


Figure 3. Basic Connection Diagram

The output rate of the AD7782 (f_{ADC}) equals:

$$f_{ADC} = 32.768 \times 10^3 / (69 \times 8 \times 3)$$

while the settling time equals:

$$t_{SETTLE} = \left(\frac{2}{f_{ADC}}\right) = 2 \times t_{ADC}$$

Normal-mode rejection is the major function of the digital filter on the AD7782. Simultaneous 50 Hz and 60 Hz rejection of better than 60 dB is achieved as notches are placed at both 50 Hz and 60 Hz. Figure 4 shows the filter rejection.

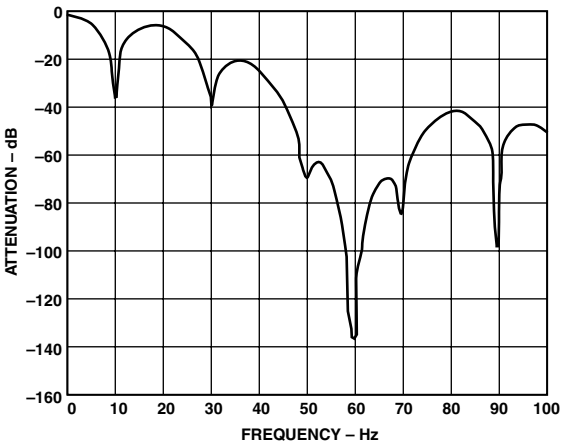


Figure 4. Filter Profile (Filter Notches at Both 50 Hz and 60 Hz)

NOISE PERFORMANCE

Table I shows the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for the two input voltage ranges. The numbers are typical and generated at a differential input voltage of 0 V. The peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

Table I. Typical Output RMS Noise and Peak-to-Peak Resolution vs. Input Range

	Input Range	
	±160 mV	**±2.56 V**
Noise (μV)	0.65	2.30
Peak-to-Peak Resolution (Bits)	16.5	18.5

DIGITAL INTERFACE

The AD7782's serial interface consists of four signals, $\overline{CS}$, SCLK, DOUT/$\overline{RDY}$, and MODE. The MODE pin is used to select the master/slave mode of operation. When the part is configured as a master, SCLK is an output while SCLK is an input when slave mode is selected. Data transfers take place with respect to this SCLK signal. The DOUT/$\overline{RDY}$ line is used for accessing data from the data register. This pin also functions as a $\overline{RDY}$ line. When a conversion is complete, DOUT/$\overline{RDY}$ goes low to indicate that data is ready to be read from the AD7782's data register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when *not* to read from the device to ensure that a data read is not attempted while the register is being updated. The digital conversion is also output on this pin.

$\overline{CS}$ is used to select the device and to place the device in standby mode. When $\overline{CS}$ is taken low, the AD7782 is powered up, the PLL locks and the device initiates a conversion on the selected channel. The device will continue to convert until $\overline{CS}$ is taken high. When $\overline{CS}$ is taken high, the AD7782 is placed in standby mode minimizing the current consumption. The conversion is aborted, DOUT and SCLK are three-stated and the result in the data register is lost.

Figure 2 shows the timing diagram for interfacing to the AD7782 with $\overline{CS}$ used to decode the part.

MASTER MODE (MODE = 0)

In this mode, SCLK is provided by the AD7782. With $\overline{CS}$ low, SCLK becomes active when a conversion is complete and generates twenty four falling and rising edges. The DOUT/$\overline{RDY}$ pin, which is normally high, goes low to indicate that a conversion is complete. Data is output on the DOUT/$\overline{RDY}$ pin following the SCLK falling edge and is valid on the SCLK rising edge. When the 24-bit word has been output, SCLK idles high until the next conversion is complete. DOUT/$\overline{RDY}$ returns high and will remain high until another conversion is available. It then operates as a $\overline{RDY}$ signal again. The part will continue to convert until $\overline{CS}$ is taken high. SCLK and DOUT/$\overline{RDY}$ are three-stated when $\overline{CS}$ is taken high.

SLAVE MODE (MODE = 1)

In slave mode, the SCLK is generated externally. SCLK must idle high between data transfers. With $\overline{CS}$ low, DOUT/$\overline{RDY}$ goes low when a conversion is complete. Twenty four SCLK pulses are needed to transfer the digital word from the AD7782. Twenty four consecutive pulses can be generated or, alternatively, the data transfer can be split into batches. This is useful when interfacing to a microcontroller which uses 8-bit transfers. Data is output following the SCLK falling edge and is valid on the SCLK rising edge.

CIRCUIT DESCRIPTION

Analog Input Channels

The ADC has two fully differential input channels. Pin $\overline{CH1}$/CH2 is used to select the channels. When $\overline{CH1}$/CH2 is low, channel AIN1(+) – AIN1(–) are selected while channel AIN2(+) – AIN2(–) are selected when $\overline{CH1}$/CH2 is high. When the analog input channel is switched, the settling time of the part must elapse before a new valid word is available from the ADC.

The output of the ADC multiplexer feeds into a high-impedance input stage of the buffer amplifier. As a result, the ADC inputs can handle significant source impedances and are tailored for direct connection to external resistive-type sensors like strain gages or Resistance Temperature Detectors (RTDs).

The absolute input voltage range on the ADC inputs is restricted to a range between GND + 100 mV and V_{DD} – 100 mV. Care must be taken in setting up the common-mode voltage and input voltage range so that these limits are not exceeded; otherwise there will be a degradation in linearity and noise performance.

Programmable Gain Amplifier

The output from the buffer on the ADC is applied to the input of the on-chip programmable gain amplifier (PGA). The PGA gain range is programmed via pin RANGE. With an external 2.5 V reference applied, the PGA can be programmed to have a bipolar range of ±160 mV (RANGE = 0) or ±2.56 V (RANGE = 1). These are the ranges that should appear at the input to the on-chip PGA.

Bipolar Configuration/Output Coding

The analog inputs on the AD7782 accept bipolar input voltage ranges. Signals on the AIN(+) input of the ADC are referenced to the voltage on the respective AIN(–) input. For example, if AIN(–) is 2.5 V and the AD7782 is configured for an analog input range of ±160 mV, the analog input range on the AIN(+) input is 2.34 V to 2.66 V (i.e., 2.5 V ± 0.16 V).

The coding is offset binary with a negative full-scale voltage resulting in a code of 000 . . . 000, a zero differential voltage resulting in a code of 100 . . . 000, and a positive full-scale voltage resulting in a code of 111 . . . 111. The output code for any analog input voltage can be represented as follows:

$$Code = 2^{N-1} \times \left[\left(AIN \times GAIN / \left(1.024 \times V_{REF}\right)\right) + 1\right]$$

Where AIN is the analog input voltage, *GAIN* is the PGA gain, i.e., 1 on the ±2.56 V range and 16 on the ±160 mV range and N = 24.

Crystal Oscillator

The AD7782 is intended for use with a 32.768 kHz watch crystal. A PLL internally locks onto a multiple of this frequency to provide a stable 4.194304 MHz clock for the ADC. The modulator sample rate is the same as the crystal oscillator frequency. The start-up time associated with 32.768 kHz crystals is typically 300 ms. In some cases, it will be necessary to connect capacitors on the crystal to ensure that it does not oscillate at overtones of its fundamental operating frequency. The values of capacitors will vary depending on the manufacturer's specifications.

Reference Input

The AD7782 has a fully-differential reference input capability for the channel. The common-mode range for these differential inputs is from GND to V_{DD}. The reference input is unbuffered and therefore excessive R-C source impedances will introduce gain errors. The reference voltage REFIN (REFIN(+) – REFIN(–)) is 2.5 V nominal for specified operation but the AD7782 is functional with reference voltages from 1 V to V_{DD}. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source will be removed as the application is ratiometric. If the AD7782 is used in a nonratiometric application, a low noise reference should be used. Recommended reference voltage sources for the AD7782 include the AD780, REF43, and REF192. It should also be noted that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources like those recommended above (e.g., AD780) will typically have low output impedances and are therefore tolerant to having decoupling capacitors on the REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN pins would not be recommended in this type of circuit configuration.

Grounding and Layout

Since the analog inputs and reference inputs on the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The digital filter will provide rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs provided these noise sources do not saturate the analog modulator. As a result, the AD7782 is more immune to noise interference than a conventional high-resolution converter. However, because the resolution of the AD7782 is so high, and the noise levels from the AD7782 so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7782 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes as it gives the best shielding.

It is recommended that the AD7782's GND pin be tied to the AGND plane of the system. In any layout, it is important that the user keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The AD7782's ground plane should be allowed to run under the AD7782 to prevent noise coupling. The power supply lines to the AD7782 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high-resolution ADCs. VDD should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to GND. To achieve the best from these decoupling components, they have to be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF ceramic capacitors to DGND.

OUTLINE DIMENSIONS

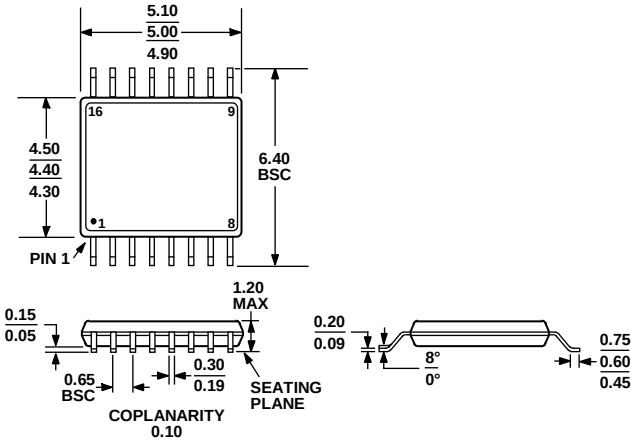


Figure 1. 16-Lead Thin Shrink SO Plastic (TSSOP)
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7782BRU-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7782BRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7782BRUZ-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7782BRUZ-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

[1] Z = RoHS Compliant Part.

REVISION HISTORY

4/12—Rev. 0 to Rev. A

Updated Format..... Universal
Changes to Figure 2 5
Updated Outline Dimensions.....10
Changes to Ordering Guide.....10

10/2001—Revision 0: Initial Version

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D02701-0-4/12(A)