

Data Sheet

AD7846-CHIPS

FEATURES

- 16-bit monotonicity over temperature
- Microprocessor compatible with read-back capability
- Unipolar or bipolar output
- Multiplying capability
- ▶ Low power dissipation: 100 mW typical

APPLICATIONS

- Instrumentation
- Automatic test equipment
- Industrial automation
- Energy grid systems
- Aerospace

GENERAL DESCRIPTION

The AD7846-CHIPS is a 16-bit digital-to-analog converter (DAC) constructed with the Analog Devices, Inc., LC^2MOS process. The device has V_{REF+} and V_{REF-} reference inputs and an on-chip output amplifier that can be configured to give a unipolar output range (0 V to +5 V or 0 V to +10 V) or bipolar output ranges (±5 V or ±10 V).

The DAC uses a segmented architecture. The four MSBs in the DAC latch select one of the segments in a 16-resistor string. Both taps of the segment are buffered by amplifiers and fed to a 12-bit DAC, which provides a further 12 bits of resolution. This architecture ensures 16-bit monotonicity. Excellent integral linearity results from tight matching between the input offset voltages of the two buffer amplifiers.

FUNCTIONAL BLOCK DIAGRAM

LC2MOS 16-Bit Voltage Output DAC

In addition to the excellent accuracy specifications, the AD7846-CHIPS also offers a comprehensive microprocessor interface. There are 16 data input and output pins, plus control lines (\overline{CS} , R/W, \overline{LDAC} , and \overline{CLR}). R/W and \overline{CS} allow writing to and reading from the input and output latch, and this read-back function is useful in ATE applications. \overline{LDAC} allows simultaneous updating of DACs in a multiDAC system, and the \overline{CLR} line resets the contents of the DAC latch to 00 ... 000 or 10 ... 000 depending on the state of R/W, which means that the DAC output can be reset to 0 V in both unipolar and bipolar configurations.

Additional application and technical information can be found in the AD7846 data sheet.

PRODUCT HIGHLIGHTS

- 16-Bit Monotonicity. The guaranteed 16-bit monotonicity over temperature makes the AD7846-CHIPS ideal for closed-loop applications.
- 2. Readback. The ability to read back the DAC register contents minimizes software routines when the AD7846-CHIPS is used in automatic test equipment systems.
- **3.** Power Dissipation. A power dissipation of 100 mW makes the AD7846-CHIPS a low power, high accuracy DAC.



Figure 1. Functional Block Diagram

Rev. A

DOCUMENT FEEDBACK

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TABLE OF CONTENTS

1
. 1
.1
1
.1
3
. 5
.5

Absolute Maximum Ratings	7
ESD Caution	7
Pin Configuration and Function Descriptions	8
Outline Dimensions	10
Die Specifications and Assembly	
Recommendations	10
Ordering Guide	11
Outline Dimensions Die Specifications and Assembly Recommendations Ordering Guide	10 10 11

REVISION HISTORY

1/2024—Rev. 0 to Rev. A	
Updated Outline Dimensions	10
Changes to Table 7	10

11/2023—Revision 0: Initial Version

 V_{DD} = +14.25 V to +15.75 V, V_{SS} = -14.25 V to -15.75 V, and V_{CC} = +4.75 V to +5.25 V. V_{OUT} loaded with 2 k Ω , 1000 pF to 0 V, V_{REF+} = +5 V, and R_{IN} connected to 0 V. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

RESOLUTION 16 Bits UNPOLAR OUTPUT Value: = 0.V. Vour = 0.V to +10.V Fallew Accuracy at 25°C ±12 LSB 11.58 = 15.3 μV Differential Nonlinearly Error ±11 LSB All grades guaranted monotonic Gain Error at 25°C ±12 LSB Vour load = 10 MΩ True to Tax ±16 LSB Vour load = 10 MΩ Offset Error at 25°C ±12 LSB Vour load = 10 MΩ Offset Error at 25°C ±12 LSB Vour load = 10 MΩ Offset Error at 25°C ±11 ppn FSR°C ppn FSR°C Offset Error at 25°C ±16 LSB LSB LSB Offset Error at 25°C ±6 LSB LSB LSB LSB Differential Nonlinearly Error ±1 LSB Vour load = 10 MΩ True to True to 10 to +10.V True to True ±6 LSB Vour load = 10 MΩ True to True to 10 to +10.V True to True ±12 LSB Vour load = 10 MΩ True to True to 10.V True to True ±1 ppn FSR°	Parameter ¹	Min	Тур	Мах	Unit	Test Conditions/Comments
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Offset Error at 25°C ± 6 LSB V_{OUT} load = 10 M Ω T_MIN to T_MAX ± 16 LSBBipolar Zero Error at 25°C ± 6 LSBT_MIN to T_MAX ± 12 LSBGain Temperature Coefficient ² ± 1 ppm FSR/°COffset Temperature Coefficient ² ± 1 ppm FSR/°CBipolar Zero Temperature Coefficient ² ± 1 ppm FSR/°CREFERENCE INPUT 40 K Ω Resistance from V_{REF+} to V_{REF-} Input Resistance 20 $K\Omega$ Typically 30 k Ω V_REF+ Range $V_{SS} + 6$ $V_{DD} - 6$ V OUTPUT CHARACTERISTICS $V_{SS} + 4$ $V_{DD} - 3$ V Capacitive Load 2 k Ω To 0 VCapacitive Load 0.3 Ω To 0 VDigital Resistance 0.3 Ω To 0 V or any power supplyDigital Resistance 0.3 Ω To 0 V or any power supplyDigital Low Voltage (V_{L}) 2.4 V VInput High Voltage (V_{L}) 0.4 V Sink current ($(I_{SUNC}) = 1.6$ mAInput Low Voltage (V_{L}) 0.4 V Sink current ($(I_{SUNC}) = 1.6$ mADigital Low Voltage (V_{CL}) 0.4 V Source current ($(I_{SUNC}) = 1.6$ mADigital Low Voltage (V_{CL}) 0.4 V Source current ($(I_{SUNC}) = 1.6$ mADigital Low Voltage (V_{CL}) 0.4 V Source current ($(I_{SUNC}) = 1.6$ mADigital Low Voltage (V_{CL}) 0.4 V Source current ($(I_{SUNC}) = 1.6$ m	T _{MIN} to T _{MAX}			±16	LSB	
T_{NIN} to T_{MAX} ± 16 LSBLSBBipolar Zero Error at 25°C ± 6 LSB T_{NIN} to T_{MAX} ± 12 LSBGain Temperature Coefficient ² ± 1 ppm FSR/°CDifset Temperature Coefficient ² ± 1 ppm FSR/°CBipolar Zero Temperature Coefficient ² ± 1 ppm FSR/°CBipolar Zero Temperature Coefficient ² ± 1 ppm FSR/°CREFERENCE INPUT20KQResistance from V_{REF+} to V_{REF-} Input Resistance20KQTypically 30 KQ V_{REF-} Range $V_{SS} + 6$ $V_{DD} - 6$ V V_{REF-} Range $V_{SS} + 6$ $V_{DD} - 6$ VOutput Voltage Swing $V_{SS} + 4$ $V_{DD} - 3$ VResistance0.3QTo 0 VOutput Voltage Swing $V_{SS} + 4$ $V_{DD} - 3$ VCapacitive Load0.3QTo 0 VOutput Resistance0.3QTo 0 V or any power supplyDIGITAL UPUTS1000pFTo 0 V or any power supplyInput Low Voltage (V_{L})0.8VInput Low Voltage (V_{L})0.4VOutput Low Voltage (V_{CR})4.0VOutput Low Voltage (V_{CR})4.0VOutput Low Voltage (V_{CR})4.0VOutput Low Voltage (V_{CR})0.4VDiGITAL UPUTS0.4VDidTAL OUTPUTS0.4VDutput Low Voltage (V_{CR})0.4VDidta Low toolage (V_{CR})	Offset Error at 25°C		±6		LSB	V_{OUT} load = 10 M Ω
Bipolar Zero Error at 25°C ± 6 LSB T_{MN} to T_{MAX} ± 12 LSBGain Temperature Coefficient ² ± 1 ppm FSR*CBipolar Zero Error at 25°C ± 1 ppm FSR*COffset Temperature Coefficient ² ± 1 ppm FSR*CBipolar Zero Error emperature Coefficient ² ± 1 ppm FSR*CREFERENCE INPUTInput Resistance20k Ω Resistance from V _{REF+} to V _{REF-} NREF- RangeV _{SS} + 6V _{DD} - 6VVV _{REF-} RangeV _{SS} + 6V _{DD} - 6VVOutput Voltage SwingV _{SS} + 4V _{DD} - 3VVResistince Load2k Ω To 0 VVOutput Voltage SwingV _{SS} + 4V _{DD} - 3VVCapacitive Load2k Ω To 0 VVOutput Voltage (V _H) ± 25 mATo 0 V or any power supplyDIGITAL INPUTS1000pFTo 0 V or any power supplyInput High Voltage (V _H) ± 10 μA Input Capacitance (C _{IN}) ² Input Low Voltage (V _H) ± 10 μA Source current ((source) = 4:0 μA Input Low Voltage (V _{OL}) 0.4 VSink current ((source) = 4:0 μA Output Low Voltage (V _{OL}) 0.4 VSource current ((source) = 4:0 μA Output Low Voltage (V _{OL}) 4.0 μA Do DO EDIGITAL OUTPUTS μA μA Do DUTPUT ((source) = 4:0 μA Output Low Voltage (V _{OL}) μA μA Do DUF = <tr< td=""><td>Τ_{ΜΙΝ} to Τ_{ΜΔΧ}</td><td></td><td></td><td>±16</td><td>LSB</td><td></td></tr<>	Τ _{ΜΙΝ} to Τ _{ΜΔΧ}			±16	LSB	
T_{MM} to T_{MAX} ± 12 LSBGain Temperature Coefficient ² ± 1 ppm FSR/°CBipolar Zero Temperature Coefficient ² ± 1 ppm FSR/°CBipolar Zero Temperature Coefficient ² ± 1 ppm FSR/°CBipolar Zero Temperature Coefficient ² ± 1 ppm FSR/°CInput Resistance20kQResistance from V_{REF+} to V_{REF-} V_{REF+} Range $V_{SS} + 6$ $V_{DD} - 6$ V V_{REF-} Range $V_{SS} + 6$ $V_{DD} - 6$ V Output Voltage Swing $V_{SS} + 4$ $V_{DD} - 3$ V Resistance0.3 Q To 0 VCapacitive Load1000pFTo 0 VOutput Voltage (V_{LA}) ± 25 mATo 0 V or any power supplyDIGTAL INPUTS2.4 V V Input Law Voltage (V_{L}) ± 10 μA Input Capacitance (C_{M}) ² Input Low Voltage (V_{L}) 0.4 V Sink current (I_{SUNRC}) = 1.6 mAOutput Low Voltage (V_{OL}) 0.4 V Source current (I_{SUNRC}) = 400 μA Input Low Voltage (V_{OL}) 0.4 V Source current (I_{SUNRC}) = 400 μA Input Low Voltage (V_{OL}) 0.4 V Source current (I_{SUNRC}) = 1.6 mAOutput High Voltage (V_{OL}) 0.4 V Source current (I_{SUNRC}) = 400 μA Input Low Voltage (V_{OL}) 0.4 V Source current (I_{SUNRC}) = 400 μA Input Low Voltage (V_{OL}) 0.4 V Source current (I_{SUNRC}) = 1.6 mA <tr< td=""><td>Bipolar Zero Error at 25°C</td><td></td><td>±6</td><td></td><td>LSB</td><td></td></tr<>	Bipolar Zero Error at 25°C		±6		LSB	
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Bipolar Zero Temperature Coefficient ² ± 1 ppm FSR/°CREFERENCE INPUT Input Resistance20k Ω Resistance from V _{REF+} to V _{REF+} Typically 30 k Ω V _{REF+} RangeV _{SS} + 6V _{DD} - 6VV _{REF-} RangeV _{SS} + 6V _{DD} - 6VOUTPUT CHARACTERISTICS0VOutput Voltage SwingV _{SS} + 4V _{DD} - 3VResistive Load2K Ω To 0 VCapacitive Load1000pFTo 0 VOutput Voltage Samce0.3 Ω To 0 V or any power supplyDIGITAL INPUTS2.4VVInput Low Voltage (V _H)±10 μ AInput Capacitance (C _{IN}) ² 0.4VDIGITAL OUTPUTS0.4VOutput Voltage (V _{OL})4.0VSource current (Isource) = 400 μ ADigital Leakage Current±10 μ AInput Low Voltage (V _{OL})0.4VDigital Lourput S0.4VDigital Lourput S0.4VDutput State Leakage Current±10 μ AFloating State Leakage Current±10 μ AFloating State Leakage Current±10 μ AFloating State Leakage Current10 μ F	Offset Temperature Coefficient ²		±1		ppm FSR/°C	
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$\begin{array}{ c c c c c c } \mbox{Input Resistance} & 20 & K\Omega & Resistance from V_{REF+} to V_{REF-} \\ & 40 & K\Omega & Typically 30 \ k\Omega & V_{REF-} to V_{REF-} \\ \hline V_{REF-} Range & V_{SS} + 6 & V_{DD} - 6 & V & V \\ \hline OUTPUT CHARACTERISTICS & & & & & & & & & & & & & & & & & & &$	REFERENCE INPUT					
V_{REF} , Range $V_{SS} + 6$ $V_{DD} - 6$ V Typically 30 kΩ V_{REF} , Range $V_{SS} + 6$ $V_{DD} - 6$ V OUTPUT CHARACTERISTICS $V_{SS} + 4$ $V_{DD} - 3$ V Output Voltage Swing $V_{SS} + 4$ $V_{DD} - 3$ V Resistive Load2kΩTo 0 VCapacitive Load1000pFTo 0 VOutput Resistance0.3ΩShort Circuit Current±25mATo 0 V or any power supplyDIGITAL INPUTS2.4VInput High Voltage (V _H)2.4VInput Current (I _N)±10 μ AInput Current (I _N)±10 μ AInput Current (I _N)0.4VSink current (I _{SINK}) = 1.6 mASource current (I _{SOURCE}) = 400 μ AFloating State Leakage Current±10 μ A	Input Resistance	20			kΩ	Resistance from V _{REF+} to V _{REF-}
V_{REF+} Range $V_{SS} + 6$ $V_{DD} - 6$ V V_{REF-} Range $V_{SS} + 6$ $V_{DD} - 6$ V $OUTPUT CHARACTERISTICSV_{SS} + 4V_{DD} - 3VOutput Voltage SwingV_{SS} + 4V_{DD} - 3VResistive Load2k\OmegaTo 0 VCapacitive Load1000pFTo 0 VOutput Resistance0.3\OmegaShort Circuit Current\pm 25DIGITAL INPUTS100PFTo 0 V or any power supplyInput High Voltage (V1L)0.8VInput Current (IN)\pm 10\mu AInput Current (IN)\pm 10\mu AInput Capacitance (CIN)20.4VDIGITAL OUTPUTS0.4VOutput High Voltage (VOL)0.4VOutput High Voltage (VOL)4.0VDIGITAL OUTPUTSUUOutput High Voltage (VOL)UOutput High Voltage (VOL)UUUUUUUUUUUUUUUUUUUUUUUUUUUUU<$	•			40	kΩ	Typically 30 kΩ
NEE Range $V_{SS} + 6$ $V_{DD} - 6$ V OUTPUT CHARACTERISTICS $V_{SS} + 4$ $V_{DD} - 3$ V Qutput Voltage Swing $V_{SS} + 4$ $V_{DD} - 3$ V Resistive Load 2 KΩ To 0 V Capacitive Load 1000 pF To 0 V Output Resistance 0.3 Ω Short Circuit Current ± 25 mA To 0 V or any power supply DIGITAL INPUTS Input High Voltage (V _{IL}) 2.4 V V Input Current (I _N) Input Current (I _N) ± 10 μA Input Current (I _N) E Input Current (I _N) Input Current (I _N) ± 10 μA Input Current (I _N) Input Current (I _N) ± 10 μA Input Capacitance (C _{IN}) ² 1.6 A Source current (I _{SOURCE}) = 4.00 μA Input Current (I _{SOURCE}) = 4.00 μA IDB0 to DB15 = 0 V to V _{CC} DB0 to DB15 = 0 V to V _{CC}	V _{REE+} Range	V _{SS} + 6		V _{DD} – 6	V	
TRUECoDoDoOUTPUT CHARACTERISTICS $V_{SS} + 4$ $V_{DD} - 3$ V Output Voltage Swing 2 $k\Omega$ To 0 VResistive Load21000pFTo 0 VOutput Resistance0.3 Ω Short Circuit Current ± 25 mATo 0 V or any power supplyDIGITAL INPUTS1nput High Voltage (V _H)2.4VVInput Low Voltage (V _H)2.4Input Low Voltage (V _{IL})0.8VInput Current (I _{IN}) ± 10 μA Input Current (I _N) ± 10 μA Source current (I _{SINK}) = 1.6 mADIGITAL OUTPUTS0.4VSource current (I _{SOURCE}) = 400 μA Diding State Leakage Current ± 10 μA DB0 to DB15 = 0 V to V _{CC} Floating State Output Capacitance ² 10 pF DB0 to DB15 = 0 V to V _{CC}	V _{REE} Range	V _{SS} + 6		V _{DD} - 6	V	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	OUTPUT CHARACTERISTICS			00		
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Capacitive LoadImage: Constraint of the	Resistive Load	2			kO	To 0 V
Output Resistance0.3 Ω Short Circuit Current ± 25 mATo 0 V or any power supplyDIGITAL INPUTSInput High Voltage (V _{IH})2.4VInput Low Voltage (V _{IL})0.8VInput Capacitance (C _{IN}) ² 10pFDIGITAL OUTPUTS0.4VOutput High Voltage (V _{OL})0.4VSink current (I _{SUNK}) = 1.6 mAOutput High Voltage (V _{OH})4.0VFloating State Leakage Current ± 10 μA Floating State Qutput Capacitance ² 10 pF	Capacitive Load	_		1000	pF	To 0 V
Short Circuit Current ± 25 mATo 0 V or any power supplyDIGITAL INPUTS Input High Voltage (V _H)2.4VInput Low Voltage (V _H)2.4VInput Current (I _N) ± 10 μA Input Capacitance (C _{IN}) ² 10pFDIGITAL OUTPUTS Output Low Voltage (V _{OL})0.4VSink current (I _{SINK}) = 1.6 mAOutput High Voltage (V _{OL})4.0VSource current (I _{SOURCE}) = 400 μA Floating State Leakage Current Floating State Qutput Capacitance ² 10	Output Resistance		0.3		Ω	
DIGITAL INPUTS2.4VInput High Voltage (V _{IL})2.4VInput Low Voltage (V _{IL})0.8VInput Current (I _{IN}) ± 10 μA Input Capacitance (C _{IN}) ² 10 pF DIGITAL OUTPUTS0.4VOutput High Voltage (V _{OL})0.4VOutput High Voltage (V _{OH})4.0VFloating State Leakage Current ± 10 μA DB0 to DB15 = 0 V to V _{CC} 10	Short Circuit Current		±25		mA	To 0 V or any power supply
Input High Voltage (V _{IH})2.4VInput Low Voltage (V _{IL})0.8VInput Current (I _{IN}) ± 10 μA Input Capacitance (C _{IN}) ² 10pFDIGITAL OUTPUTS0.4VOutput High Voltage (V _{OL})0.4VOutput High Voltage (V _{OH})4.0VFloating State Leakage Current ± 10 μA DB0 to DB15 = 0 V to V _{CC} 10pF	DIGITAL INPUTS					
Input Low Voltage (VIL)0.8VInput Current (IN) ± 10 μA Input Capacitance (CIN) ² 10 pF DIGITAL OUTPUTS0.4VOutput Low Voltage (VOL)0.4VSink current (ISINK) = 1.6 mAOutput High Voltage (VOH)4.0Floating State Leakage Current ± 10 Floating State Output Capacitance ² 10	Input High Voltage (V _{IH})	2.4			V	
Input Current (I _{IN}) ± 10 μA Input Capacitance (C _{IN}) ² 10 pF DIGITAL OUTPUTS 0.4 V Sink current (I _{SINK}) = 1.6 mA Output High Voltage (V _{OL}) 0.4 V Source current (I _{SOURCE}) = 400 μA Floating State Leakage Current ± 10 μA DB0 to DB15 = 0 V to V _{CC} Floating State Output Capacitance ² 10 pF	Input I ow Voltage (V ₁)			0.8	V	
Input Capacitance $(C_{IN})^2$ 10 pF DIGITAL OUTPUTS 0.4 V Sink current $(I_{SINK}) = 1.6 \text{ mA}$ Output Low Voltage (V_{OL}) 0.4 V Source current $(I_{SOURCE}) = 400 \ \mu A$ Floating State Leakage Current ± 10 μA DB0 to DB15 = 0 V to V _{CC} Floating State Output Capacitance ² 10 pF pF	Input Current (Im)			+10	uA	
DIGITAL OUTPUTS 0.4 V Sink current (I _{SINK}) = 1.6 mA Output Low Voltage (V _{OL}) 0.4 V Source current (I _{SOURCE}) = 400 µA Floating State Leakage Current ±10 µA DB0 to DB15 = 0 V to V _{CC} Floating State Output Capacitance ² 10 pF	Input Capacitance $(C_{IN})^2$			10	pF	
Output Low Voltage (V _{OL}) 0.4 V Sink current (I _{SINK}) = 1.6 mA Output High Voltage (V _{OH}) 4.0 V Source current (I _{SOURCE}) = 400 µA Floating State Leakage Current ±10 µA DB0 to DB15 = 0 V to V _{CC} Floating State Output Capacitance ² 10 pF						
Output High Voltage (V_{OH})4.0VSource current (I_{SOURCE}) = 400 µAFloating State Leakage Current±10µADB0 to DB15 = 0 V to V _{CC} Floating State Output Capacitance ² 10pF	Output Low Voltage (Vol.)			0.4	V	Sink current (Ising) = 1.6 mA
Floating State Leakage Current ±10 μA DB0 to DB15 = 0 V to V _{CC} Floating State Output Capacitance ² 10 νF	Output High Voltage (Volt)	4.0		•••	v	Source current (Isource) = 400 IIA
Floating State Output Capacitance ²	Floating State Leakage Current			+10	uA	DB0 to DB15 = 0 V to V_{co}
	Floating State Output Capacitance ²			10	pF	

Table 1. Specifications (Continued)

Parameter ¹	Min	Тур	Мах	Unit	Test Conditions/Comments
POWER REQUIREMENTS ³					
V _{DD}	+11.4		+15.75	V	
V _{SS}	-11.4		-15.75	V	
V _{CC}	+4.75		+5.25	V	
V _{DD} Current (I _{DD})			5	mA	V _{OUT} unloaded
V _{SS} Current (I _{SS})			5	mA	V _{OUT} unloaded
V _{CC} Current (I _{CC})			1	mA	
Power Supply Sensitivity ⁴			1.5	LSB/V	
Power Dissipation		100		mW	V _{OUT} unloaded

¹ Temperature range is-40°C to +105°C.

² Guaranteed by design and characterization, not production tested.

³ The AD7846-CHIPS is functional with power supplies of ±12 V. See the Typical Performance Characteristics section in the AD7846 data sheet.

 4 $\,$ Sensitivity of gain error, offset error, and bipolar zero error to V_{DD} and V_{SS} variations.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance and are not subject to test. $V_{REF+} = +5 V$, $V_{DD} = +14.25 V$ to +15.75 V, $V_{SS} = -14.25 V$ to -15.75 V, $V_{CC} = +4.75 V$ to +5.25 V, and R_{IN} connected to 0 V, unless otherwise noted. The minimum, typical, and maximum values are the limits at T_{MIN} to T_{MAX} .

Table 2. AC Performance Characteristics

Parameter	Min	Тур	Max	Unit	Test Conditions/Comments
Output Settling Time ¹			6	μs	To 0.006% FSR, V _{OUT} loaded, V _{REF} = 0 V, typically 3.5 μ s
			9	μs	To 0.003% FSR, V _{OUT} loaded, V _{REF-} = –5 V, typically 6.5 μ s
Slew Rate		7		V/µs	
Digital-to-Analog Glitch					
Impulse		70		nV-sec	DAC alternately loaded with 10 0000 and 01 1111, V_{OUT} unloaded
AC Feedthrough		0.5		mV p-p	$V_{\text{REF-}}$ = 0 V, $V_{\text{REF+}}$ = 1 V RMS, 10 kHz sine wave, DAC loaded with all 0s
Digital Feedthrough		10		nV-sec	DAC alternately loaded with all 1s and all 0s, $\overline{\text{CS}}$ high
Output Noise Voltage Density, 1 kHz to 100 kHz		50		nV/√Hz	Measured at V _{OUT} , DAC loaded with 0111011 11, V _{REF+} = V _{REF-} = 0 V

¹ LDAC = 0. Settling time does not include deglitching time of 2.5 µs (typ).

TIMING CHARACTERISTICS

 V_{DD} = +14.25 V to +15.75 V, V_{SS} = -14.25 V to -15.75 V, and V_{CC} = +4.75 V to +5.25 V, unless otherwise noted. The minimum, typical, and maximum value limits are T_{MIN} to T_{MAX} .

Parameter ¹	Min	Тур	Max	Unit	Test Conditions/Comments	
t ₁	0			ns	R/\overline{W} to \overline{CS} setup time	
t ₂	60			ns	CS pulse width (write cycle)	
t ₃	0			ns	R/\overline{W} to \overline{CS} hold time	
t ₄	60			ns	Data setup time	
t ₅	0			ns	Data hold time	
t ₆ ²			120	ns	Data access time	
t ₇ ³	10			ns	Bus relinquish time	
			60	ns		
t ₈	0			ns	CLR setup time	
t ₉	70			ns	CLR pulse width	
t ₁₀	0			ns	CLR hold time	
t ₁₁	70			ns	LDAC pulse width	
t ₁₂	130			ns	CS pulse width (read cycle)	

¹ Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

² t₆ is measured with the load circuits of Figure 3 and Figure 4 and defined as the time required for an output to cross 0.8 V or 2.4 V.

³ t₇ is defined as the time required for an output to change 0.5 V when loaded with the circuits of Figure 5 and Figure 6.

Timing Diagrams



Figure 2. Timing Diagram





Figure 4. Load Circuits for Bus Relinquish Time (t_6)—High Z to V_{OL}

$$DBx \circ \underbrace{ \begin{array}{c} \bullet \\ & &$$

Figure 5. Load Circuit for Access Time (t_7)—High Z to V_{OH}

305



Figure 6. Load Circuits for Bus Relinquish Time (t7)—High Z to VOL

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
V _{DD} to DGND	-0.4 V to +17 V
V _{CC} to DGND	-0.4 V, V _{DD} + 0.4 V, or +7 V (whichever is
	lower)
V _{SS} to DGND	+0.4 V to -17 V
V _{REF+} to DGND	V _{DD} + 0.4 V, V _{SS} - 0.4 V
V _{REF-} to DGND	V _{DD} + 0.4 V, V _{SS} - 0.4 V
V _{OUT} to DGND ¹	V_{DD} + 0.4 V, V_{SS} – 0.4 V, or ±10 V (whichever is
	lower)
R _{IN} to DGND	V _{DD} + 0.4 V, V _{SS} - 0.4 V
Digital Input Voltage to DGND	-0.4 V to V _{CC} + 0.4 V
Digital Output Voltage to DGND	-0.4 V to V _{CC} + 0.4 V
Power Dissipation	
To 75°C	1000 mW
Derates Above 75°C	10 mW/°C
Temperature	
Operating Range	-40°C to +105°C
Storage Range	-65°C to +150°C

¹ V_{OUT} can be shorted to DGND, V_{DD}, V_{SS}, or V_{CC} provided that the power dissipation of the die is not exceeded.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES 1. NC = NO CONNECT. PROBE PAD. DO NOT CONNECT TO THIS PAD.



200

Table 5. Pad Function Descriptions

Ded No.	Mnomonio	Pod Tyrpo	V Avia	V Avia	Decarintian
Pau No.	whemonic	Pau Type	X-AXIS	T-AXIS	Description
1	DB2	Single	+158	+1759	Data Input and Output.
2	DB1	Single	-240	+1759	Data Input and Output.
3	DB0	Single	-735	+1825	Data Input and Output, LSB.
4A	N	Daubla	-1335	+1812	Depitive Supply for the Apples Circuits, 15 V Neminal
4B	VDD	Double	-1515	+1812	
5	V _{OUT}	Single	-1675	+1631	DAC Output.
6	R _{IN}	Single	-1675	+901	Input to Summing Resistor of the DAC Output Amplifier. R _{IN} is used to select the output voltage ranges.
7A		Daubla	-1617	+312	
7B	V _{REF+}	Double	-1617	+132	VREF+ Input. The DAC is specified for VREF+ = 5 V.
8A		Dauble	-1617	-56	
8B	V _{REF} -	Double	-1617	-236	VREF- Input. For unipolar operation, connect VREF- to UV, and for bipolar operation, connect it to -5 V.
9	V _{SS}	Single	-1676	-738	Negative Supply for the Analog Circuitry, -15 V Nominal.
10	DB15	Single	-1662	-1223	Data Input and Output, MSB.
11	DB14	Single	-1662	-1624	Data Input and Output.
12	DB13	Single	-1223	-1756	Data Input and Output.
13	DB12	Single	-821	-1756	Data Input and Output.
14	DB11	Single	-124	-1756	Data Input and Output.
15	DB10	Single	+270	-1756	Data Input and Output.
16	DB9	Single	+744	-1758	Data Input and Output.
17	DB8	Single	+1118	-1758	Data Input and Output.
18	DB7	Single	+1541	-1767	Data Input and Output.
19	DB6	Single	+1660	-1347	Data Input and Output.
20	DGND	Single	+1613	-883	Ground for the Digital Circuitry.
21	Vcc	Single	+1645	-333	Positive Supply for the Digital Circuitry, 5 V Nominal.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pad Function Descriptions (Continued)

Pad No.	Mnemonic	Pad Type	X-Axis	Y-Axis	Description
22	R/W	Single	+1674	+283	R/W Input. This pin can be used to load data to the DAC or to read back the DAC latch contents.
23	CS	Single	+1676	+643	Chip Select Input. This pin selects the device.
24	CLR	Single	+1676	+1329	Clear Input. The DAC can be cleared to 000000 or 100000.
25	LDAC	Single	+1654	1720	Asynchronous Load Input to the DAC.
26	DB5	Single	+1256	+1747	Data Input and Output.
27	DB4	Single	+907	+1747	Data Input and Output.
28	DB3	Single	+573	+1747	Data Input and Output.
N/A	NC	Single	+675	+1409	Probe pad. Do not connect to this pad.
N/A	NC	Single	-725	-908	Probe pad. Do not connect to this pad.
N/A	NC	Single	-1048.5	+1809.4	Probe pad. Do not connect to this pad.
N/A	NC	Single	-1174.5	+1809.4	Probe pad. Do not connect to this pad.
N/A	NC	Single	-1669	-464.9	Probe pad. Do not connect to this pad.
N/A	NC	Single	-515	-1803.9	Probe pad. Do not connect to this pad.
N/A	NC	Single	+1675	+846.5	Probe pad. Do not connect to this pad.
N/A	NC	Single	+1675.4	+1021	Probe pad. Do not connect to this pad.

Table 6. Output Voltage Ranges

Output Range (V)	V _{REF+} (V)	V _{REF-} (V)	R _{IN} (V)
0 to +5	+5	0	V _{OUT}
0 to +10	+5	0	0
+5 to -5	+5	-5 V	V _{OUT}
+5 to -5	+5	0	+5
+10 to -10	+5	-5	0

OUTLINE DIMENSIONS



Figure 8. 28-Pad Bare Die [CHIP] (C-28-3) Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 7. Die Specifications

Parameter	Value	Unit
Die Size	3820 × 4070	μm (maximum)
Thickness	300	μm (typical)
Bond Pad	92 × 92	μm (typical)
Minimum Bond Pad Pitch	180	μm
Bond Pad Composition	Aluminum (AI)/1.0 Silicon (Si)/0.5 Copper (Cu)	%

Table 8. Assembly Recommendations

Assembly Component	Recommendation			
Die Attach	Epoxy dispense			
Bonding Method	Thermosonic gold ball bonding			
Bonding Sequence	Bond Pad 20 (DGND) first			

12-12-2023-A

OUTLINE DIMENSIONS

Updated: January 18, 2024

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD7846-CHIPS	-40°C to +105°C	CHIPS OR DIE	C-28-3

¹ The AD7846-CHIPS is a RoHS compliant part.

