Data Sheet

AD7846-CHIPS

LC2MOS 16-Bit Voltage Output DAC

FEATURES

- 16-bit monotonicity over temperature
- Microprocessor compatible with read-back capability
- Unipolar or bipolar output
- Multiplying capability
- Low power dissipation: 100 mW typical

APPLICATIONS

- Instrumentation
- Automatic test equipment
- Industrial automation
- Energy grid systems
- Aerospace

GENERAL DESCRIPTION

The AD7846-CHIPS is a 16-bit digital-to-analog converter (DAC) constructed with the Analog Devices, Inc., LC^{2}MOS process. The device has V_{REF+} and V_{REF-} reference inputs and an on-chip output amplifier that can be configured to give a unipolar output range (0 V to +5 V or 0 V to +10 V) or bipolar output ranges (±5 V or ±10 V).

The DAC uses a segmented architecture. The four MSBs in the DAC latch select one of the segments in a 16-resistor string. Both taps of the segment are buffered by amplifiers and fed to a 12-bit DAC, which provides a further 12 bits of resolution. This architecture ensures 16-bit monotonicity. Excellent integral linearity results from tight matching between the input offset voltages of the two buffer amplifiers.

In addition to the excellent accuracy specifications, the AD7846-CHIPS also offers a comprehensive microprocessor interface. There are 16 data input and output pins, plus control lines ($\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$, and $\overline{CLR}$). R/$\overline{W}$ and $\overline{CS}$ allow writing to and reading from the input and output latch, and this read-back function is useful in ATE applications. $\overline{LDAC}$ allows simultaneous updating of DACs in a multiDAC system, and the $\overline{CLR}$ line resets the contents of the DAC latch to 00 … 000 or 10 … 000 depending on the state of R/$\overline{W}$, which means that the DAC output can be reset to 0 V in both unipolar and bipolar configurations.

Additional application and technical information can be found in the AD7846 data sheet.

PRODUCT HIGHLIGHTS

1. 16-Bit Monotonicity. The guaranteed 16-bit monotonicity over temperature makes the AD7846-CHIPS ideal for closed-loop applications.
2. Readback. The ability to read back the DAC register contents minimizes software routines when the AD7846-CHIPS is used in automatic test equipment systems.
3. Power Dissipation. A power dissipation of 100 mW makes the AD7846-CHIPS a low power, high accuracy DAC.

FUNCTIONAL BLOCK DIAGRAM

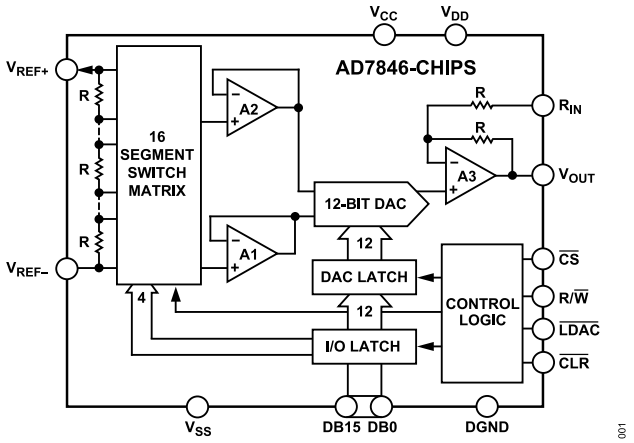

Figure 1. Functional Block Diagram

Rev. A

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

1/2024—Rev. 0 to Rev. A

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11/2023—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = +14.25 V to +15.75 V, V_{SS} = −14.25 V to –15.75 V, and V_{CC} = +4.75 V to +5.25 V. V_{OUT} loaded with 2 kΩ, 1000 pF to 0 V, V_{REF+} = +5 V, and R_{IN} connected to 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1. Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
RESOLUTION		16		Bits	
UNIPOLAR OUTPUT					V_{REF-} = 0 V, V_{OUT} = 0 V to +10 V
Relative Accuracy at 25°C		±12		LSB	1 LSB = 153 µV
T_{MIN} to T_{MAX}			±16	LSB	
Differential Nonlinearity Error			±1	LSB	All grades guaranteed monotonic
Gain Error at 25°C		±12		LSB	V_{OUT} load = 10 MΩ
T_{MIN} to T_{MAX}			±16	LSB	
Offset Error at 25°C		±12		LSB	
T_{MIN} to T_{MAX}			±16	LSB	
Gain Temperature Coefficient[2]		±1		ppm FSR/°C	
Offset Temperature Coefficient[2]		±1		ppm FSR/°C	
BIPOLAR OUTPUT					V_{REF-} = –5 V, V_{OUT} = −10 V to +10 V
Relative Accuracy at 25°C		±6		LSB	1 LSB = 305 µV
T_{MIN} to T_{MAX}			±8	LSB	
Differential Nonlinearity Error			±1	LSB	All grades guaranteed monotonic
Gain Error at 25°C		±6		LSB	V_{OUT} load = 10 MΩ
T_{MIN} to T_{MAX}			±16	LSB	
Offset Error at 25°C		±6		LSB	V_{OUT} load = 10 MΩ
T_{MIN} to T_{MAX}			±16	LSB	
Bipolar Zero Error at 25°C		±6		LSB	
T_{MIN} to T_{MAX}			±12	LSB	
Gain Temperature Coefficient[2]		±1		ppm FSR/°C	
Offset Temperature Coefficient[2]		±1		ppm FSR/°C	
Bipolar Zero Temperature Coefficient[2]		±1		ppm FSR/°C	
REFERENCE INPUT					
Input Resistance	20			kΩ	Resistance from V_{REF+} to V_{REF-}
			40	kΩ	Typically 30 kΩ
V_{REF+} Range	V_{SS} + 6		V_{DD} − 6	V	
V_{REF-} Range	V_{SS} + 6		V_{DD} − 6	V	
OUTPUT CHARACTERISTICS					
Output Voltage Swing	V_{SS} + 4		V_{DD} − 3	V	
Resistive Load	2			kΩ	To 0 V
Capacitive Load			1000	pF	To 0 V
Output Resistance		0.3		Ω	
Short Circuit Current		±25		mA	To 0 V or any power supply
DIGITAL INPUTS					
Input High Voltage (V_{IH})	2.4			V	
Input Low Voltage (V_{IL})			0.8	V	
Input Current (I_{IN})			±10	µA	
Input Capacitance (C_{IN})[2]			10	pF	
DIGITAL OUTPUTS					
Output Low Voltage (V_{OL})			0.4	V	Sink current (I_{SINK}) = 1.6 mA
Output High Voltage (V_{OH})	4.0			V	Source current (I_{SOURCE}) = 400 µA
Floating State Leakage Current			±10	µA	DB0 to DB15 = 0 V to V_{CC}
Floating State Output Capacitance[2]			10	pF	

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS[3]					
V_{DD}	+11.4		+15.75	V	
V_{SS}	−11.4		−15.75	V	
V_{CC}	+4.75		+5.25	V	
V_{DD} Current (I_{DD})			5	mA	V_{OUT} unloaded
V_{SS} Current (I_{SS})			5	mA	V_{OUT} unloaded
V_{CC} Current (I_{CC})			1	mA	
Power Supply Sensitivity[4]			1.5	LSB/V	
Power Dissipation		100		mW	V_{OUT} unloaded

1 Temperature range is−40°C to +105°C.

2 Guaranteed by design and characterization, not production tested.

3 The AD7846-CHIPS is functional with power supplies of ±12 V. See the Typical Performance Characteristics section in the AD7846 data sheet.

4 Sensitivity of gain error, offset error, and bipolar zero error to V_{DD} and V_{SS} variations.

SPECIFICATIONS

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance and are not subject to test. V_{REF+} = +5 V, V_{DD} = +14.25 V to +15.75 V, V_{SS} = −14.25 V to −15.75 V, V_{CC} = +4.75 V to +5.25 V, and R_{IN} connected to 0 V, unless otherwise noted. The minimum, typical, and maximum values are the limits at T_{MIN} to T_{MAX}.

Table 2. AC Performance Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Settling Time[1]			6	µs	To 0.006% FSR, V_{OUT} loaded, V_{REF-} = 0 V, typically 3.5 µs
			9	µs	To 0.003% FSR, V_{OUT} loaded, V_{REF-} = –5 V, typically 6.5 µs
Slew Rate		7		V/µs	
Digital-to-Analog Glitch					
Impulse		70		nV-sec	DAC alternately loaded with 10 … 0000 and 01 … 1111, V_{OUT} unloaded
AC Feedthrough		0.5		mV p-p	V_{REF-} = 0 V, V_{REF+} = 1 V RMS, 10 kHz sine wave, DAC loaded with all 0s
Digital Feedthrough		10		nV-sec	DAC alternately loaded with all 1s and all 0s, $\overline{CS}$ high
Output Noise Voltage Density, 1 kHz to 100 kHz		50		nV/√Hz	Measured at V_{OUT}, DAC loaded with 0111011 … 11, V_{REF+} = V_{REF-} = 0 V

[1] $\overline{LDAC}$ = 0. Settling time does not include deglitching time of 2.5 µs (typ).

TIMING CHARACTERISTICS

V_{DD} = +14.25 V to +15.75 V, V_{SS} = −14.25 V to −15.75 V, and V_{CC} = +4.75 V to +5.25 V, unless otherwise noted. The minimum, typical, and maximum value limits are T_{MIN} to T_{MAX}.

Table 3. Timing Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
t_1	0			ns	R/$\overline{W}$ to $\overline{CS}$ setup time
t_2	60			ns	$\overline{CS}$ pulse width (write cycle)
t_3	0			ns	R/$\overline{W}$ to $\overline{CS}$ hold time
t_4	60			ns	Data setup time
t_5	0			ns	Data hold time
t_6[2]			120	ns	Data access time
t_7[3]	10			ns	Bus relinquish time
			60	ns	
t_8	0			ns	$\overline{CLR}$ setup time
t_9	70			ns	$\overline{CLR}$ pulse width
t_{10}	0			ns	$\overline{CLR}$ hold time
t_{11}	70			ns	$\overline{LDAC}$ pulse width
t_{12}	130			ns	$\overline{CS}$ pulse width (read cycle)

[1] Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2] t_6 is measured with the load circuits of Figure 3 and Figure 4 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3] t_7 is defined as the time required for an output to change 0.5 V when loaded with the circuits of Figure 5 and Figure 6.

SPECIFICATIONS

Timing Diagrams

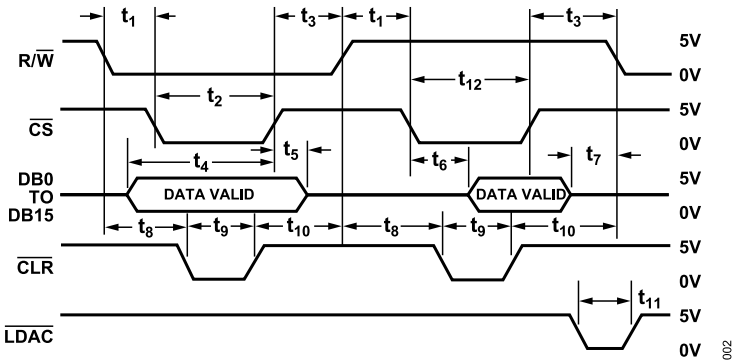

Figure 2. Timing Diagram

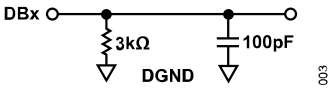

Figure 3. Load Circuit for Access Time (t_6)—High Z to V_{OH}

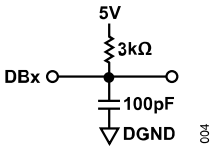

Figure 4. Load Circuits for Bus Relinquish Time (t_6)—High Z to V_{OL}

Figure 5. Load Circuit for Access Time (t_7)—High Z to V_{OH}

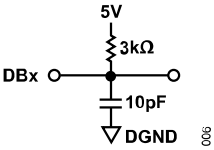

Figure 6. Load Circuits for Bus Relinquish Time (t_7)—High Z to V_{OL}

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
V_{DD} to DGND	−0.4 V to +17 V
V_{CC} to DGND	−0.4 V, V_{DD} + 0.4 V, or +7 V (whichever is lower)
V_{SS} to DGND	+0.4 V to −17 V
V_{REF+} to DGND	V_{DD} + 0.4 V, V_{SS} − 0.4 V
V_{REF-} to DGND	V_{DD} + 0.4 V, V_{SS} − 0.4 V
V_{OUT} to DGND[1]	V_{DD} + 0.4 V, V_{SS} − 0.4 V, or ±10 V (whichever is lower)
R_{IN} to DGND	V_{DD} + 0.4 V, V_{SS} − 0.4 V
Digital Input Voltage to DGND	−0.4 V to V_{CC} + 0.4 V
Digital Output Voltage to DGND	−0.4 V to V_{CC} + 0.4 V
Power Dissipation	
To 75°C	1000 mW
Derates Above 75°C	10 mW/°C
Temperature	
Operating Range	−40°C to +105°C
Storage Range	−65°C to +150°C

[1] V_{OUT} can be shorted to DGND, V_{DD}, V_{SS}, or V_{CC} provided that the power dissipation of the die is not exceeded.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

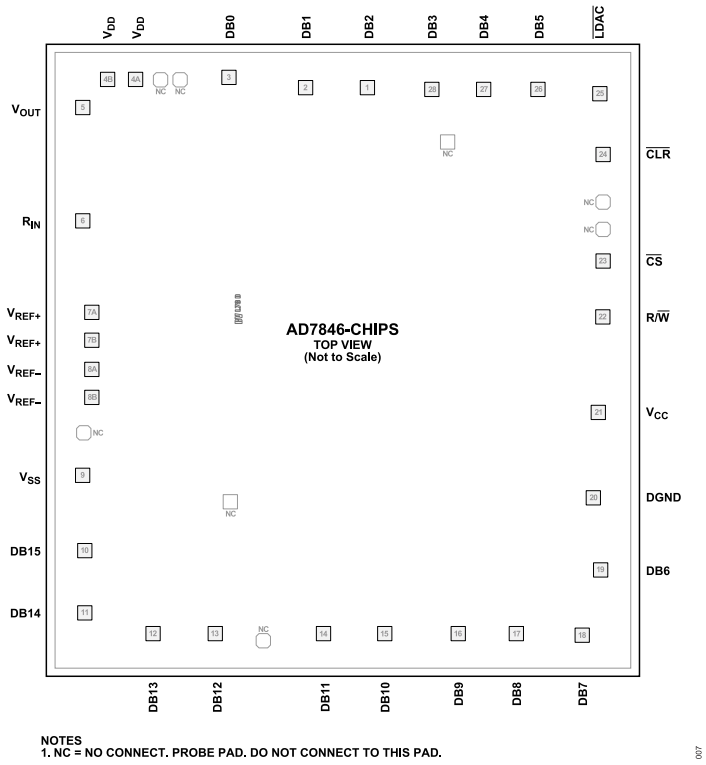

Figure 7. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	Mnemonic	Pad Type	X-Axis	Y-Axis	Description
1	DB2	Single	+158	+1759	Data Input and Output.
2	DB1	Single	−240	+1759	Data Input and Output.
3	DB0	Single	−735	+1825	Data Input and Output, LSB.
4A	V_{DD}	Double	−1335	+1812	Positive Supply for the Analog Circuitry, 15 V Nominal.
4B			−1515	+1812	
5	V_{OUT}	Single	−1675	+1631	DAC Output.
6	R_{IN}	Single	−1675	+901	Input to Summing Resistor of the DAC Output Amplifier. R_{IN} is used to select the output voltage ranges.
7A	V_{REF+}	Double	−1617	+312	VREF+ Input. The DAC is specified for VREF+ = 5 V.
7B			−1617	+132	
8A	V_{REF-}	Double	−1617	−56	VREF− Input. For unipolar operation, connect VREF− to 0 V, and for bipolar operation, connect it to −5 V.
8B			−1617	−236	
9	V_{SS}	Single	−1676	−738	Negative Supply for the Analog Circuitry, −15 V Nominal.
10	DB15	Single	−1662	−1223	Data Input and Output, MSB.
11	DB14	Single	−1662	−1624	Data Input and Output.
12	DB13	Single	−1223	−1756	Data Input and Output.
13	DB12	Single	−821	−1756	Data Input and Output.
14	DB11	Single	−124	−1756	Data Input and Output.
15	DB10	Single	+270	−1756	Data Input and Output.
16	DB9	Single	+744	−1758	Data Input and Output.
17	DB8	Single	+1118	−1758	Data Input and Output.
18	DB7	Single	+1541	−1767	Data Input and Output.
19	DB6	Single	+1660	−1347	Data Input and Output.
20	DGND	Single	+1613	−883	Ground for the Digital Circuitry.
21	V_{CC}	Single	+1645	−333	Positive Supply for the Digital Circuitry, 5 V Nominal.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pad Function Descriptions (Continued)

Pad No.	Mnemonic	Pad Type	X-Axis	Y-Axis	Description
22	R/$\overline{W}$	Single	+1674	+283	R/$\overline{W}$ Input. This pin can be used to load data to the DAC or to read back the DAC latch contents.
23	$\overline{CS}$	Single	+1676	+643	Chip Select Input. This pin selects the device.
24	$\overline{CLR}$	Single	+1676	+1329	Clear Input. The DAC can be cleared to 000…000 or 100…000.
25	$\overline{LDAC}$	Single	+1654	1720	Asynchronous Load Input to the DAC.
26	DB5	Single	+1256	+1747	Data Input and Output.
27	DB4	Single	+907	+1747	Data Input and Output.
28	DB3	Single	+573	+1747	Data Input and Output.
N/A	NC	Single	+675	+1409	Probe pad. Do not connect to this pad.
N/A	NC	Single	−725	−908	Probe pad. Do not connect to this pad.
N/A	NC	Single	−1048.5	+1809.4	Probe pad. Do not connect to this pad.
N/A	NC	Single	−1174.5	+1809.4	Probe pad. Do not connect to this pad.
N/A	NC	Single	−1669	−464.9	Probe pad. Do not connect to this pad.
N/A	NC	Single	−515	−1803.9	Probe pad. Do not connect to this pad.
N/A	NC	Single	+1675	+846.5	Probe pad. Do not connect to this pad.
N/A	NC	Single	+1675.4	+1021	Probe pad. Do not connect to this pad.

Table 6. Output Voltage Ranges

Output Range (V)	V_{REF+} (V)	V_{REF-} (V)	R_{IN} (V)
0 to +5	+5	0	V_{OUT}
0 to +10	+5	0	0
+5 to −5	+5	−5 V	V_{OUT}
+5 to −5	+5	0	+5
+10 to −10	+5	−5	0

OUTLINE DIMENSIONS

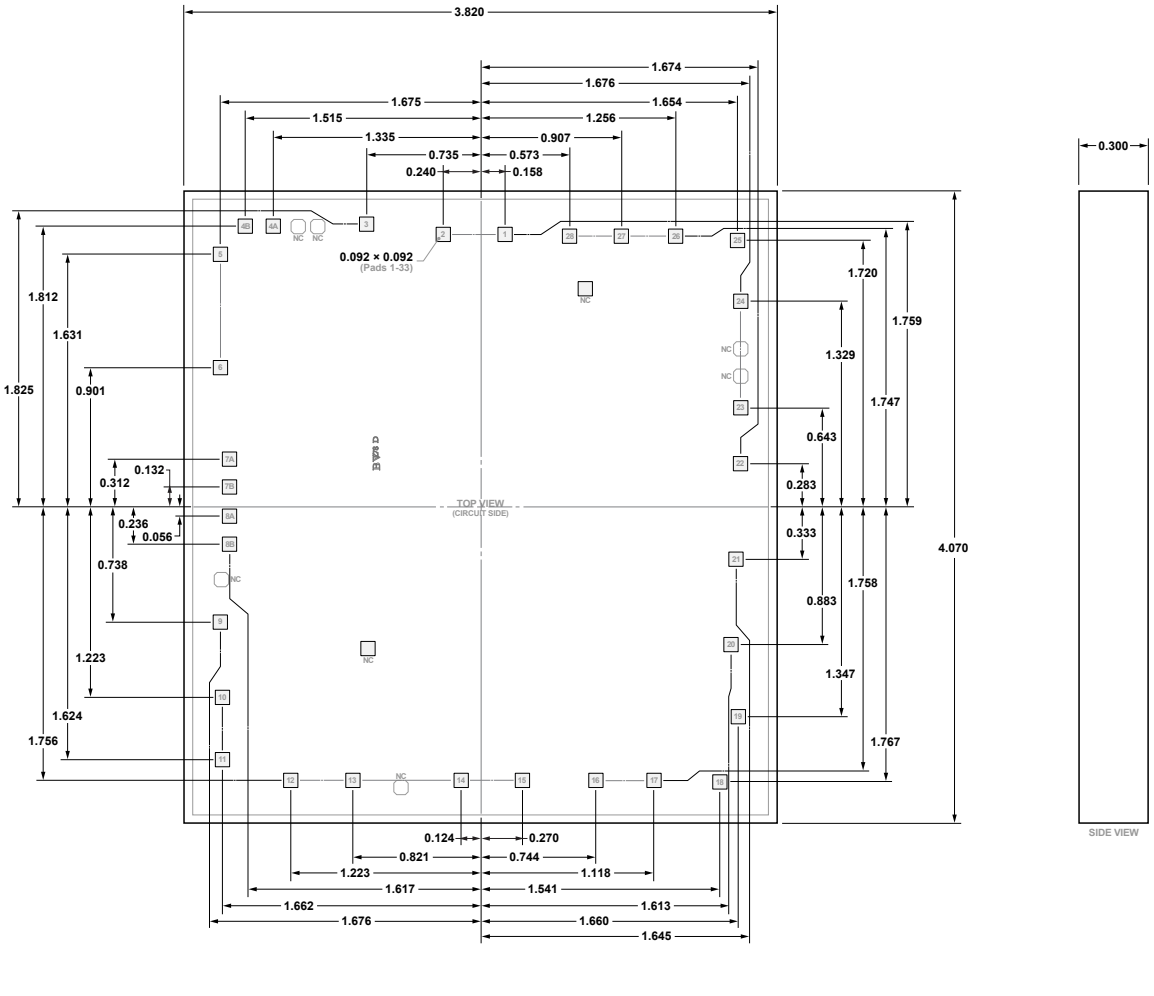

Figure 8. 28-Pad Bare Die [CHIP]
(C-28-3)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 7. Die Specifications

Parameter	Value	Unit
Die Size	3820 × 4070	µm (maximum)
Thickness	300	µm (typical)
Bond Pad	92 × 92	µm (typical)
Minimum Bond Pad Pitch	180	µm
Bond Pad Composition	Aluminum (Al)/1.0 Silicon (Si)/0.5 Copper (Cu)	%

Table 8. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy dispense
Bonding Method	Thermosonic gold ball bonding
Bonding Sequence	Bond Pad 20 (DGND) first

OUTLINE DIMENSIONS

Updated: January 18, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7846-CHIPS	-40°C to +105°C	CHIPS OR DIE	C-28-3

[1] The AD7846-CHIPS is a RoHS compliant part.