2x15W Stereo / 1x30W Mono Digital Audio Amplifier

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR (A-weighting)
  Loudspeaker: 97dB (PSNR), 105dB (DR) @24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x, 1024x Fs
  256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz/176.4kHz/192kHz
- Supply voltage
  3.3V for digital circuit
  10V~26V for loudspeaker driver
- Loudspeaker output power for 24V
  10W x 2CH into 8Ω @0.27% THD+N for stereo
  15W x 2CH into 8Ω @0.35% THD+N for stereo
  20W x 1CH into 4Ω @0.25% THD+N for mono
  30W x 1CH into 4Ω @0.32% THD+N for mono
- Anti-pop design
- Over-temperature protection
- Internal PLL
- Under-voltage shutdown
- Over-current protection
- I^2C control interface
- Zero detection
- Power limit function
- Quaternary and ternary switch

Applications

- CD and DVD
- LCD TV
- Car audio
- Boom-box
- MP3 docking systems
- Powered speaker
- Wireless audio
- USB speaker

Description

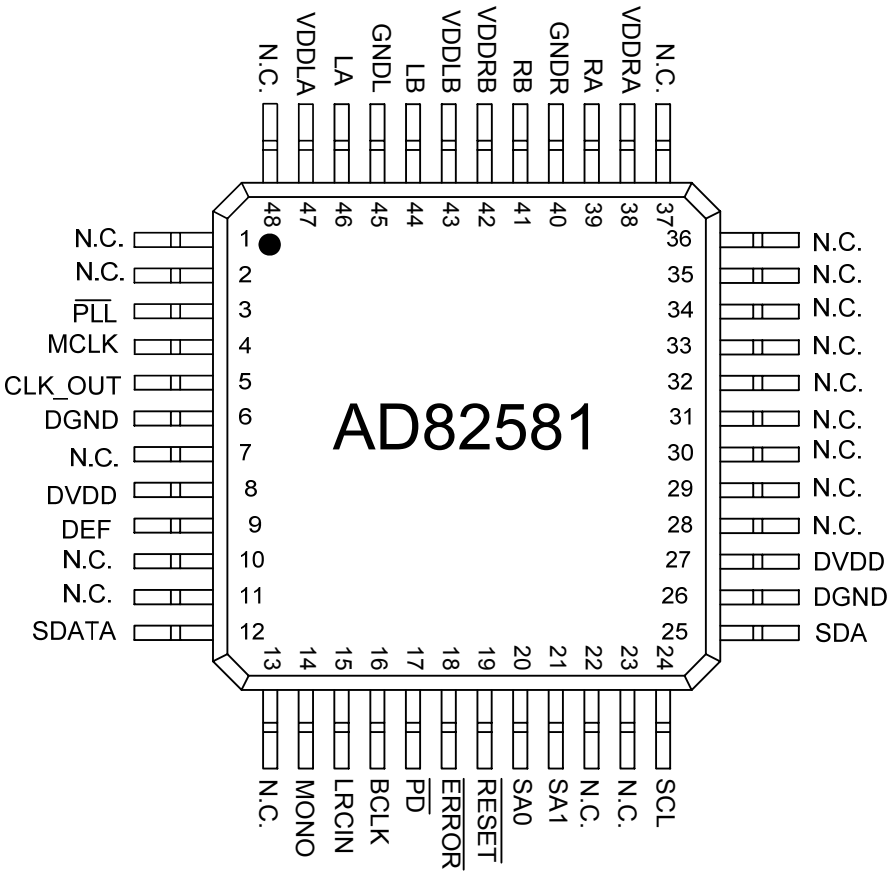
AD82581 is a digital audio amplifier capable of driving a pair of 8 Ω,15W or a single 4 Ω,30W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control AD82581's input format selection, mute and volume control functions. AD82581 has many built-in protection circuits to safeguard AD82581 from connection errors.

ORDERING INFORMATION

Product ID	Package	Packing / MPQ	Comments
AD82581-LE48NAY	E-LQFP-48L 7x7 mm	2.5K Units / Small Box (250 Units / Tray, 10 Trays / Small Box	Green

Pin Assignment



Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	N.C.	NC		
2	N.C.	NC		
3	$\overline{PLL}$	I	PLL enable, low active	Schmitt trigger TTL input buffer
4	MCLK	I	Master clock input	Schmitt trigger TTL input buffer
5	CLK_OUT	O	Clock output from PLL	TTL output buffer
6	DGND	P	Digital Ground	
7	N.C.	NC		
8	DVDD	P	Digital Power	
9	DEF	I	Default volume setting	Schmitt trigger TTL input buffer
10	N.C.	NC		
11	N.C.	NC		
12	SDATA	I	Serial audio data input	Schmitt trigger TTL input buffer
13	N.C.	NC		
14	MONO	I	MONO mode enable, high active	Schmitt trigger TTL input buffer

15	LRCIN	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer
16	BCLK	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer
17	$\overline{PD}$	I	Power down, low active	Schmitt trigger TTL input buffer
18	$\overline{ERROR}$	O	Error status, low active	Open-drain output
19	$\overline{RESET}$	I	Reset, low active	Schmitt trigger TTL input buffer
20	SA0	I	I^2C select address 0	Schmitt trigger TTL input buffer
21	SA1	I	I^2C select address 1	Schmitt trigger TTL input buffer
22	N.C.	NC		
23	N.C.	NC		
24	SCL	I	I^2C serial clock input	Schmitt trigger TTL input buffer
25	SDA	I/O	I^2C bi-directional serial data	Schmitt trigger TTL input buffer
26	DGND	P	Digital Ground	
27	DVDD	P	Digital Power	
28	N.C.	NC		
29	N.C.	NC		
30	N.C.	NC		
31	N.C.	NC		
32	N.C.	NC		
33	N.C.	NC		
34	N.C.	NC		
35	N.C.	NC		
36	N.C.	NC		
37	N.C.	NC		
38	VDDRA	P	Right channel supply A	
39	RA	O	Right channel output A	
40	GNDR	P	Right channel ground	
41	RB	O	Right channel output B	
42	VDDRB	P	Right channel supply B	
43	VDDLB	P	Left channel supply B	
44	LB	O	Left channel output B	
45	GNDL	P	Left channel ground	
46	LA	O	Left channel output A	
47	VDDLA	P	Left channel supply A	
48	N.C.	NC		