2x20W Stereo / 1x40W Mono Class-D Audio Amplifier With Power Limit Control

Features

- Single supply voltage
  4.5 ~ 26V for loudspeaker driver
- Input digital audio interface
- Sampling frequency: 32kHz, 44.1kHz and 48kHz
- Left-justified, MSB first, 1-bit delay with digital audio data 24-bits
- Loudspeaker power @ 24V supply
  15W / CH with 8Ω < 0.5% THD+N
- Efficiency 87% (PVDD=24V, RL=8Ω, Po=10W)
- Distortion ration (THD+N) < 0.1% @ Po=7.5W
- PSNR ratio 99dB (PVDD=24V)
- Residual noise 130uVrms (A-weighted filter)
- Channel separation > 90 dB
- Power limit function
- Gain setting function
- Stereo/Mono switching function
- Output mute function (Quick mute / Quick start)
- Sleep function
- Pop noise reduction function
- Over current protection function (OCP)
- Over voltage protection function (OVP)
- Over temperature protection function (OTP)
- Under voltage lockout (UVLO)
- DC detection function (DCDET)
- Clock detection function (CKDET)
- Package available in both of QFN-32L and E-TSSOP-24L

Applications

- TV audio
- Boom-Box
- Powered speaker
- Consumer Audio Equipment

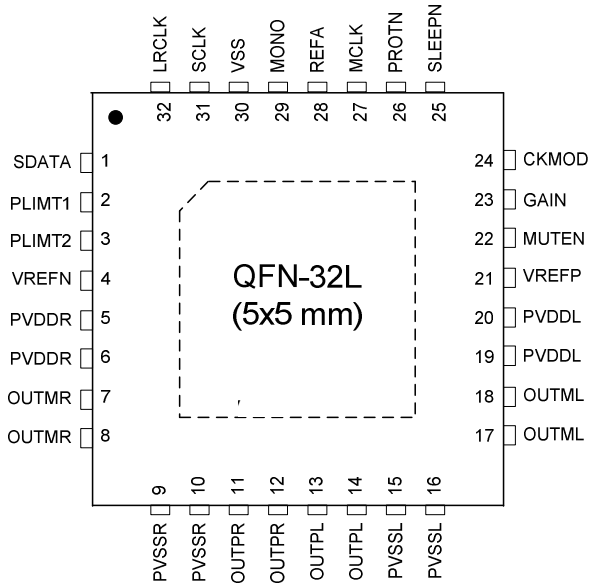
Description

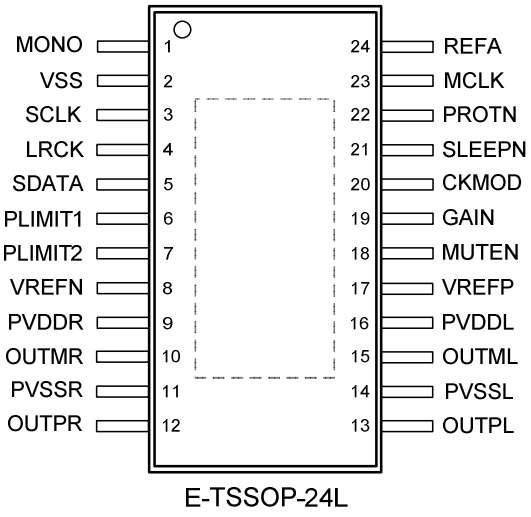
AD82583 is a high-performance digital audio amplifier IC that delivers up to 20W×2ch, which has a digital audio interface, and is capable of operating at a supply voltage ranging from 4.5V to 26V.

AD82583 allows a speaker to be directly connected to the output. In addition, this amplifier is insusceptible to supply voltage fluctuation because of a feedback-type digital amplifier, and have the feature with high power supply noise tolerance. As a result, power supply can be simplified and allowing a simple amplifier system with less external components to be configured.

AD82583 has the following functions: gain setting function, power limit function, pop noise reduction function, over current protection function for speaker output pins, internal over temperature protection function, under voltage lockout, and DC detection function.

Pin Assignments (TOP VIEW)





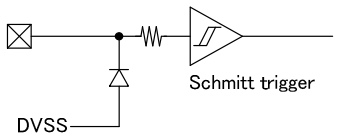
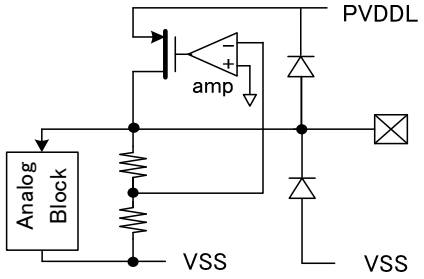
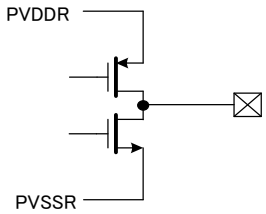
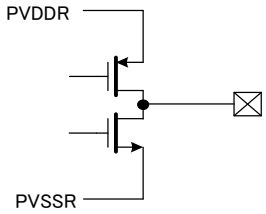
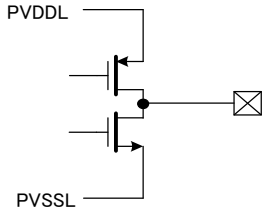
E-TSSOP-24L

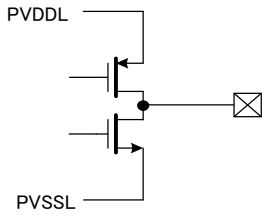
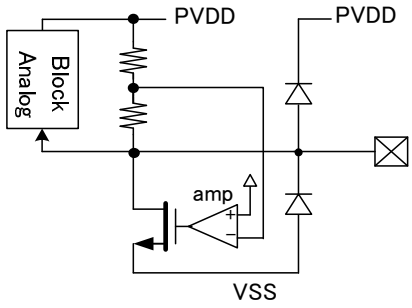
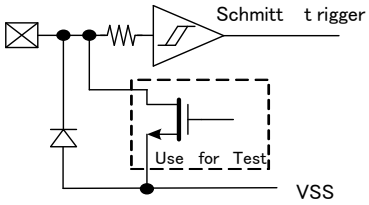
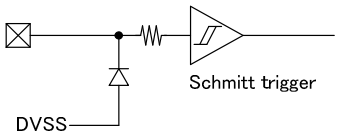
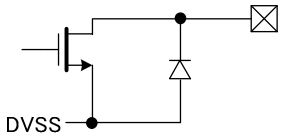
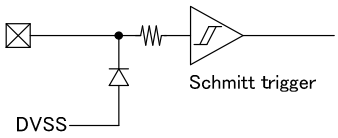
Pin Description

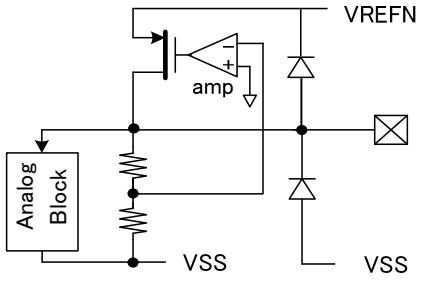
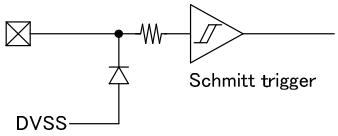
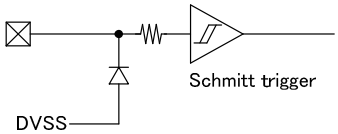
NAME	QFN-32L Pin #	E-TSSOP-24L Pin #	TYP (Note1)	DESCRIPTION
SDATA	1	5	I	Audio data input pin.
PLIMIT1	2	6	A	Power limit setting pin 1.
PLIMIT2	3	7	A	Power limit setting pin 2.
VREFN	4	8	O	Internal regulator output pin.
PVDDR	5, 6	9	P	Power pin for the digital amplifier output Rch.
OUTMR	7, 8	10	O	Digital amplifier output pin Rch-.
PVSSR	9, 10	11	P	GND pin for digital amplifier output Rch.
OUTPR	11, 12	12	O	Digital amplifier output pin Rch+.
OUTPL	13, 14	12	O	Digital amplifier output pin Lch+.
PVSSL	15, 16	14	P	GND pin for digital amplifier output Lch.
OUTML	17, 18	15	O	Digital amplifier output pin Lch-.
PVDDL	19, 20	16	P	Power pin for the digital amplifier output Lch.
VREFP	21	17	O	Internal regulator output pin.
MUTEN	22	18	I	Mute pin.
GAIN	23	19	A	Gain setting pin.
CKMOD	24	20	I	Clock mode setting pin.
SLEEPN	25	21	I	Sleep reset, a voltage for supplying SLEEPN pin with “H” level should be applied from an external power supply. Do not apply from REFA pin output.
PROTN	26	22	O/D	Error flag output pin.
MCLK	27	23	I	Master clock input pin.
REFA	28	24	O	Internal regulator output pin.
MONO	29	1	A	Stereo/Mono setting pin.
VSS	30	2	P	GND pin.
SCLK	31	3	I	Bit clock input pin.
LRCLK	32	4	I	Word clock input pin.
Thermal pad			P	Must be soldered to PCB’s ground plane.

Note 1: “TYP” of description, I: Input pin, O: Output pin, A: Analog pin, O/D: Open-Drain output pin, P: Power pin.

Pin Internal Circuit

Name	QFN 32L Pin #	E-TSSOP-24L Pin #	Equivalent Circuit
SDATA	1	5	
PLIMIT1	2	6	
PLIMIT2	3	7	
VREFN	4	8	
PVDDR	5,6	9	—
OUTMR	7,8	10	
PVSSR	9,10	11	—
OUTPR	11,12	12	
OUTPL	13,14	13	
PVSSL	15,16	14	—

OUTML	17,18	15	
PVDDL	19,20	16	—
VREFP	21	17	
MUTEN	22	18	
PLIMIT1	23	19	
PLIMIT2	24	20	
GAIN	25	21	
PROTN	26	22	
MCLK	27	23	

REFA	28	24	
MONO	29	1	
VSS	30	2	—
SCLK	31	3	
LRCLK	32	4	

Ordering Information

Product ID	Package	Packing	Comments
AD82583-HJ32NRY	QFN 32L (5mmx5mm)	490 Units / Tray 10 trays / Inner Box	Green
AD82583-HJ32NRR		5K Units Tape & Reel	
AD82583-QG24NRT	E-TSSOP 24L	62 Units / Tube 100 Tubes / Small Box	Green
AD82583-QG24NRR		2.5K Units Tape & Reel	

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	θ_{jt}(℃/W)	Ψ_{jt}(℃/W)	Exposed Thermal Pad
QFN 32L	AD82583	34	14.4	1.1	Yes (Note2)
E-TSSOP 24L		26.8	27.1	1.83	

Note 2.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 2.2: θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 2.3: θ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface (The junction-to-top thermal resistance is obtained by simulating a cold plate test on the top of the package).

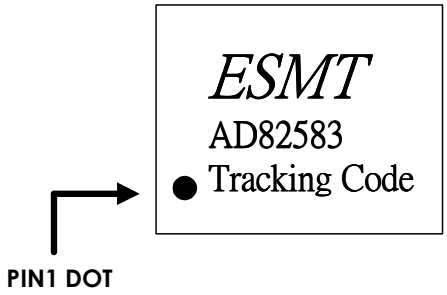
Note 2.4: Ψ_{jt} represents the heat resistance for the heat flow between the chip and the exposed pad's center (The junction-to-top characterization parameter is extracted from the simulation data to obtain θ_{ja}).

Marking Information

AD82583

- Marking Information

Line 1：LOGO
Line 2：Product No
Line 3：Tracking Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVDD	Supply for driver stage	PVDDR, PVDDL	-0.3	30	V
V_I	Interface pin voltage	MUTEN, MCLK, SCLK, LRCLK, SDATA, SLEEPN, CKMOD, GAIN, MONO, PLIMIT1, and PLIMIT2	-0.3	3.8	V
V_{PROTN}	PROTN terminal voltage range	PROTN	-0.3	3.8	V
T_A	Operating free-air temperature range		-40	85	^oC
T_J	Operating junction temperature range		-40	150	^oC
T_{stg}	Storage temperature range		-65	150	^oC
R_L	Minimum Load Resistance	Stereo (BTL)	3.6		Ω

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage for driver stage	PVDD	4.5	-	26	V
Digital terminals input voltage	V_{IN}	2.2	3.3	3.6	V
Operating Ambient Temperature	T_a	-40	-	85	°C
Stereo Speaker Impedance (Note 3)	R_L	4	8	-	Ω

Note 3: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

General Electrical Characteristics

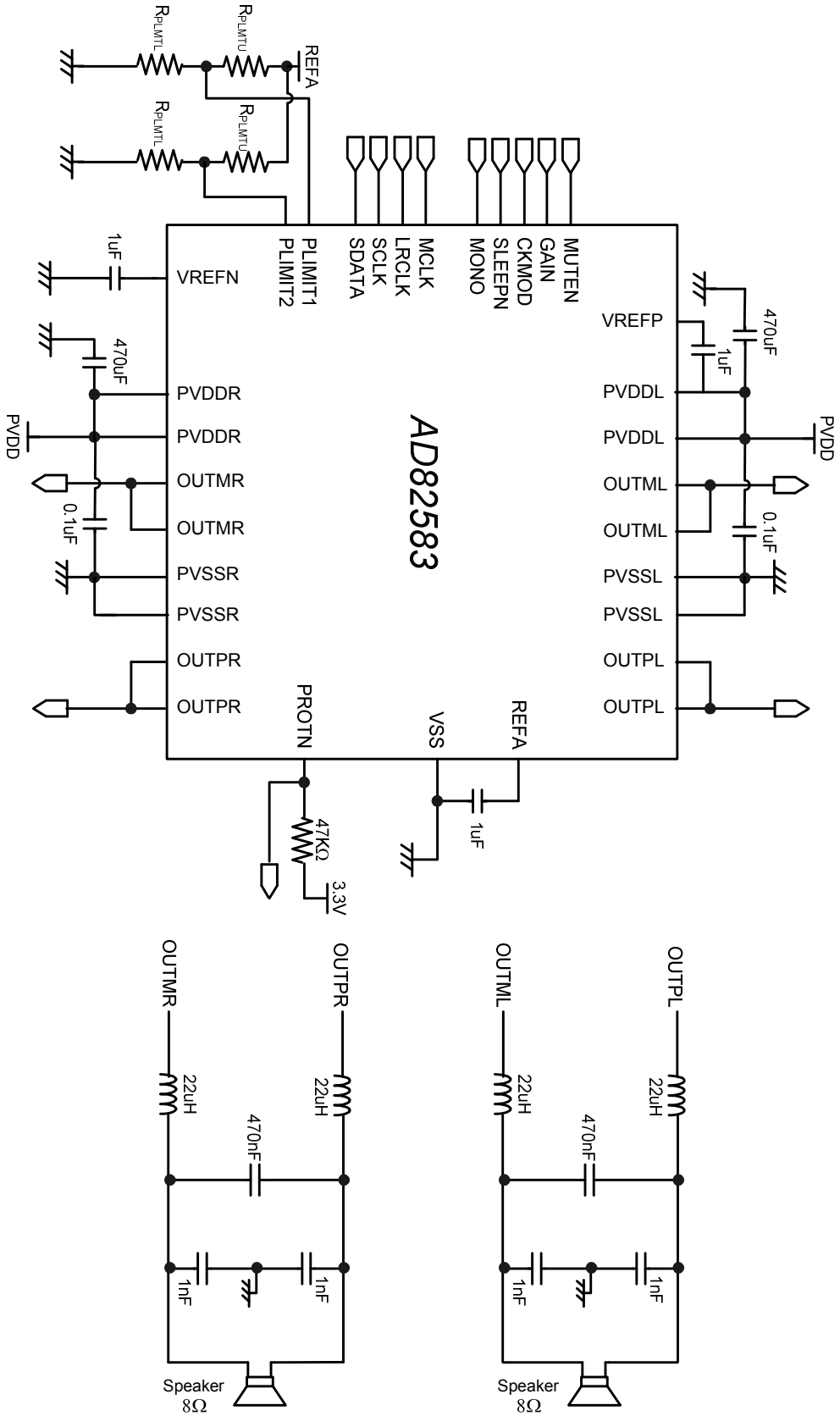
- PVDD=5V to 24V, T_A=25°C, unless otherwise specified.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
PVDD pin	Startup Threshold Voltage	V_{HUVLH}	–	–	4.1	–	V
	Shutdown Threshold Voltage	V_{HUVLL}	–	–	4	–	V
Digital pins (note4)	Input Voltage H level	V_{IH}	–	2.0	–	–	V
	Input Voltage L level	V_{IL}	–	–	–	0.8	V
	Input Impedance	R_{IN_D}	–	3.3	–	–	MΩ
SLEEPN pin	Input Voltage H level	V_{IH}	–	2.2	–	–	V
	Input Voltage L level	V_{IL}	–	–	–	0.5	V
	Input Impedance	R_{IN_D}	–	3.3	–	–	MΩ
PROTN pin Output Voltage		V_{OL}	I_{OL}=2mA	–	–	0.4	V
REFA pin Output Voltage		V_{REFA}	–	–	1.8	–	V
VREFN pin Output Voltage		V_{REFN}	PVDD =24V		5.5		V
VREFP pin Output Voltage		V_{REFP}	PVDD =24V		18.5		V
Current drawn from PVDD	at idling state	I_{DDPP}	PVDD =24V, No load	–	34	–	mA
	at power-down state (SLEEPN="L")	I_{DDPS}	PVDD =24V, No load	–	20	–	μA
	at mute state (MUTEN="L")	I_{DDPM}	PVDD =24V, No load	–	26	–	mA
Static drain to source on state resistor, PMOS		Rds-on	PVDD=24V Id=250mA		234		mΩ
Static drain to source on state resistor, NMOS					218		mΩ

Note4: Digital Pins: MUTEN, MLCK, SCLK, LRCLK, SDATA, and CKMOD

Application Circuit Example

- Application circuit for Stereo mode

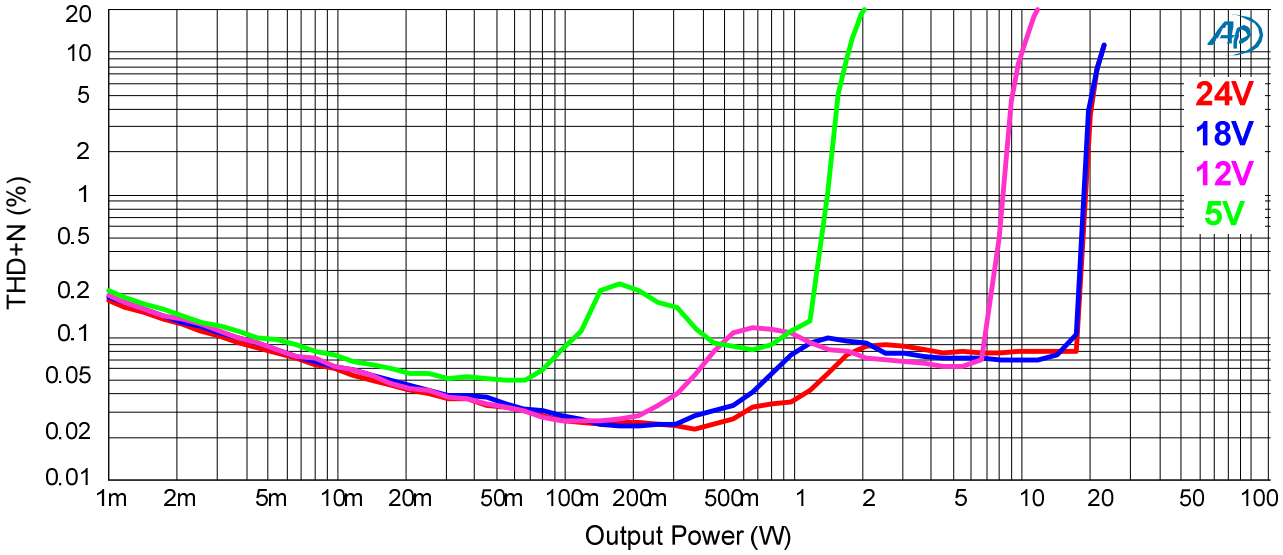


Electrical Characteristics and Specifications of Loudspeaker Driver

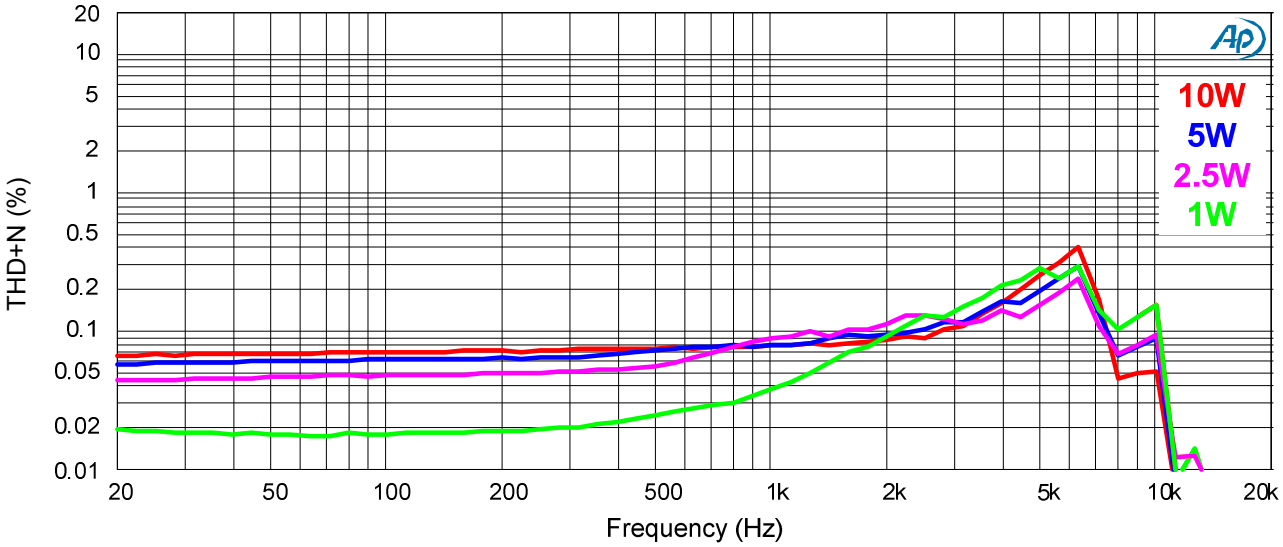
- PVDD=24V, T_A=25°C, R_L=8Ω,unless otherwise specified.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Instantaneous Output	Stereo	Po	PVDD=24V, R_L=8Ω, THD+N=2.9%	–	20	–	W
			PVDD=12V, R_L=8Ω, THD+N=10%	–	10	–	W
			PVDD=12V, R_L=4Ω THD+N=10%	–	15	–	W
	Mono		PVDD=24V, R_L=4Ω, THD+N=10%	–	40	–	W
Total Harmonic Distortion	Stereo, Mono	THD+N	R_L=8Ω, Po=7.5W	–	0.1	–	%
Residual Noise	Stereo, Mono	Vn	R_L=8Ω, A-Weighted Filter	–	130	–	μVrms
S/N Ratio	Stereo, Mono	SNR	R_L=8Ω, A-Weighted Filter	–	99	–	dB
Channel Separation (L vs R)		CS	R_L=8Ω, 1kHz	–	93	–	dB
PSRR	Stereo, Mono	PSRR	PVDD applied, Vripple=200mVpp, f=1kHz	–	70	–	dB
Maximum Efficiency	Stereo	η	PVDD=24V, R_L=8Ω, Po=10W	–	87	–	%
			PVDD=12V, R_L=4Ω, Po=10W	–	86	–	%
	Mono		PVDD=24V, R_L=8Ω, Po=10W	–	87	–	%
			PVDD=12V, R_L=4Ω, Po=10W	–	90	–	%
Output Offset Voltage	Stereo, Mono	Vo	–	–	10	20	mV
Frequency Characteristics	Stereo, Mono	f	20Hz	–1	0	1	dB
			20kHz	–3	0	1	dB

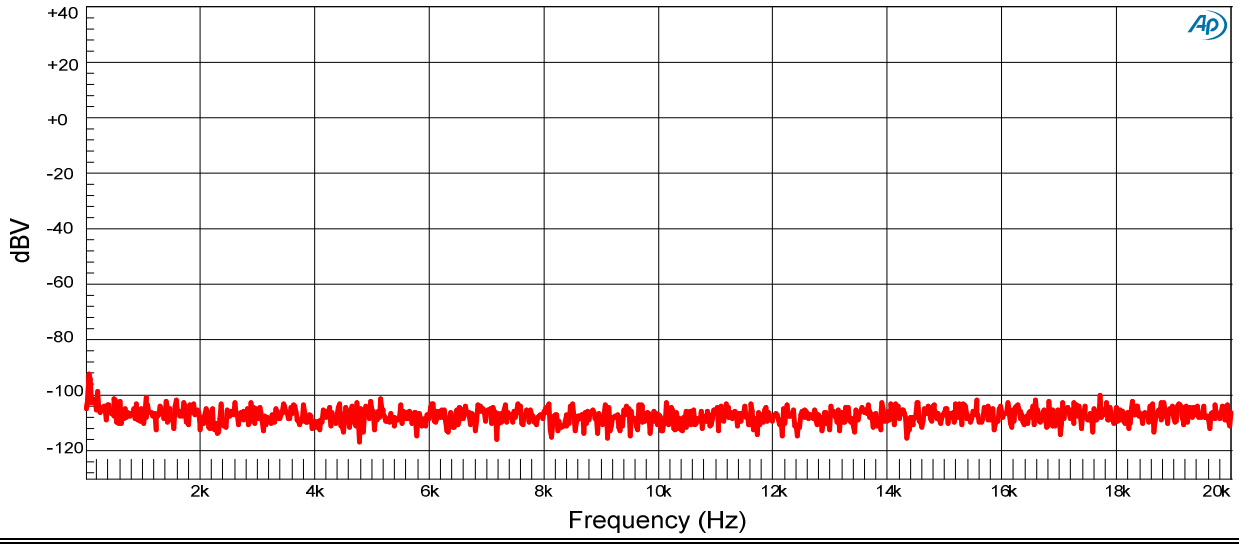
THD + N (%) v.s. Output power (Stereo, RL=8Ω)



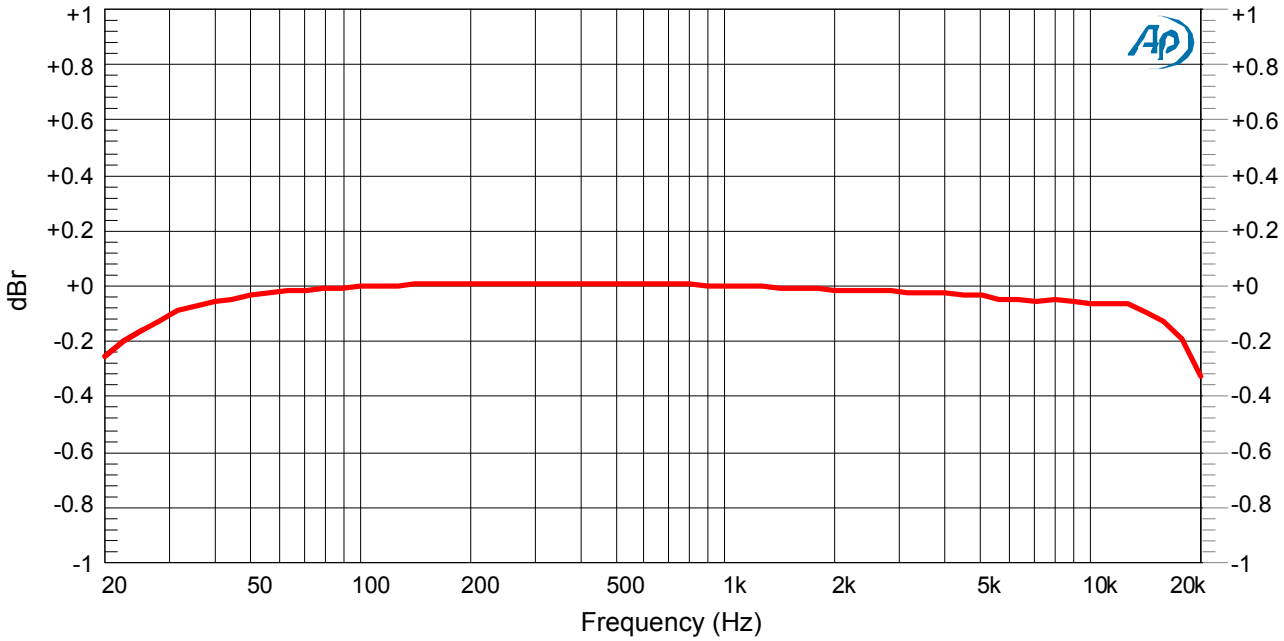
THD + N (%) v.s. Frequency (24V, Stereo, RL=8Ω)



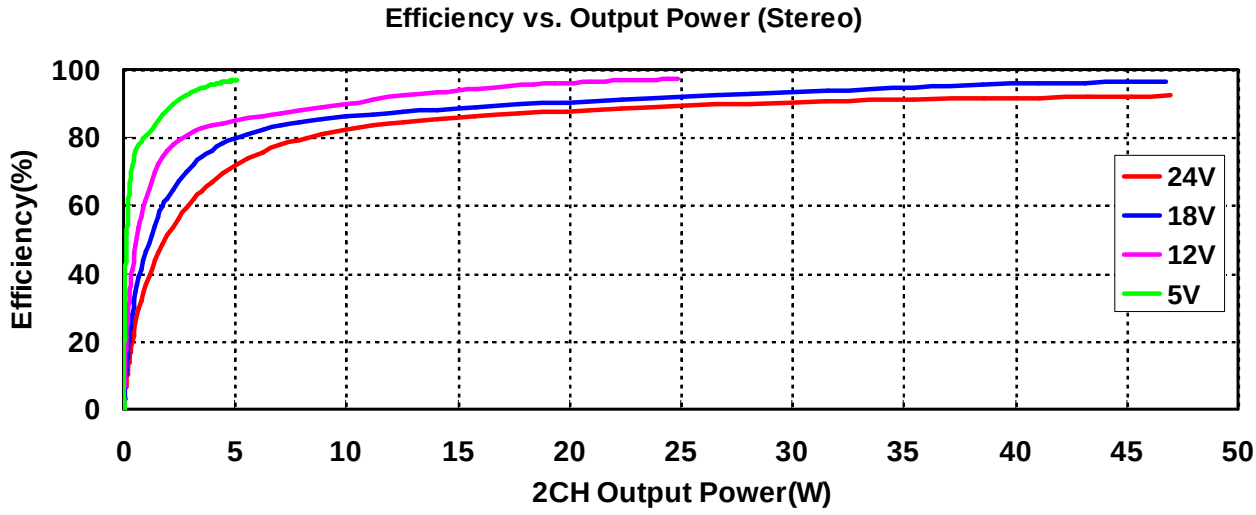
Noise FFT (24V, Stereo, RL=8Ω)



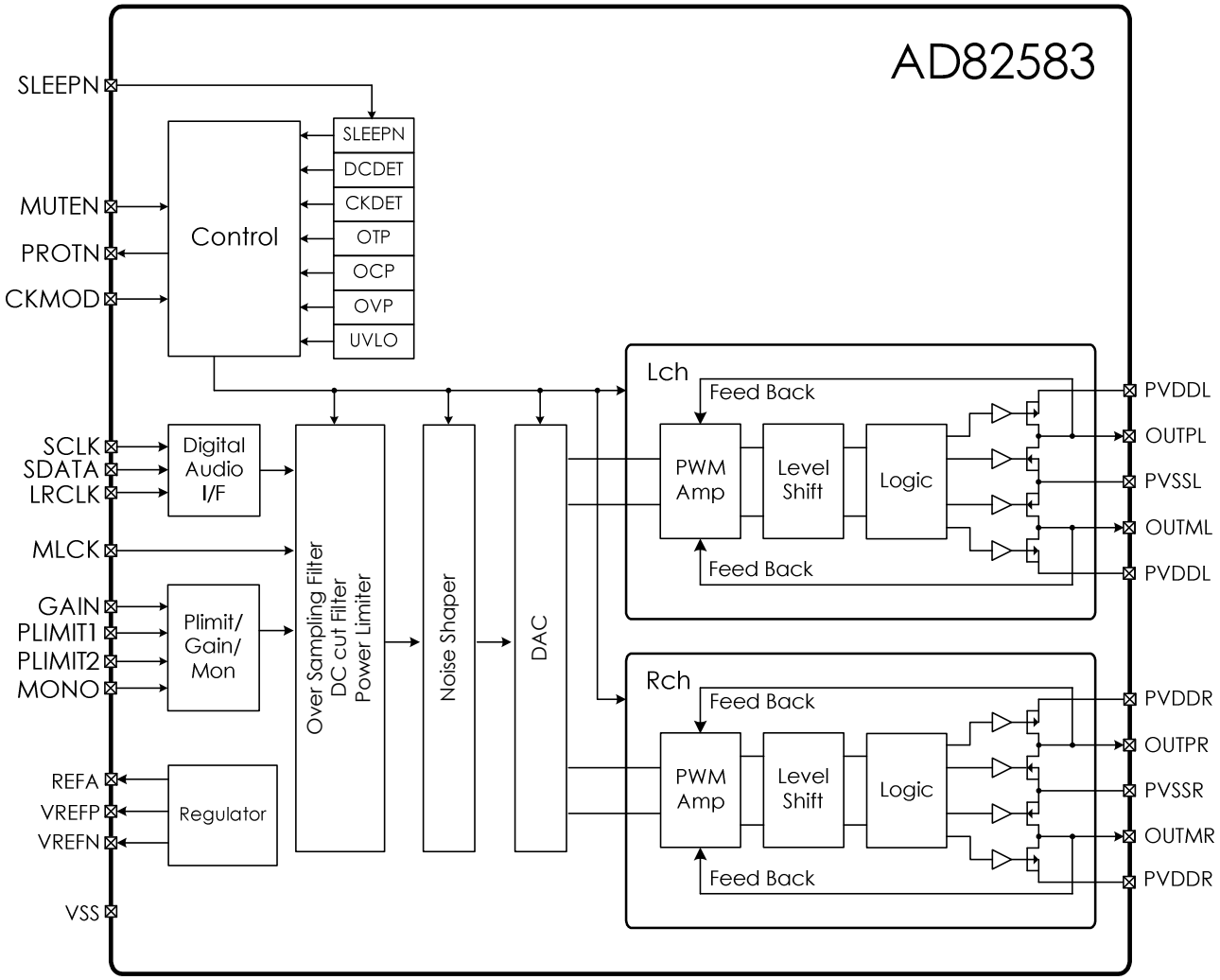
Frequency Response (24V, 1W, Stereo, RL=8Ω)



Efficiency (Stereo, RL=8Ω)

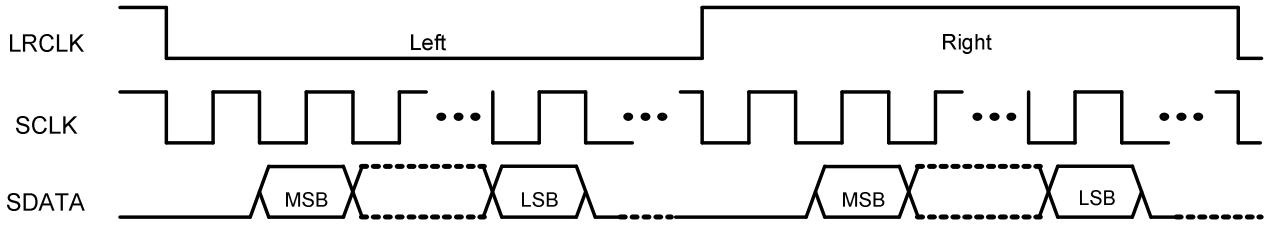


Functional Block Diagram

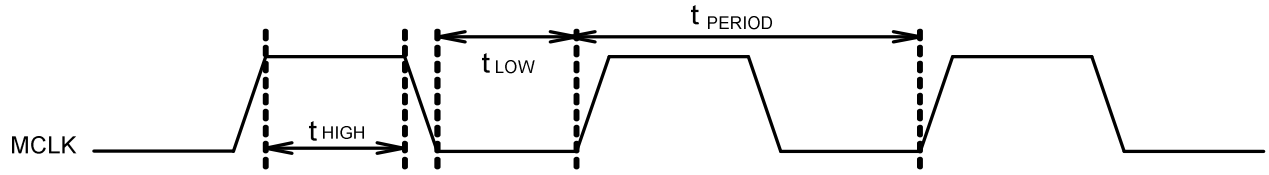


Interface Configuration

- I^2S



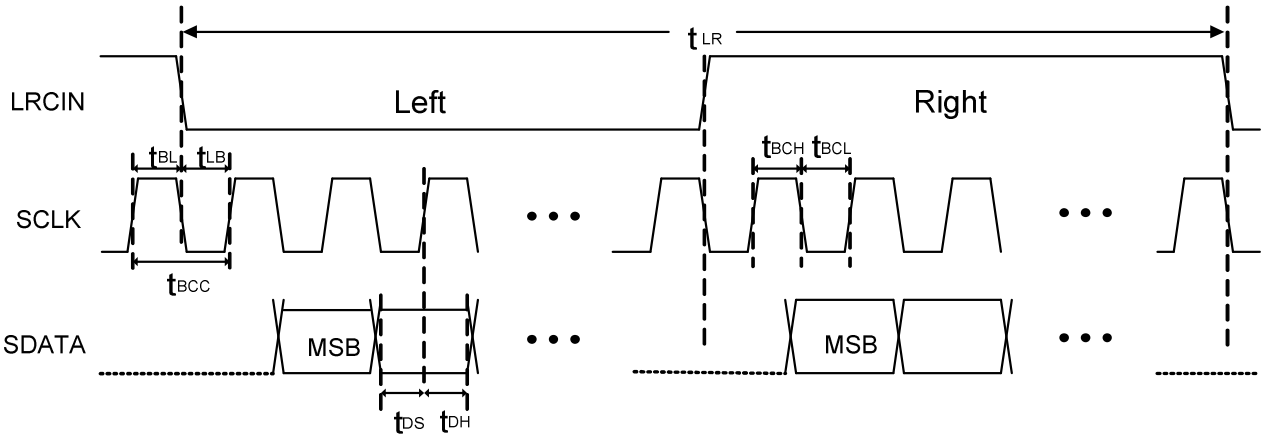
- System Clock Timing



$t_{HIGH} \geqq 40.4$ ns, $t_{LOW} \geqq 40.4$ ns, $t_{PERIOD} \geqq 80.8$ ns Default setting when PLL is enable

$t_{HIGH} \geqq 10.1$ ns, $t_{LOW} \geqq 10.1$ ns, $t_{PERIOD} \geqq 20.2$ ns When PLL is disable

- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCLK Period ($1/F_S$)	20.83		31.25	µs
t_{BL}	SCLK Rising Edge to LRCLK Edge	100			ns
t_{LB}	LRCLK Edge to SCLK Rising Edge	100			ns
t_{BCC}	SCLK Period ($1/64F_S$)	325.52		488.3	ns
t_{BCH}	SCLK Pulse Width High	162.76		244	ns
t_{BCL}	SCLK Pulse Width Low	162.76		244	ns
t_{DS}	SDATA Set-Up Time	100			ns
t_{DH}	SDATA Hold Time	100			ns

Operation Descriptions

The description below shows AD82583 functions and operations

- **Digital Amplifier Modulation Method**

  AD82583 has a 20W (Max.)×2ch digital amplifier with digital input and PWM pulse output. The pulse frequency that appears between OUTP* and OUTM* pins is called “Carrier Clock Frequency.” The figure 1 below shows the output waveform for when a sine wave is input about the characteristics of modulation method. As shown in B of the figure, the frequency that appears between GND and OUTP* pins and between GND and OUTM* pins at no-signal input becomes the half of a carrier clock frequency. As shown in A, C of the figure, when the output power increases, one side stops its switching and the other serves as a carrier clock frequency.

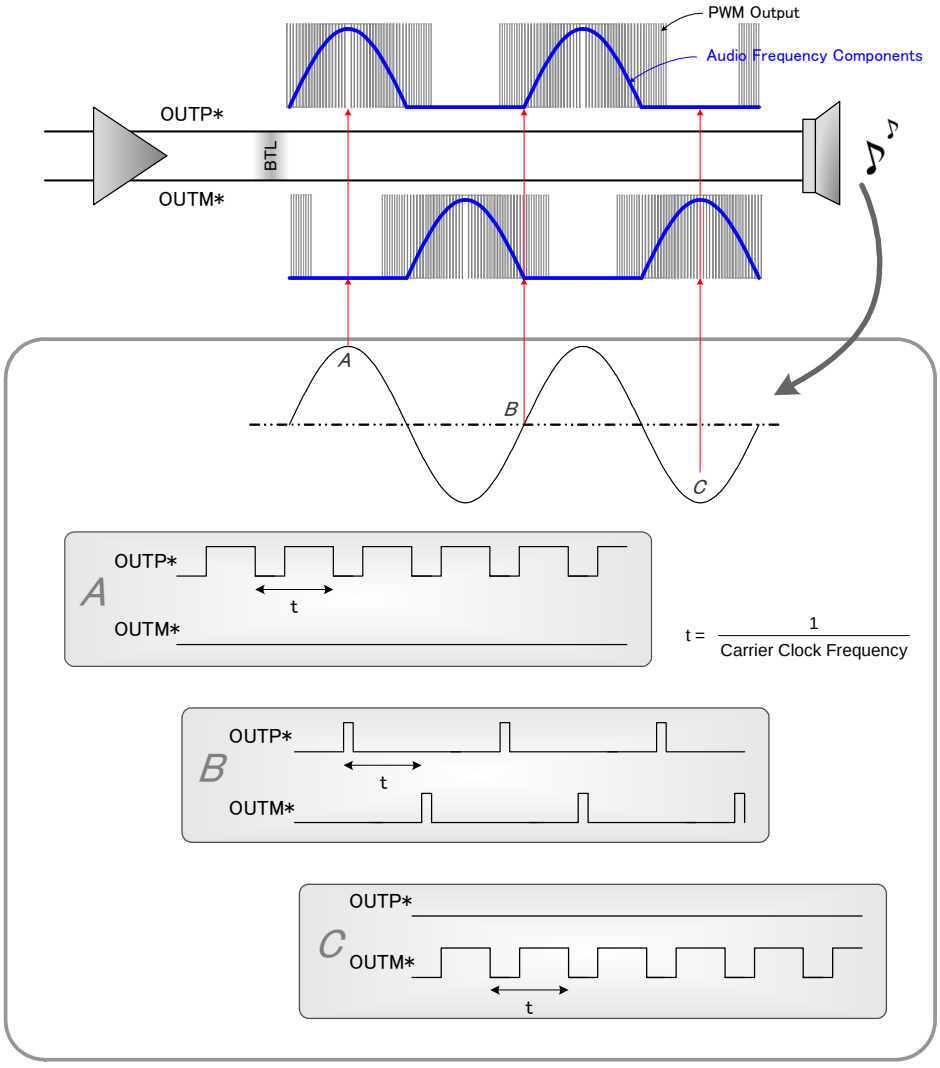


Figure 1, Modulation Method with AD82583

- **Digital Audio Interface**

AD82583 receives digital audio data using SCLK, LRCLK, and SDATA pins. The following sampling frequencies are supported: 32kHz, 44.1kHz, and 48kHz

- Audio signal format: Left-justified format, MSB first, 1-bit delay, 24 bits.
- LRCLK and SDATA are loaded at the rising edge of SCLK.
- The number of valid SDATA bits is up to 24 bits.
- 24bit×2ch audio data are input through SDATA pin during one sample period. Fill the unused bits after 24th bit with "L" data.

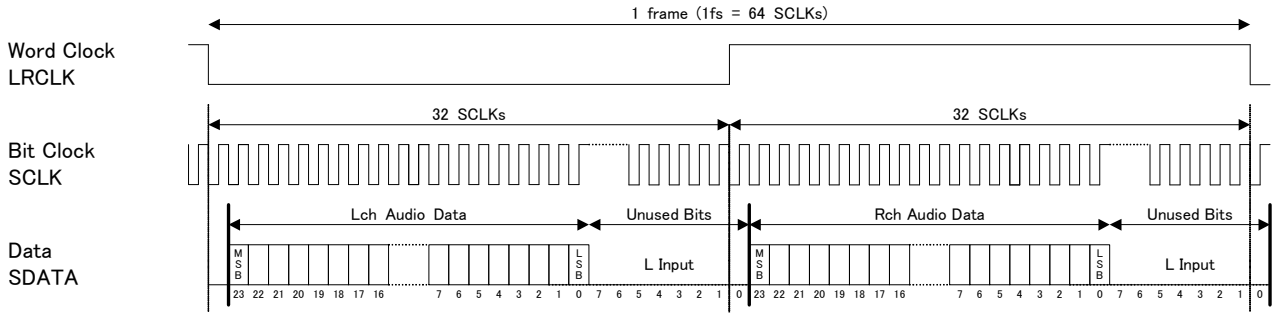


Figure 2, Digital Audio Interface Timing

- **Carrier Clock Frequency Control Function**

This is the function to set a carrier frequency with the following control pins. The way to control the frequency is as follows:

・LRCLK, SCLK and MCL pins

According to condition used, input clock to LRCLK, SCLK, and MCLK pins as shown in Table.

・CKMOD pin

CKMOD pin is the clock mode setting pin. It should be set as shown in the table 1 according to MCLK frequency to input. Frequencies and pin settings other than the listed values are not available. MCLK frequency must be just an integral multiple of SCLK frequency. And, the frequencies must be derived from the same oscillator. There is no restriction about the phase relationship of MCLK and SCLK. To change SCLK and LRCLK frequencies, MUTEN pin must be set to “L”. To change MCLK frequencies and CKMOD pin setting, SLEEPN pin must be set to “L” or power must be down.

Table 1, Carrier Clock Frequency

Fs [kHz]	LRCLK(1fs) [kHz]	SCLK(64fs) [kHz]	MCLK [kHz]	MCLK [Fs]	CKMOD	Carrier Clock Frequency [kHz]
32	32	2048	24576	768	L	768
32	32	2048	16384	512	H	1024
32	32	2048	12288	384	H	768
44.1	44.1	2822.4	22579	512	L	705.6
44.1	44.1	2822.4	11290	256	H	705.6
48	48	3072	24576	512	L	768
48	48	3072	12288	256	H	768

- **Gain Setting function**

Two discrete resistors on the GAIN pin select AD82583 amplifier gain from one of eight values. Gain setting circuit is shown below.

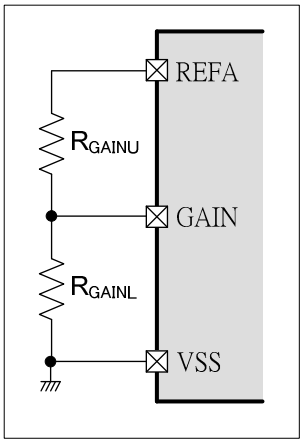


Figure 3, Gain Setting Circuit

The amplifier gain can be set to one of the three fixed levels (*Mode* 6 through 8 in *Table 2*), or a level that satisfies full scale output distortion figures of less than 1 %, or at 5 %, 10 %, 20 %, or 30 % (*Mode* 1 through 5 in *Table 2*). As an example, it becomes the following operations, when a GAIN pin is set as Mode 1 (THD+N=10%), PLIMIT2 pin is set as Mode 1, and PLIMIT1 pin is set as Mode H (Power limit setting is 10W, RL is 8 Ω).

・If 0dBFS signal is inputted, output power is 10W (min) by THD+N 10%.
・If -20dBFS signal is inputted, output level is as follow.

4.81 + (DBLMT + DBGAIN10) = 4.81 – 6.86 + 2.473 = 0.423 [dBV]

To change GAIN pin setting, MUTEN pin must be set to “L” or power must be down. Table 2 shows digital amplifier gain setting.

Table 2 shows digital amplifier gain setting

Mode	Resistance Value Setting (E12 series 1% accuracy)		DB_{GAIN**}[dB]	Output level [dBV] When –20dBFS input	Power Limiter bounded (at the 0 dBFS distortion figure)
	R_{GAINU}	R_{GAINL}			
1	Short	Open	DB_{GAIN10} : 2.473	4.81＋(DB_{LMT}+ DB_{GAIN10}) *5）	10%
2	3.3kΩ	33kΩ	DB_{GAIN30} : 9.159	4.81＋(DB_{LMT}+ DB_{GAIN30}) *5）	30%
3	10kΩ	27kΩ	DB_{GAIN20} : 5.197	4.81＋(DB_{LMT}+ DB_{GAIN20}) *5）	20%
4	15kΩ	20kΩ	DB_{GAIN5} : 1.376	4.81＋(DB_{LMT}+ DB_{GAIN5}) *5）	5%
5	27kΩ	20kΩ	DB_{GAIN0} : 0	4.81＋(DB_{LMT}+DB_{GAIN0}) *5）	<1%
6	56kΩ	22kΩ	–	–1.19	–
7	68kΩ	10kΩ	–	10.81	–
8	Open	Short	–	4.81	–

Note:

Gain setting resistors (RGAINU, RGAINL) draw current when not in sleep state (SLEEPN = “L”).

The external resistance should use the above-mentioned value and the 1% accuracy.

*5: DBLMT values are described in *Table 4 Power Limiter Setting Example*

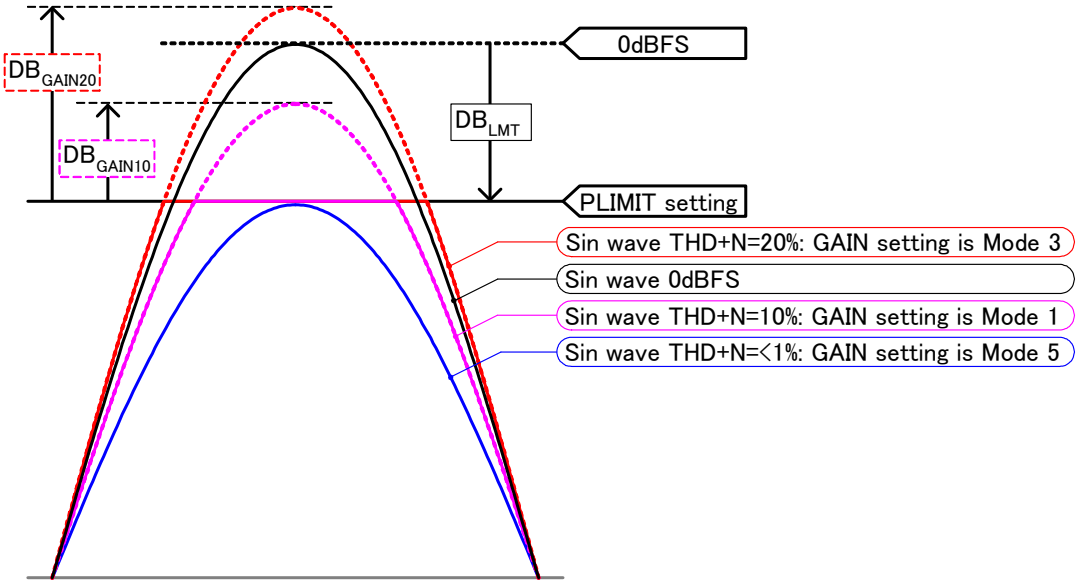


Figure 4, Power Limiter bounded gain controls

- **Power Limit function**

This function, limiting the output peak voltage, protects an external speaker and controls the increase of internal temperature. *PLIMIT1* and *PLIMIT2* can be strapped to one of 8 *Modes* in *Table 3, A* through *H* and *1* through *8* respectively with two external resistors on each pin as shown in *Figure 5.* The combination of *PLIMIT1 Mode* and *PLIMIT2 Mode* configures 63 Power Limiter levels as shown in *Table 4.*

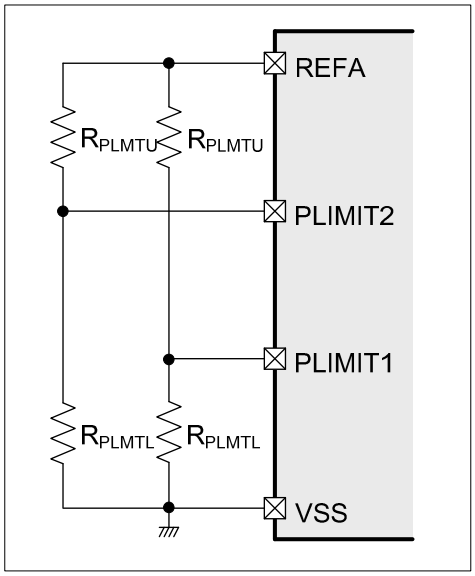


Figure 5, PLIMIT1 and PLIMIT2 pin setting circuit

Table 3, Power Limit Setting

Mode		Resistance Value Setting (E12 series 1% accuracy)	
PLIMIT2 pin	PLIMIT1 pin	R_{PLMTU}	R_{PLMTL}
1	A	Short	Open
2	B	3.3kΩ	33kΩ
3	C	10kΩ	27kΩ
4	D	15kΩ	20kΩ
5	E	27kΩ	20kΩ
6	F	56kΩ	22kΩ
7	G	68kΩ	10kΩ
8	H	Open	Short

Note: The external resistance should use the above-mentioned value and the 1% accuracy.

Table 4 shows sample Power Limiter levels using the Mode combinations. Power Limiter levels for 8 Ω, 6 Ω, or 4 Ω loads, and stereo or mono output configuration are shown. **Boldface** limits apply only for the operating PVDD = 12V.

Table 4, Power Limiter levels using the Mode combinations

PLIMIT1 Power Limit Setting (Min., THD+N=10%)

PLIMIT2 Power Limit Setting (Min., THD+N=10%)		Load	A	B	C	D	E	F	G	H
1	Stereo	8Ω	4.00W	0.30W	0.50W	0.70W	0.75W	1.00W	1.25W	10.00W
		6Ω	5.33W	0.40W	0.67W	0.93W	1.00W	1.33W	1.67W	–
		4Ω	8.00W	0.60W	1.00W	1.40W	1.50W	2.00W	2.50W	–
	Mono	8Ω	4.00W	0.30W	0.50W	0.70W	0.75W	1.00W	1.25W	10.00W
		6Ω	5.33W	0.40W	0.67W	0.93W	1.00W	1.33W	1.67W	13.33W
		4Ω	8.00W	0.60W	1.00W	1.40W	1.50W	2.00W	2.50W	20.00W
	DB_{LMT}[dB]		-10.84dB	-22.09dB	-19.87dB	-18.41dB	-18.11dB	-16.86dB	-15.89dB	-6.86dB
2	Stereo	8Ω	1.50W	0.23W	0.25W	0.35W	0.38W	0.53W	0.60W	2.00W
		6Ω	2.00W	0.30W	0.33W	0.47W	0.50W	0.70W	0.80W	2.67W
		4Ω	3.00W	0.45W	0.50W	0.70W	0.75W	1.05W	1.20W	4.00W
	Mono	8Ω	1.50W	0.23W	0.25W	0.35W	0.38W	0.53W	0.60W	2.00W
		6Ω	2.00W	0.30W	0.33W	0.47W	0.50W	0.70W	0.80W	2.67W
		4Ω	3.00W	0.45W	0.50W	0.70W	0.75W	1.05W	1.20W	4.00W
	DB_{LMT}[dB]		-15.10dB	-23.34dB	-22.88dB	-21.42dB	-21.12dB	-19.66dB	-19.08dB	-13.85dB
3	Stereo	8Ω	2.25W	0.65W	0.83W	0.90W	1.13W	1.75W	1.88W	2.50W
		6Ω	3.00W	0.87W	1.10W	1.20W	1.50W	2.33W	2.50W	3.33W
		4Ω	4.50W	1.30W	1.65W	1.80W	2.25W	3.50W	3.75W	5.00W
	Mono	8Ω	2.25W	0.65W	0.83W	0.90W	1.13W	1.75W	1.88W	2.50W
		6Ω	3.00W	0.87W	1.10W	1.20W	1.50W	2.33W	2.50W	3.33W
		4Ω	4.50W	1.30W	1.65W	1.80W	2.25W	3.50W	3.75W	5.00W
	DB_{LMT}[dB]		-13.34dB	-18.73dB	-17.70dB	-17.32dB	-16.35dB	-14.43dB	-14.13dB	-12.88dB
4	Stereo	8Ω	17.5W	2.63W	3.38W	4.13W	4.88W	5.50W	6.25W	3.00W
		6Ω	–	3.50W	4.50W	5.50W	6.50W	7.33W	8.33W	4.00W
		4Ω	–	5.25W	6.75W	8.25W	9.75W	–	–	6.00W
	Mono	8Ω	17.5W	2.63W	3.38W	4.13W	4.88W	5.50W	6.25W	3.00W
		6Ω	26.25W	3.50W	4.50W	5.50W	6.50W	7.33W	8.33W	4.00W
		4Ω	35W	5.25W	6.75W	8.25W	9.75W	11.00W	12.50W	6.00W
	DB_{LMT}[dB]		-4.43dB	-12.67dB	-11.58dB	-10.71dB	-9.98dB	-9.46dB	-8.90dB	-12.09dB
5	Stereo	8Ω	18W	6.38W	6.50W	7.00W	7.13W	8.25W	8.50W	3.50W
		6Ω	–	8.50W	8.67W	9.33W	9.50W	–	–	4.67W
		4Ω	–	–	–	–	–	–	–	7.00W
	Mono	8Ω	18W	6.38W	6.50W	7.00W	7.13W	8.25W	8.50W	3.50W
		6Ω	27W	8.50W	8.67W	9.33W	9.50W	11.00W	11.33W	4.67W
		4Ω	36W	12.75W	13.00W	14.00W	14.25W	16.50W	17.00W	7.00W
	DB_{LMT}[dB]		-4.31dB	-8.82dB	-8.73dB	-8.41dB	-8.33dB	-7.70dB	-7.57dB	-11.42dB
6	Stereo	8Ω	4.25W	9.00W	9.50W	9.75W	10.50W	11.00W	11.25W	4.50W
		6Ω	5.67W	–	–	–	–	–	–	6.00W
		4Ω	8.50W	–	–	–	–	–	–	9.00W
	Mono	8Ω	4.25W	9.00W	9.50W	9.75W	10.50W	11.00W	11.25W	4.50W
		6Ω	5.67W	12.00W	12.67W	13.00W	14.00W	14.67W	15.00W	6.00W
		4Ω	8.50W	18.00W	19.00W	19.50W	21.00W	22.00W	22.50W	9.00W
	DB_{LMT}[dB]		-10.58dB	-7.32dB	-7.09dB	-6.97dB	-6.65dB	-6.45dB	-6.35dB	-10.33dB
7	Stereo	8Ω	20W	11.50W	13.00W	13.50W	14.00W	14.50W	Reserved	5.00W
		6Ω	–	–	–	–	–	–		6.67W
		4Ω	–	–	–	–	–	–		10.00W
	Mono	8Ω	20W	11.50W	13.00W	13.50W	14.00W	14.50W		5.00W
		6Ω	30W	15.33W	17.33W	18.00W	18.67W	19.33W		6.67W
		4Ω	40W	23.00W	26.00W	27.00W	28.00W	29.00W		10.00W
	DB_{LMT}[dB]		-3.85dB	-6.26dB	-5.72dB	-5.56dB	-5.40dB	-5.25dB		-9.87dB
8	Stereo	8Ω	3.75W	5.63W	6.00W	7.50W	8.00W	12.00W	12.50W	15.00W
		6Ω	5.00W	7.50W	8.00W	10.00W	–	–	–	–
		4Ω	7.50W	**11.25W**	**12.00W**	**15.00W**	–	–	–	–
	Mono	8Ω	3.75W	5.63W	6.00W	7.50W	8.00W	12.00W	12.50W	15.00W
		6Ω	5.00W	7.50W	8.00W	10.00W	10.67W	16.00W	16.67W	20.00W
		4Ω	7.50W	11.25W	12.00W	15.00W	16.00W	24.00W	25.00W	30.00W
	DB_{LMT}[dB]		-11.12dB	-9.36dB	-9.08dB	-8.11dB	-7.83dB	-6.07dB	-5.89dB	-5.10dB

Note: Power limit setting resistors (R_{PLMTU}, R_{PLMTTL}) draw current when not in sleep state (SLEEPN = "L"). Parasitic DC resistances of signal traces and inductors are taken into account for each loading condition as follows. 8Ω load: 0.10Ω, 6Ω load: 0.075Ω, 4Ω load: 0.05Ω. Output power is the minimum value which taken into account for the above-mentioned parasitic DC resistance ingredient.

- **Stereo / Mono mode Setting Function**

AD82583 can be configured as stereo or mono amplifier by external resistors on *MONO* pin.

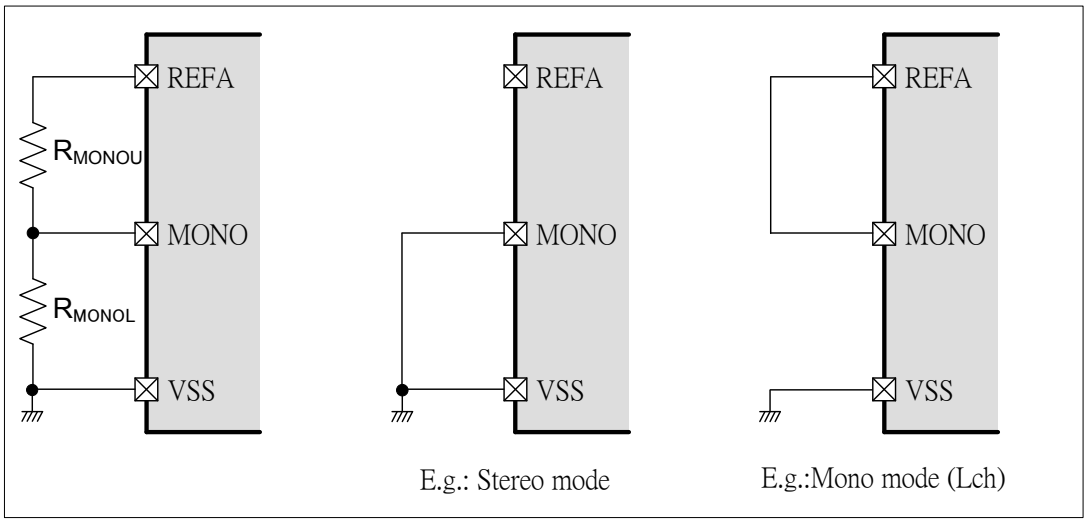


Figure 6, Mono pin setting circuit

AD82583 can be configured as stereo or mono amplifier by external resistors on *MONO* pin. For mono configuration, these resistors also determine which mono channel is used as the mono source. The source signal is amplified and put on both L- and R-channel outputs.

Table 5, Mono pin setting

Mode	Resistance Value Setting (E12 series 1% accuracy)	
	R_{MONOU}	R_{MONOL}
Mono mode (Rch)	3.3kΩ	33kΩ
Mono mode (Lch+Rch,-6dB)	15kΩ	20kΩ
Mono mode (Lch)	Short	Open
Stereo mode	Open	Short

Note: Mono setting resistors (R_{MONOU}, R_{MONOL}) draw current when not in sleep state (SLEEPN = “L”). The external resistance should use the above-mentioned value and the 1% accuracy.

When using in stereo mode, this device should be connected as shown in “Stereo Mode” of application circuit. When using in monaural mode, OUTPL and OUTML should be connected to OUTPR and OUTMR respectively as shown in “Monaural Mode” of application circuit. Be sure to turn off the power before selecting stereo or monaural mode or making the appropriate connection.

- **Quick Mute/Quick Start Function**

Quick Mute/Quick Start function allows intermittent sound to be reduced significantly and uncomfortable feeling to be removed by varying the output envelope at a slow rate at the time of MUTE ON/OFF.

Table 6, MUTEN pin setting

MUTEN pin	Mode
L	Digital Amplifier Mute State
H	Normal Operation State

By setting MUTEN pin to “L”, AD82583 performs Quick Mute operation (Decreasing the volume linearly by taking 512×1/fs), (16×96) / (carrier clock frequency)[s] later, it sets the digital amplifier output to WL (Weak Low: a state grounded through a high-value resistance), resulting in Mute state (Output Disabled).

By setting MUTEN pin to “H”, AD82583 moves from the mute state to normal operation state while turned down volume. Afterwards, the quick start operation (where the volume is increased linearly over 256×1/fs) is executed. Mute recovery time from Mute state is t_{mrcv}(Typ.). If the mute state is cancelled during the Quick Mute Sequence, Quick Start Sequence will start after the quick mute sequence.

When the voltage at PVDD pin becomes lower than PVDD pin Shutdown Threshold Voltage (V_{HUVLL}) in the mute state, for shutting down the system safely, the amplifier output is set to WL (Weak Low : a state grounded through a high-value resistance) after outputting a low signal for a given period of time.

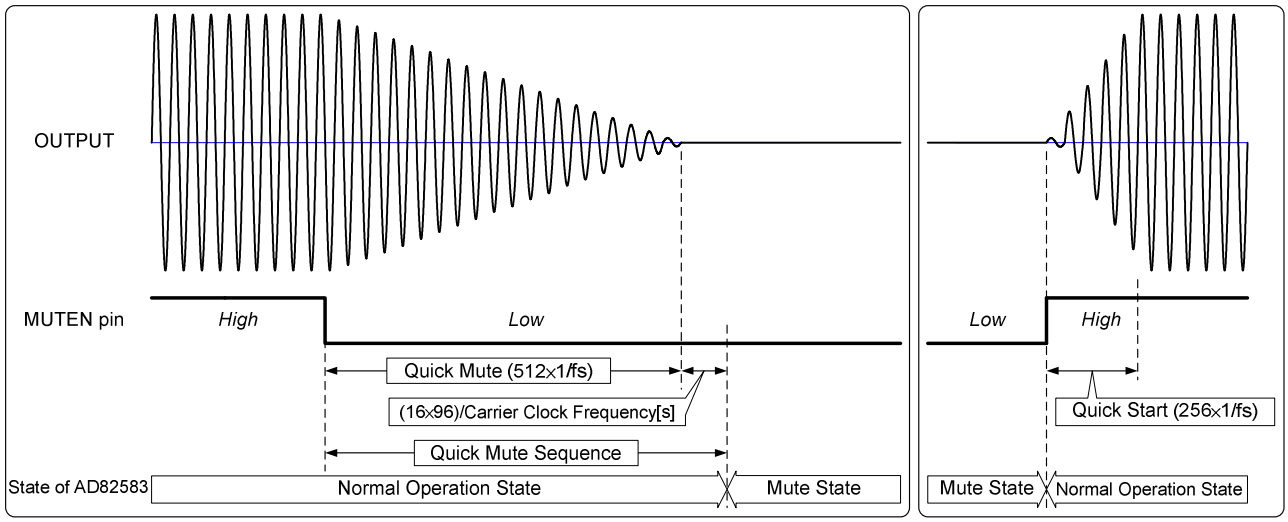


Figure 7, Quick Mute and Quick Start

- **Sleep Function**

In Sleep state, all circuit functions are stopped and consumption current becomes the minimum (IDDPS). VREFA and VREFN pins outputs are pulled down, and VREFP pin is pulled high.

Table 7, SLEEPN pin setting

SLEEPN pin	Mode
L	Sleep State
H	Normal Operation State

By setting SLEEPN pin to “L”, AD82583 performs Quick Mute operation (Decreasing the volume linearly by taking 1024×1/fs), (16×96) / (carrier clock frequency) [s] later, it sets the digital amplifier output to WL(Weak Low: a state grounded through a high-value resistance).

AD82583 goes to Sleep state when max.160ms has passed after setting SLEEPN pin to "L."
When going to sleep mode while some protection state is being activated, this protection mode is cancelled and PROTN pin output goes to Hi-Z state.

With PVDD pin output being higher than the threshold voltage to cancel the low-voltage malfunction preventing function, when changing the state of SLEEPN pin from “L” to “H,” the digital amplifier terminates the sleep state, simultaneously starts the Startup Sequence and does the quick start (raises the volume level linearly by taking 256×1/fs) to activate the oscillation after max.300ms.

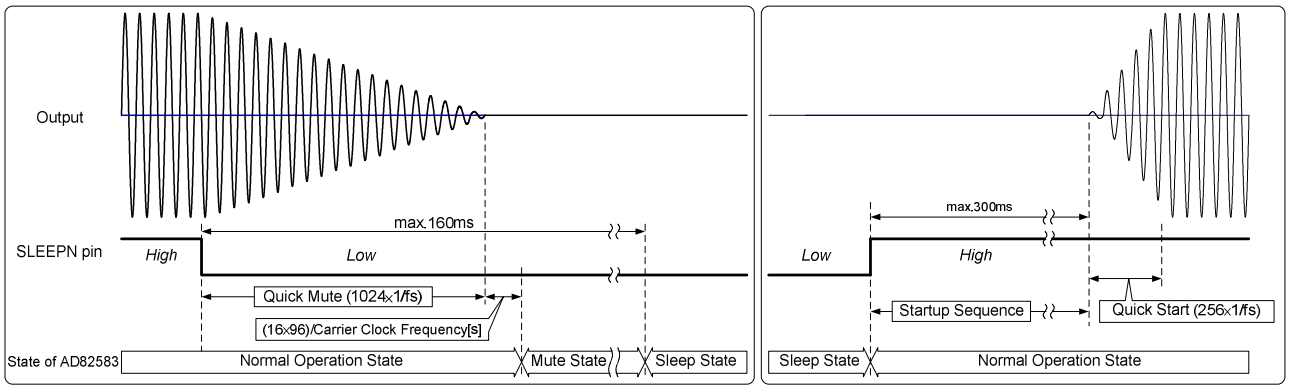


Figure 8, Sleep Function

- **DC-cut Function**

  AD82583 includes DC-cut filter (cut-off frequency=10Hz) for input digital audio data.

- **Supply Voltage Regulation**

  AD82583 adopts a circuit method that feeds back the output signal. This method allows the deterioration in distortion characteristics to be minimized even when a supply voltage fluctuates (in case of a power supply not regulated). Whereas, with a non-feedback type digital amplifier, a power supply with high-regulation capability is required because this fluctuation is added to the output waveform.

- **REFA Voltage Output Function**

  AD82583 includes series regulator. The voltage inputted from a PVDD power supply pin is supplied to a regulator. REFA pin outputs the voltage (VREFA) regulated from the voltage coming from PVDD pin. For its stabilization, connect a bypass capacitor of 1.0μF to 4.7μF between REFA and AVSS pins (0.8μF or more should be secured including its variation and temperature change.). REFA pin must not be connected to other devices.

- **VREFN Voltage Output Function**

  The voltage inputted from a PVDD power supply pin is supplied to a regulator. VREFN pin outputs the voltage (VREFN) regulated from the voltage coming from PVDD pin. For its stabilization, connect a bypass capacitor of 1.0μF to 4.7μF between VREFN and VSS pins (0.8μF or more should be secured including its variation and temperature change.). VREFN pin must not be connected to other devices.

- **VREFP Voltage Output Function**

  The voltage inputted from a PVDD power supply pin is supplied to a regulator. VREFP pin outputs the voltage (VREFN) regulated from the voltage coming from PVDD pin. For its stabilization, connect a bypass capacitor of 1.0μF to 4.7μF between VREFP and PVDDL(PVDDR) pins (0.8μF or more should be secured including its variation and temperature change.). VREFP pin must not be connected to other devices

- **Digital Amplifier Startup/Shutdown Procedure**

  It is recommended to use the following sequences as digital amplifier start and shutdown procedure. With different sequence, unusual sound or pop noise may occur.

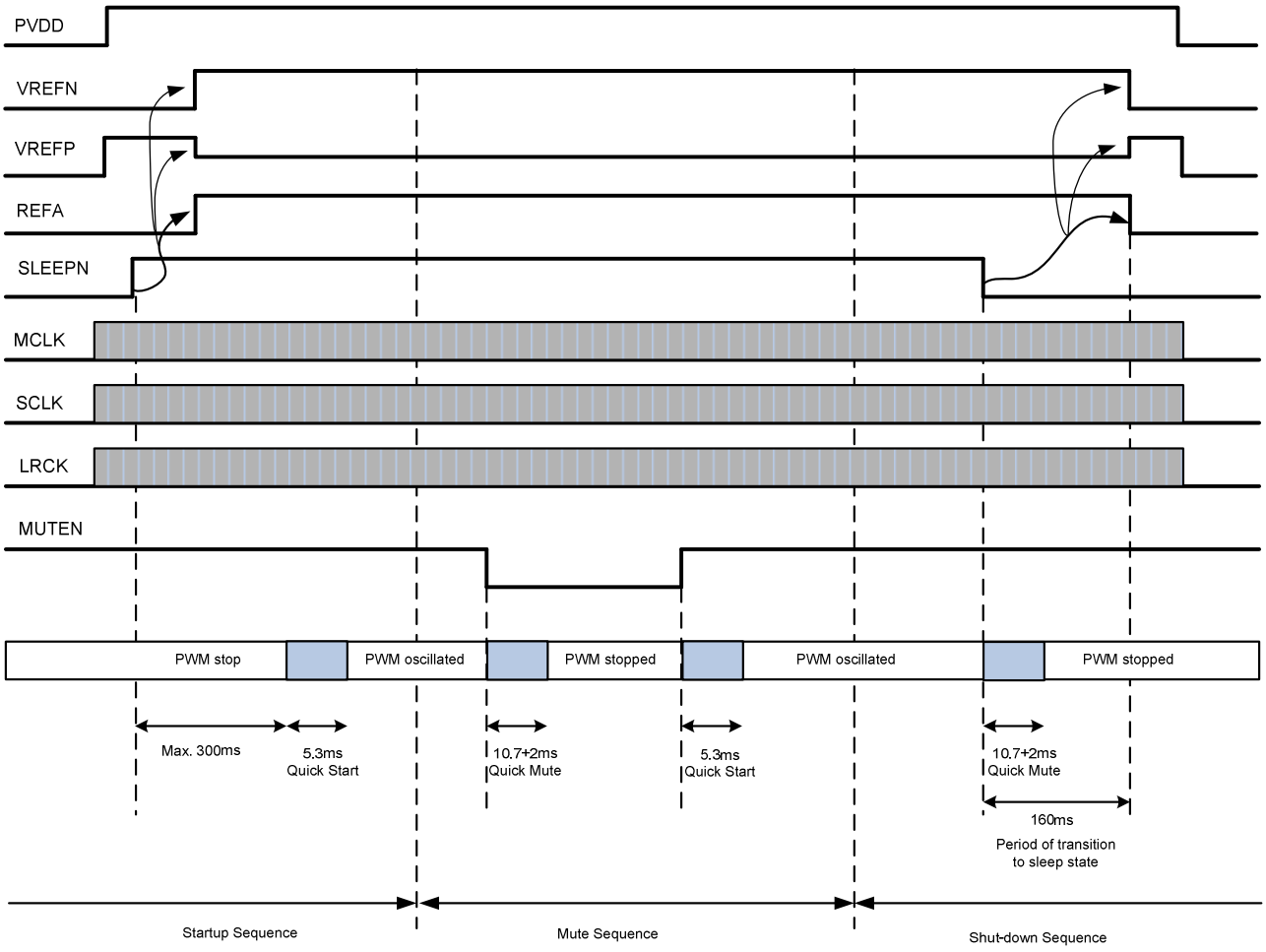
- **Recommended Digital Amplifier Startup Sequence**

  1. Supply the power to PVDD pin.
  2. When the supply voltage reaches at the recommended voltage range, input clocks to MCLK, SCLK, and LRCLK pins.
  3. Change the logical state of SLEEPN pin from “L” to “H”.

- **Recommended Digital Amplifier Shutdown Sequence**

  1. Change the logical state of SLEEPN pin from “H” to “L”.
  2. After 160ms or more, stop input the signal to the input pins and shut down the power to PVDD pin.

  * As long as SLEEPN pin was changed from “H” to “L” and Quick Mute {512×1/fs + (16×96) / (Carrier Clock Frequency) }[s]” has elapsed, unusual sound or pop noise is not generated even if the power is shut down.



- **LC Filter**

  On the other hand, when using a LC filter, the output circuit as shown in Figure 10, 11 should be used with the constants listed in Table 8. The use of these constants enables the filter to be a low-pass filter with its cut-off frequency being 50kHz or so and Q being 0.6 or so. When disconnecting a speaker, turn off the power in advance. When operating the device without a speaker, consumption current may increase or over current detection circuit may work due to the resonance in LC filter. When removing a speaker during operation, SLEEPN or MUTEN pin should be set to “L” or PVDD should be shut down.

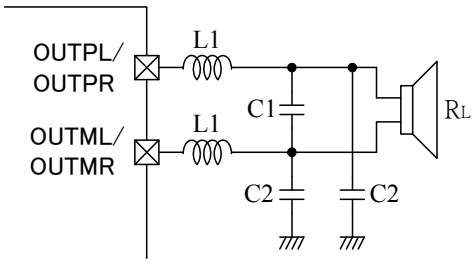


Figure 10, LC Filter Circuit (Stereo)

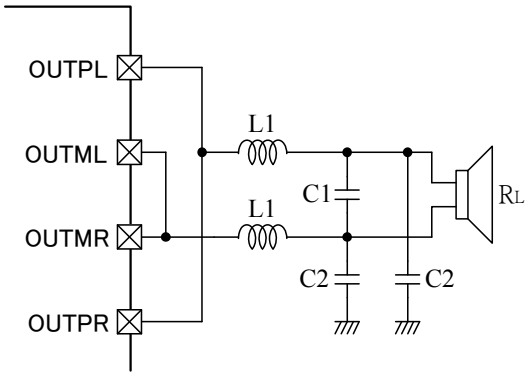


Figure 11, LC Filter Circuit (Mono)

R_L	L1	C1	C2	fc	Q
4Ω	10μH	0.47μF	1nF	51.9kHz	0.61
6Ω	15μH	0.33μF	1nF	50.6kHz	0.62
8Ω	22μH	0.47μF	1nF	35kHz	0.82
16Ω	47μH	0.1μF	1nF	51.9kHz	0.52

$$f_C = \frac{1}{2\pi\sqrt{L_1 \times (2 \times C_1 + C_2)}}$$

$$f_C(toGND) = \frac{1}{2\pi\sqrt{L_1 C_2}}$$

$$Q = \frac{\sqrt{\frac{2 \times C_1 + C_2}{L_1}} \times R_L}{2}$$

When using AD82583 with a speaker connected directly without connecting LC filters, or when using it with EMI countermeasure components, such as ferrite beads etc., in addition to a speaker, a speaker with an inductance higher than 20μH should be used. Otherwise, loss of the speaker and AD82583 may increase.

- **Protection Function**

AD82583 has the following protection functions.

Table 9, Protection Function List

Protection Function	PROTN Pin Output	Digital Amplifier Output	Quick Mute	Automatic Recovery
Over current Protection	L	WL (Note 7)	–	Applicable (Note 5)
Over Temperature Protection	L (Note 6)	WL (Note 7)	–	Not Applicable (However, it returns when the temperature decreases.)
Under Voltage Lock Out (PVDD pin)	H	WL (Note 7)	–	Not Applicable (However, it recovers from the lock out once the voltage level rise after startup sequence.)
Over Voltage Lock Out (PVDD pin)	L (Note 6)	WL (Note 7)		Not Applicable (However, it recovers from the lock out once the voltage level decrease after startup sequence.)
DC Detection	L	WL (Note 7)	–	Applicable (Note 5)
Clock Detection (MCLK, SCLK pin)	H	WL (Note 7)	–	Not Applicable (However, it returns when the clock input.)

Note5: Automatic recovery is performed 2.7 to 5.4 seconds (at fs=48kHz) after a protecting function is activated, and then PROTN pin goes to "H."

Note6: When an over temperature condition is cleared, PROTN is returned to "H."

Note7: WL=Weak Low (a state grounded through a high-value resistance)

For shutting down the system safely, the amplifier output is set to WL after outputting a low or high signal for a given period of time.

PROTN pin has an open-drain output. Use a resistor of 47kΩ to pull up the pin with respect to an external power supply source lower than 3.3V. In order to prevent the current in excess of 2mA from being flowed into PROTN pin being in L state. If multiple AD82583s are used, all the PROTNs can be tied together for wired OR connection. PROTN pin must not connect to pins of AD82583. PROTN pin should be left open when not used.

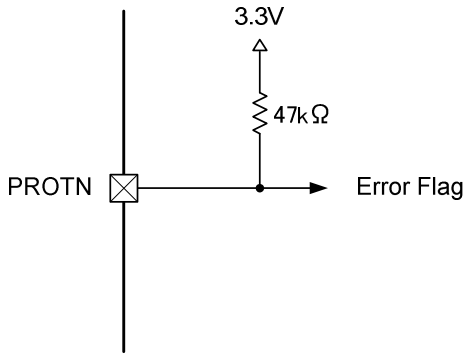


Figure 12, PROTN pin Pull-up Termination

- **Digital Amplifier Over-current Protection Function (OCP)**

  This function, detecting an over current condition at the digital amplifier output, enables the over-current protection state, in which the following short-circuiting conditions are detected: VSS short (Ground or any other lower-potential point), PVDD short (supply voltage or a higher-potential point), or short-circuiting between ±output pins. The detection current, for pin-to-pin short-circuiting, is 7A (typ., PVDD=24V). In this state, digital amplifier outputs are forced to "WL" state (Weak Low: a state grounded through a high-value resistance) and PROTN pin goes to "L". The automatic recovery operation is performed 2.7 to 5.4 seconds (at fs=48kHz) after the protection state is activated. When detected eight times in all, the protection state is held without being cancelled. The held protection state can be cancelled by setting SLEEPN pin to "L" temporarily or shutting down the power. This protection state is provided not for guarantee of IC protection in case of exceeding the maximum rating (speaker impedance) but for safety in case of unusual conditions.

- **Over Temperature Protection Function (OTP)**

  This function, detecting an unusual high-temperature condition in the chip, and protect IC by output disable. In this over temperature protection state, in which digital amplifier outputs are forced to "WL" state (Weak Low: a state grounded through a high-value resistance) and PROTN pin goes to "L". When such unusual temperature in the chip is lowered, this protection state is cancelled and PROTN goes to "Hi-Z.". At the same time, normal operation will start again after a quick start. This protection function is provided not for guaranteeing the protection in case of exceeding the maximum ratings (junction temperature) but for ensuring safety in case of unusual conditions.

- **Over Voltage Protection Function (OVP)**

  This function, detecting an unusual condition where the voltage at PVDD pin becomes higher than "PVDD pin Shutdown Threshold Voltage", and prevent malfunction etc. In this high-voltage protection state, digital amplifier outputs become WL state (Weak Low: a state grounded through a high-value resistance). When voltages at PVDD pin become lower than high-voltage cancel threshold voltage, the high-voltage protection state is cancelled and the normal operation starts after max. 300ms. This function does not guarantee all operations even if PVDD pin voltage is over the startup threshold voltage. Be sure to use this IC within the recommended supply voltage.

- **PVDD Under Voltage Lock Out Function (UVLO)**

  This function, detecting an unusual condition where the voltage at PVDD pin becomes lower than “PVDD pin Shutdown Threshold Voltage”, and prevent malfunction etc. In this low-voltage protection state, digital amplifier outputs become WL state (Weak Low: a state grounded through a high-value resistance). When voltages at PVDD pin become higher than low-voltage cancel threshold voltage (VHUVLH), the low-voltage protection state is cancelled and the normal operation starts after max. 300ms. This function does not guarantee all operations even if PVDD pin voltage is over the startup threshold voltage VHUVLH. Be sure to use this IC within the recommended supply voltage.

- **DC Detection Function (DCDET)**

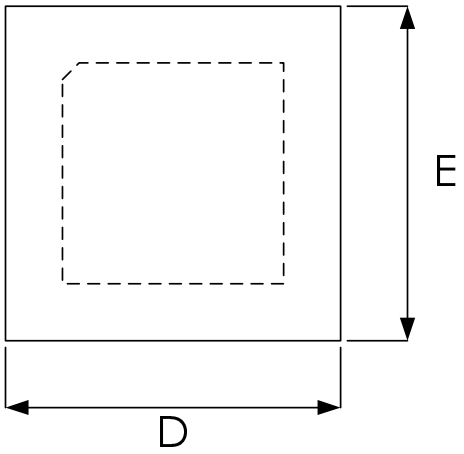
  This function is activated when detecting a DC signal in excess of 3.3V (PVDD=15V) for a given period of time (0.67s to 1.33s) at the digital amplifier output and stops the output. In DC protection state, digital amplifier outputs are forced to WL state (Weak Low: a state grounded through a high-value resistance) and also L level is output to PROTN pin. The automatic recovery operation is performed 2.7 to 5.4 seconds (at fs=48kHz) after the activation of this protection state. When detected eight times in all, the protection state is held without being cancelled. The held protection state can be cancelled by setting SLEEPN pin to “L” temporarily or shutting down the power. This protection function is provided for ensuring safety, and does not guarantee the protection of the speaker.

- **Clock Detection Function (CKDET)**

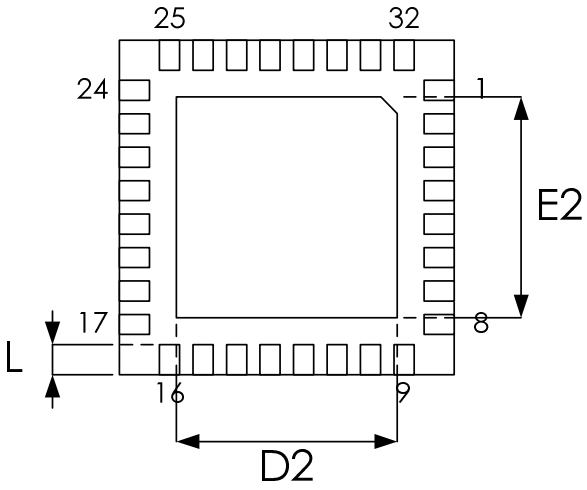
  This is the function to prevent DC signals from being transmitted in case any clock to SCLK or MCLK pin is stopped during the playback. When any clock is stopped, the internal free-running clock supersedes it and the digital amplifier output are forced to WL state (Weak Low: a state grounded through a high-value resistance). And, when a clock is received again at SCLK or MCLK pin, the operation shifts to the normal operation state. This protection function is provided for ensuring safety, and does not guarantee the protection of the speaker.

Package Outline Drawing

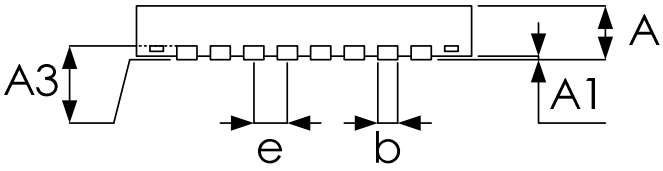
- **QFN 32L (5x5 mm)**



TOP VIEW



BOTTOM VIEW



SIDE VIEW

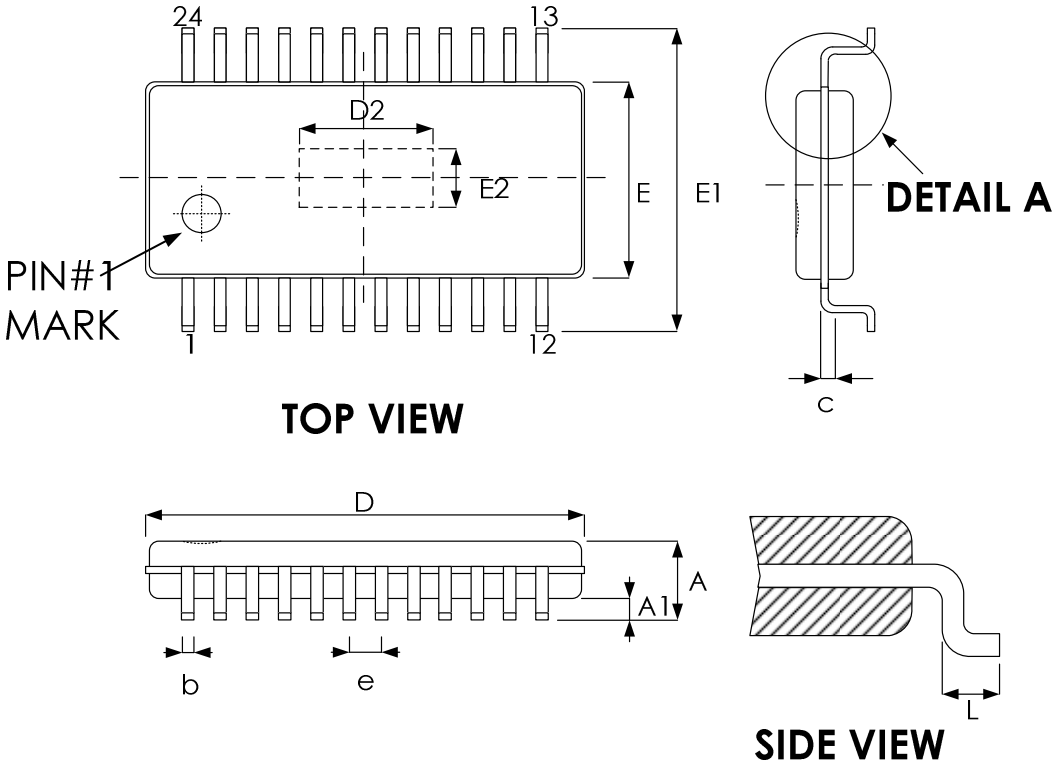
Symbol	Dimension in mm	
	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.203 REF.	
b	0.18	0.30
D	5.00 BSC	
E	5.00 BSC	
e	0.50 BSC	
L	0.35	0.45

Exposed pad

	Dimension in mm	
	Min	Max
D2	3.10	3.25
E2	3.10	3.25

Package Outline Drawing

- **E-TSSOP 24L**



Symbol	Dimension in mm	
	Min	Max
A	1.00	1.20
A1	0.00	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
D2	3.70	4.62
E2	2.20	2.85

Revision History

Revision	Date	Description
0.1	2015.09.14	Original.
0.2	2015.11.30	1. Modify Maximum Instantaneous Output in Electrical Characteristics and Specifications of Loudspeaker Driver 2. Modify description of Gain Setting function. 3. Modify Table 2 in Gain Setting function. 4. Modify Table 4.in Power Limit function.
0.3	2016.04.18	Modify Timing Spec in Interface Configuration.
1.0	2016.07.04	1. Remove preliminary word and modify version to 1.0 2. Modify ordering information
1.1	2016.08.02	Modify ordering information
1.2	2017.01	Modify PVDD voltage range.

Important Notice

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.