
2x20W Stereo / 1x 40W Mono Digital Audio Amplifier With 20 bands EQ Functions, DRC and 2.1CH Mode

Features

- 16/18/20/24-bits input with I²S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
Loudspeaker: 96dB (PSNR), 108dB (DR) @24V
- Multiple sampling frequencies (Fs)
32kHz / 44.1kHz / 48kHz and
64kHz / 88.2kHz / 96kHz and
128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
64x~512x Fs for 64kHz / 88.2kHz / 96kHz
64x~256x Fs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
3.3V for digital circuit
10V~26V for loudspeaker driver
- Supports 2.0CH/2.1CH/Mono configuration
- Loudspeaker output power@24V for stereo
10W x 2CH into 8Ω @0.24% THD+N
15W x 2CH into 8Ω @0.3% THD+N
20W x 2CH into 8Ω @0.38% THD+N
- Sound processing including :
20 bands parametric speaker EQ
Volume control (+24dB~-103dB, 0.125dB/step)
Dynamic range control
Dual Band Dynamic range control
Power Clipping
3D surround sound
Channel mixing
Noise gate with hysteresis window
Bass/Treble tone control
Bass management crossover filter
DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I²C control interface with selectable device address
- Support hardware and software reset
- Internal PLL

- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode

Applications

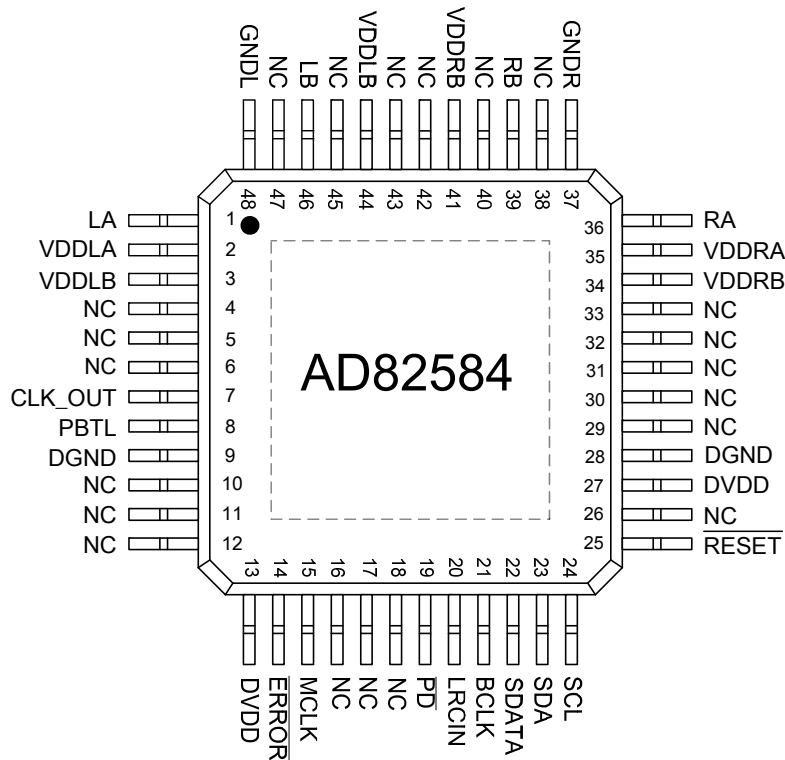
- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

AD82584 is a digital audio amplifier capable of driving 15W (BTL) each to a pair of 8Ω load speaker and 30W (PBTL) to a 4Ω load speaker operating at 24V supply without external heat-sink or fan requirement with play music. AD82584 is also capable of driving 4Ω, 10W (SE)x2 + 8Ω, 20W (BTL)x1 at 24V supply for 2.1CH application.

AD82584 can provide advanced audio processing functions, such as volume control, 20 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I²C control interface. Robust protection circuits are provided to protect AD82584 from damage due to accidental erroneous operating condition. The full digital circuit design of AD82584 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog class-AB or class-D audio amplifier counterpart implemented by analog circuit design. AD82584 is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment



Pin Description

| PIN | NAME | TYPE | DESCRIPTION | CHARACTERISTICS |
|-----|---------|------|--|--|
| 1 | LA | O | Left channel output A | |
| 2 | VDDLA | P | Left channel supply A | |
| 3 | VDDL B | P | Left channel supply B | |
| 4 | NC | | Not connected | |
| 5 | NC | | Not connected | |
| 6 | NC | | Not connected | |
| 7 | CLK_OUT | O | Clock output from PLL | TTL output buffer |
| 8 | PBTL | I | Stereo/Mono configuration pin (0: Stereo ; 1: Mono) | Schmitt trigger TTL input buffer, internal pull low with a 80Kohm resistor |
| 9 | DGND | P | Digital Ground | |
| 10 | NC | | Not connected | |
| 11 | NC | | Not connected | |
| 12 | NC | | Not connected | |
| 13 | DVDD | P | Digital Power | |
| 14 | ERROR | O | Error status, low active | Open-drain output |
| 15 | MCLK | I | Master clock input | Schmitt trigger TTL input buffer |
| 16 | NC | | Not connected | |

| | | | | |
|----|---------------------------|-----|---|----------------------------------|
| 17 | NC | | Not connected | |
| 18 | NC | | Not connected | |
| 19 | $\overline{\text{PD}}$ | I | Power down, low active | Schmitt trigger TTL input buffer |
| 20 | LRCIN | I | Left/Right clock input (Fs) | Schmitt trigger TTL input buffer |
| 21 | BCLK | I | Bit clock input (64Fs) | Schmitt trigger TTL input buffer |
| 22 | SDATA | I | Serial audio data input | Schmitt trigger TTL input buffer |
| 23 | SDA | I/O | I ² C bi-directional serial data | Schmitt trigger TTL input buffer |
| 24 | SCL | I | I ² C serial clock input | Schmitt trigger TTL input buffer |
| 25 | $\overline{\text{RESET}}$ | I | Reset, low active | Schmitt trigger TTL input buffer |
| 26 | NC | | Not connected | |
| 27 | DVDD | P | Digital Power | |
| 28 | DGND | P | Digital Ground | |
| 29 | NC | | Not connected | |
| 30 | NC | | Not connected | |
| 31 | NC | | Not connected | |
| 32 | NC | | Not connected | |
| 33 | NC | | Not connected | |
| 34 | VDDRB | P | Right channel supply B | |
| 35 | VDDRA | P | Right channel supply A | |
| 36 | RA | O | Right channel output A | |
| 37 | GNDR | P | Right channel ground | |
| 38 | NC | | Not connected | |
| 39 | RB | O | Right channel output B | |
| 40 | NC | | Not connected | |
| 41 | VDDRB | P | Right channel supply B | |
| 42 | NC | | Not connected | |
| 43 | NC | | Not connected | |
| 44 | VDDL B | P | Left channel supply B | |
| 45 | NC | | Not connected | |
| 46 | LB | O | Left channel output B | |
| 47 | NC | | Not connected | |
| 48 | GNDL | P | Left channel ground | |