2X20W Stereo / 1X40W Mono Digital Audio Amplifier

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
  Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x, 1024x Fs
  256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz /176.4kHz/192kHz
- Supply voltage
  3.3V for digital circuit
  10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
  10W x 2ch into 8Ω @ 0.16% THD+N
  15W x 2ch into 8Ω @ 0.18% THD+N
  20W x 2ch into 8Ω @ 0.24% THD+N
- Loudspeaker output power for Mono@ 24V
  20W x 1ch into 4Ω @ 0.17% THD+N
  30W x 1ch into 4Ω @ 0.2% THD+N
  40W x 1ch into 4Ω @ 0.24% THD+N
- Sounds processing including:
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Power clipping
  Channel mixing
  User programmed noise gate with hysteresis window
  DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I^2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode
- Dynamic temperature control

Applications

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

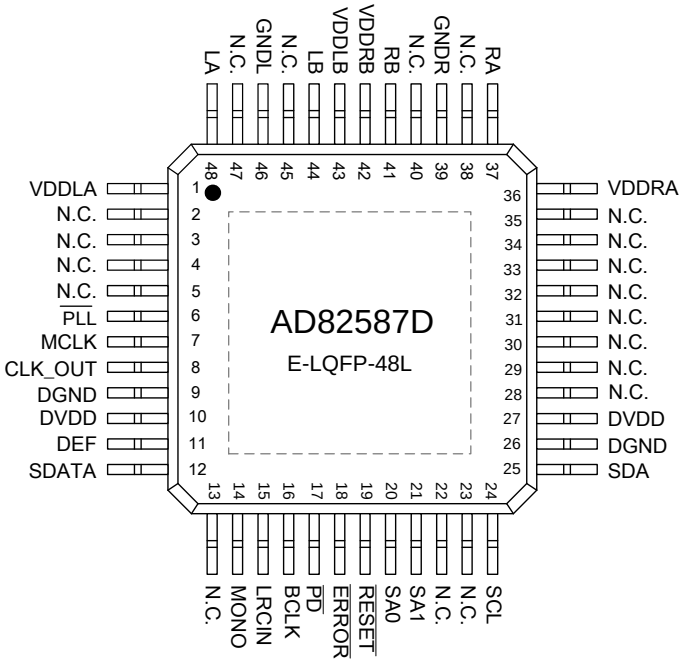
AD82587D is a digital audio amplifier capable of driving a pair of 8Ω,20W or a single 4Ω,40W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

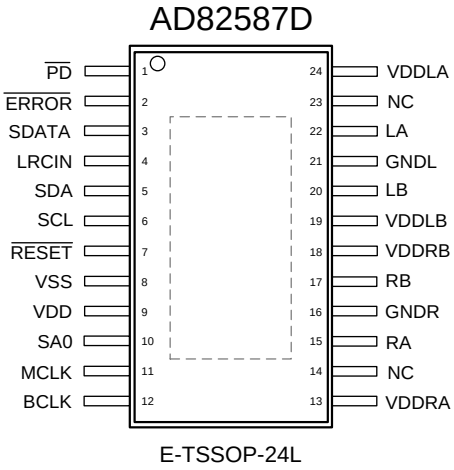
Using I^2C digital control interface, the user can control AD82587D's input format selection, mute and volume control functions. AD82587D has many built-in protection circuits to safeguard AD82587D from connection errors.

ORDERING INFORMATION

Product ID	Package	Packing code	Packing / MPQ	Comments
AD82587D-LG48NA	E-LQFP-48L (7x7 mm)	Y	2.5K Units / Small Box (250 Units / Tray, 10 Trays / Small Box	Green
AD82587D-QG24NA	E-TSSOP 24L	T	62 Units / Tube 100 Tubes / Small Box	Green
AD82587D-QG24NA		R	2.5K Units Tape & Reel	Green

Pin Assignment (Top View)



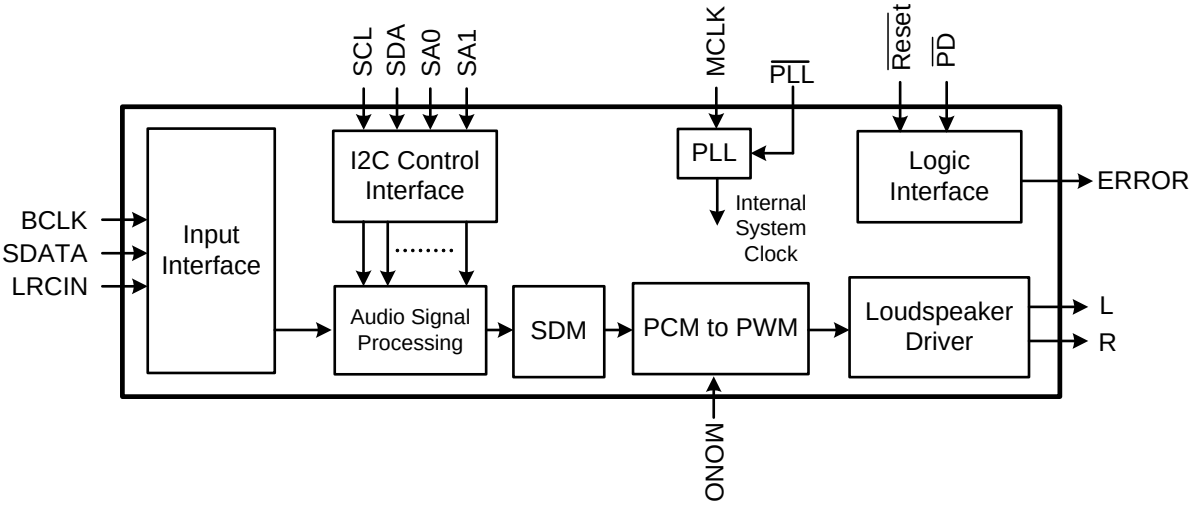


Pin Description

NAME	E-LQFP 48L	E-TSSOP 24L	TYPE	DESCRIPTION	CHARACTERISTICS
VDDLA	1	24	P	Left channel supply A	
N.C.	2	NA	NC		
N.C.	3	NA	NC		
N.C.	4	NA	NC		
N.C.	5	NA	NC		
$\overline{PLL}$	6	NA	I	PLL enable, low active	Schmitt trigger TTL input buffer
MCLK	7	11	I	Master clock input	Schmitt trigger TTL input buffer
CLK_OUT	8	NA	O	Clock output from PLL	TTL output buffer
DGND	9	NA	P	Digital Ground	
DVDD	10	NA	P	Digital Power	
DEF	11	NA	I	Default volume setting	Schmitt trigger TTL input buffer
SDATA	12	3	I	Serial audio data input	Schmitt trigger TTL input buffer
N.C.	13	NA	NC		
MONO	14	NA	I	MONO mode enable, high active	Schmitt trigger TTL input buffer
LRCIN	15	4	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer
BCLK	16	12	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer
$\overline{PD}$	17	1	I	Power down, low active	Schmitt trigger TTL input buffer
$\overline{ERROR}$	18	2	O	Error status, low active	Open-drain output

$\overline{\text{RESET}}$	19	7	I	Reset, low active	Schmitt trigger TTL input buffer
SA0	20	10	I	I^2C select address 0	Schmitt trigger TTL input buffer
SA1	21	NA	I	I^2C select address 1	Schmitt trigger TTL input buffer
N.C.	22	NA	NC		
N.C.	23	NA	NC		
SCL	24	6	I	I^2C serial clock input	Schmitt trigger TTL input buffer
SDA	25	5	I/O	I^2C bi-directional serial data	Schmitt trigger TTL input buffer
DGND	26	8	P	Digital Ground	
DVDD	27	9	P	Digital Power	
N.C.	28	NA	NC		
N.C.	29	NA	NC		
N.C.	30	NA	NC		
N.C.	31	NA	NC		
N.C.	32	NA	NC		
N.C.	33	NA	NC		
N.C.	34	NA	NC		
N.C.	35	NA	NC		
VDDRA	36	13	P	Right channel supply A	
RA	37	15	O	Right channel output A	
N.C.	38	14	NC		
GNDR	39	16	P	Right channel ground	
N.C.	40	NA	NC		
RB	41	17	O	Right channel output B	
VDDRB	42	18	P	Right channel supply B	
VDDLB	43	19	P	Left channel supply B	
LB	44	20	O	Left channel output B	
N.C.	45	NA	NC		
GNDL	46	21	P	Left channel ground	
N.C.	47	23	NC		
LA	48	22	O	Left channel output A	

Functional Block Diagram



Available Package

Package Type	Device No.	θ ja(℃/W)	Ψ jt(℃/W)	θ jt(℃/W)	Exposed Thermal Pad
E-LQFP-48L	AD82587D	22.9	1.05	34.9	Yes (Note1)
E-TSSOP 24L		26.8	0.35	27.1	

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface.

Note 1.4: Ψ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface center.

Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_J	Junction Operating Temperature	0~125	^oC
T_A	Ambient Operating Temperature	0~70	^oC

General Electrical Characteristics

Condition: T_A=25 ^oC (unless otherwise specified).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}(HV)	PVDD Supply Current during Power Down	PVDD=24V		40	200	uA
I_{PD}(LV)	DVDD Supply Current during Power Down	DVDD=3.3V		4	20	uA
T_{SENSOR}	Junction Temperature for Driver Shutdown			160		^oC
	Temperature Hysteresis for Recovery from Shutdown			35		^oC
UV_H	Under Voltage Disabled (For DVDD)			2.8		V
UV_L	Under Voltage Enabled (For DVDD)			2.7		V
Rds-on	Static Drain-to-Source On-state Resistor, PMOS	PVDD=24V, Id=500mA		260		mΩ
	Static Drain-to-Source On-state Resistor, NMOS			175		mΩ
I_{SC}	L(R) Channel Over-Current Protection (Note 2)	PVDD=24V		5.2		A
	Mono Channel Over-Circuit Protection (Note 2)	PVDD=24V		10.4		A
V_{IH}	High-Level Input Voltage	DVDD=3.3V	2.0			V
V_{IL}	Low-Level Input Voltage	DVDD=3.3V			0.8	V
V_{OH}	High-Level Output Voltage	DVDD=3.3V	2.4			V
V_{OL}	Low-Level Output Voltage	DVDD=3.3V			0.4	V
C_I	Input Capacitance			6.4		pF

Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Marking Information

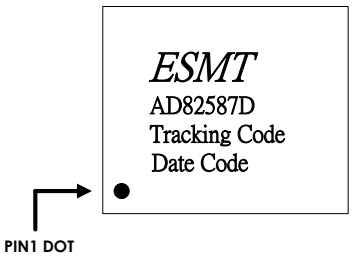
AD82587D

Line 1 : LOGO

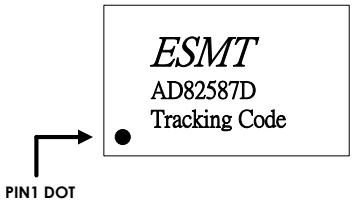
Line 2 : Product no.

Line 3 : Tracking Code

Line 4 : Date Code

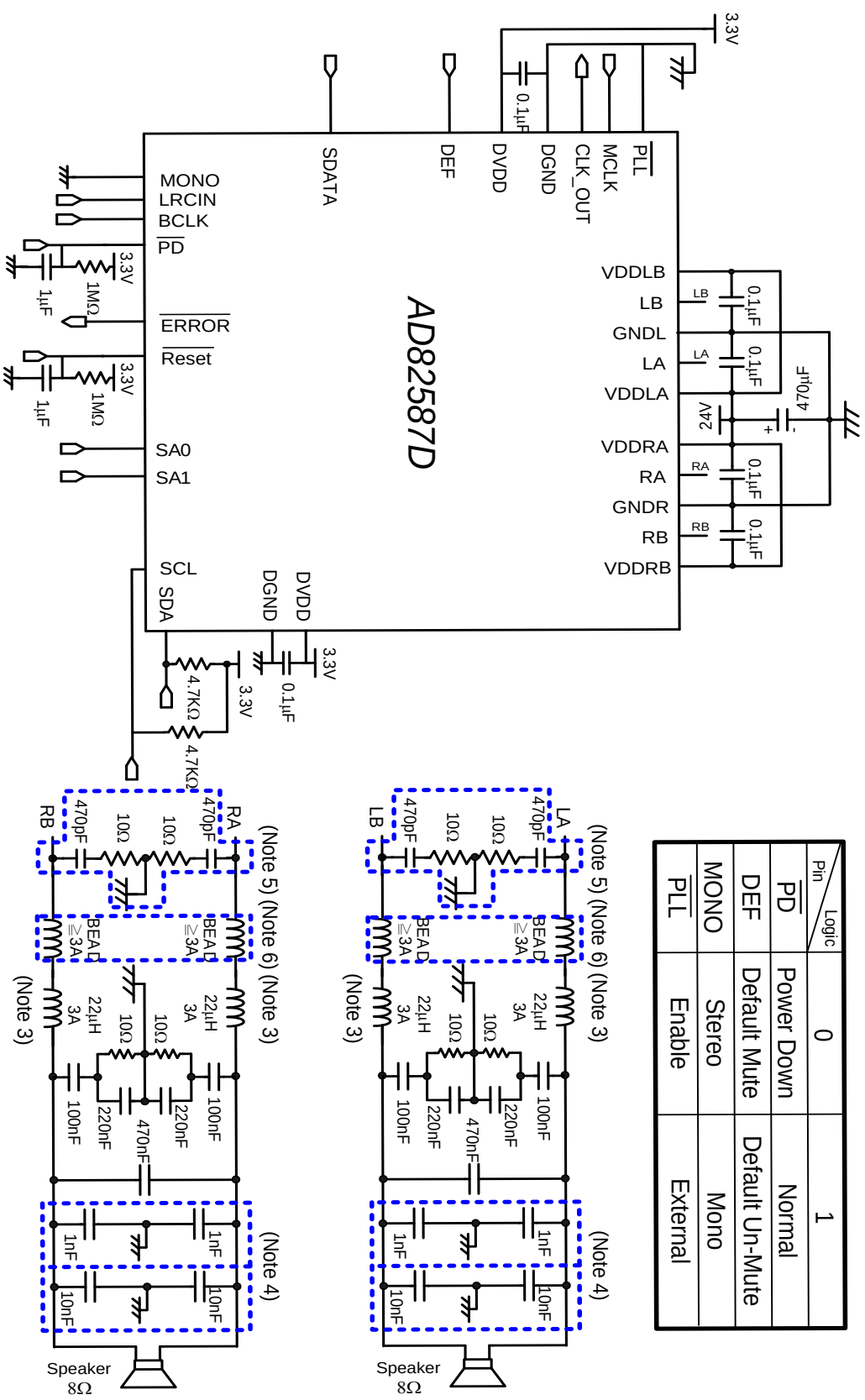


E-LQFP 48L



E-TSSOP-24L

Application Circuit Example for Stereo



Pin / Logic	0	1
PD	Power Down	Normal
DEF	Default Mute	Default Un-Mute
MONO	Stereo	Mono
PLL	Enable	External

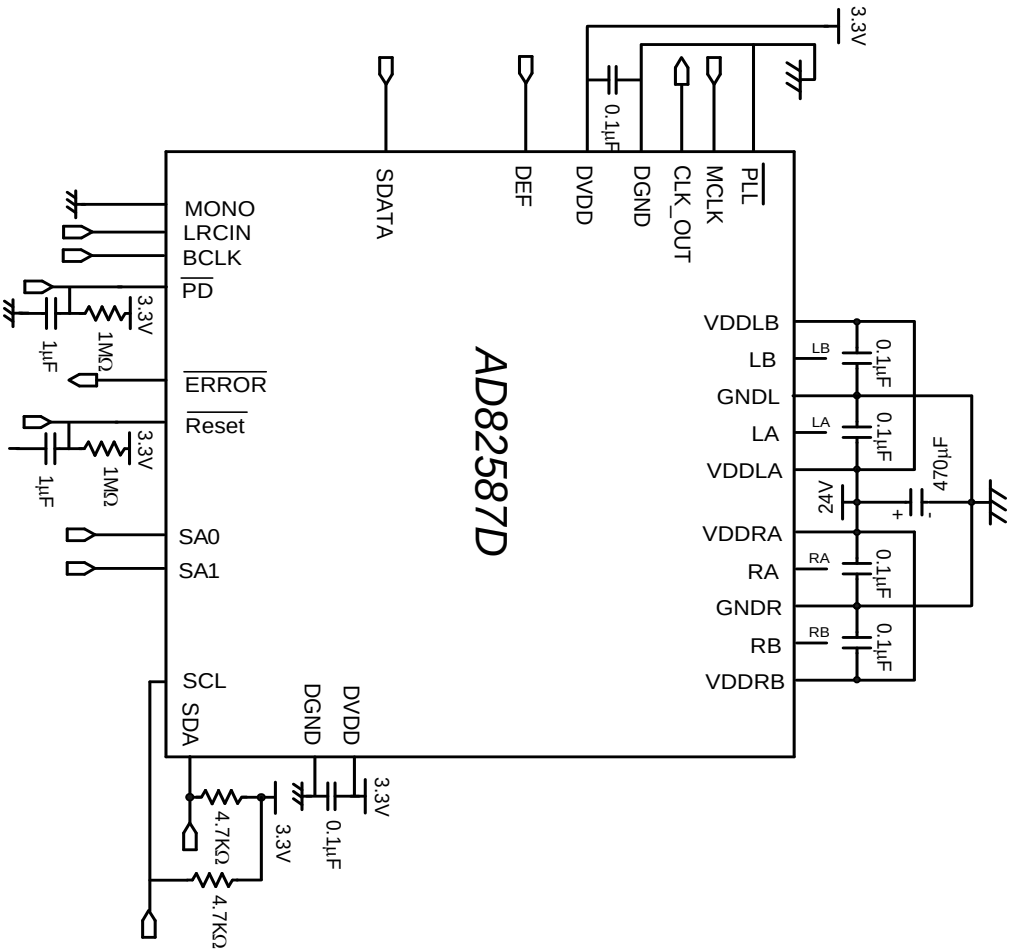
Note 3: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 5A.

Note 4: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

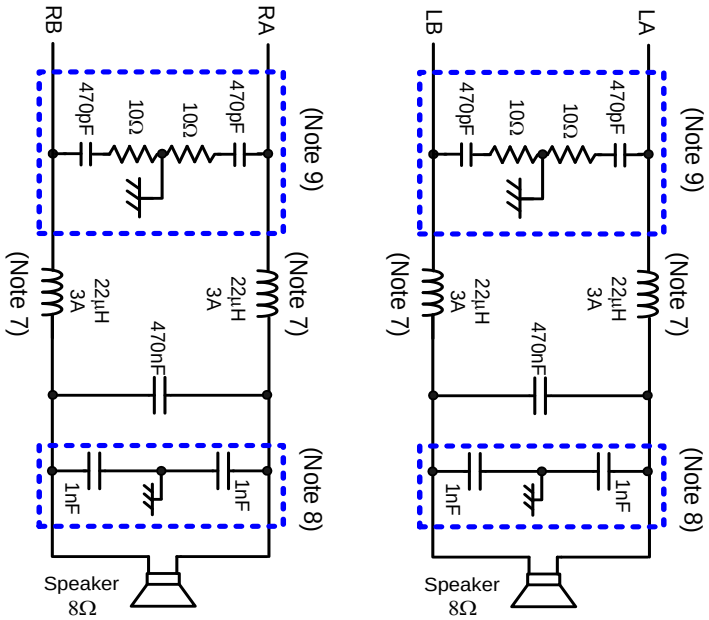
Note 5: The snubber circuit can be removed while the PVDD <=20V.

Note 6: The bead (option component) can be removed if the system EMI test result is good enough.

Application Circuit Example for Stereo (Economic type, moderate EMI suppression)



Pin / Logic	0	1
PD	Power Down	Normal
DEF	Default Mute	Default Un-Mute
MONO	Stereo	Mono
PLL	Enable	External

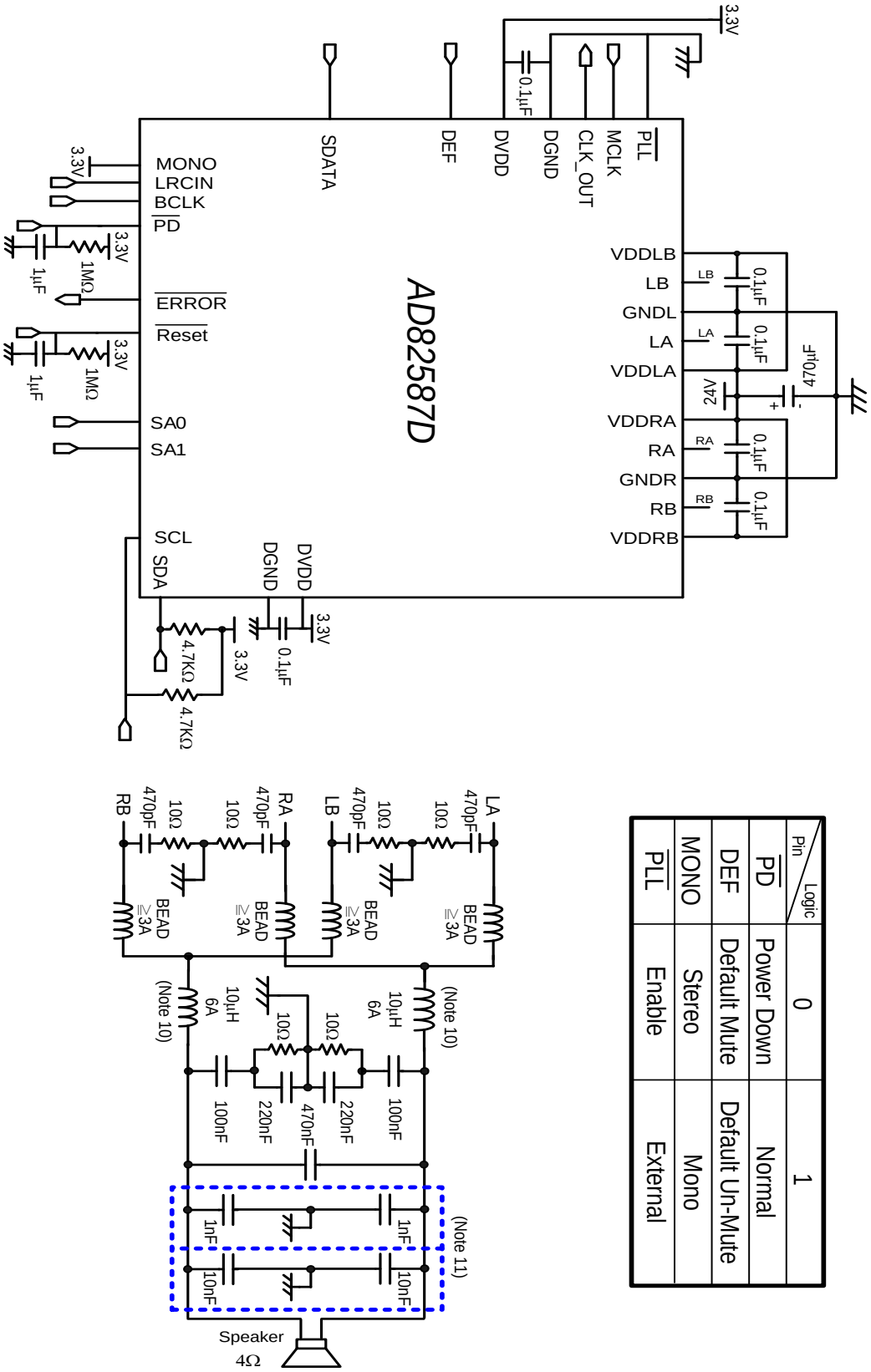


Note 7: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 5A.

Note 8: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 9: The snubber circuit can be removed while the PVDD <=20V.

Application Circuit Example for Mono



Pin / Logic	0	1
PD	Power Down	Normal
DEF	Default Mute	Default Un-Mute
MONO	Stereo	Mono
PLL	Enable	External

Note 10: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 10A.

Note 11: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Electrical Characteristics and Specifications for Loudspeaker

- **Stereo output with 24V supply voltage**

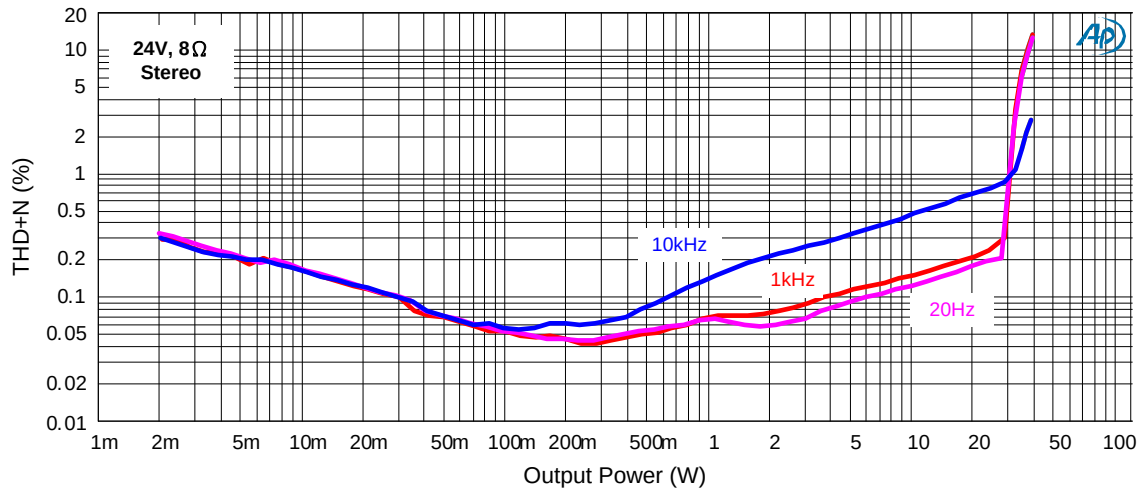
Condition: T_A=25 °C, DVDD=3.3V, VDDL=VDDR=24V, F_S=48kHz, Load=8Ω with passive LC lowpass filter (L=22μ H with R_{DC}=0.12Ω , C=470nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 13)	RMS Output Power (THD+N=0.21%)	+8dB volume			20		W
	RMS Output Power (THD+N=0.18%)				15		W
	RMS Output Power (THD+N=0.16%)				10		W
THD+N	Total Harmonic Distortion + Noise	P_O=7.5W			0.14		%
SNR	Signal to Noise Ratio (Note 12)	+8dB volume	-9dB		97		dB
DR	Dynamic Range (Note 12)	+8dB volume	-68dB		105		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz			77		dB
	Channel Separation (non-shield choke)	P_O=1W at 1kHz			70		dB

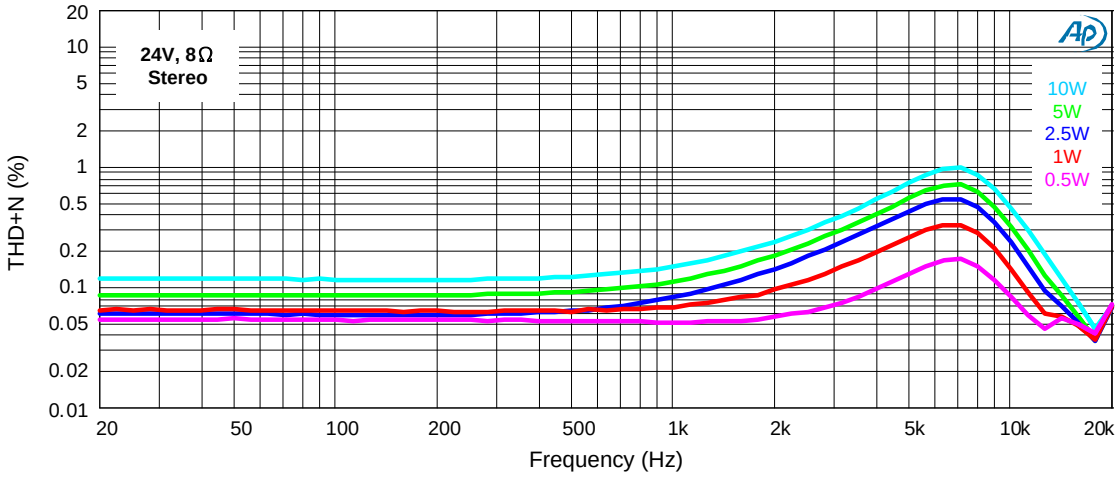
Note 12: Measured with A-weighting filter.

Note 13: Thermal dissipation is limited by package type and PCB design, the external heat-sink or system cooling method should be adopted for RMS power output.

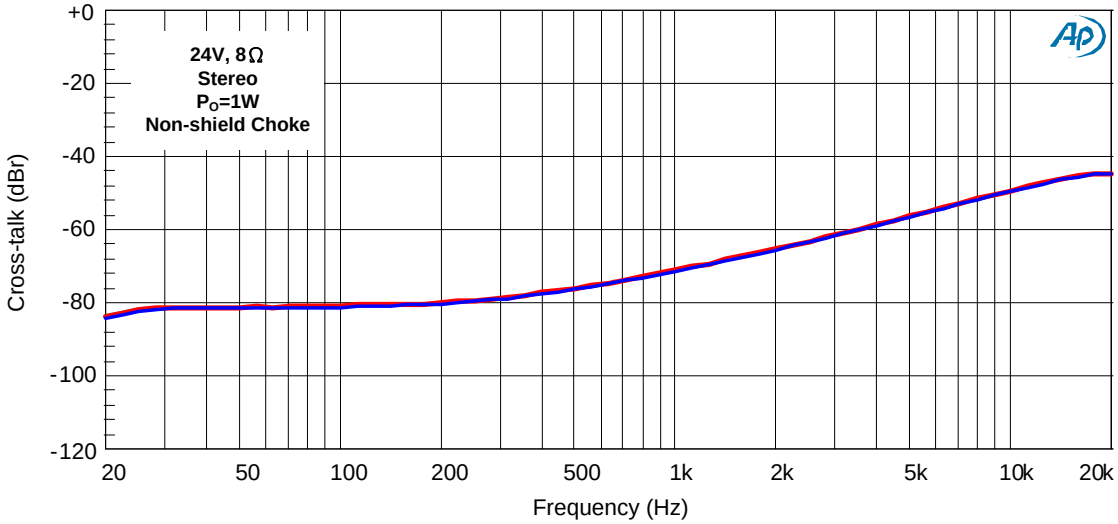
Total Harmonic Distortion + Noise vs. Output Power (Stereo)



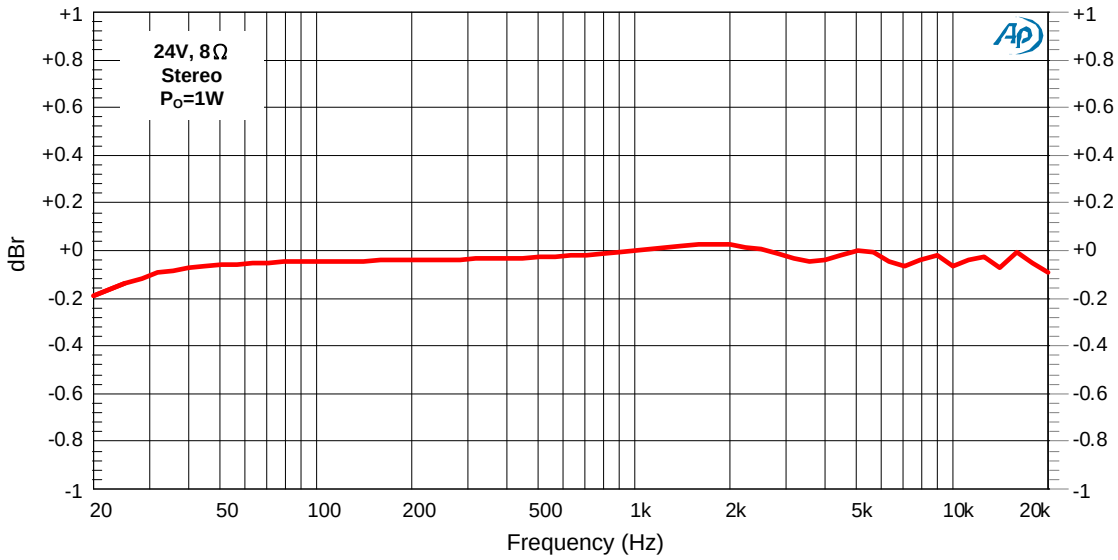
Total Harmonic Distortion + Noise vs. Frequency (Stereo)



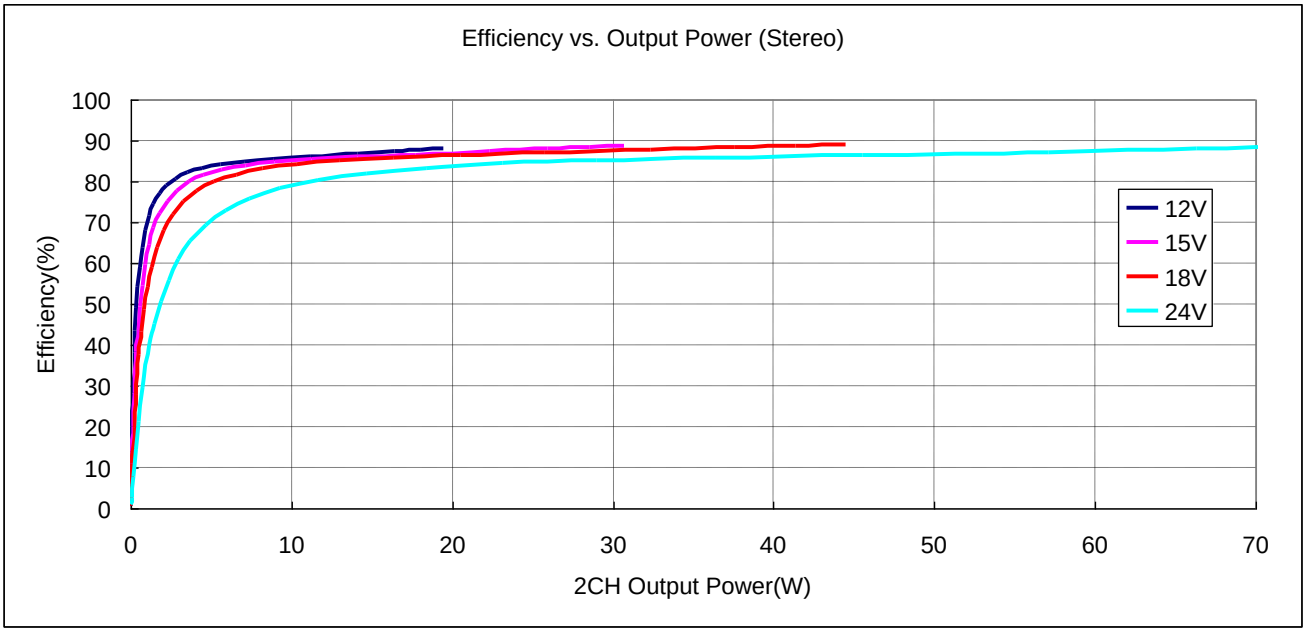
Cross-talk (Stereo)



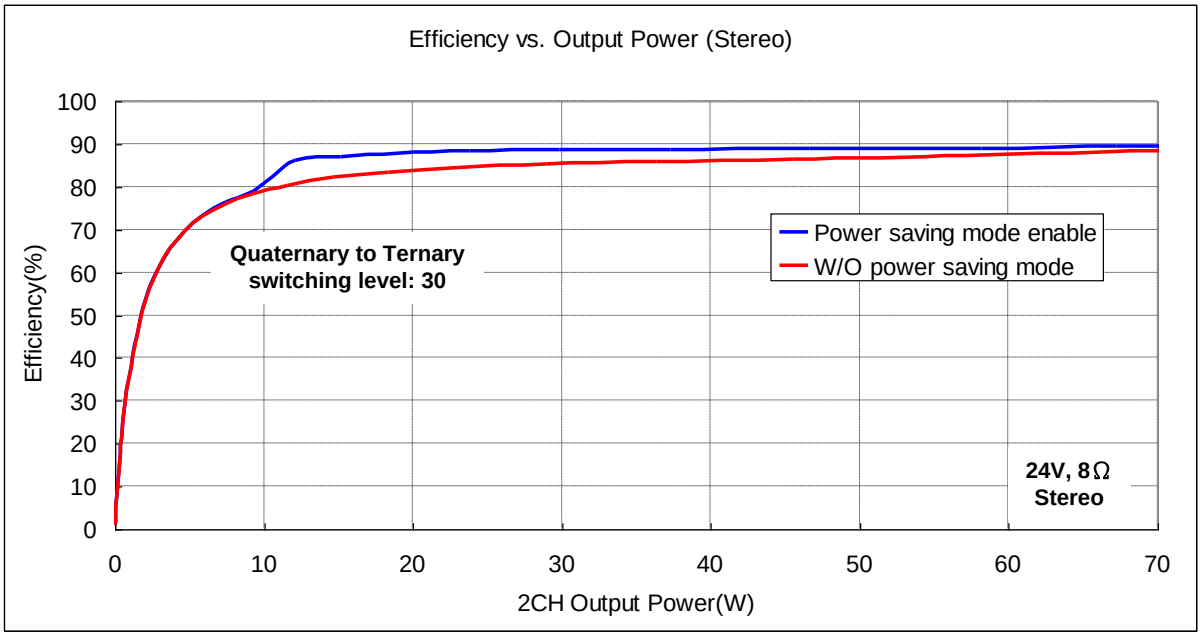
Frequency Response (Stereo)



Efficiency (Stereo)



Efficiency (Stereo) for PWM of Power Saving Mode



Electrical Characteristics and Specifications for Loudspeaker

- **Mono output with 24V supply voltage**

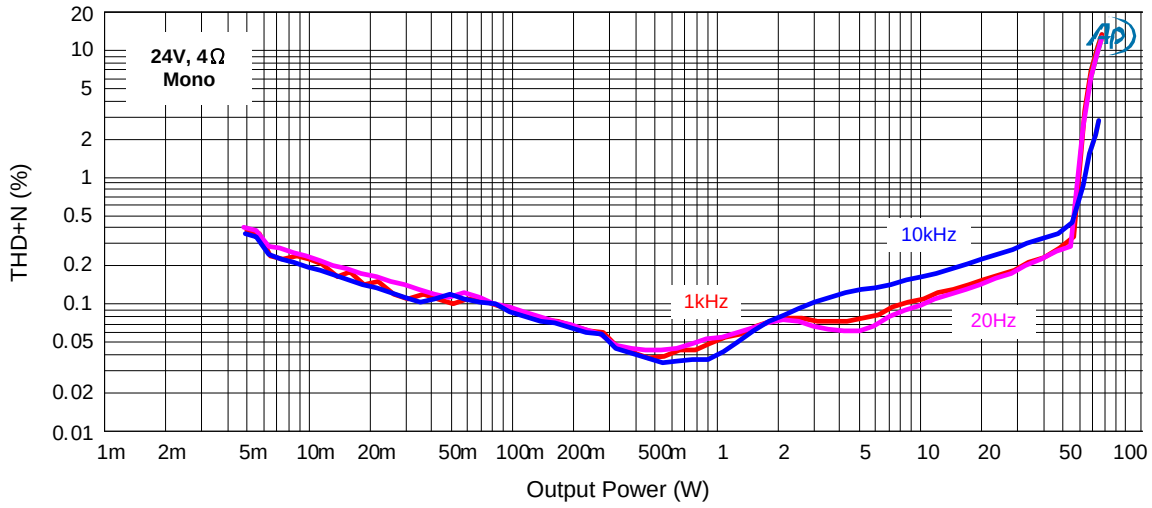
Condition: T_A=25 °C, DVDD=3.3V, VDDL=VDDR=24V, F_S=48kHz, Load=4Ω with passive LC lowpass filter (L=10μ H with R_{DC}=27mΩ , C=470nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 13)	RMS Output Power (THD=0.24%)	+8dB volume			40		W
	RMS Output Power (THD=0.2%)	+8dB volume			30		W
	RMS Output Power (THD=0.17%)	+8dB volume			20		W
THD+N	Total Harmonic Distortion + Noise	P_o=15W			0.15		%
SNR	Signal to Noise Ratio(Note 12)	+8dB volume	-9dB		97		dB
DR	Dynamic Range(Note 12)	+8dB volume	-68dB		105		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz			77		dB

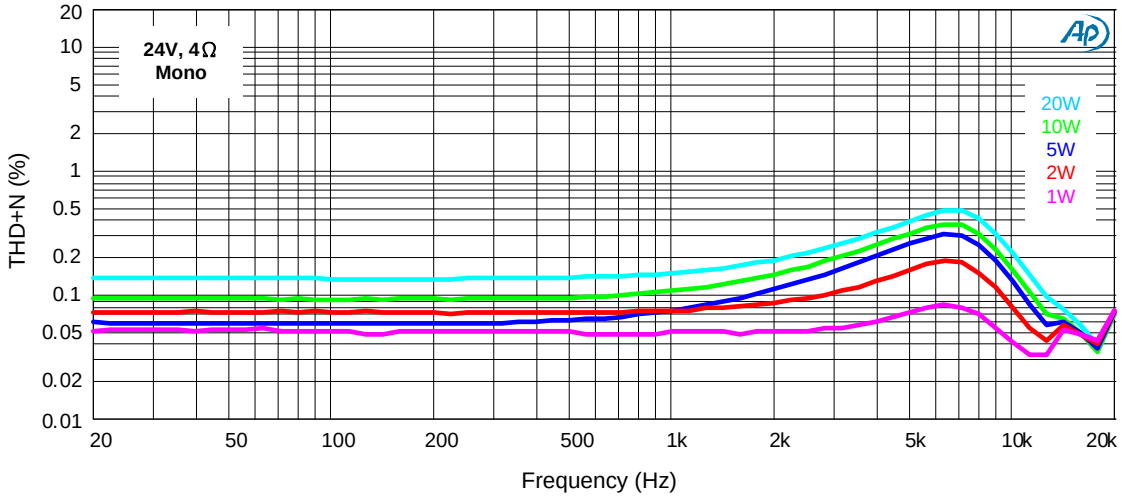
Note 12: Measured with A-weighting filter.

Note 13: Thermal dissipation is limited by package type and application PCB design, the external heat-sink or system cooling method should be adopted for maximum power output.

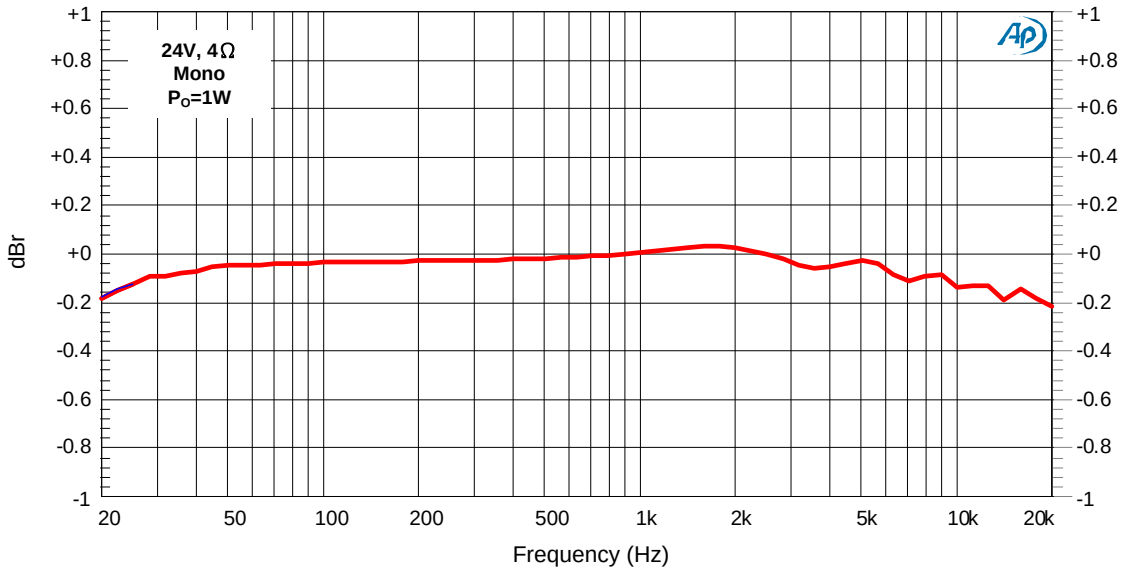
Total Harmonic Distortion + Noise vs. Output Power (Mono)



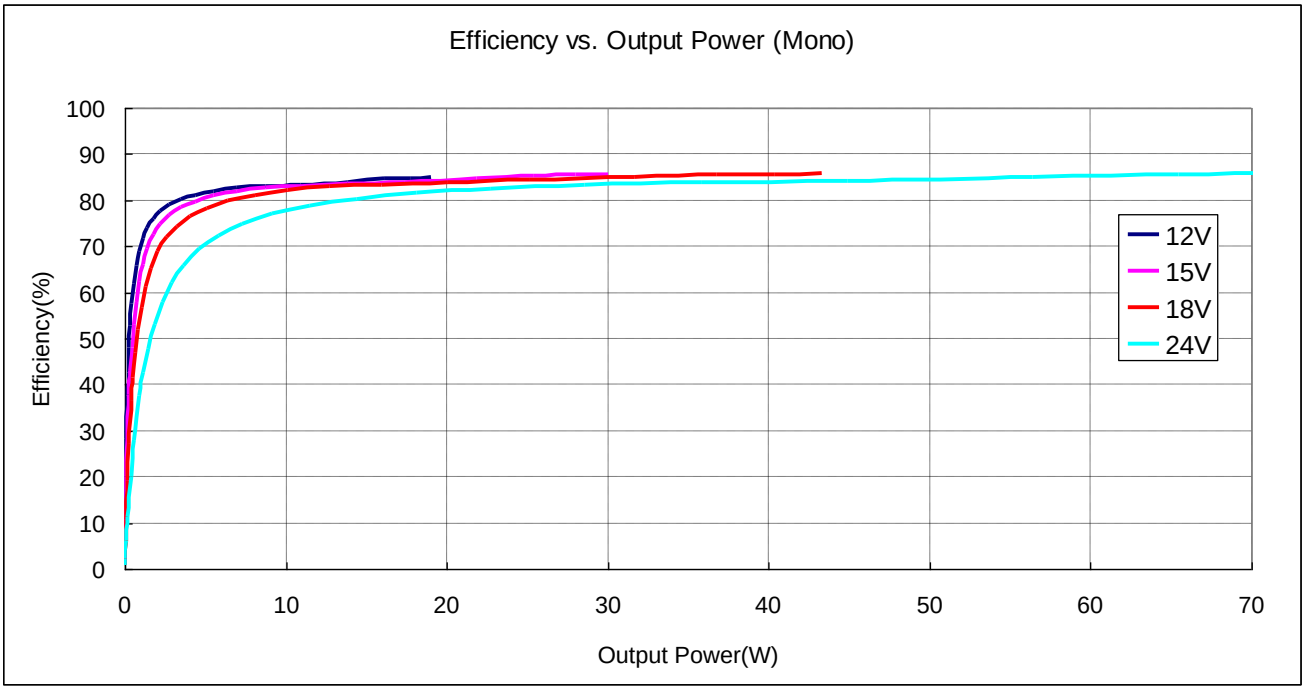
Total Harmonic Distortion + Noise vs. Frequency (Mono)



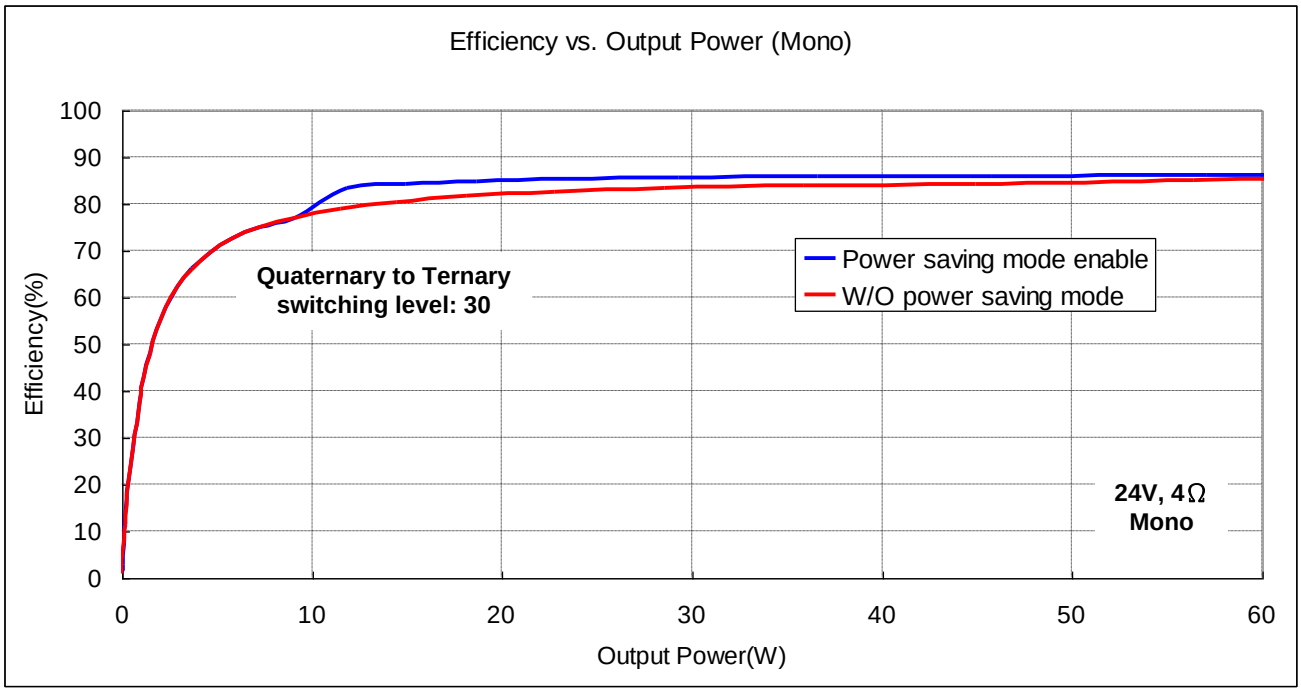
Frequency Response (Mono)



Efficiency (Mono)

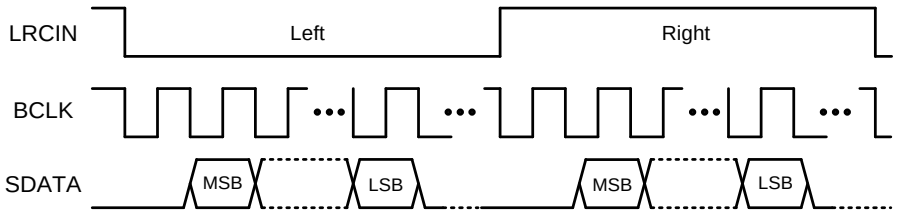


Efficiency (Mono) for PWM of Power Saving Mode

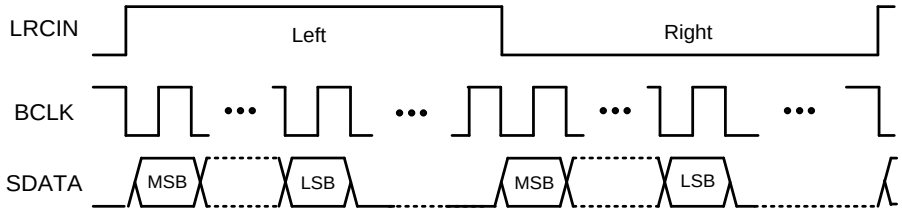


Interface Configuration

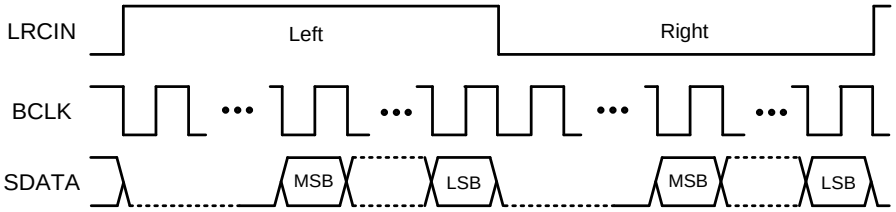
- I^2S



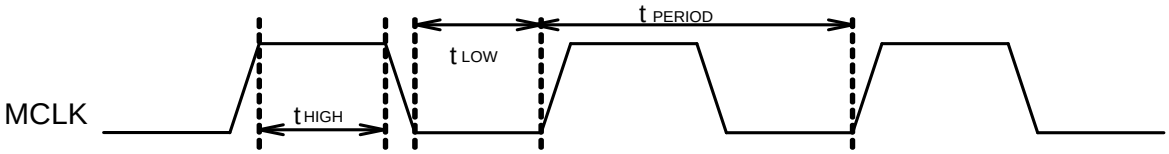
- Left-Alignment



- Right-Alignment

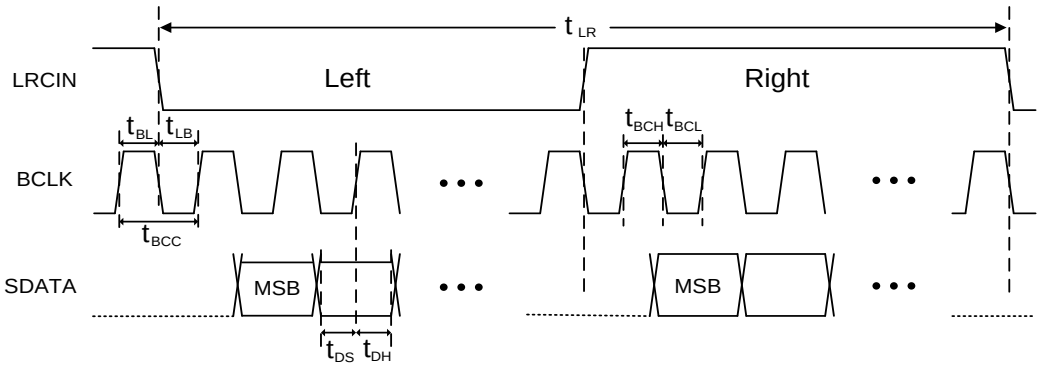


- System Clock Timing



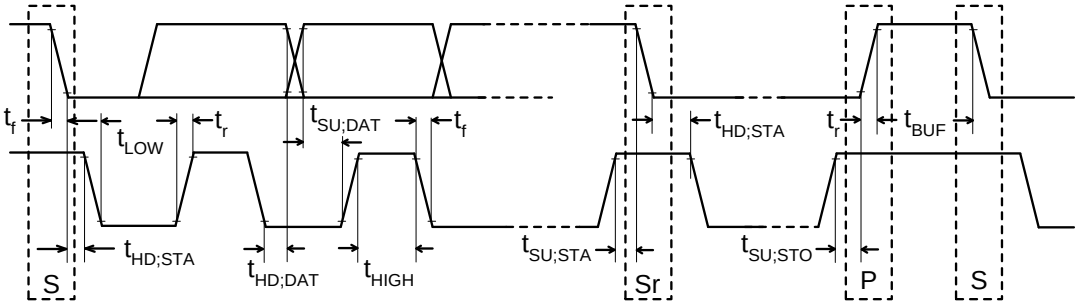
$t_{HIGH} \geqq 40.4$ ns , $t_{LOW} \geqq 40.4$ ns , $t_{PERIOD} \geqq 80.8$ ns	Default setting,when PLL is enable
$t_{HIGH} \geqq 10.1$ ns , $t_{LOW} \geqq 10.1$ ns , $t_{PERIOD} \geqq 20.2$ ns	When PLL is disable

- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	10.41		31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	50			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	50			ns
t_{BCC}	BCLK Period ($1/64F_S$)	162.76		488.3	ns
t_{BCH}	BCLK Pulse Width High	81.38		244	ns
t_{BCL}	BCLK Pulse Width Low	81.38		244	ns
t_{DS}	SDATA Set-Up Time	50			ns
t_{DH}	SDATA Hold Time	50			ns

- I^2C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time for repeated START condition	$t_{HD,STA}$	4.0	---	0.6	---	μs
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	μs
Setup time for repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	μs
Hold time for I^2C bus data	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Setup time for I_2C bus data	$t_{SU;DAT}$	250	---	100	---	ns
Rise time of both SDA and SDL signals	t_r	---	1000	20+0.1Cb	300	ns
Fall time of both SDA and SDL signals	t_f	---	300	20+0.1Cb	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	μs
Bus free time between STOP and the next START condition	t_{BUF}	4.7	---	1.3	---	μs
Capacitive load for each bus line	C_b		400		400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	---	$0.1V_{DD}$	---	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	---	$0.2V_{DD}$	---	V

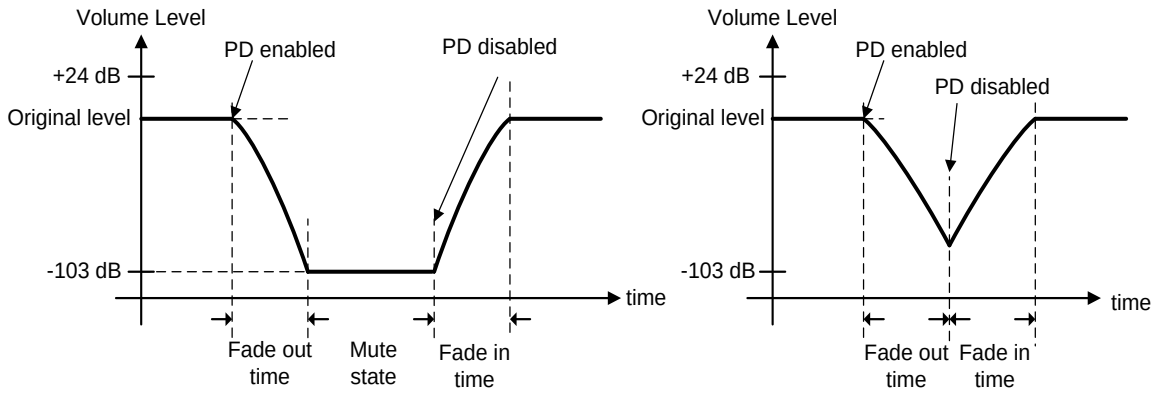
Operation Description

- Reset

When the $\overline{\text{RESET}}$ pin is lowered, AD82587D will clear the stored data and reset the register table to default values. AD82587D will exit reset state at the 256th MCLK cycle after the $\overline{\text{RESET}}$ pin is raised to high.

- Power down control

AD82587D has a built-in volume fade-in/fade-out design for PD/Mute function. The relative PD timing diagrams for loudspeakers are shown below.



$$(10^{\frac{target(dB)}{80}} - 10^{\frac{original(dB)}{80}}) x 512 x (1/96K)$$

The volume level will be decreased to -∞dB in several LRCIN cycles. Once the fade-out procedure is finished, AD82587D will turn off the power stages, clock signals (for digital circuits) and current (for analog circuits). After PD pin is pulled low, AD82587D requires T_{fade} to finish the forementioned work before entering power down state. Users can not program AD82587D during power down state. Also, all settings in the registers will remain intact unless DVDD is removed.

If the PD signal is removed during the fade-out procedure (above, right figure), AD82587D will still execute the fade-in procedure. In addition, AD82587D will establish the analog circuits' bias current and send the clock signals to digital circuits. Afterwards, AD82587D will return to its normal status.

- Internal PLL ($\overline{PLL}$)

AD82587D has a built-in PLL with multiple MCLK/FS ratio, which is selected by I^2C control interface. If $\overline{PLL}$ pin is pulled low, the built-in PLL is enabled; if $\overline{PLL}$ pin is pulled high, an external clock source for MCLK less than 50MHz should be provided. The MCLK/FS ratio will be fixed at 1024x, 512x, or 256x with a sample frequency of 48kHz, 96kHz, or 192kHz respectively.

When using AD82587D without I^2C control interface, the operation is as follows.

$\overline{PLL}$ pin is set to high:

Internal PLL is bypassed (Disable). The following master clock frequency is inputted into a MCLK pin by the sampling frequency. When the following master clock frequency cannot be inputted, $\overline{PLL}$ pin is set low. A career clock frequency is the frequency divided by 128 of master clock.

Fs	MCLK frequency	PWM career frequency
48kHz	49.152MHz	384kHz
44.1kHz	45.158MHz	352.8kHz
32kHz	32.768MHz	256kHz

$\overline{PLL}$ pin is set to low:

Internal PLL is enabled. The master clock inputted into the MCLK pin becomes the frequency of quad edge evaluation. A career clock frequency is the frequency divided by 32 of master clock.

Fs	MCLK/FS Setting Ratio for PLL	MCLK Frequency	Multiple edge evaluation for master clock	PWM Career Frequency
48kHz	256x	12.288MHz	4x	384kHz
44.1kHz	256x	11.289MHz	4x	352.8kHz
32kHz	256x	8.192MHz	4x	256kHz

- Anti-pop design

AD82587D will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- Default volume (DEF)

The volume of AD82587D is +1.625dB when DEF pin is high, and the volume is muted when DEF pin low. When using AD82587D without I2C control interface, user should set the pin high. The user can change the values of the register table setting for volume control. For detailed information, refer to the register table section.

- Self-protection circuits

AD82587D has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

(i) When the internal junction temperature is higher than 160℃, power stages will be turned off and AD82587D will return to normal operation once the temperature drops to 125℃. The temperature values may vary around 10%.

(ii) The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or GND/VDD. For normal 24V operations, the current flowing through the power stage will be less than 5A for stereo configuration or less than 10A for mono configuration. Otherwise, the short-circuit detectors may pull the $\overline{\text{ERROR}}$ pin to DGND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain $\overline{\text{ERROR}}$ pin will be pulled low and latched into ERROR state. Once the over-temperature or short-circuit condition is removed, AD82587D will exit ERROR state when one of the following conditions is met: (1) $\overline{\text{RESET}}$ pin is pulled low, (2) $\overline{\text{PD}}$ pin is pulled low, (3) Master mute is enabled through the I^2C interface.

(iii) Once the DVDD voltage is lower than 2.7V, AD82587D will turn off its loudspeaker power stages and cease the operation of digital processing circuits. When DVDD becomes larger than 2.8V, AD82587D will return to normal operation.

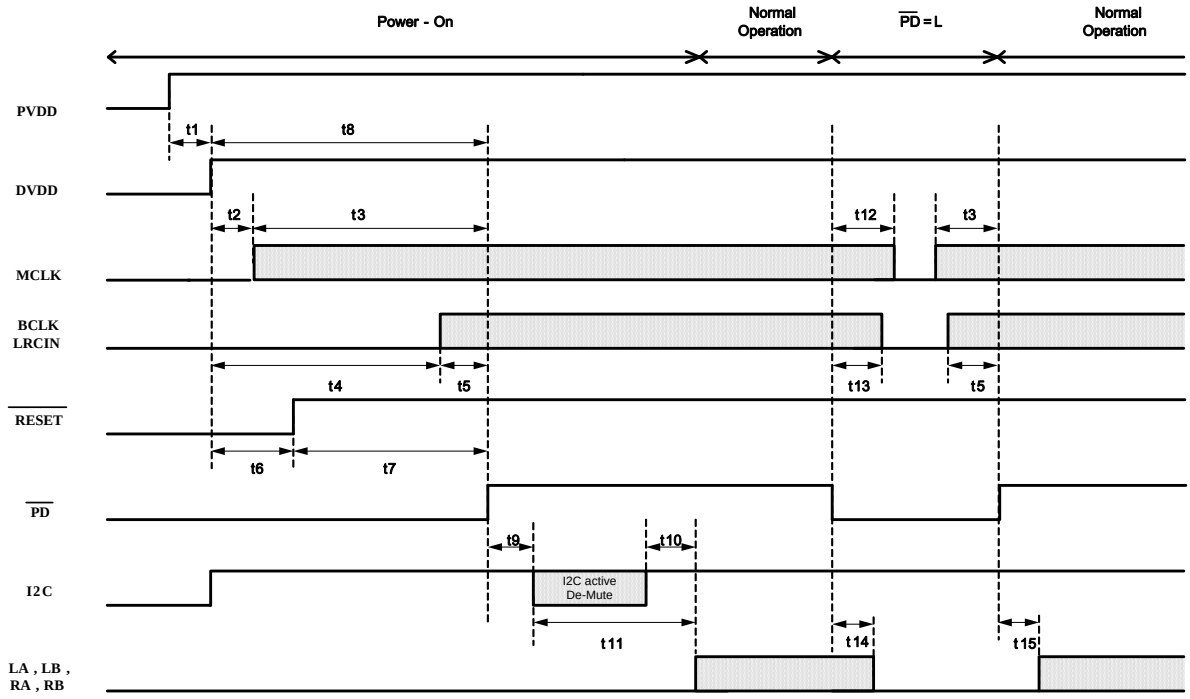
(iv) If the master clock inputted into MCLK pin stops during the period for 500 ns or more, AD82587D detect the stop of MCK. In this state, amplifier outputs are forced to Weak Low. If master clock is inputted normally again, $\overline{\text{ERROR}}$ pin is set to low. AD82587D won't leave ERROR state until one of the following conditions: (1) $\overline{\text{Reset}}$ pin is pulled low, (2) $\overline{\text{PD}}$ pin is pulled low, (3) Programming master mute via I^2C interface.

$\overline{\text{PD}}$ pin is set to low, when stop the clock inputted into MCLK, BCLK, and LRCIN during operation.

(v) If it will be in the state where PVDD power supply is OFF and DVDD power supply is ON, $\overline{\text{ERROR}}$ pin is set to Low.

- Power on sequence

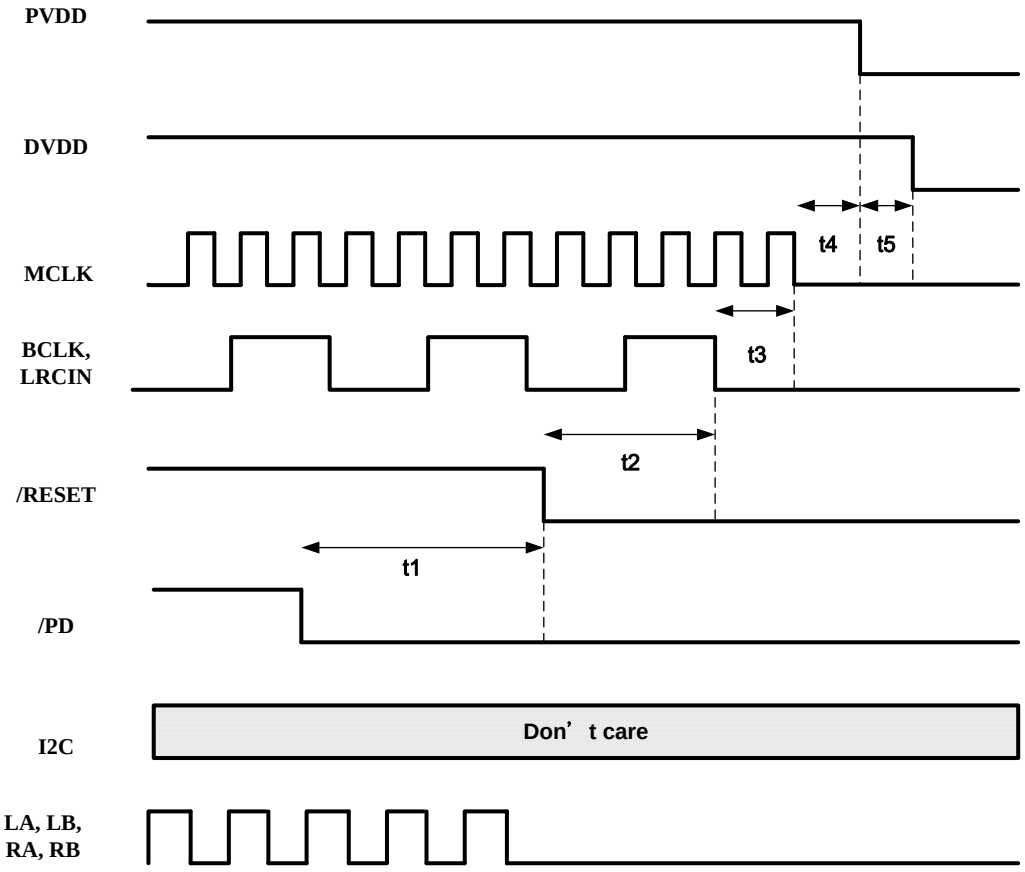
Hereunder is AD82587D's power on sequence. Please note that we suggested users set DEF pin at low state initially, and than give a de-mute command via I^2C when the whole system is stable.



Symbol	Condition	Min	Max	Units
t1		0	-	msec
t2		0	-	msec
t3		10	-	msec
t4		0	-	msec
t5		10	-	msec
t6		10	-	msec
t7		0	-	msec
t8		200	-	msec
t9		20	-	msec
t10	DEF=L	-	1	msec
t11	DEF=H	-	1	msec
t12		25	-	msec
t13		25	-	msec
t14		-	22	msec
t15	DEF= L or H	-	1	msec

- Power off sequence

Hereunder is AD82587D's power off sequence.



Symbol	Condition	Min	Max	Units
t1		35	-	msec
t2		0.1	-	msec
t3		0	-	msec
t4		1	-	msec
t5		1	-	msec

I²C-Bus Transfer Protocol

- Introduction

  AD82587D employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD82587D is always an I²C slave device.

- Protocol

  - START and STOP condition

    START is identified by a high to low transition of the SDA signal.. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD82587D and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

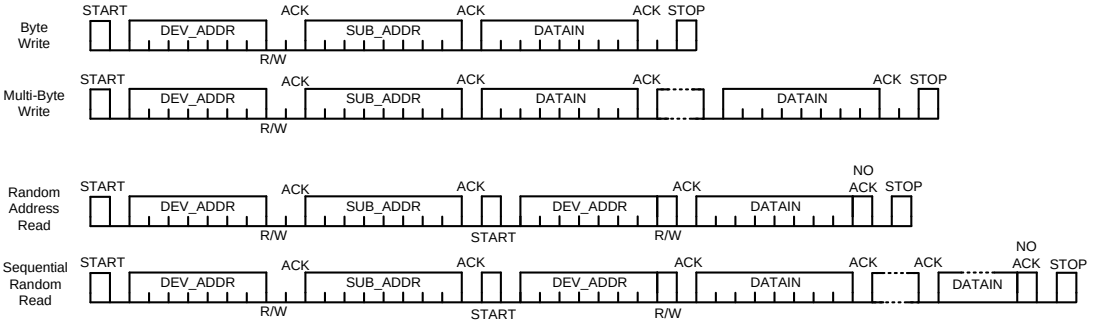
    The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD82587D samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

    The master generates 7-bit address to recognize slave devices. When AD82587D receives 7-bit address matched with 0110x0y for E-LQFP 48L package (where x and y can be selected by external SA0 and SA1 pins, respectively) and address matched with 0110x00 for E-TSSOP 24L package (where x can be selected by external SA0 pin), AD82587D will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD82587D internal sub-addresses.

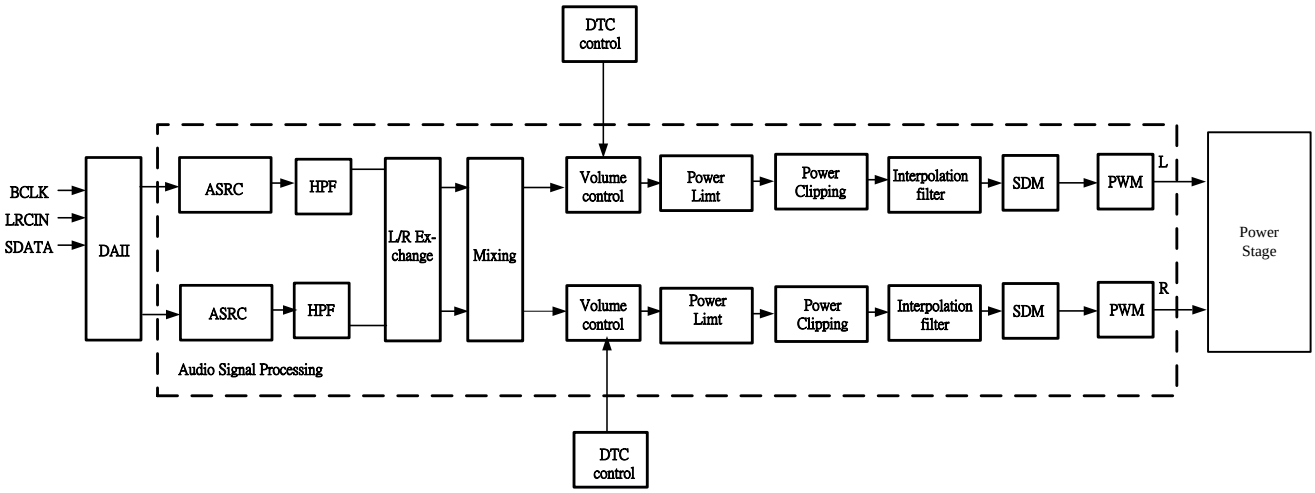
  - Data transferring

    Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD82587D supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



Register Table

The audio signal processing data flow is shown as the following figure. Users can control these function by programming appropriate setting to register table. In this section, the register table is summarized first. The definition of each register follows in the next section.



Address	Register	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0X00	SCTL1	IF[2]	IF[1]	IF[0]	LREXC	PWML_X	PWMRX	PwmMode	NGE
0X01	SCTL 2	Reserved		FS[1]	FS[0]	PMF[3]	PMF[2]	PMF[1]	PMF[0]
0X02	SCTL 3	EN_CLKO	HPB	LV_UVSEL	SW_RSTB	MUTE	CM1	CM2	CompSDMEn
0X03	MVOL	MV[7]	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]
0X04	C1VOL	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
0X05	C2VOL	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
0X06	HVUV	DIS_HVUV	Reserved			HVUVSEL[3]	HVUVSEL[2]	HVUVSEL[1]	HVUVSEL[0]
0X07	SCTL 4	C1MX_EN	C2MX_EN	PC_EN	DRC_EN	MONO_EN	Reserved		
0X08	LAR	LA[3]	LA[2]	LA[1]	LA[0]	LR[3]	LR[2]	LR[1]	LR[0]
0X09	QT_SW_LEVEL	Reserved			QTS[4]	QTS[3]	QTS[2]	QTS[1]	QTS[0]
0X0A		Reserved							
0X0B	OC SET	Reserved							
0X0C	STATUS	Reserved							
0X0D	ACFG	Reserved							
0X0E	TM_CTRL	Reserved							
0X0F	PWM_CTRL	Reserved							
0X10	ATT	Reserved			ATT[4]	ATT[3]	ATT[2]	ATT[1]	ATT[0]
0X11	ATM	ATM[7]	ATM[6]	ATM[5]	ATM[4]	ATM[3]	ATM[2]	ATM[1]	ATM[0]
0X12	ATB	ATB[7]	ATB[6]	ATB[5]	ATB [4]	ATB [3]	ATB [2]	ATB [1]	ATB [0]

0X13	PCT	Reserved			PCT[4]	PCT[3]	PCT[2]	PCT[1]	PCT[0]
0X14	PCM	PCM[7]	PCM[6]	PCM[5]	PCM[4]	PCM[3]	PCM[2]	PCM[1]	PCM[0]
0X15	PCB	PCB[7]	PCB[6]	PCB[5]	PCB [4]	PCB [3]	PCB [2]	PCB [1]	PCB [0]
0X16	NGG	Reserved			DIS_ZD _FADE	Reserved		NG_GAIN[1]	NG_GAIN[0]
0X17	VFT	MV_FT[1]	MV_FT[0]	C1V_FT[1]	C1V_FT[0]	C2V_FT[1]	C2V_FT[0]	Reserved	
0X18	DTC	DTC_EN	DTC_TH[1]	DTC_TH[0]	DTC_RATE[1]	DTC_RATE[0]	Reserved		
0X19		Reserved							
0X1A	NGALT	NGALT[7]	NGALT[6]	NGALT[5]	NGALT[4]	NGALT[3]	NGALT[2]	NGALT[1]	NGALT[0]
0X1B	NGALM	NGALM[7]	NGALM[6]	NGALM[5]	NGALM[4]	NGALM[3]	NGALM[2]	NGALM[1]	NGALM[0]
0X1C	NGALB	NGALB[7]	NGALB [6]	NGALB [5]	NGALB [4]	NGALB [3]	NGALB [2]	NGALB [1]	NGALB [0]
0X1D	NGRLT	NGRLT[7]	NGRLT[6]	NGRLT[5]	NGRLT[4]	NGRLT[3]	NGRLT[2]	NGRLT[1]	NGRLT[0]
0X1E	NGRLM	NGRLM[7]	NGRLM[6]	NGRLM[5]	NGRLM[4]	NGRLM[3]	NGRLM[2]	NGRLM[1]	NGRLM[0]
0X1F	NGRLB	NGRLB[7]	NGRLB [6]	NGRLB[5]	NGRLB[4]	NGRLB [3]	NGRLB [2]	NGRLB [1]	NGRLB [0]
0X20	DRC_ECT	DRC_ECT[7]	DRC_ECT[6]	DRC_ECT[5]	DRC_ECT[4]	DRC_ECT[3]	DRC_ECT[2]	DRC_ECT[1]	DRC_ECT[0]
0X21	DRC_ECB	DRC_ECB[7]	DRC_ECB[6]	DRC_ECB[5]	DRC_ECB[4]	DRC_ECB[3]	DRC_ECB[2]	DRC_ECB[1]	DRC_ECB[0]
0X22	RTT	Reserved			RTT[4]	RTT[3]	RTT[2]	RTT[1]	RTT[0]
0X23	RTM	RTM[7]	RTM[6]	RTM[5]	RTM[4]	RTM[3]	RTM[2]	RTM[1]	RTM[0]
0X24	RTB	RTB[7]	RTB[6]	RTB[5]	RTB [4]	RTB [3]	RTB [2]	RTB [1]	RTB [0]

Detail Description for Register

In this section, please note that the highlighted columns are the default value of these tables. If no highlighted, it is because the default setting of this bit is determined by external pin.

- Address 0X00 : State control 1

  AD82587D support multiple serial data input formats including I^2S, Left-alignment and Right-alignment. These formats is chosen by user via bit7~bit5 of address 0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I^2S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
			other	Reversed
B[4]	LREXC	Left/Right (L/R) Channel Exchanged	0	No exchanged
			1	L/R exchanged
B[3]	PWML_X	LA/LB Exchange	0	No exchange
			1	Exchange
B[2]	PWMR_X	RA/RB Exchange	0	No exchange
			1	Exchange
B[1]	PwmMode	PWM Mmode	0	Quarternary+Ternary
			1	Quarternary
B[0]	NGE	Noise Gate Enable	0	Disable
			1	Enable

- Address 0X01 : State control 2

AD82587D has built-in PLL which can be bypassed by pull high the $\overline{PLL}$ pin. When PLL is enabled, multiple MCLK/FS ratio is supported. Detail setting is shown as the above table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	X	Reserved		
B[5:4]	FS	Sampling Frequency	00	32/44.1/48kHz
			01	32/44.1/48kHz
			10	64/88.2/96kHz
			11	128/176.4/192kHz

Multiple MCLK/FS ratio setting table

BIT	NAME	DESCRIPTION	VALUE	B[5:4]=00/01	B[5:4]=10	B[5:4]=11
B[3:0]	PMF[3:0]	Multiple MCLK/FS Ratio Setting	0001	Reset Default (256x)	Reset Default (128x)	Reset Default (64x)
			0010	512x	256x	128x
			0011	768x	384x	192x
			0100	1024x	512x	256x

- Address 0X02 : State control 3

To prevent the DC current from damaging the speaker, a high pass filter (3dB frequency = 5Hz) is built into the AD82587D. It can be enabled or disabled by bit 6 of address 2.

AD82587D has a mute function which includes master mute and individual channel mute modes. When the master mute mode is enabled, both left and right processing channels are muted. On the other hand, either channel can be muted by using the channel mute mode. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

The default settings of B[3:1] are determined by DEF pin. When DEF pin is pulled low or high, the default setting is muted or unmated.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	EN_CLK_OUT	PLL Clock Output	0	Disabled
			1	Enabled
B[6]	HPB	DC Blocking HPF Bypass	0	Enable
			1	Disabled
B[5]	LV_UVSEL	LV Under Voltage Selection	0	2.7V
			1	3.0V
B[4]	SW_RSTB	Software reset	0	Reset
			1	Normal operating
B[3]	MUTE	Master Mute	0	Un-Mute (DEF=1)
			1	Mute (DEF=0)
B[2]	CM1	Channel 1 Mute	0	Un-Mute (DEF=1)
			1	Mute (DEF=0)
B[1]	CM2	Channel 2 Mute	0	Un-Mute (DEF=1)
			1	Mute (DEF=0)
B[0]	CompSDMEn	Compensate SDM Frequency Response	0	Disable
			1	Enable

- Address 0X03 : Master volume

AD82587D supports both master-volume and channel-volume control for the stereo processing channels. Both master volume control (Address 0X03) and channel volume (Address 0X04 and 0X05) settings range from +12dB ~ -102dB. Given master volume level, say, Level A (in dB unit) and channel volume level, say Level B (in dB unit), the total volume equals to Level A plus with Level B and its range is from +24dB ~ -102dB, i.e., -103dB ≦ Total Volume (Level A + Level B) ≦ +24dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MV[7:0]	Master Volume	00000000	+12dB
			00000001	+11.5dB
			00000010	+11dB
			:	:
			00010111	0.5dB
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			1111111	-∞dB

- Address 0X04 : Channel1 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1V[7:0]	Channel 1 Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			1111111	-∞dB

- Address 0X05 : Channel2 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2V[7:0]	Channel 2 Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			1111111	-∞dB

- Address 0X06 : Under voltage selection for high voltage supply

AD82587D provides HV under voltage detection which can be enable or disable via bit 7. The under-voltage detection level is programmable via bit3~ bit0. Once the output stage voltage drops below the preset value (see table), AD82587D will fade out audio signals to turn off the speaker.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	Dis_HVUV	Disable HV Under Voltage Circuit	0	Enable
			1	Disable
B[6:4]	X	Reserved		
B[3:0]	HVUVSEL[3:0]	HV Under Voltage Selection (Active)	Other	9.7V
			1100	19.5V
			0100	15.5V
			0011	13.2V
			0001	9.7V
			0000	8.2V

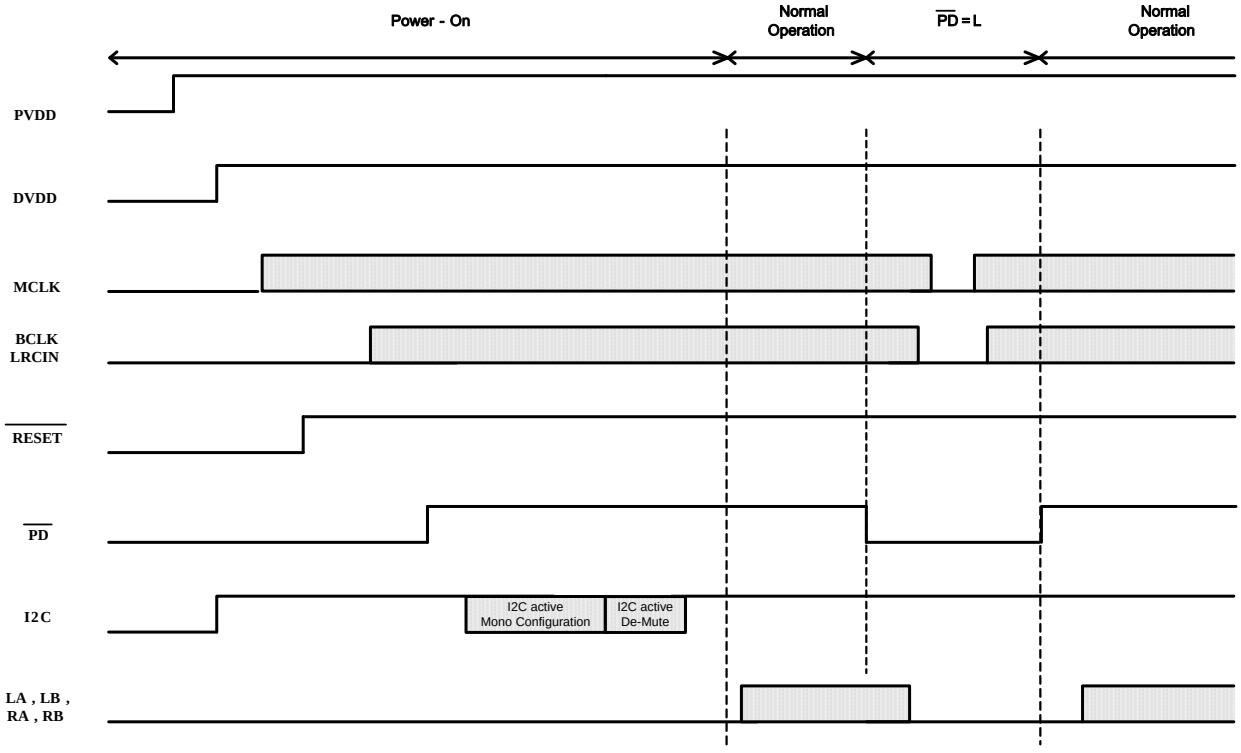
Note: under voltage range has +/- 10% max variation due to process window.

- Address 0X07 : State control 4

AD82587D provides channel mix, power clipping, and dynamic range control (DRC) function. These functions can be enable or not as the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	C1MX_EN	Channel1 Mixing Enable	0	Disable(MONO=0)
			1	Enable (MONO=1)
B[6]	C2MX_EN	Channel2 Mixing Enable	0	Disable(MONO=0)
			1	Enable(MONO=1)
B[5]	PC_EN	Power Clipping Enable	0	Disable
			1	Enable
B[4]	DRC_EN	DRC Enable	0	Disable
			1	Enable
B[3]	MONO_EN	MONO or Stereo Configure	0	Stereo
			1	MONO
B[2:0]	X	Reserved		

AD82587D also provides MONO configuration via register bit 3 of address 0X07. The output configuration (please refer to the page 8, Mono application circuit) shall be right connected before Mono configuration enable. That's possible to damage chips due to channel shoot-through if the wrong output configuration is connected.



- Address 0X08 : Attack rate and Release rate for Dynamic Range Control (DRC)

The attack/release rates of AD82587D are defined as following table,

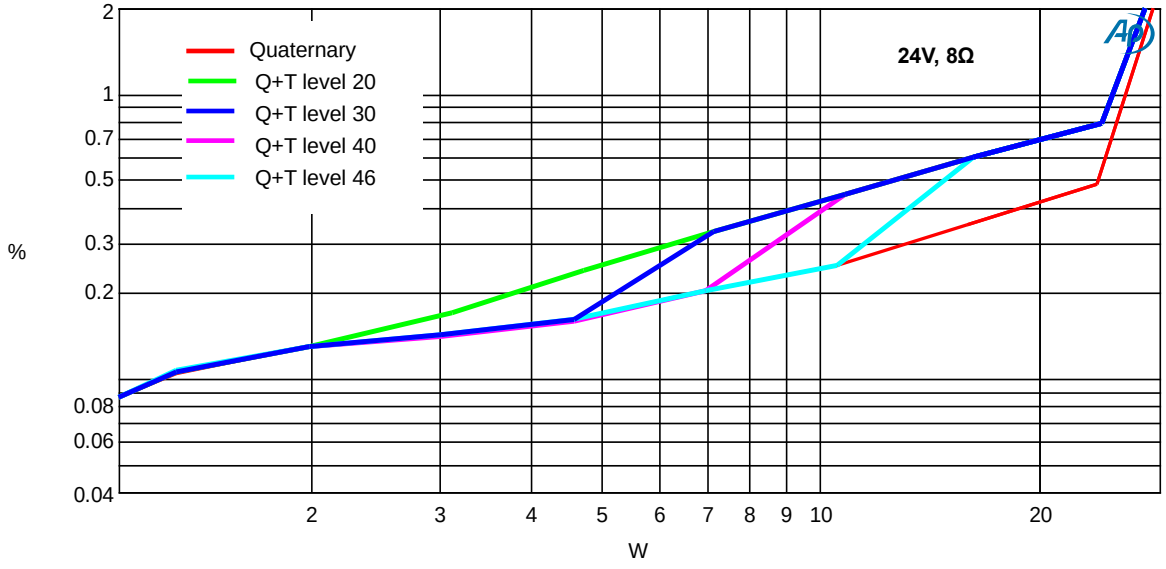
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	LA[3:0]	DRC Attack Rate	0000	3 dB/ms
			0001	2.667 dB/ms
			0010	2.182 dB/ms
			0011	1.846 dB/ms
			0100	1.333 dB/ms
			0101	0.889 dB/ms
			0110	0.4528 dB/ms
			0111	0.2264 dB/ms
			1000	0.15 dB/ms
			1001	0.1121 dB/ms
			1010	0.0902 dB/ms
			1011	0.0752 dB/ms
			1100	0.0645 dB/ms
			1101	0.0563 dB/ms
			1110	0.0501 dB/ms
			1111	0.0451 dB/ms
B[3:0]	LR[3:0]	DRC Release Rate	0000	0.5106 dB/ms
			0001	0.1371 dB/ms
			0010	0.0743 dB/ms
			0011	0.0499 dB/ms
			0100	0.0360 dB/ms
			0101	0.0299 dB/ms
			0110	0.0264 dB/ms
			0111	0.0208 dB/ms
			1000	0.0198 dB/ms
			1001	0.0172 dB/ms
			1010	0.0147 dB/ms
			1011	0.0137 dB/ms
			1100	0.0134 dB/ms
			1101	0.0117 dB/ms
			1110	0.0112 dB/ms
			1111	0.0104 dB/ms

- Address 0X09 : Power saving mode switching level

If the PWM exceeds the programmed switching power level (default 30*40ns), the modulation algorithm will change from quaternary to ternary modulation. Ternary modulation has less switching loss, resulting in higher power efficiency during larger power output operations. If the PWM drops below the programmed switching power level, the modulation algorithm will change back to quaternary modulation.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	X	Reserved		
B[4:0]	QTS[4:0]	Quaternary and Ternary Switching Level	11111	62
			11110	60
			:	:
			:	:
			10000	32
			01111	30
			01110	28
			01101	26
			:	:
			00001	4
			00000	4

Total Harmonic Distortion + Noise v.s. Output Power



- Address 0X10 : Top 5 bits of attack threshold for Dynamic Range Control (DRC)

The AD82587D provides dynamic range control function. When the input RMS exceeds the programmable attack threshold value, the output power will be limited by this threshold power level via gradual gain reduction. Attack threshold is defined by 21-bit representation composed of registers controlled by I2C. The device addresses of DRC attack threshold are 0X10, 0X11, and 0X12.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	X	Reserved		
B[4:0]	ATT[4:0]	Top 5 Bits of Attack Threshold	X	User programmed
			01000	0dB

- Address 0X11 : Middle 8 bits of attack threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	ATM[7:0]	Middle 8 Bits of Attack Threshold	X	User programmed
			00000000	0dB

- Address 0X12 : Bottom 8 bits of attack threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	ATB[7:0]	Bottom 8 bits of attack threshold	X	User programmed
			00000000	0dB

- Address 0X13 : Top 8 bits of power clipping

The AD82587D provides power clipping function to avoid excessive signal that may destroy loud speaker. The power clipping level is defined by 21-bit representation composed of registers controlled by I2C. The device addresses of power clipping threshold are 0X13, 0X14, and 0X15.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	X	Reserved		
B[4:0]	PCT[4:0]	Top 5 Bits of Power Clipping Level	X	User programmed
			01000	0dB

- Address 0X14 : Middle 8 bits of power clipping

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCM[7:0]	Middle 8 Bits of Power Clipping Level	X	User programmed
			00000000	0dB

- Address 0X15 : Bottom 8 bits of power clipping level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCB[7:0]	Bottom 8 Bits of Power Clipping Level	X	User programmed
			00000000	0dB

The following table shows the power clipping level's numerical representation.

Sample calculation for power clipping

Max amplitude	dB	Linear	Decimal	Hex (2.19 format)
PVDD	0	1	524288	80000
PVDD*0.707	-3	0.707	370727	5A827
PVDD*0.5	-6	0.5	262144	40000
PVDD*L	x	$L=10^{(x/20)}$	D=524288xL	H=dec2hex(D)

- Address 0X16 : Noise gate gain control

AD82587D provide noise gate function if receiving 2048 signal sample points less than noise gate attack level. User can change noise gate gain via bit1~ bit0. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, x0). User can select fade out or not via bit 4.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	X	Reserved		
B[4]	DIS_NG_FADE	Disable Noise Gate Fade	0	Fade
			1	No fade
B[3:2]	X	Reserved		
B[1:0]	NG_GAIN	Noise Gate Detection Gain	00	x1/8
			01	x1/4
			10	x1/2
			11	Mute

- Address 0X17 : Volume fine tune

AD82587D supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MV_FT	Master Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C1V_FT	Channel 1 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C2V_FT	Channel 2 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]	X	Reserved		

- Address 0X18 : Dynamic Temperature Control (DTC)

AD82587D supports dynamic temperature control. The table describes the setting of DTC.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	DTC_EN	DTC Enable	0	Disable
			1	Enable
B[6:5]	DTC_TH	DTC Threshold	00	110 °C
			01	120 °C
			10	130 °C
			11	140 °C
B[4:3]	DTC_RATE	DTC Attack and Release Rate	00	1dB/sec
			01	0.5dB/sec
			10	0.33dB/sec
			11	0.25dB/sec
B[2:0]	X	Reserved		

Release threshold is always 10 °C smaller than attack threshold.

For example:

DTC threshold (attack threshold) =130 °C, the release threshold = 120 °C.

DTC threshold (attack threshold) =120 °C, the release threshold = 110 °C.

If junction temperature (Tj) exceeds 130 °C, amplifier gain will be lowered to timing of 1dB/sec. If amplifier gain falls and junction temperature (Tj) turns into less than 130 °C and larger than 120 °C, the gain will not increase or decrease. If amplifier gain falls and junction temperature (Tj) turns into less than 120 °C, amplifier gain will be raised to timing of 1dB/sec.

- Address 0X1A : Top 8 bits of noise gate attack level

When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or zero if the noise gate function is enabled. Noise gate attack level is defined by 24-bit representation composed of registers controlled by I2C. The device addresses of noise gate attack level are 0X1A, 0X1B, and 0X1C

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGALT[7:0]	Top 8 Bits of Noise Gate Attack Level	X	User programmed
			00000000	-110dB

- Address 0X1B : Middle 8 bits of noise gate attack level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGALM[7:0]	Middle 8 Bits of Noise Gate Attack Level	X	User programmed
			00000000	-110dB

- Address 0X1C : Bottom 8 bits of noise gate attack level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGALB[7:0]	Bottom 8 Bits of Noise Gate Attack Level	X	User programmed
			00011010	-110dB

- Address 0X1D : Top 8 bits of noise gate release level

After entering the noise gating status, the noise gain will be removed whenever AD82587D receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 24-bit representation composed of registers controlled by I2C. The device addresses of noise gate release level are 0X1D, 0X1E, and 0X1F.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRLT[7:0]	Top 8 Bits of Noise Gate Release Level	X	User programmed
			00000000	-100dB

- Address 0X1E : Middle 8 bits of noise gate release level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRLM[7:0]	Middle 8 Bits of Noise Gate Release Level	X	User programmed
			00000000	-100dB

- Address 0X1F : Bottom 8 bits of noise gate release level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRLB[7:0]	Bottom 8 Bits of Noise Gate Release Level	X	User programmed
			01010011	-100dB

The following table shows the noise gate attack and release threshold level's numerical representation.

Sample calculation for noise gate attack and release level

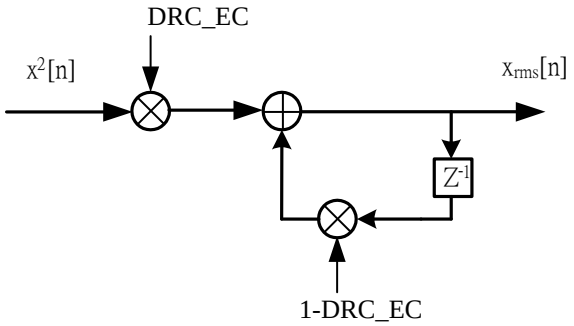
Input amplitude (dB)	Linear	Decimal	Hex (1.23 format)
0	1	8388607	7FFFFF
-100	10^{-5}	83	53
-110	$10^{-5.5}$	26	1A
X	$L=10^{(x/20)}$	D=8388607xL	H=dec2hex(D)

- Address 0X20 : Top 8 bits of DRC energy coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_ECT [7:0]	Top 8 Bits of DRC Energy Coefficient	X	User programmed
			00000000	1/256

- Address 0X21 : Bottom 8 bits of DRC energy coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_ECB [7:0]	Bottom 8 Bits of DRC Energy Coefficient	X	User programmed
			00010000	1/256



The above figure illustrates the digital processing of calculating RMS signal power. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Energy coefficient is defined by 16-bit representation composed of registers controlled by I2C. The device addresses of DRC energy coefficient are 0X20, and 0X21. The following table shows the DRC energy coefficient numerical representation.

Sample calculation for DRC energy coefficient

DRC energy coefficient	dB	Linear	Decimal	Hex (1.12 format)
1	0	1	4095	FFF
1/256	-48.2	1/256	16	10
1/1024	-60.2	1/1024	4	4
L	x	$L=10^{(x/20)}$	D=4095xL	H=dec2hex(D)

- Address 0X22 : Top 8 bits of release threshold for Dynamic Range Control (DRC)

  After AD82587D has reached the attack threshold, its output power will be limited to that level. The output power level will be gradually adjusted to the programmable release threshold level. Release threshold is defined by 21-bit representation composed of registers controlled by I2C. The device addresses of release threshold are 0X22, 0X23, and 0X24.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	X	Reserved		
B[4:0]	RTT[4:0]	Top 5 Bits of Release Threshold	X	User programmed
			00000010	-6dB

- Address 0X23 : Middle 8 bits of release threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	RTM[7:0]	Middle 8 Bits of Release Threshold	X	User programmed
			00000000	-6dB

- Address 0X24 : Bottom 8 bits of release threshold

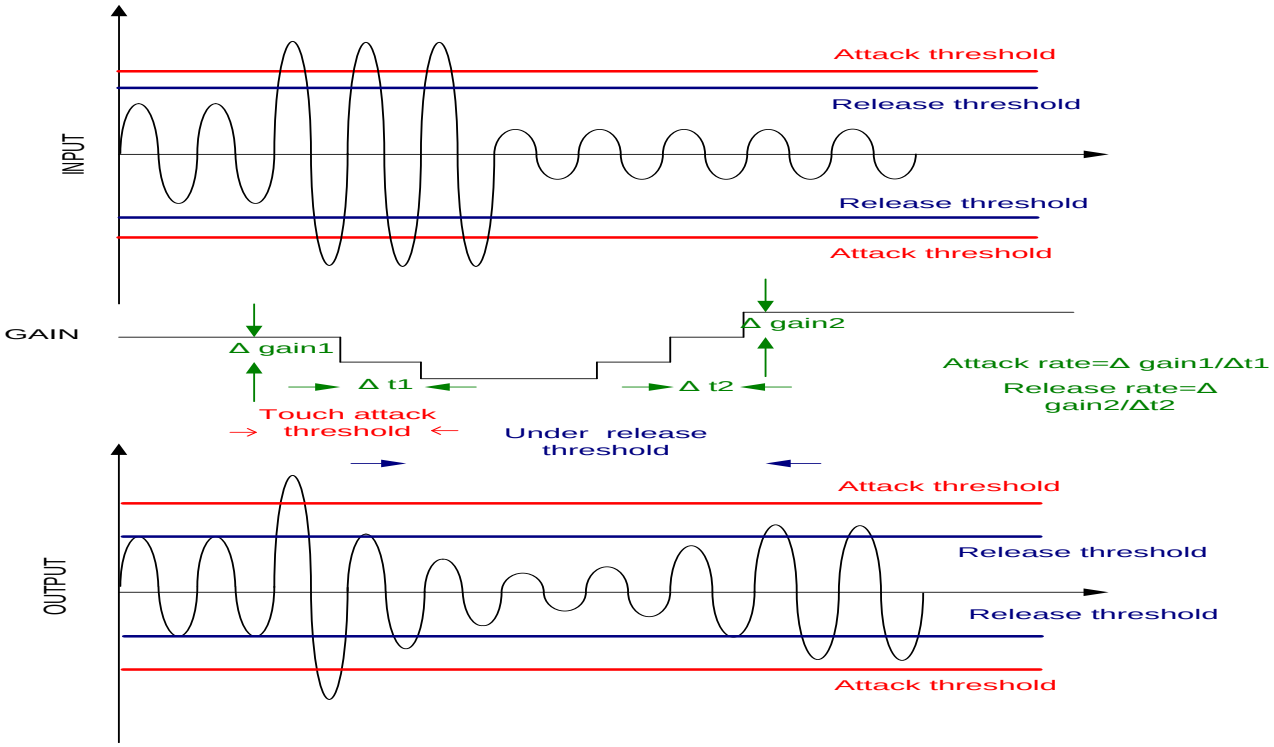
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	RTB[7:0]	Bottom 8 Bits of Release Threshold	X	User programmed
			00000000	-6dB

The following table shows the attack and release threshold's numerical representation.

Sample calculation for attack and release threshold

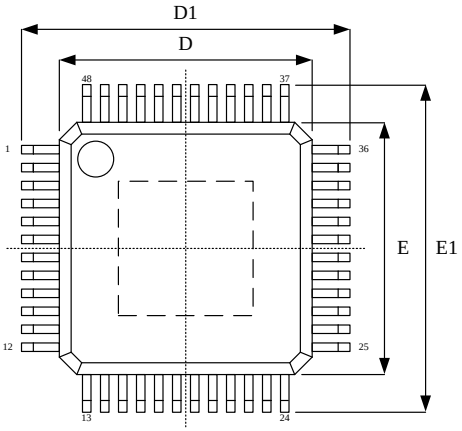
Power	dB	Linear	Decimal	Hex (2.19 format)
(PVDD^2)/R	0	1	524288	80000
(PVDD^2)/2R	-3	0.5	262144	40000
(PVDD^2)/4R	-6	0.25	131072	20000
((PVDD^2)/R)*L	x	$L=10^{(x/10)}$	D=524288xL	H=dec2hex(D)

To best illustrate the dynamic range control function, please refer to the following figure.

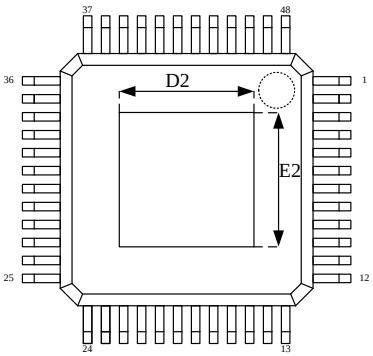


Package Dimensions

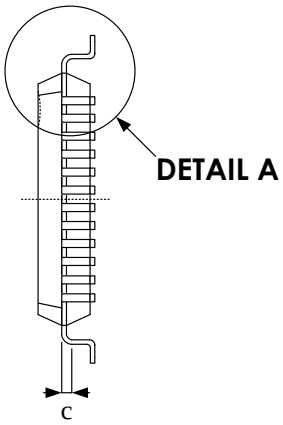
- **E-LQFP 48L (7x7mm)**

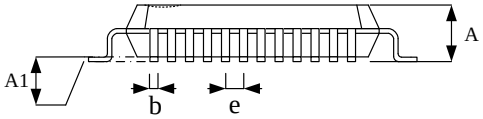


TOP VIEW

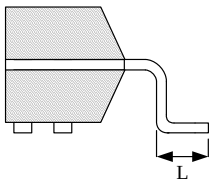


BOTTOM VIEW





SIDE VIEW



DETAIL A

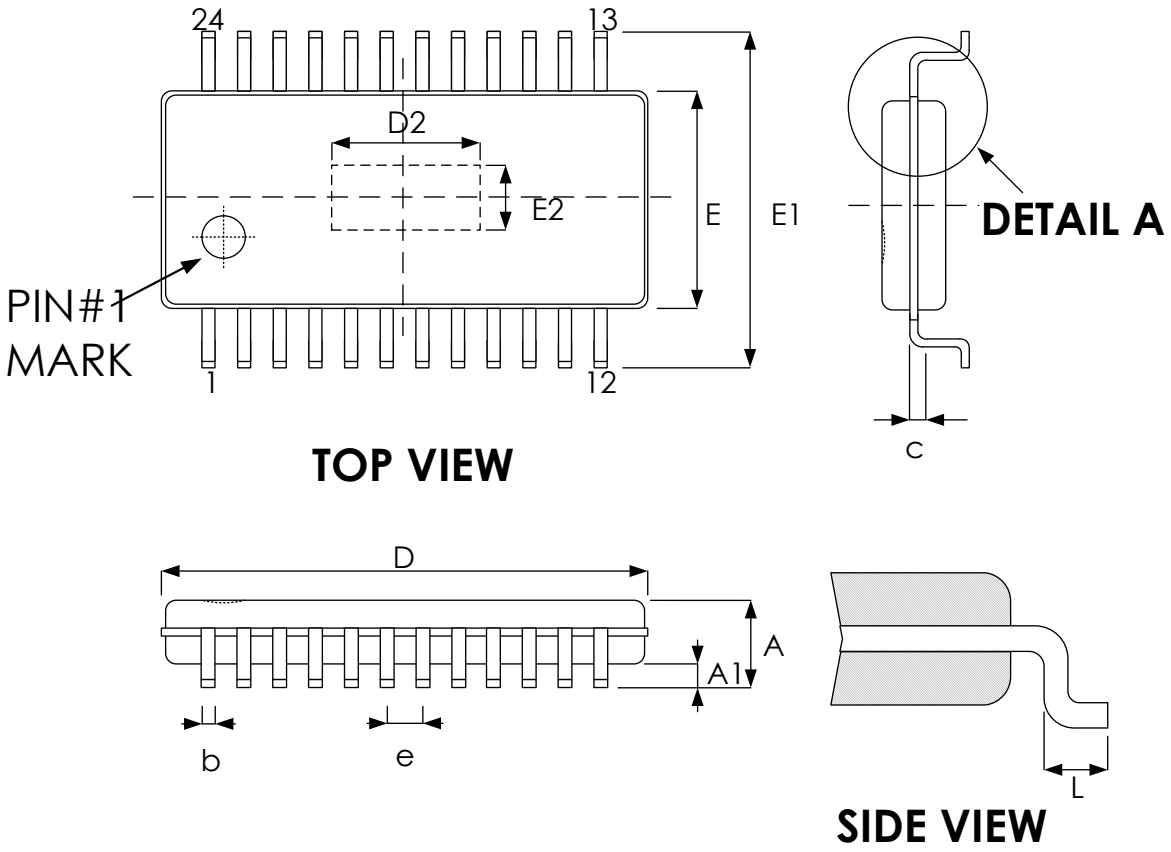
Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.17	0.27
c	0.09	0.20
D	6.90	7.10
D1	8.90	9.10
E	6.90	7.10
E1	8.90	9.10
e	0.50 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	4.31	5.21
E2	4.31	5.21

Package Dimensions

- **E-TSSOP 24L**



Symbol	Dimension in mm	
	Min	Max
A	1.00	1.20
A1	0.00	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
D2	3.70	4.62
E2	2.20	2.85

Revision History

Revision	Date	Description
0.1	2012.08.27	Original.
0.2	2013.01.07	1) Update address 0X02, register table B[4] content. 2) Improved OC protection level on this version. 3) Updated package thermal data2. 4) Added Power-OFF sequence into this datasheet.
0.3	2013.02.08	1) Fade-out and fade-in time formula revised. 2) Added DTC explanation at address 0X18. 3) Showed Ψ_{jt} values to replace of Ψ_{jb}.
0.4	2013.04.26	1) Modified the typical value of I_{SC} in General Electrical Characteristics. 2) Modified color for curve and legend.
1.0	2014.05.26	1) Removed the letters of “Preliminary” 2) Added note6 to Application Circuit Example for Stereo. 3) Modified the description of Device addressing.
1.1	2014.12.17	Updated MONO configuration description via register bit of address 0X07.
1.2	2015.02.03	Add E-TSSOP 24L reel information
1.3	2016.03.08	Added Class-D HVUV range information into.
1.4	2016.06.30	Modify order information
1.5	2017.09.21	Modify timing of power on sequence.
1.6	2018.01.26	Modify PLL table.

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