
2x15W Stereo / 1x 30W Mono Digital Audio Amplifier with 18 Bands EQ

Features

- 16/18/20/24-bits input with I²S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
Loudspeaker: 94dB (PSNR), 103dB (DR) @24V
- Multiple sampling frequencies (Fs)
32kHz / 44.1kHz / 48kHz and
64kHz / 88.2kHz / 96kHz and
128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
64x~512x Fs for 64kHz / 88.2kHz / 96kHz
64x~256x Fs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
3.3V for digital circuit
10V~26V for loudspeaker driver
- Loudspeaker output power for stereo at 24V
15W x 2CH into 4Ω @0.17% THD+N
- Loudspeaker output power for mono at 24V
30W x 1CH into 4Ω @0.095% THD+N
- Sound processing including :
18 bands parametric speaker EQ
Volume control (+24dB~-103dB, 0.125dB/step),
Dynamic range control
Power Clipping
3D surround sound
Channel mixing
Automatic Zero-detection mute and noise gate
Bass/Treble tone control
Bass management crossover filter
DC-blocking high-pass filter
- Anti-pop design
- Over-temperature protection
- I²C control interface with selectable device address
- Support hardware and software reset
- Internal PLL

- LV Under-voltage shutdown and HV Under-voltage detection
- Short-circuit protection
- Over-temperature protection
- Power saving mode
- Support initial EEPROM setting

Applications

- CD and DVD
- TV audio
- Car audio
- Boom-box
- MP3 docking systems
- Powered speaker
- Wireless audio

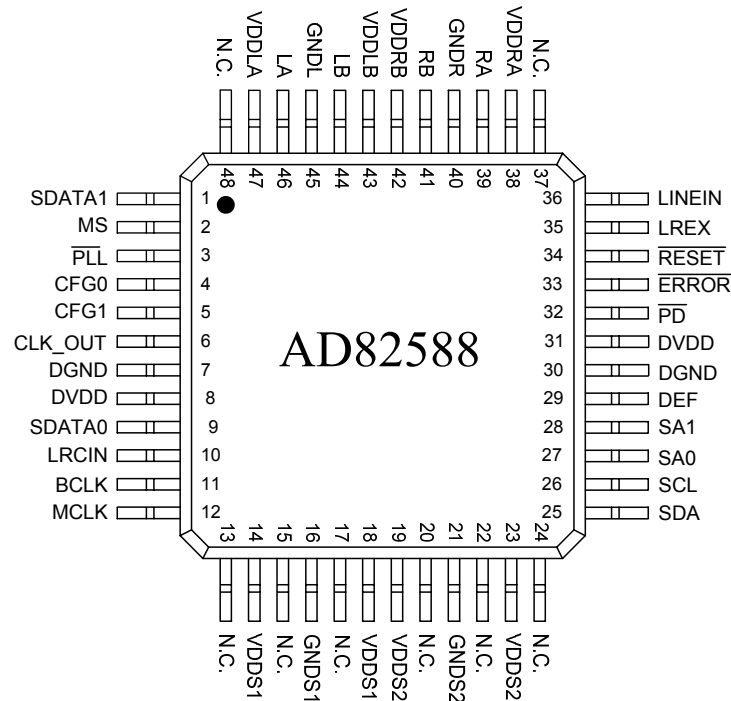
Description

AD82588 is a digital audio amplifier capable of driving a pair of 8Ω, 15W or a single 4Ω, 30W operating at 24V supply.

AD82588 can provide advanced audio processing capabilities, such as volume control, 18 bands speaker EQ, audio mixing, 3D surround and Dynamic Range Control (DRC). These functions are fully programmable via a simple I²C control interface. Robust protection circuits are provided to protect AD82588 from damage due to accidental erroneous operating condition. AD82588 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. AD82588 is pop free during instantaneous power switch because of its built-in, robust anti-pop circuit.

The output stage is flexibly configurable for stereo channel or mono applications.

Pin Assignment



Pin Description

| PIN | NAME | TYPE | DESCRIPTION | CHARACTERISTICS |
|-----|---------|------|-------------------------------|----------------------------------|
| 1 | SDATA1 | I | Serial audio data input 1 | Schmitt trigger TTL input buffer |
| 2 | MS | I | EEPROM selection | Schmitt trigger TTL input buffer |
| 3 | PLL | I | PLL enable, low active | Schmitt trigger TTL input buffer |
| 4 | CFG0 | I | Stereo/Mono configuration pin | Schmitt trigger TTL input buffer |
| 5 | CFG1 | I | Stereo/Mono configuration pin | Schmitt trigger TTL input buffer |
| 6 | CLK_OUT | O | Clock output from PLL | TTL output buffer |
| 7 | DGND | P | Digital Ground | |
| 8 | DVDD | P | Digital Power | |
| 9 | SDATA0 | I | Serial audio data input 0 | Schmitt trigger TTL input buffer |
| 10 | LRCIN | I | Left/Right clock input (Fs) | Schmitt trigger TTL input buffer |
| 11 | BCLK | I | Bit clock input (64Fs) | Schmitt trigger TTL input buffer |
| 12 | MCLK | I | Master clock input | Schmitt trigger TTL input buffer |
| 13 | N.C. | | | |
| 14 | VDD1 | P | Subwoofer1 channel supply | |
| 15 | N.C. | O | | |
| 16 | GND1 | P | Subwoofer1 channel ground | |
| 17 | N.C. | O | | |
| 18 | VDD1 | P | Subwoofer1 channel supply | |
| 19 | VDD2 | P | Subwoofer2 channel supply | |

| | | | | |
|----|---------------------------|-----|--|----------------------------------|
| 20 | N.C. | O | | |
| 21 | GNDS2 | P | Subwoofer2 channel ground | |
| 22 | N.C. | O | | |
| 23 | VDDS2 | P | Subwoofer2 channel supply | |
| 24 | N.C. | | | |
| 25 | SDA | I/O | I ² C bi-directional serial data | Schmitt trigger TTL input buffer |
| 26 | SCL | I/O | I ² C serial clock input | Schmitt trigger TTL input buffer |
| 27 | SA0 | I | I ² C select address 0 | Schmitt trigger TTL input buffer |
| 28 | SA1 | I | I ² C select address 1 | Schmitt trigger TTL input buffer |
| 29 | DEF | I | Initial default volume setting (1:Un-Mute ; 0:Mute) | Schmitt trigger TTL input buffer |
| 30 | DGND | P | Digital Ground | |
| 31 | DVDD | P | Digital Power | |
| 32 | $\overline{\text{PD}}$ | I | Power down, low active | Schmitt trigger TTL input buffer |
| 33 | $\overline{\text{ERROR}}$ | O | Error status, low active | Open-drain output |
| 34 | $\overline{\text{RESET}}$ | I | Reset, low active | Schmitt trigger TTL input buffer |
| 35 | LREX | I | Left/Right channel exchange (0:Unchanged ; 1:Exchanged) | Schmitt trigger TTL input buffer |
| 36 | LINEIN | I | Select input data (0:SDATA0 ; 1:SDATA1) | Schmitt trigger TTL input buffer |
| 37 | N.C. | | | |
| 38 | VDDRA | P | Right channel supply A | |
| 39 | RA | O | Right channel output A | |
| 40 | GNDR | P | Right channel ground | |
| 41 | RB | O | Right channel output B | |
| 42 | VDDRB | P | Right channel supply B | |
| 43 | VDDL B | P | Left channel supply B | |
| 44 | LB | O | Left channel output B | |
| 45 | GNDL | P | Left channel ground | |
| 46 | LA | O | Left channel output A | |
| 47 | VDDL A | P | Left channel supply A | |
| 48 | N.C. | | | |