2x20W Stereo / 1x40W Mono Digital Audio Amplifier With 24 Bands EQ Functions

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR (A-weighting)
  Loudspeaker: 102dB (PSNR), 108dB (DR) @24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- I^2C control interface
- Channel mixing
- Volume control (+12dB ~ -103dB, 0.125dB/step)
- Power clipping function
- DRC and DTC function
- 24 bands parametric speaker EQ
- Bass/Treble tone control
- DRC and post scale boost
- Check-sum coefficient protection
- Noise gate function
- Pop noise less muting (Quick Mute/Quick Start)
- Sleep function
- X3 over sampling for 32kHz FS
- AM interference frequency switching
- Level meter
- Post-scale and DRC offset volume support
- Over current protection function (OCP)
- Over temperature protection function (OTP)
- Under voltage lock out (UVLO)
- Over voltage protection function (OVP)
- DC detection function (DCDET)
- Clock detection function (CKDET)
- Lead-free E-LQFP-48L

Applications

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

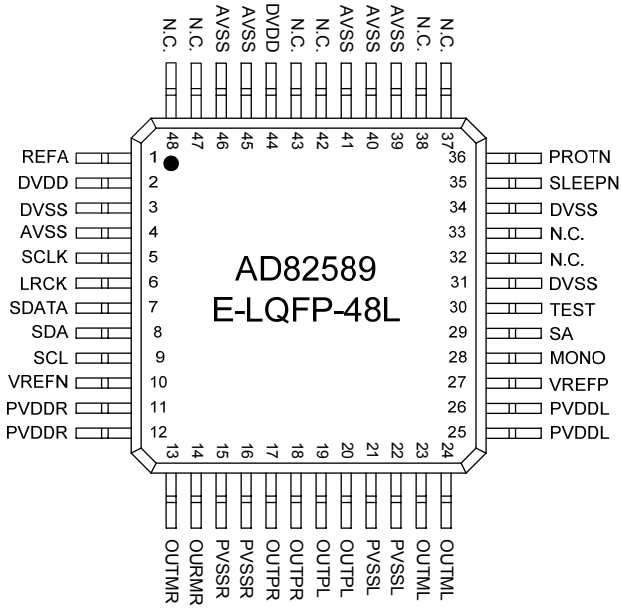
AD82589 is an integrated audio system solution, embedding digital audio processing power stage amplifier.

AD82589 has a programmable slew-rate controlled output buffer, which drives one (mono) or two (stereo) speakers directly. In addition, it is insusceptible to supply voltage fluctuation due to the close-loop design.

AD82589 can provide advanced audio processing capabilities, such as volume control, 24 bands EQ, audio mixing and Dynamic Range Control (DRC). These functions are fully programmable via a simple I^2C interface.

Robust protection circuits are provided to protect AD82589 from damage due to accidental erroneous operation. AD82589, being a digital circuit design, is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. Furthermore, AD82589 is pop free during instantaneous power switching because of its built-in, robust anti-pop circuit.

Pin Assignment



Pin Description

NAME	Pin no.	TYPE	DESCRIPTION	CHARACTERISTICS
REFA	1	O	1.8V Regulator voltage output.	
DVDD	2	P	3.3V Power supply for internal digital circuit.	
DVSS	3	P	Ground terminal for internal digital circuitry.	
AVSS	4	P	Ground terminal for internal analog circuitry.	
SCLK	5	I	Serial audio port bit clock.	
LRCK	6	I	Serial audio port word clock.	
SDATA	7	I	Serial audio port serial data in.	
SDA	8	I/O	I^2C data input.	
SCL	9	I/O	I^2C clock input.	
VREFN	10	O	Low side gate drive internal regulator output.	
PVDDR	11	P	RCH power supply for power stage.	
PVDDR	12	P	RCH power supply for power stage.	
OUTMR	13	O	Negative terminal for RCH differential speaker amplifier output.	
OUTMR	14	O	Negative terminal for RCH differential speaker amplifier output.	
PVSSR	15	P	RCH ground for power stage.	
PVSSR	16	P	RCH ground for power stage.	
OUTPR	17	O	Positive terminal for RCH PWM output.	
OUTPR	18	O	Positive terminal for RCH PWM output.	
OUTPL	19	O	Positive terminal for LCH PWM output.	
OUTPL	20	O	Positive terminal for LCH PWM output.	

PVSSL	21	P	LCH ground for power stage.	
PVSSL	22	P	LCH ground for power stage.	
OUTML	23	O	Negative terminal for LCH PWM output.	
OUTML	24	O	Negative terminal for LCH PWM output.	
PVDDL	25	P	LCH power supply for power stage.	
PVDDL	26	P	LCH power supply for power stage.	
VREFP	27	O	High side gate drive internal regulator output.	
MONO	28	I	MONO output control pin.	
SA	29	I	I^2C address setup.	
TEST	30	I	This pin must be connected to GND.	
DVSS	31	P	Ground terminal for internal digital circuitry.	
NC	32	—	No connect.	
NC	33	—	No connect.	
DVSS	34	P	Ground terminal for internal digital circuitry.	
SLEEPN	35	I	Power down control (Low for power down).	
PROTN	36	O	Error indicator, Low stands for error signal.	
NC	37	—	No connect.	
NC	38	—	No connect.	
AVSS	39	P	Ground terminal for internal analog circuitry.	
AVSS	40	P	Ground terminal for internal analog circuitry.	
AVSS	41	P	Ground terminal for internal analog circuitry.	
NC	42	—	No connect.	
NC	43	—	No connect.	
DVDD	44	P	3.3V Power supply for internal digital circuit.	
AVSS	45	P	Ground terminal for internal analog circuitry.	
AVSS	46	P	Ground terminal for internal analog circuitry.	
NC	47	—	No connect.	
NC	48	—	No connect.	

Note:

P: Power or ground pins; I: Input pins; O: Output pins; I/O: The bidirectional pins.

Functional Block Diagram

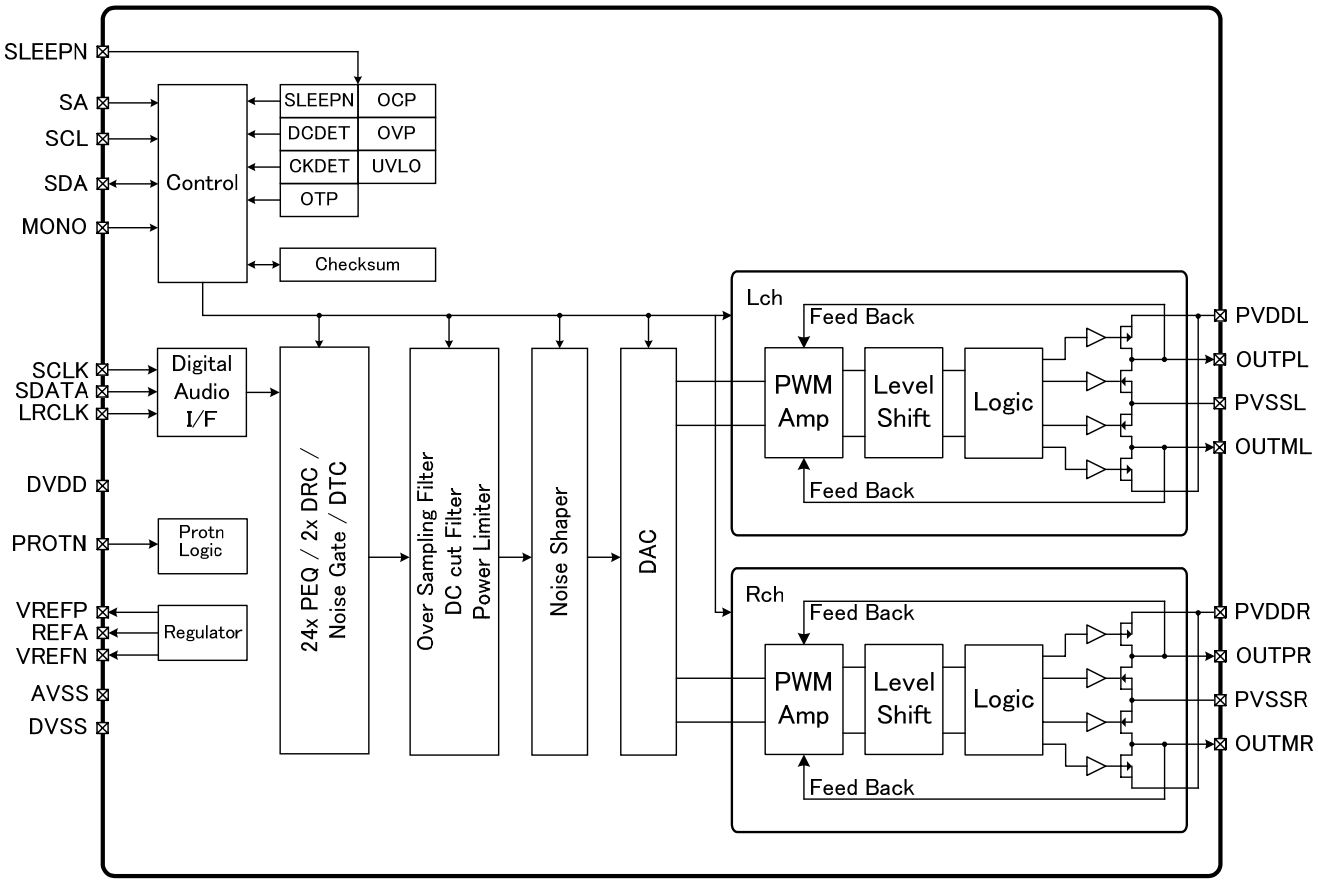
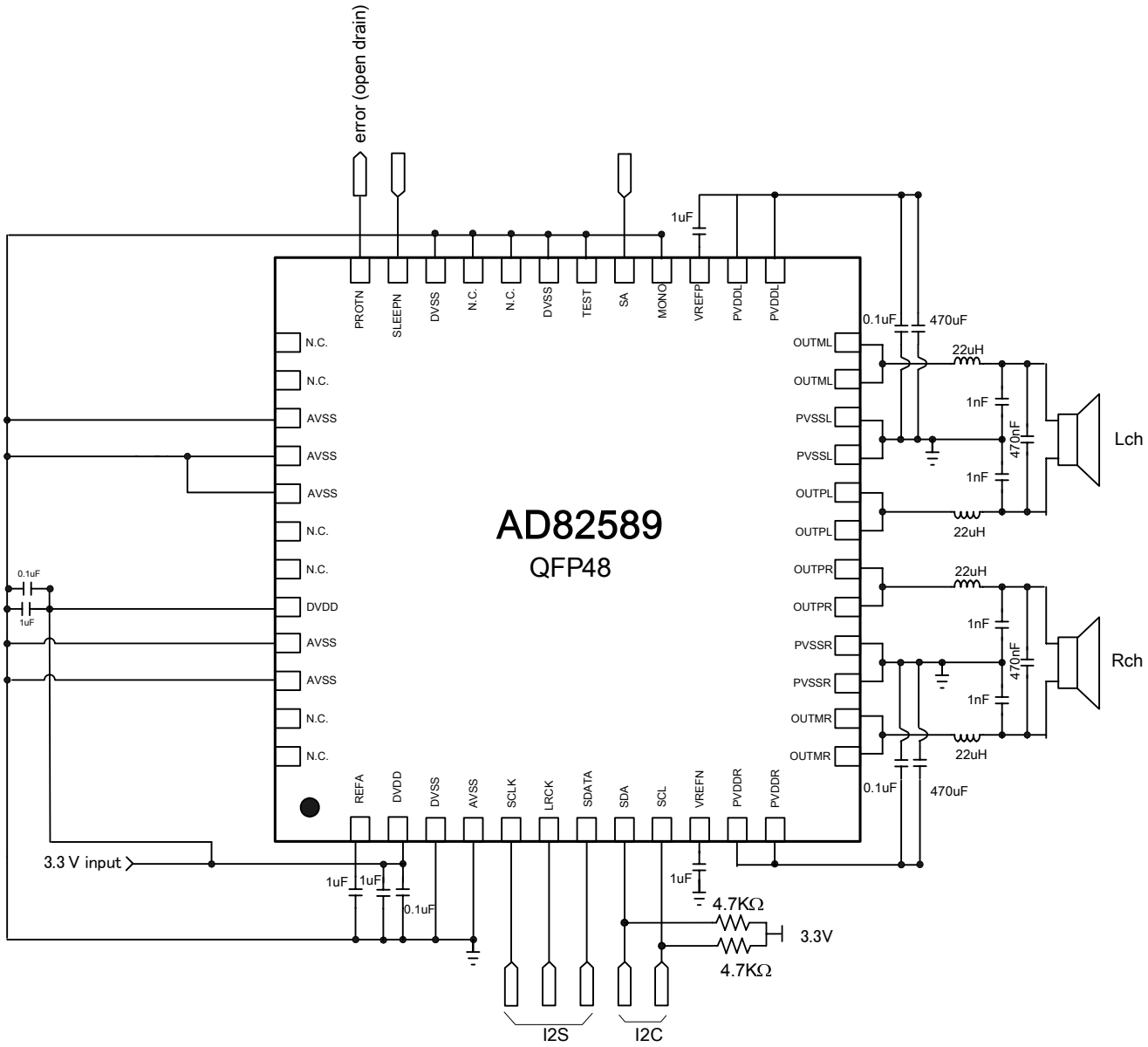


Figure 1

Application Circuit Example

- Application circuit for stereo mode



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD82589-LG48NRY	E-LQFP-48L 7X7	250Units / Tray 2.5K Units / Box(10 Tray)	Green
AD82589-LG48NRR		2K Units Tape & Reel	

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	θ_{jt} (℃/W)	Ψ_{jb} (℃/W)	Exposed Thermal Pad
E-LQFP-48L 7X7	AD82589	22.9	34.9	1.64	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface. (The junction-to-top thermal resistance is obtained by simulating a cold plate test on the top of the package).

Note 1.4: Ψ_{jb} represents the heat resistance for the heat flow between the chip and the exposed pad center. (The junction-to-top characterization parameter is extracted from the simulation data to obtain θ_{ja}).

Marking Information

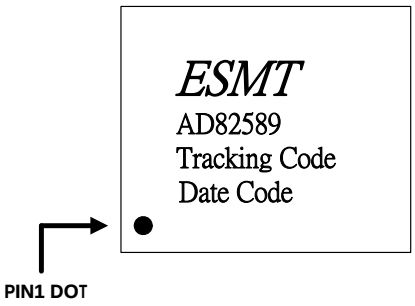
AD82589

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code

Line 4 : Date Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings (<100msec)* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVDD	Supply for driver stage	PVDDL and PVDDR	-0.3	30	V
DVDD	Supply for low voltage	DVDD	-0.3	3.6	V
V_{SI}	Speaker interface pin voltage	SCLK, LRCLK, SDATA,SCL, SDA,SA,TEST,MONO, and SLEEPN	-0.3	3.8	V
V_{PROTN}	PROTN terminal voltage range	PROTN	-0.3	3.8	V
T_J	Operating junction temperature range		-40	150	°C
T_{stg}	Storage temperature range		-65	150	°C
R_L	Minimum load resistance	Stereo (BTL)	3.2		Ω
		Mono (PBTL)	1.8		
ESD	Human body model (all pins)	HBM	±2		KV
	Charged-device model (all pins)	CDM	±500		V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage for driver stage	PVDD	4.5	-	26.4	V
Power supply voltage for low voltage	DVDD	3.0		3.6	V
Digital terminals input voltage	V_{IN}	2.2	3.3	3.6	V
Operating ambient temperature	T_A	-40	-	85	°C
Stereo speaker impedance (Note 2)	R_L	4	8	-	Ω
Mono speaker impedance (Note 2)		2	4		

Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

General Electrical Characteristics

- PVDD=4.5V to 26.4V, T_A=25°C, unless otherwise specified.

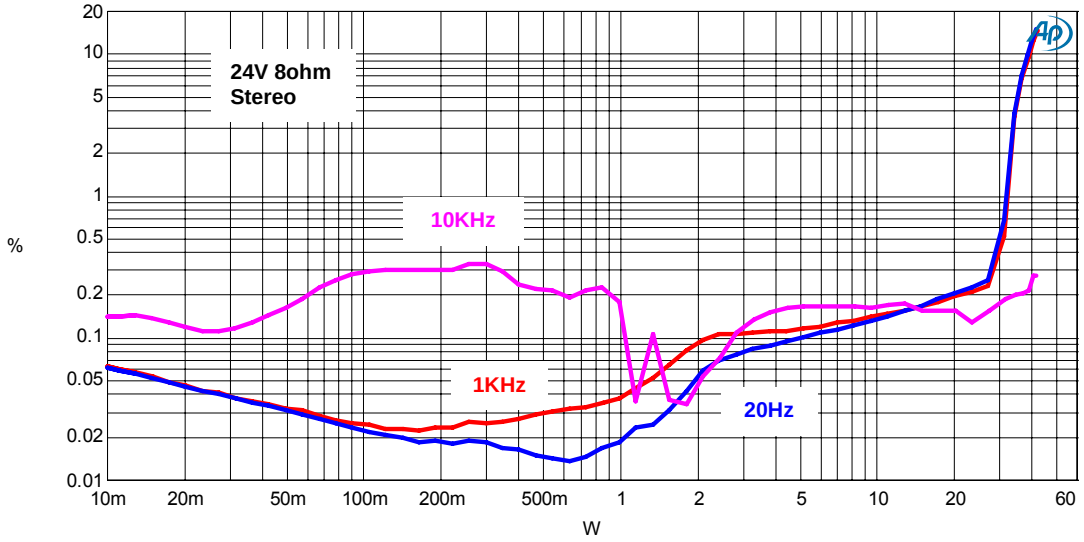
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
PVDD under voltage	Under voltage lock out threshold voltage	V_{HUVLL}	–	–	3.8	–	V
	Under voltage release threshold voltage	V_{HUVLH}	–	–	4	–	V
DVDD under voltage	Under voltage lock out threshold voltage	V_{LUVLL}	–	–	2.65	–	V
	Under voltage release threshold voltage	V_{LUVLH}	–	–	2.8	–	V
Digital pins	Input voltage H level	V_{IH}	–	2.0	–	–	V
	Input voltage L level	V_{IL}	–	–	–	0.8	V
	Input impedance	R_{IN_D}	–	3.3	–	–	MΩ
SLEEPN pin	Input voltage H level	V_{IH}	–	2.2	–	–	V
	Input voltage L level	V_{IL}	–	–	–	0.6	V
	Input impedance	R_{IN_D}	–	3.3	–	–	MΩ
PROTN pin output voltage		V_{OL}	I_{OL}=2mA	–	–	0.4	V
SDA pin output voltage		V_{OL}	I_{OL}=2mA	–	–	0.4	V
REFA pin output voltage		V_{REFA}	–	–	1.8	–	V
VREFN pin output voltage		V_{REFN}	PVDD=24V		5.5		V
VREFP pin output voltage		V_{REFP}	PVDD=24V		18.5		V
Current drawn from DVDD		I_{DVDD}	DVDD=3.3V		30		mA
Current drawn from PVDD	at idling state	I_{DDPP}	PVDD=24V, No load	–	23	–	mA
	at power-down state (SLEEPN="L")	I_{DDPS}	PVDD=24V, No load	–	17	–	μA
	at mute state (AMP_HARD_MUTE=1)	I_{DDPM}	PVDD=24V, No load	–	14	–	mA
Over current detection threshold		I_{OCP}	PVDD=24V		6		A
			PVDD=12V		6		
			PVDD=5V		3.3		
Static drain to source on state resistor, PMOS		Rds-on	PVDD=24V Id=250mA		234		mΩ
Static drain to source on state resistor, NMOS					218		mΩ

Electrical Characteristics and Specifications of Loudspeaker Driver

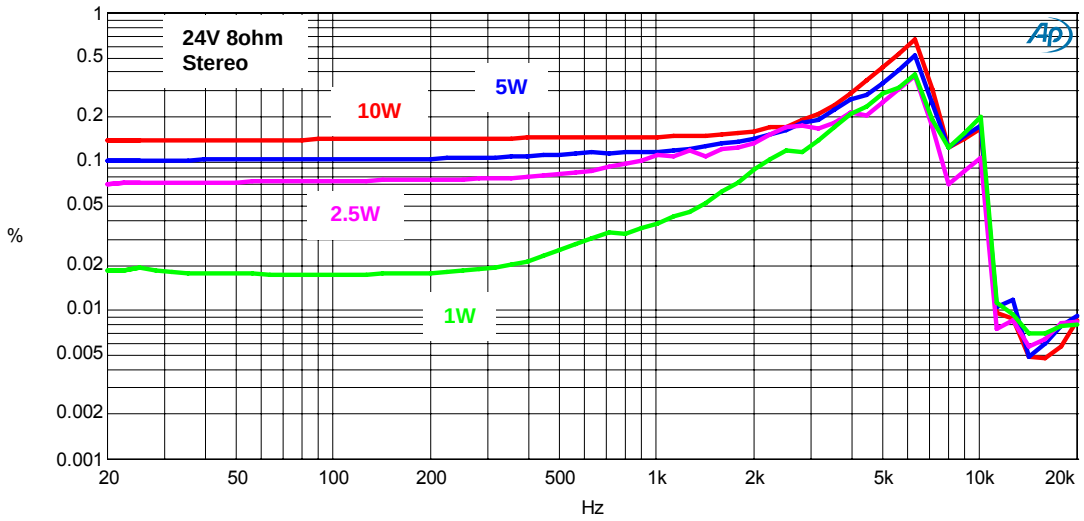
- PVDD=24V, T_A=25°C, R_L=8Ω, unless otherwise specified.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum instantaneous output	Stereo	Po	PVDD=24V, R_L=8Ω, THD+N=0.2%	–	20	–	W
			PVDD=12V, R_L=8Ω, THD+N=10%	–	10	–	W
			PVDD=12V, R_L=4Ω THD+N=10%	–	15	–	W
	Mono		PVDD=24V, R_L=4Ω, THD+N=0.16%	–	40	–	W
Total harmonic distortion	Stereo, Mono	THD+N	R_L=8Ω, Po=10W	–	0.15	–	%
Residual noise	Stereo, Mono	Vn	R_L=8Ω, A-Weighted Filter	–	120	–	μVrms
S/N ratio	Stereo, Mono	SNR	R_L=8Ω, A-Weighted Filter	–	102	–	dB
Channel separation (L-ch vs. R-ch)		CS	R_L=8Ω, 1kHz (with shielding inductor)	–	90	–	dB
PSRR	Stereo, Mono	PSRR	PVDD applied, Vripple=200mVpp, f=1kHz	–	70	–	dB
Maximum efficiency	Stereo	η	PVDD=24V, R_L=8Ω, Po=20W	–	89	–	%
			PVDD=12V, R_L=4Ω, Po=10W	–	84	–	%
	Mono		PVDD=24V, R_L=4Ω, Po=40W	–	90	–	%
			PVDD=12V, R_L=4Ω, Po=20W	–	94	–	%
Output offset voltage	Stereo, Mono	Vo	–	–	13	–	mV
Frequency response	Stereo, Mono	f	20Hz	–1	0	1	dB
			20kHz	–3	0	1	dB

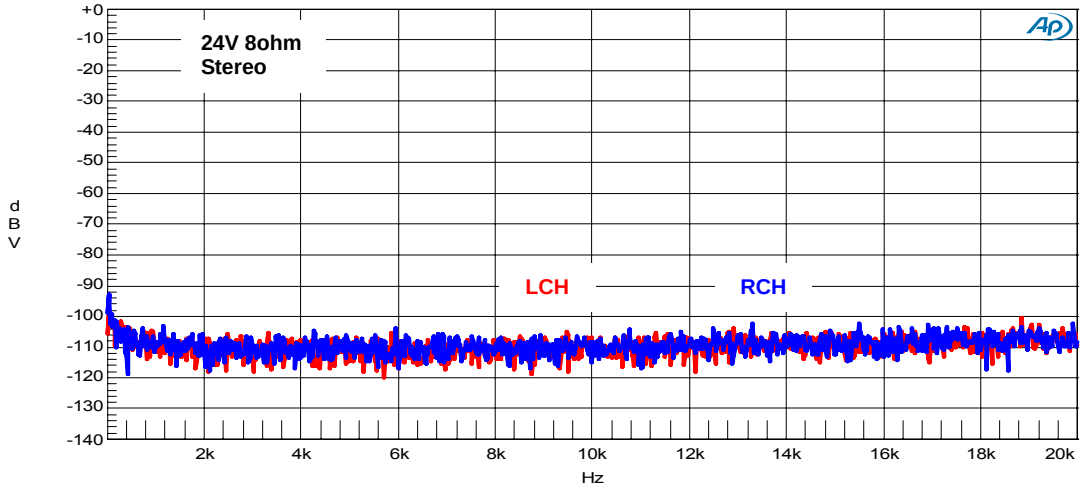
THD + N (%) v.s. Output power (Stereo, 8ohm load)



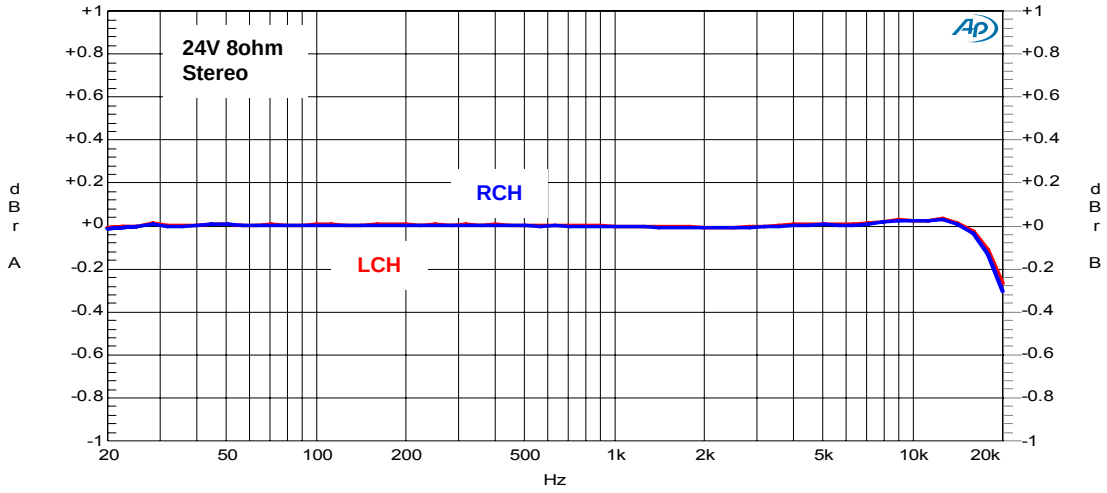
THD + N (%) v.s. Frequency



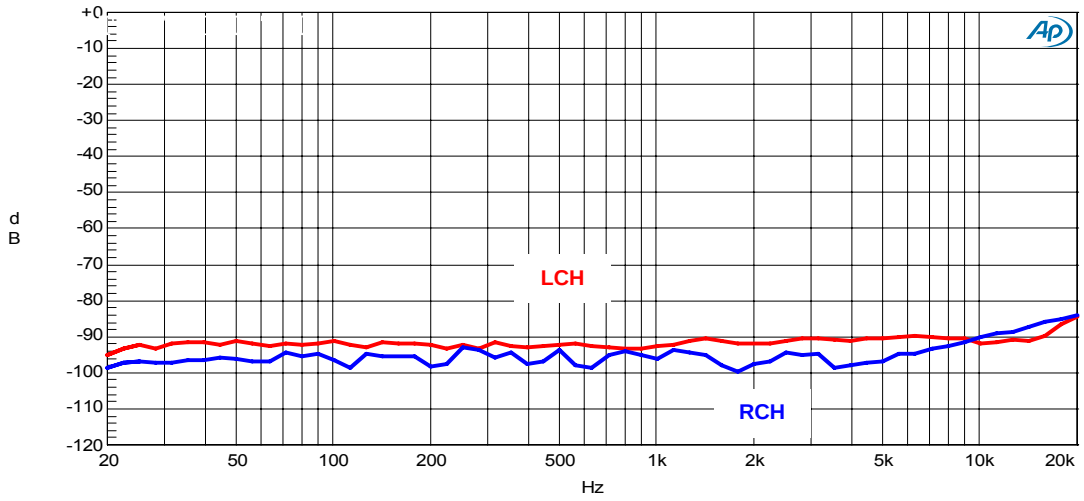
Noise FFT



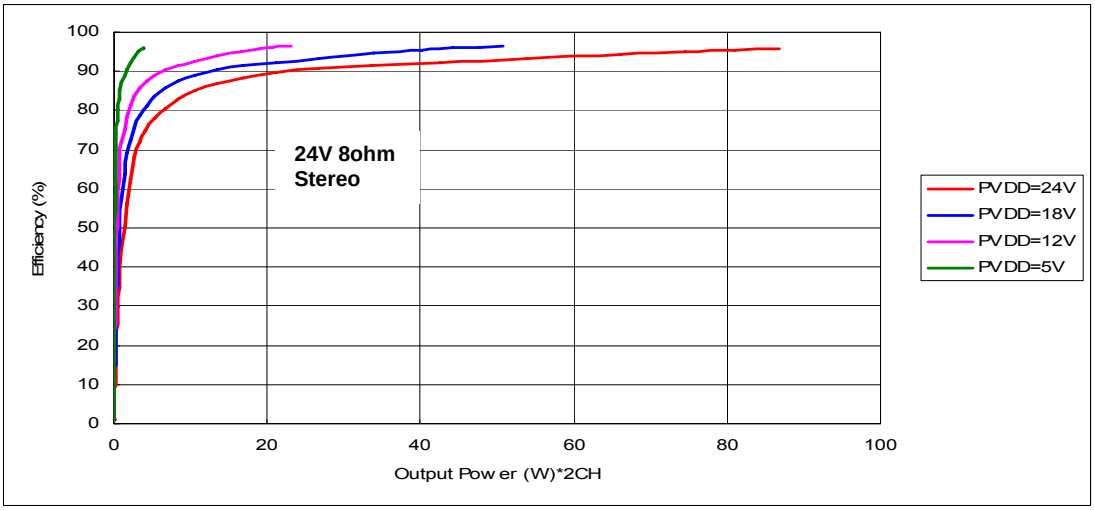
Frequency Response



Crosstalk

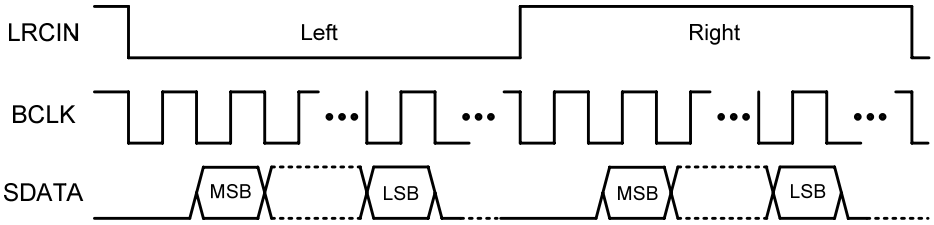


Efficiency

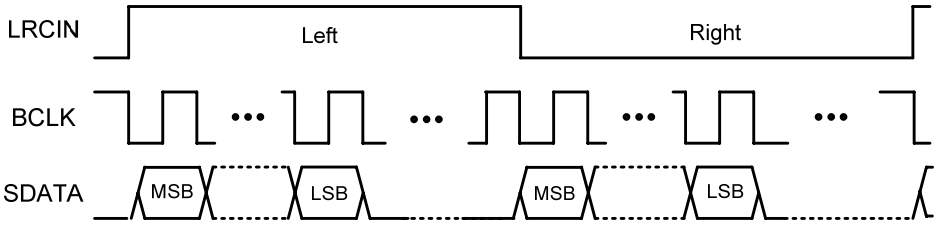


Interface configuration

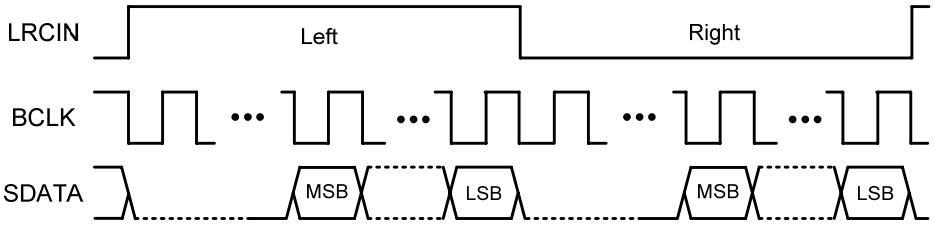
- I^2S



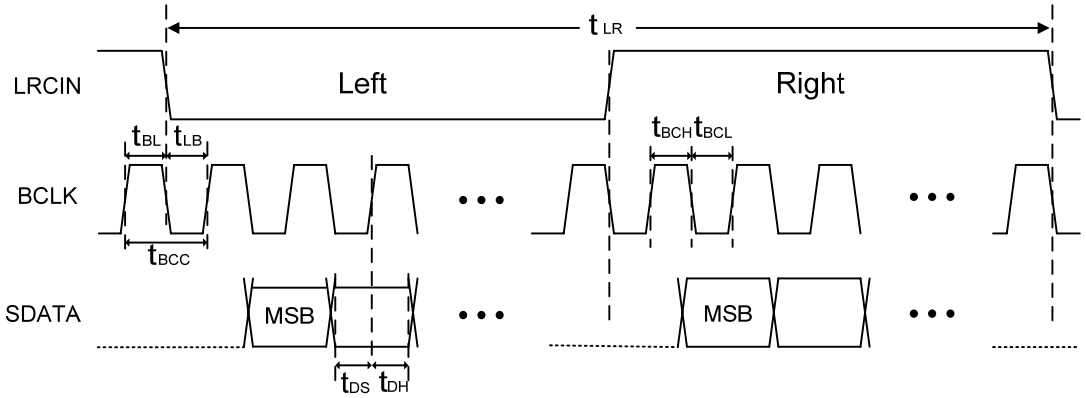
- Left-Alignment



- Right-Alignment

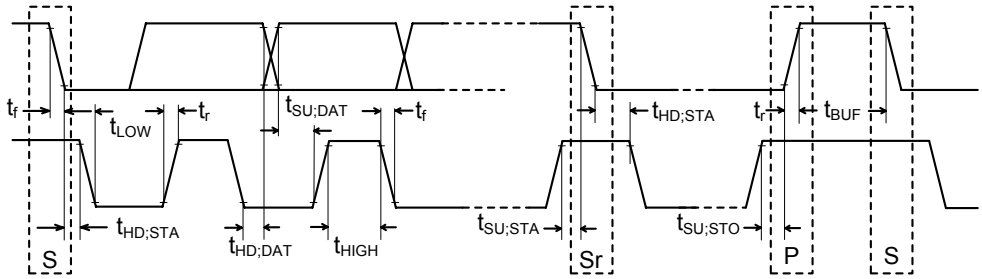


- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	5.2		31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	25			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	25			ns
t_{BCC}	BCLK Period ($1/64F_S$)	81.38		488.3	ns
t_{BCH}	BCLK Pulse Width High	40.69		244	ns
t_{BCL}	BCLK Pulse Width Low	40.69		244	ns
t_{DS}	SDATA Set-Up Time	25			ns
t_{DH}	SDATA Hold Time	25			ns

- I^2C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time for repeated START condition	$t_{HD,STA}$	4.0	---	0.6	---	μs
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	μs
Setup time for repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	μs
Hold time for I^2C bus data	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Setup time for I^2C bus data	$t_{SU;DAT}$	250	---	100	---	ns
Rise time of both SDA and SCL signals	t_r	---	1000	---	300	ns
Fall time of both SDA and SCL signals	t_f	---	300	---	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	μs
Bus free time between STOP and the next START condition	t_{BUF}	4.7	---	1.3	---	μs
Capacitive load for each bus line	C_b		400		400	pF

I²C-Bus Transfer Protocol

- Introduction

AD82589 employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD82589 is always an I²C slave device.

- Protocol

  - START and STOP condition

START is identified by a high to low transition of the SDA signal. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD82589 and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

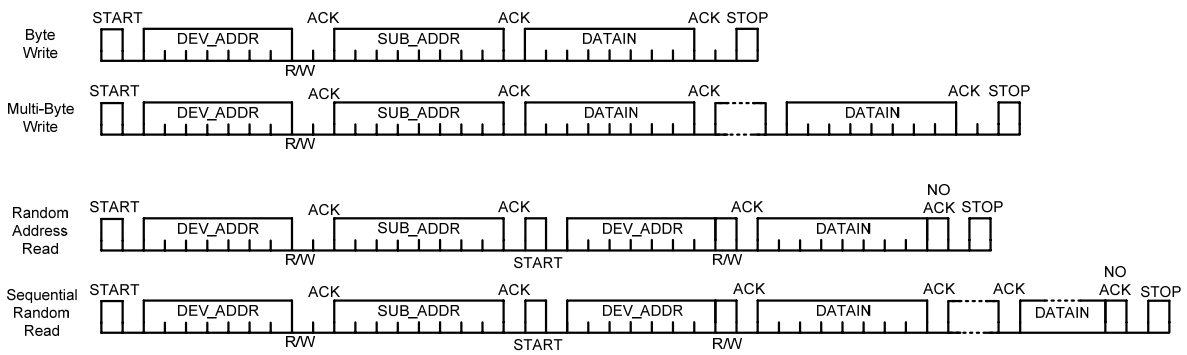
The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD82589 samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

The master generates 7-bit address to recognize slave devices. When AD82589 receives 7-bit address matched with 0110x01 (where x can be selected by external SA pins), AD82589 will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD82589 internal sub-addresses.

  - Data transferring

Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD82589 supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



Operation Descriptions

The description below explains AD82589 functions and operations,

- **Digital Amplifier Modulation Method**

  AD82589 has a built-in stereo digital Class-D amplifier with digital signal processing capability. After the digital input audio signal is processed, the signal is modulated and generates Pulse Width Modulated (PWM) outputs. The pulse frequency that appears between OUTP* and OUTM* pins is called “Carrier Clock Frequency.” Figure 2 below shows the PWM output waveforms for an audio sine wave about the characteristics of modulation method. As shown in B of the figure, the frequency that appears between GND and OUTP* pins and between GND and OUTM* pins at no-signal input becomes the half of a carrier clock frequency. As shown in A, C of the figure, when the output power increases, one side stops its switching and the other serves as a carrier clock frequency.

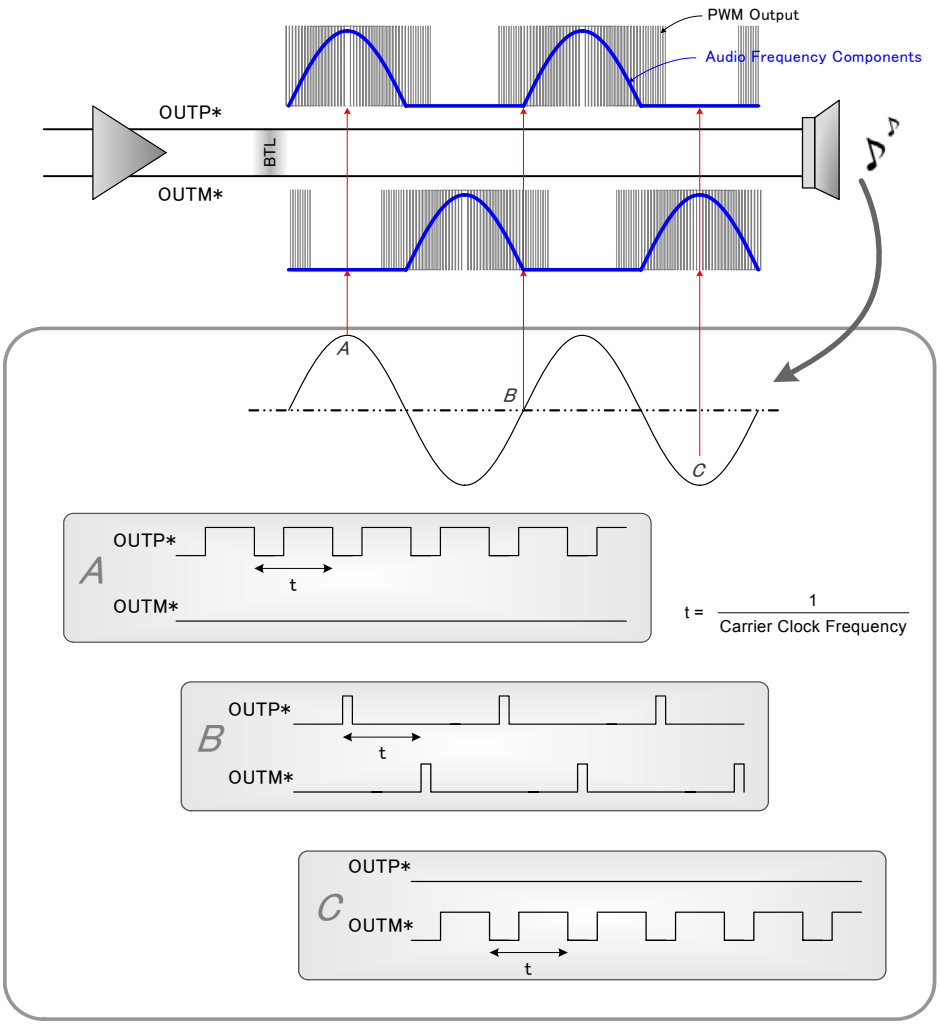


Figure 2, modulation method with AD82589

- **Quick Mute/Quick Start Function**

Quick Mute/Quick Start function reduces pop sound significantly by varying the output envelope at a slower rate when AMP_HARD_MUTE register is turned ON or OFF.

AMP_HARD_MUTE register	Mode
L	Normal Operation State
H	Digital Amplifier Mute State

Table 1

By setting AMP_HARD_MUTE register to "H" via I^2C, AD82589 performs Quick Mute operation (Decreasing the volume linearly by taking 1024×1/96K), (16×96) / (carrier clock frequency)[s] later, it sets the digital amplifier output to WL (Weak Low: a state grounded through a high-value resistance), resulting in mute state (Output Disabled).

By setting AMP_HARD_MUTE register to "L" via I^2C, AD82589 moves from the mute state to normal operation state while turned down volume. Afterwards, the quick start operation (where the volume is increased linearly over 512×1/96K) is executed. Mute recovery time from Mute state is t_{mrcv}(Typ.). If the mute state is cancelled during the Quick Mute sequence, Quick Start sequence will start after the quick mute sequence.

When the voltage at PVDD pin becomes lower than PVDD pin Shutdown threshold voltage (V_{HUVLL}) in the mute state, for shutting down the system safely, the amplifier output is set to WL (Weak Low: a state grounded through a high-value resistance) after outputting a low signal for a given period of time.

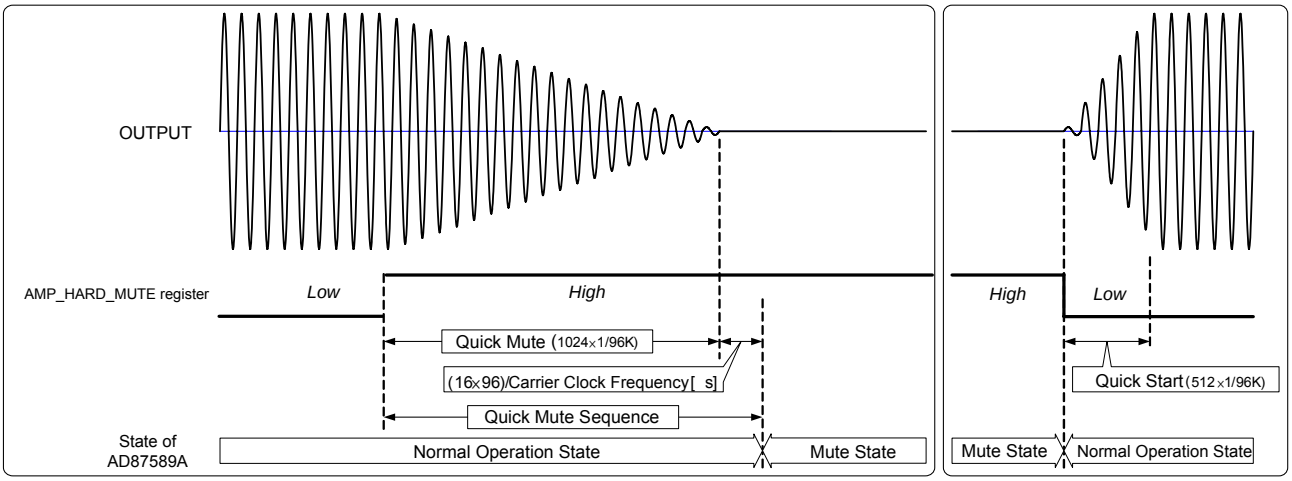


Figure 3, Quick Mute and Quick Start

- **Sleep Function**

In sleep state, the device are stopped and consumption current becomes the minimum (I_{DDPS}). REFA and VREFN pins outputs are pulled down, and VREFP pin is pulled high.

SLEEPN pin	Mode
L	Sleep State
H	Normal Operation State

Table 2

By setting SLEEPN pin to “L”, AD82589 performs Quick Mute operation (Decreasing the volume linearly by taking 1024×1/96K), (16×96) / (carrier clock frequency) [s] later, it sets the digital amplifier output to WL (Weak Low: a state grounded through a high-value resistance).

AD82589 goes to sleep state when max.160ms has passed after setting SLEEPN pin to "L."
When going to sleep mode while some protection state is being activated, this protection mode is cancelled and PROTN pin output goes to Hi-Z state.

With PVDD pin output being higher than the threshold voltage to cancel the low-voltage malfunction preventing function, when changing the state of SLEEPN pin from “L” to “H,” the digital amplifier terminates the sleep state, simultaneously starts the Startup Sequence and does the quick start (raises the volume level linearly by taking 512×1/96K) to activate the oscillation after max.300ms.

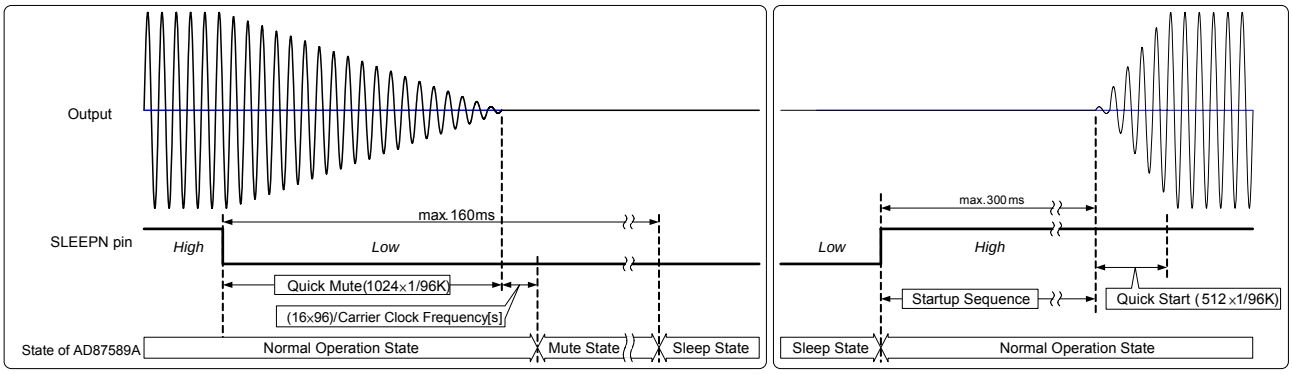


Figure 4, Sleep Function

- **Supply Voltage Regulation**

  AD82589 adopts a circuit method that feeds back the output signal. This method allows the deterioration in distortion characteristics to be minimized even when a supply voltage fluctuates (in case of a power supply not regulated). Whereas, with a non-feedback type digital amplifier, a power supply with high-regulation capability is required because this fluctuation is added to the output waveform. AD82589 includes three regulators to generate REFA, VREFN, and VREFP voltages.

- **REFA Voltage Output Function**

  The voltage inputted from a DVDD power supply pin is supplied to a regulator. REFA pin outputs the voltage (REFA) regulated from the voltage coming from DVDD pin. For its stabilization, connect a bypass capacitor of 1.0μF to 4.7μF between REFA and AVSS pins (0.8μF or more should be secured including its variation and temperature change.). REFA pin must not be connected to other devices.

- **VREFN Voltage Output Function**

  The voltage inputted from a PVDD power supply pin is supplied to a regulator. VREFN pin outputs the voltage (VREFN) regulated from the voltage coming from PVDD pin. For its stabilization, connect a bypass capacitor of 1.0μF to 4.7μF between VREFN and PVSS pins (0.8μF or more should be secured including its variation and temperature change.). VREFN pin must not be connected to other devices.

- **VREFP Voltage Output Function**

  The voltage inputted from a PVDD power supply pin is supplied to a regulator. VREFP pin outputs the voltage (VREFP) regulated from the voltage coming from PVDD pin. For its stabilization, connect a bypass capacitor of 1.0μF to 4.7μF between VREFP and PVDD pins (0.8μF or more should be secured including its variation and temperature change.). VREFP pin must not be connected to other devices

- **Digital Amplifier Startup/Shutdown Procedure**

  It is recommended to use the following sequences as digital amplifier start and shutdown procedure. With different sequence, unusual sound or pop noise may occur.

- **Recommended Digital Amplifier Startup Sequence**

  1. Supply the power to PVDD pin.
  2. When the supply voltage reaches at the recommended voltage range, input clocks to SCLK, and LRCK pins. The I^2S formation and sampling frequency (address 0X01, state control 1) shall be setting in advance of input clocks to SCLK, and LRCK pins.
  3. Change the logical state of SLEEPN pin from “L” to “H”

● **Recommended Digital Amplifier Shutdown Sequence**

1. Change the logical state of SLEEPN pin from “H” to “L”.
2. After 160ms or more, stop input the signal to the input pins and shut down the power to PVDD pin.

* As long as SLEEPN pin was changed from “H” to “L” and Quick Mute {1024×1/96k + (16×96) / (Carrier Clock Frequency） }[s]” has elapsed, unusual sound or pop noise is not generated even if the power is shut down.

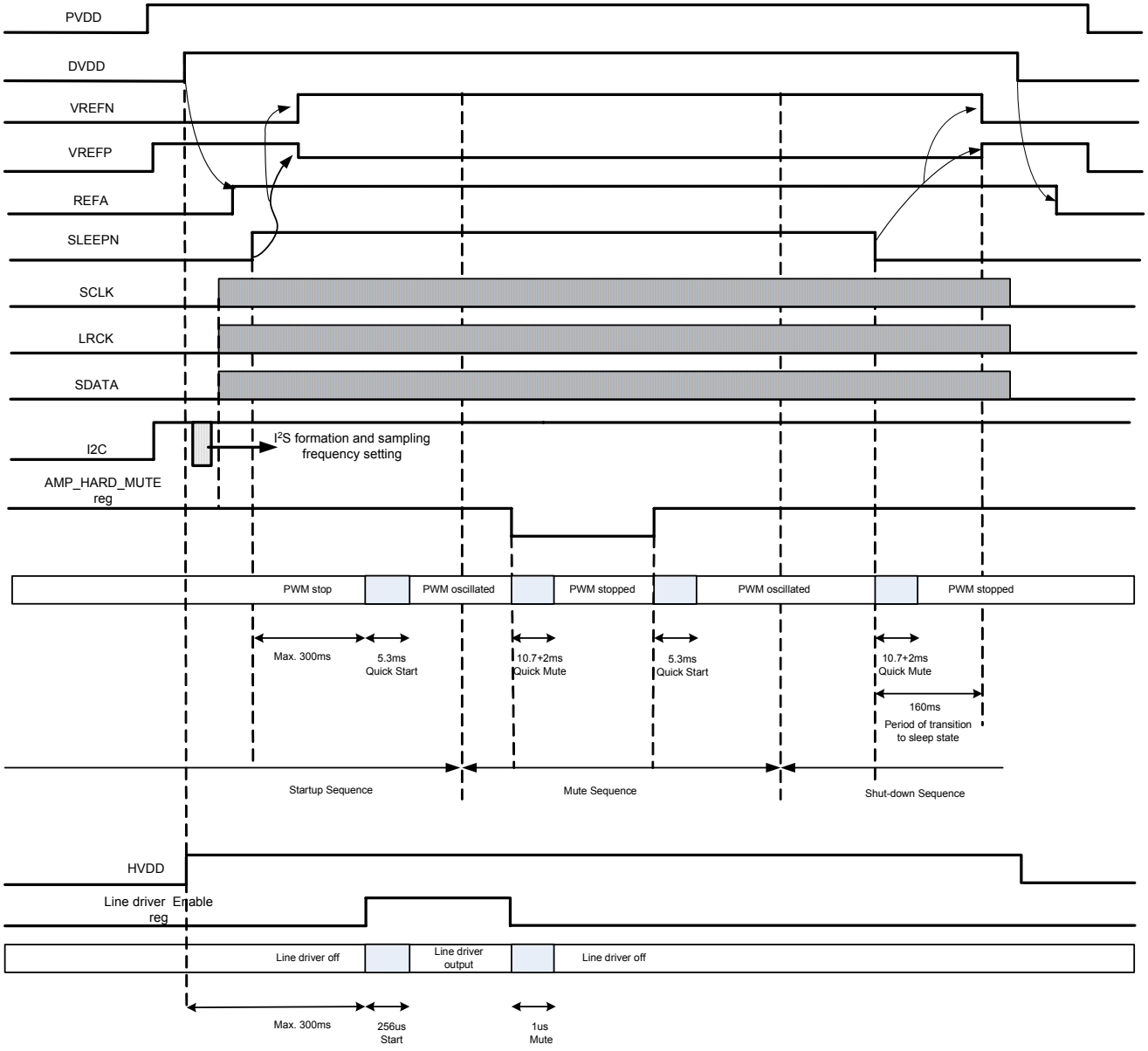


Figure 5, Startup and Shutdown sequence

- **LC Filter**

On the other hand, when using a LC filter, the output circuit as shown in Figure 6, 7 should be used with the constants listed in Table 3. The use of these constants enables the filter to be a low-pass filter with its cut-off frequency being 50kHz or so and Q being 0.6 or so. When disconnecting a speaker, turn off the power in advance. When operating the device without a speaker, consumption current may increase or over current detection circuit may work due to the resonance in LC filter. When removing a speaker during operation, SLEEPN or MUTEN pin should be set to "L" or PVDD should be shut down.

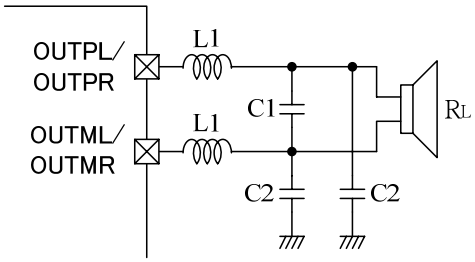


Figure 6, LC Filter Circuit (Stereo)

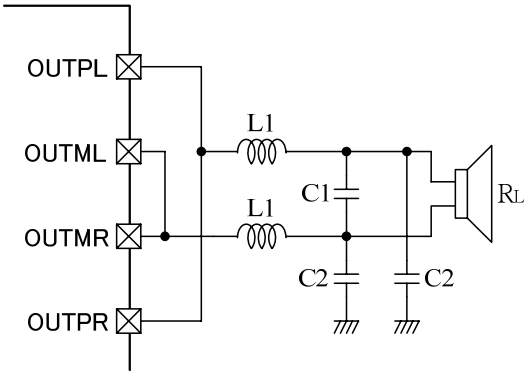


Figure 7, LC Filter Circuit (Mono)

R_L	L1	C1	C2	fc	Q
4Ω	10μH	0.47μF	1nF	51.9kHz	0.61
6Ω	15μH	0.33μF	1nF	50.6kHz	0.62
8Ω	22μH	0.47μF	1nF	35kHz	0.82
16Ω	47μH	0.1μF	1nF	51.9kHz	0.52

Table 3

$$f_C = \frac{1}{2\pi\sqrt{L_1 \times (2 \times C_1 + C_2)}}$$

$$f_C(toGND) = \frac{1}{2\pi\sqrt{L_1 C_2}}$$

$$Q = \frac{\sqrt{\frac{2 \times C_1 + C_2}{L_1}} \times R_L}{2}$$

When using AD82589 with a speaker connected directly without connecting LC filters, or when using it with EMI countermeasure components, such as ferrite beads etc., in addition to a speaker, a speaker with an inductance higher than 20μH should be used. Otherwise, loss of the speaker and AD82589 may increase.

- Protection function

AD82589 has over current protection, over temperature protection, under voltage lock out function, DC detection, clock detection and over voltage lock out functions. In SLEEPN=Low, UVLO state and early stage of start up sequence, all protection function is disabled.

Table4, Protection functions

Protection Function	PROTN Output	Digital Amplifier Output	Automatic Recovery	Detect Seq.
Over current Protection	L	WL(*3	Applicable(*1	100ms H/L WL
Over Temperature Protection	L*2)	WL(*3	Not Applicable (Recover when temperature go down)	100ms L WL
Under Voltage Lock Out (PVDD,DVDD pin)	H	WL(*3	Not Applicable (Recover when pin voltage go up)	100ms L WL
DC Detection	L	WL(*3	Applicable(*1	100ms L WL
Clock Detection (SCLK,PLLCLK)	H	WL(*3	Not Applicable (Recover when clock frequency go up)	1msec L WL
DAIF error	H	normal	Not Applicable (Recover when keep 64fs)	maintain previous cycle data
Over Voltage Protection	L	WL	Not Applicable (Recover when voltage go down)	100ms L WL

Note:
*1): Automatic recovery is performed 2.7 to 5.4 seconds (at Fs=48kHz) after a protecting function is activated, and then PROTN pin goes to "H."
*2): When an over temperature condition is cleared, PROTN is returned to "H."
*3): To shutting down the system safely, the amplifier output is set to WL after outputting a low or high signal for a given period of time.

PROTN pin has an open-drain output. Use a resistor of 47kΩ to pull up the pin with respect to an external power supply source lower than 3.3V. In order to prevent the current in excess of 2mA from being flowed into PROTN pin being in L state. If multiple AD82589s are used, all the PROTNs can be tied together for wired OR connection. PROTN pin must not connect to pins of AD82589. PROTN pin should be left open when not used.

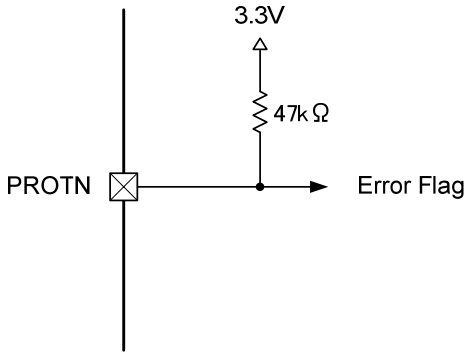


Figure 8

- **Over current protection**

  This function, detecting an over current condition at the digital amplifier output, enables the over-current protection state, in which the following short-circuiting conditions are detected: VSS short (ground or any other lower-potential point), PVDD short (supply voltage or a higher-potential point), or short-circuiting between ±output pins. The detection current, for pin-to-pin short-circuiting, is 6A (typ., PVDD=24V). In this state, digital amplifier outputs are forced to “WL” state (Weak Low: a state grounded through a high-value resistance) and PROTN pin goes to “L”. The automatic recovery operation is performed 2.7 to 5.4 seconds (at fs=48kHz) after the protection state is activated. When detected eight times in all, the protection state is held without being cancelled. The held protection state can be cancelled by setting SLEEPN pin to “L” temporarily or shutting down the power. This protection state is provided not for guarantee of IC protection in case of exceeding the maximum rating (speaker impedance) but for safety in case of unusual conditions.

- **Over Voltage Protection Function (OVP)**

  This function, detecting an unusual condition where the voltage at PVDD pin becomes higher than PVDD pin shutdown threshold voltage, and prevent malfunction etc. In this high-voltage protection state, digital amplifier outputs become WL state (Weak Low: a state grounded through a high-value resistance). When voltages at PVDD pin become lower than high-voltage cancel threshold voltage, the high-voltage protection state is cancelled and the normal operation starts after max. 300ms. This function does not guarantee all operations even if PVDD pin voltage is over the startup threshold voltage. Be sure to use this IC within the recommended supply voltage.

- **Over Temperature Protection Function (OTP)**

  This function, detecting an unusual condition high temperature condition in the chip, and protect IC by output disable. In this over temperature protection state, in which digital amplifier outputs are forced to “WL” state (Weak Low: a state grounded through a high-value resistance) and PROTN pin goes to “L”. When such unusual temperature in the chip is lowered, the protection state is cancelled and PROTN goes to “Hi-Z”. At the same time, normal operation will start again after a quick start. This protection function is provided not for guaranteeing the protection in case of exceeding the maximum ratings (junction temperature) but for ensuring safety in case of unusual conditions.

- **PVDD Under Voltage Lock Out Function (HUVLO)**

  This function, detecting an unusual condition where the voltage at PVDD pin becomes lower than PVDD pin under voltage lock out threshold. In this low-voltage protection state, digital amplifier outputs become WL state (Weak Low: a state grounded through a high-value resistance). When voltages at PVDD pin become higher than under voltage release threshold voltage (V_{HUVLH}), the low-voltage protection state is cancelled and the normal operation starts after max. 300ms. This function does not guarantee all operations even if PVDD pin voltage is over the startup threshold voltage V_{HUVLH}. Be sure to use this IC within the recommended supply voltage.

- **DVDD Under Voltage Lock Out Function (UVLO)**

  This function, detecting an unusual condition where the voltage at DVDD pin becomes lower than DVDD pin under voltage lock out threshold. In this low-voltage protection state, digital amplifier outputs become WL state (Weak Low: a state grounded through a high-value resistance). When voltages at DVDD pin become higher than low-voltage cancel threshold voltage (around 2.7V), the low-voltage protection state is cancelled and the normal operation starts after max. 300ms. This function does not guarantee all operations even if DVDD pin voltage is over the startup threshold voltage. Be sure to use this IC within the recommended supply voltage.

- **DC Detection Function (DCDET)**

  This function is activated when detecting a DC signal in excess of 4.1V (PVDD=24V) for a given period of time (0.67s to 1.33s) at the digital amplifier output and stops the output. In DC protection state, digital amplifier outputs are forced to WL state (Weak Low: a state grounded through a high-value resistance) and also L level is output to PROTN pin. The automatic recovery operation is performed 2.7 to 5.4 seconds (at fs=48kHz) after the activation of this protection state. When detected eight times in all, the protection state is held without being cancelled. The held protection state can be cancelled by setting SLEEPN pin to “L” temporarily or shutting down the power. This protection function is provided for ensuring safety, and does not guarantee the protection of the speaker.

- **Clock Detection Function (CKDET)**

  This is the function to prevent DC signals from being transmitted in case any clock to SCLK pin is stopped during the playback. When any clock is stopped, the internal free-running clock supersedes it and the digital amplifier output are forced to WL state (Weak Low: a state grounded through a high-value resistance). When a clock is received again at SCLK pin, the operation shifts to the normal operation state. This protection function is provided for ensuring safety, and does not guarantee the protection of the speaker.

Audio Processing

The AD82589's audio signal processing data flow is shown below. Users can control these functions by appropriate settings in the register table.

- Two bands DRC disable

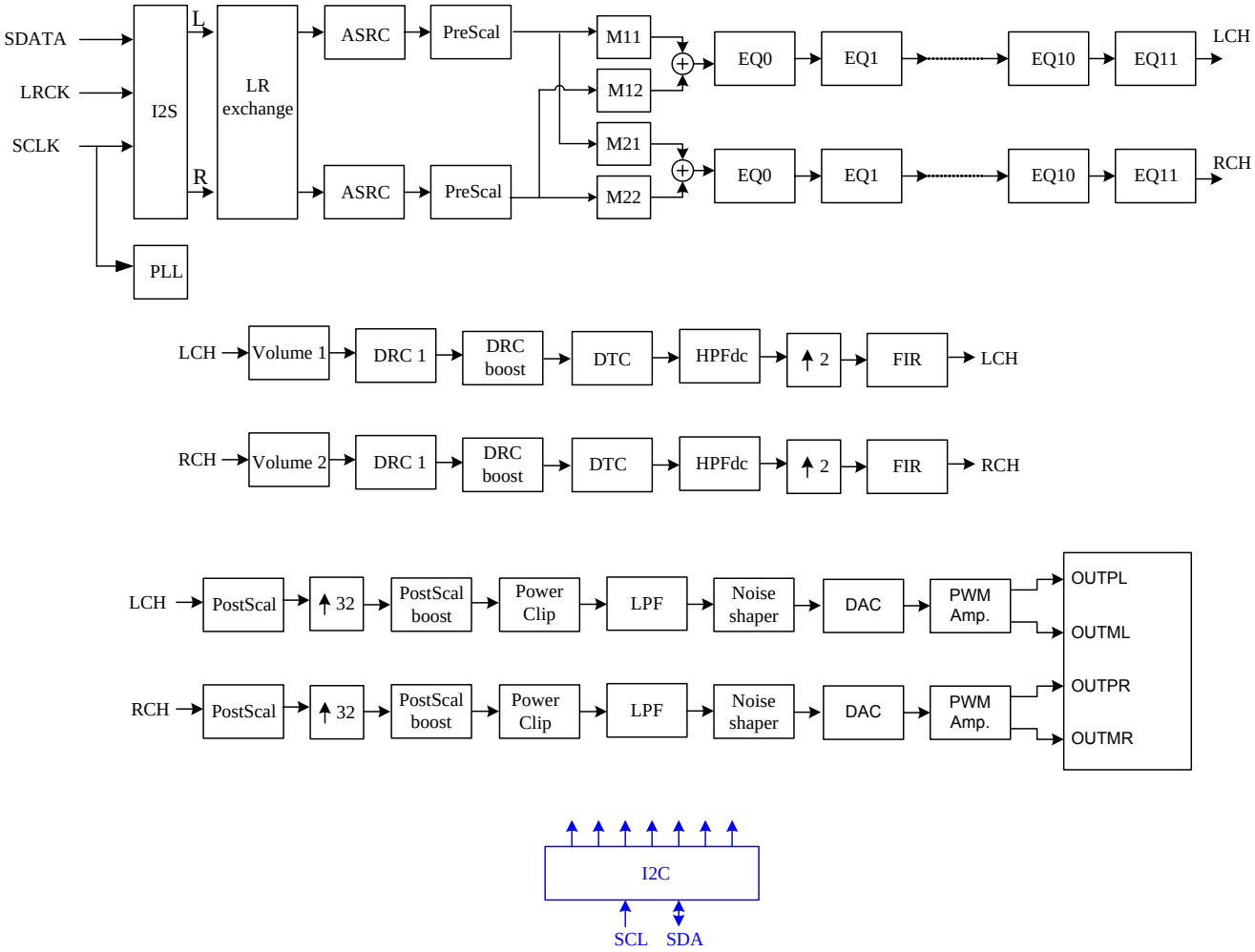


Figure 9

- Two bands DRC enable

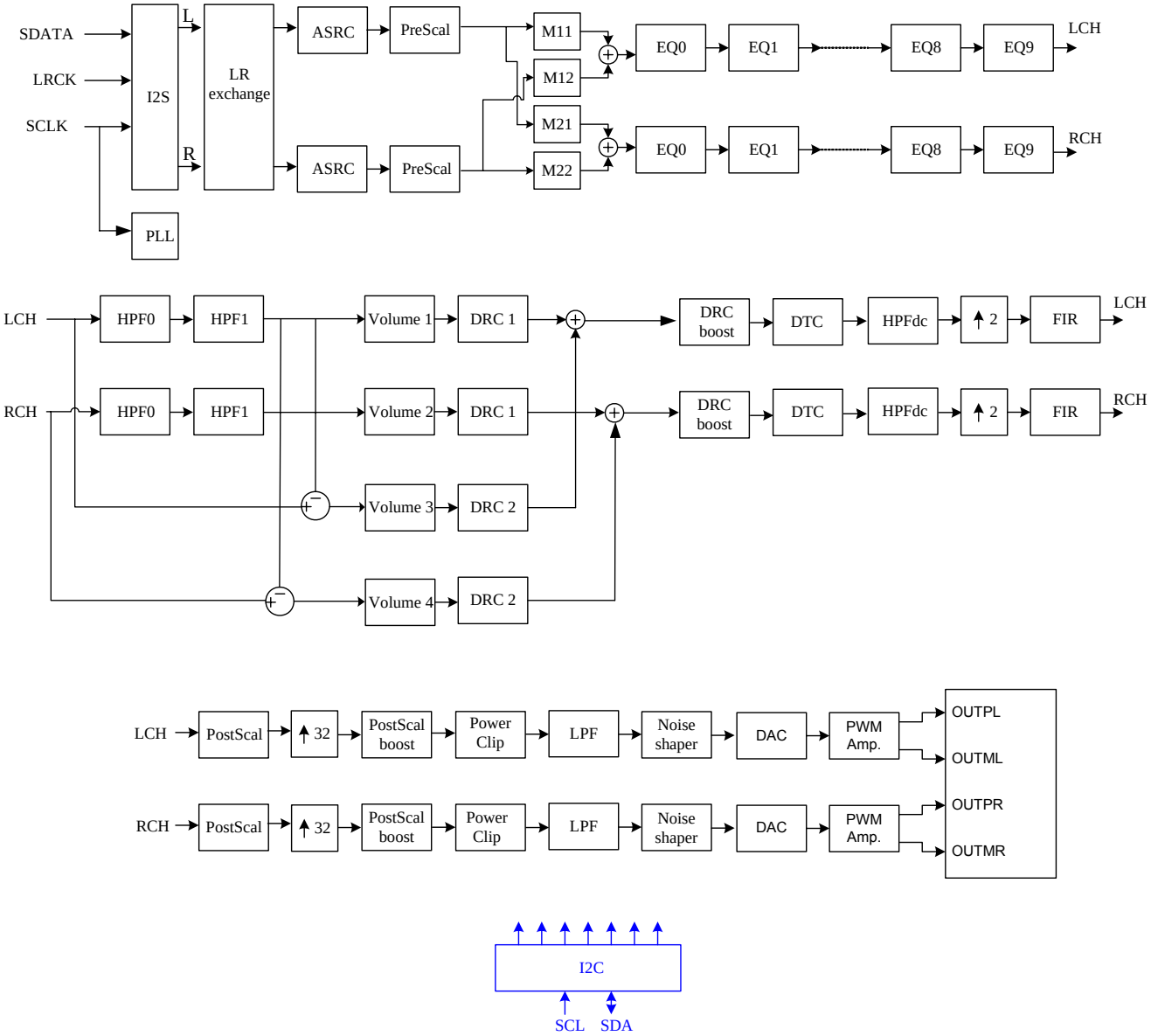


Figure 10

Register Table

The AD82589's audio signal processing data flow is shown below. Users can control these functions by programming appropriate settings in the register table. In this section, the register table is summarized first. The definition of each register follows in the next section.

Address	Name	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0X00	DEVICE ID	Device code				Version code			
0X01	STCL1	IF[2]	IF[1]	IF[0]	32kX3	FS[2]	FS[1]	FS[0]	Reserved
0X02	STCL2	HOPP[1]	HOPP[0]	Reserved	MMUTE	CM1	CM2	CM3	CM4
0X03	STCL3	LREXC	FQHALF	AMP_HARD_MUTE	NG_FADE_EN	DTC_EN	NG_GAIN[1]	NG_GAIN[0]	NG_EN
0X04	STCL4	BTE	TBDRC	DRC Boost	Post Boost	EQL	PSL	DSPB	Reserved
0X05	C1CFG	Reserved	Reserved	Reserved	C1DRCM	PC_C1_EN	DRC_C1_EN	Reserved	VOL_C1_EN
0X06	C2CFG	Reserved	Reserved	Reserved	C2DRCM	PC_C2_EN	DRC_C2_EN	Reserved	VOL_C2_EN
0X07	C3CFG	Reserved	Reserved	Reserved	C3DRCM	Reserved	DRC_C3_EN	Reserved	VOL_C3_EN
0X08	C4CFG	Reserved	Reserved	Reserved	C4DRCM	Reserved	DRC_C4_EN	Reserved	VOL_C4_EN
0X09	UVP	HVUV_EN	HV_UVSEL[3]	HV_UVSEL[2]	HV_UVSEL[1]	HV_UVSEL[0]	Reserved	Reserved	Reserved
0X0A	DTC	DTC_TH[1]	DTC_TH[0]	DTC_RATE[1]	DTC_RATE[0]	Reserved	Reserved	Reserved	Reserved
0X0B	TEST1	Reserved							
0X0C	TEST2	Reserved							
0X0D	MBIST	Prohibited							
0X0E	Protection	A_OCP_N	A_UVLO_N	A_LVDET	A_DC_ERR_N	A_CK_ERR_N	A_OTP_N	A_OVP_N	DAIF_ERR_N
0X0F	Protection Latch	A_OCP_N_LATCH	A_UVLO_N_LATCH	A_LVDET_N_LATCH	A_DC_ERR_N_LATCH	A_CK_ERR_N_LATCH	A_OTP_N_LATCH	A_OVP_N_LATCH	DAIF_ERR_N_LATCH
0X10	Error clear	A_OCP_N_CLEAR	A_ UVLO _N_CLEAR	A_ LVDET_N_CLEAR	A_DC_ERR_N_CLEAR	A_CK_ERR_N_CLEAR	A_OTP_N_CLEAR	A_OVP_N_CLEAR	DAIF_ERR _N_CLEAR
0X11	VFT1	MV_FT[1]	MV_FT[0]	C1V_FT[1]	C1V_FT[0]	C2V_FT[1]	C2V_FT[0]	C3V_FT[1]	C3V_FT[0]
0X12	VFT2	C4V_FT[1]	C4V_FT[0]						
0X13	MV	MV[7]	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]
0X14	C1V	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
0X15	C2V	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
0X16	C3V	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
0X17	C4V	C4V[7]	C4V[6]	C4V[5]	C4V[4]	C4V[3]	C4V[2]	C4V[1]	C4V[0]
0X18	LAR1	LA1[3]	LA1[2]	LA1[1]	LA1[0]	LR1[3]	LR1[2]	LR1[1]	LR1[0]
0X19	LAR2	LA2[3]	LA2[2]	LA2[1]	LA2[0]	LR2[3]	LR2[2]	LR2[1]	LR2[0]
0X1A	Reserved	Reserved							
0X1B	Reserved	Reserved							
0X1C	Reserved	Reserved							
0X1D	Reserved	Reserved							

0X1E	Reserved	Reserved							
0X1F	Reserved	Reserved							
0X20	Reserved	Reserved							
0X21	Reserved	Reserved							
0X22	Reserved	Reserved							
0X23	Reserved	Reserved							
0X24	Reserved	Reserved							
0X25	Reserved	Reserved							
0X26	Reserved	Reserved							
0X27	Reserved	Reserved							
0X28	BTONE	Reserved	Reserved	Reserved	BTC[4]	BTC[3]	BTC[2]	BTC[1]	BTC[0]
0X29	TTONE	Reserved	Reserved	Reserved	TTC[4]	TTC[3]	TTC[2]	TTC[1]	TTC[0]
0X2A	Reserved	Reserved							
0X2B	CFADDR	CFA[7]	CFA[6]	CFA[5]	CFA[4]	CFA[3]	CFA[2]	CFA[1]	CFA[0]
0X2C	A1CF1	C1B[23]	C1B[22]	C1B[21]	C1B[20]	C1B[19]	C1B[18]	C1B[17]	C1B[16]
0X2D	A1CF2	C1B[15]	C1B[14]	C1B[13]	C1B[12]	C1B[11]	C1B[10]	C1B[9]	C1B[8]
0X2E	A1CF3	C1B[7]	C1B[6]	C1B[5]	C1B[4]	C1B[3]	C1B[2]	C1B[1]	C1B[0]
0X2F	A2CF1	C2B[23]	C2B[22]	C2B[21]	C2B[20]	C2B[19]	C2B[18]	C2B[17]	C2B[16]
0X30	A2CF2	C2B[15]	C2B[14]	C2B[13]	C2B[12]	C2B[11]	C2B[10]	C2B[9]	C2B[8]
0X31	A2CF3	C2B[7]	C2B[6]	C2B[5]	C2B[4]	C2B[3]	C2B[2]	C2B[1]	C2B[0]
0X32	B1CF1	C3B[23]	C3B[22]	C3B[21]	C3B[20]	C3B[19]	C3B[18]	C3B[17]	C3B[16]
0X33	B1CF2	C3B[15]	C3B[14]	C3B[13]	C3B[12]	C3B[11]	C3B[10]	C3B[9]	C3B[8]
0X34	B1CF3	C3B[7]	C3B[6]	C3B[5]	C3B[4]	C3B[3]	C3B[2]	C3B[1]	C3B[0]
0X35	B2CF1	C4B[23]	C4B[22]	C4B[21]	C4B[20]	C4B[19]	C4B[18]	C4B[17]	C4B[16]
0X36	B2CF2	C4B[15]	C4B[14]	C4B[13]	C4B[12]	C4B[11]	C4B[10]	C4B[9]	C4B[8]
0X37	B2CF3	C4B[7]	C4B[6]	C4B[5]	C4B[4]	C4B[3]	C4B[2]	C4B[1]	C4B[0]
0X38	A0CF1	C5B[23]	C5B[22]	C5B[21]	C5B[20]	C5B[19]	C5B[18]	C5B[17]	C5B[16]
0X39	A0CF2	C5B[15]	C5B[14]	C5B[13]	C5B[12]	C5B[11]	C5B[10]	C5B[9]	C5B[8]
0X3A	A0CF3	C5B[7]	C5B[6]	C5B[5]	C5B[4]	C5B[3]	C5B[2]	C5B[1]	C5B[0]
0X3B	CFRW	Reserved				RA	R1	WA	W1
0X3C	RAM1_ CFADDR	Prohibited							
0X3D	RAM1_ A1CF1	Prohibited							
0X3E	RAM1_ A1CF2	Prohibited							

0X3F	RAM1_ A1CF3	Prohibited							
0X40	RAM1_ CFRW	Prohibited							
0X41	RAM2_ CFADDR	Prohibited							
0X42	RAM2_ A1CF1	Prohibited							
0X43	RAM2_ A1CF2	Prohibited							
0X44	RAM2_ A1CF3	Prohibited							
0X45	RAM2_ CFRW	Prohibited							
0X46	Reserved	Reserved							
0X47	CHS_STAT	CHK_DRC_P	CHK_DRC_AM	CHK_DRC_R	CHK_DRC_EN	CHK_BEQ_P	CHK_ BEQ_AM	CHK_ BEQ _R	CHK_ BEQ _EN
0X48	CHS_DRC_V	CHS_DRC_V[23]	CHS_DRC_V[22]	CHS_DRC_V[21]	CHS_DRC_V[20]	CHS_DRC_V[19]	CHS_DRC_V[18]	CHS_DRC_V[17]	CHS_DRC_V[16]
0X49	CHS_DRC_V	CHS_DRC_V[15]	CHS_DRC_V[14]	CHS_DRC_V[13]	CHS_DRC_V[12]	CHS_DRC_V[11]	CHS_DRC_V[10]	CHS_DRC_V[9]	CHS_DRC_V[8]
0X4A	CHS_DRC_V	CHS_DRC_V[7]	CHS_DRC_V[6]	CHS_DRC_V[5]	CHS_DRC_V[4]	CHS_DRC_V[3]	CHS_DRC_V[2]	CHS_DRC_V[1]	CHS_DRC_V[0]
0X4B	CHS_BEQ_V	CHS_ BEQ _V[23]	CHS_ BEQ _V[22]	CHS_ BEQ _V[21]	CHS_ BEQ _V[20]	CHS_ BEQ _V[19]	CHS_ BEQ _V[18]	CHS_BEQ _V[17]	CHS_ BEQ _V[16]
0X4C	CHS_ BEQ _V	CHS_ BEQ _V[15]	CHS_ BEQ _V[14]	CHS_ BEQ _V[13]	CHS_ BEQ _V[12]	CHS_ BEQ _V[11]	CHS_ BEQ _V[10]	CHS_ BEQ _V[9]	CHS_ BEQ _V[8]
0X4D	CHS_ BEQ _V	CHS_ BEQ _[7]	CHS_ BEQ _V[6]	CHS_ BEQ _V[5]	CHS_ BEQ _V[4]	CHS_ BEQ _V[3]	CHS_ BEQ _V[2]	CHS_ BEQ _V[1]	CHS_ BEQ _V[0]
0X4E	CHS_DRC_R	CHS_DRC_R[23]	CHS_DRC_R[22]	CHS_DRC_R[21]	CHS_DRC_R[20]	CHS_DRC_R[19]	CHS_DRC_R[18]	CHS_DRC_R[17]	CHS_DRC_R[16]
0X4F	CHS_DRC_R	CHS_DRC_R[15]	CHS_DRC_R[14]	CHS_DRC_R[13]	CHS_DRC_R[12]	CHS_DRC_R[11]	CHS_DRC_R[10]	CHS_DRC_R[9]	CHS_DRC_R[8]
0X50	CHS_DRC_R	CHS_DRC_R[7]	CHS_DRC_R[6]	CHS_DRC_R[5]	CHS_DRC_R[4]	CHS_DRC_R[3]	CHS_DRC_R[2]	CHS_DRC_R[1]	CHS_DRC_R[0]
0X51	CHS_BEQ_R	CHS_ BEQ _R[23]	CHS_ BEQ _R[22]	CHS_ BEQ _R[21]	CHS_ BEQ _R[20]	CHS_ BEQ _R[19]	CHS_ BEQ _R[18]	CHS_BEQ _R[17]	CHS_ BEQ _R[16]
0X52	CHS_ BEQ _R	CHS_ BEQ_R[15]	CHS_ BEQ _R[14]	CHS_ BEQ _R[13]	CHS_ BEQ _R[12]	CHS_ BEQ _R[11]	CHS_ BEQ _R[10]	CHS_ BEQ _R[9]	CHS_ BEQ _R[8]
0X53	CHS_ BEQ _R	CHS_ BEQ _R[7]	CHS_ BEQ _R[6]	CHS_ BEQ _R[5]	CHS_ BEQ _R[4]	CHS_ BEQ _R[3]	CHS_ BEQ _R[2]	CHS_ BEQ _R[1]	CHS_ BEQ _R[0]
0X54	Reserved	Reserved							
0X55	Reserved	Reserved							

0X56	**CLR_LEVEL**	C1_CLR	C2_CLR	C3_CLR	C4_CLR	Reserved	Reserved	Reserved	Reserved
0X57	**C1_LEVEL**	C1_LEVEL[23]	C1_LEVEL[22]	C1_LEVEL[21]	C1_LEVEL[20]	C1_LEVEL[19]	C1_LEVEL[18]	C1_LEVEL[17]	C1_LEVEL[16]
0X58	**C1_LEVEL**	C1_LEVEL[15]	C1_LEVEL[14]	C1_LEVEL[13]	C1_LEVEL[12]	C1_LEVEL[11]	C1_LEVEL[10]	C1_LEVEL[9]	C1_LEVEL[8]
0X59	**C1_LEVEL**	C1_LEVEL[7]	C1_LEVEL[6]	C1_LEVEL[5]	C1_LEVEL[4]	C1_LEVEL[3]	C1_LEVEL[2]	C1_LEVEL[1]	C1_LEVEL[0]
0X5A	**C2_LEVEL**	C2_LEVEL[23]	C2_LEVEL[22]	C2_LEVEL[21]	C2_LEVEL[20]	C2_LEVEL[19]	C2_LEVEL[18]	C2_LEVEL[17]	C2_LEVEL[16]
0X5B	**C2_LEVEL**	C2_LEVEL[15]	C2_LEVEL[14]	C2_LEVEL[13]	C2_LEVEL[12]	C2_LEVEL[11]	C2_LEVEL[10]	C2_LEVEL[9]	C2_LEVEL[8]
0X5C	**C2_LEVEL**	C2_LEVEL[7]	C2_LEVEL[6]	C2_LEVEL[5]	C2_LEVEL[4]	C2_LEVEL[3]	C2_LEVEL[2]	C2_LEVEL[1]	C2_LEVEL[0]
0X5D	**C3_LEVEL**	C3_LEVEL[23]	C3_LEVEL[22]	C3_LEVEL[21]	C3_LEVEL[20]	C3_LEVEL[19]	C3_LEVEL[18]	C3_LEVEL[17]	C3_LEVEL[16]
0X5E	**C3_LEVEL**	C3_LEVEL[15]	C3_LEVEL[14]	C3_LEVEL[13]	C3_LEVEL[12]	C3_LEVEL[11]	C3_LEVEL[10]	C3_LEVEL[9]	C3_LEVEL[8]
0X5F	**C3_LEVEL**	C3_LEVEL[7]	C3_LEVEL[6]	C3_LEVEL[5]	C3_LEVEL[4]	C3_LEVEL[3]	C3_LEVEL[2]	C3_LEVEL[1]	C3_LEVEL[0]
0X60	**C4_LEVEL**	C4_LEVEL[23]	C4_LEVEL[22]	C4_LEVEL[21]	C4_LEVEL[20]	C4_LEVEL[19]	C4_LEVEL[18]	C4_LEVEL[17]	C4_LEVEL[16]
0X61	**C4_LEVEL**	C4_LEVEL[15]	C4_LEVEL[14]	C4_LEVEL[13]	C4_LEVEL[12]	C4_LEVEL[11]	C4_LEVEL[10]	C4_LEVEL[9]	C4_LEVEL[8]
0X62	**C4_LEVEL**	C4_LEVEL[7]	C4_LEVEL[6]	C4_LEVEL[5]	C4_LEVEL[4]	C4_LEVEL[3]	C4_LEVEL[2]	C4_LEVEL[1]	C4_LEVEL[0]
0X63	**ROM_A_RD**	Prohibited							
0X64	**ROM_OUT_RD**	Prohibited							
0X65	**ROM_OUT_RD**	Prohibited							
0X66	**ROM_OUT_RD**	Reserved							

Detail Description for Register

Note that the highlighted columns are default values of these tables.

- Address 0X00 : Device number and version number

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Device ID	0010	Device ID
B[3:0]		Version ID	0001	Version ID

- Address 0X01 : State control 1

AD82589 supports multiple serial data input formats including I^2S, Left-alignment and Right-alignment. These formats are selected by users via bit7~bit5 of address 0X01.

When 32 kHz Fs is used, the default x2 oversampling ratio can be increased to x3 oversampling. Activation of this feature, it is possible to have a 96kHz DSP processing when 32kHz used. The PWM carrier frequency of this feature is the same as FS=48kHz. (768kHz) When 32Kx3 bit is set to “1” ,This feature is activated. But this feature is activated only FS=32kHz. It is not suggested to active this feature at other sample frequency.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF	Input format	000	I2S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
			110	Prohibited
			111	Prohibited
B[4]	32Kx3	X3 Over sampling	0	X2 over sampling
			1	X3 over sampling
B[3:1]	FS	Sampling frequency	000	32kHz
			001	44.1kHz,48kHz
			010	64kHz
			011	88.2kHz,96kHz
			100	128kHz
			101	176.4kHz,192kHz

- Address 0X02 : State control 2

AD82589 has mute function including master mute and channel mute. When master mute is enabled, all 2 processing channels are muted, and the output will be idle pulse. User can mute the each channel individually by channel mute. In two band mode, channel 1 and channel 3 mute will lead L channel idle pulse. On the other, channel 2 and channel 4 mute will lead R channel idle pulse. When mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	HOP	PWM frequency hopping	00	HOP0 (no hopping)
			01	HOP1
			10	HOP2
			11	Prohibited
B[4]	MMUTE	Master mute	0	All channel not muted
			1	All channel muted
B[3]	CM1	Channel 1 mute	0	CH1 not muted
			1	CH1 muted
B[2]	CM2	Channel 2 mute	0	CH2 not muted
			1	CH2 muted
B[1]	CM3	Channel 3 mute	0	CH3 not muted
			1	CH3 muted
B[0]	CM4	Channel 4 mute	0	CH4 not muted
			1	CH4 muted

Carrier Clock setting function

Carrier frequency (FCARRIER) is calculated by FS frequency which is defined in FS register. User should set FS register before sending digital audio data or Low MUTE register condition. Relationship between FS and FCARRIER is shown in Table 5. If HOP register is set to “1”, provided for setting the carrier clock frequency hopping, can change the carrier clock frequency. With an application having AM tuner, it is possible to reduce the interference between harmonic frequencies of the carrier and AM carrier frequency by varying the carrier clock frequency. For applications other than that, normally, this register should be set to “0”.

Table 5 Carrier frequency definition in register control mode

F_S (kHz)	F_{PWM}(kHz) HOP0	F_{PWM}(kHz) HOP1	F_{PWM}(kHz) HOP2
32,64,128	512	409.6	341.4
44.1,88.2,176.4	352	403.2	470.4
48,96,192	384	438.9	512

Changing HOP and 32KX3 register will change PWM frequency. User need set before sending audio data or give a mute command to avoid abnormal sounds. The carrier clock frequency for each setting is as shown in Table 6

Table 6. The carrier clock frequency setting for 32KX3

F_S (kHz)	F_{PWM}(kHz) (32Kx3 disable)	F_{PWM}(kHz) (32Kx3 enable)
32	512	384
48	384	Prohibited

- Address 0X03 : State control 3

The left/right channels can be exchanged to each other by programming to bit7, LREXC.
AD82589 PWM frequency can be changed to half via bit6, FQHALF.
PWM output can be stopped by set bit5 “1”, it is different from MMUTE, bit4 of address 0X02.
When set AMP_HARD_MUTE from “0” to “1”, the quick mute time is 12.7ms to stop the PWM.
When set AMP_HARD_MUTE from “1” to “0”, the quick start time is 5.3ms to recovery original amplitude.

AD82589 provide noise gate function if receiving 2048 signal sample points of both L and R channel smaller than noise gate attack level. User can change noise gate gain via bit2~ bit1. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, x0). User can select fade out or not via bit 4.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	LREXC	Left/Right channel input exchange	0	No exchange
			1	
B[6]	FQHALF	PWM frequency half	0	Default PWM frequency
			1	PWM frequency divide 2
B[5]	AMP_HARD_MUTE	Amp hard mute	0	Un-mute
			1	Mute
B[4]	NG_FADE_EN	Noise gate fade enable	0	Fade disable
			1	Fade enable
B[3]	DTC_EN	DTC enable	0	DTC disable
			1	DTC enable
B[2:1]	NG_GAIN	Noise gate detection gain	00	x1/8
			01	x1/4
			10	x1/2
			11	x0
B[0]	NG_EN	Noise gate enable	0	NG disable
			1	NG enable

- Address 0X04 : State control 4

The AD82589 provides several DSP setting as following.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	BTE	Bass/treble selection enable	0	Bass/treble disable
			1	Bass/treble enable
B[6]	TBDRC	Two band DRC enable	0	Two band DRC disable
			1	Two band DRC enable
B[5]	DRC boost	DRC boost +36dB	0	0dB
			1	+36dB
B[4]	Post boost	Post scale boost +48dB	0	0dB
			1	+48dB
B[3]	EQL	EQ link	0	Each channel use individual EQ
			1	Use channel-1 EQ
B[2]	PSL	Post-scale link	0	Each channel use individual post-scale
			1	Use channel-1 post-scale
B[1]	DSPB	EQ bypass	0	EQ enable
			1	EQ disable

- Address 0X05, 0X06, 0X07, and 0X08: Channel configuration registers

The AD82589 can configure each channel to enable or bypass DRC and channel volume and select the limiter set. AD82584 supports two modes of DRC: RMS and PEAK detection which can be selected via bit 4.

Address 0X05 and 0X06; where X=1or 2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[4]	CXDRCM	Channel x DRC mode	0	Peak detection
			1	RMS detection
B[3]	PC_CX_EN	Channel X power clipping enable	0	Channel x PC disable
			1	Channel x PC enable
B[2]	DRC_CX_EN	Channel X DRC enable	0	Channel x DRC disable
			1	Channel x DRC enable
B[0]	VOL_CX_EN	Channel X Master volume enable	0	Channel x master volume disable
			1	Channel x master volume enable

Address 0X07 and 0X08; where X=3 or 4

Channel 3 means the low frequency part of L channel when two band DRC enable.

Channel 4 means the low frequency part of R channel when two band DRC enable.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[4]	CXDRCM	Channel x DRC mode	0	Peak detection
			1	RMS detection
B[2]	DRC_CX_EN	Channel X DRC enable	0	Channel x DRC disable
			1	Channel x DRC enable
B[0]	VOL_CX_EN	Channel X Master volume enable	0	Channel x master volume disable
			1	Channel x master volume enable

Note. Channel 3 and channel 4 configurations are useless if two band DRC is disabled.

- Address 0X09 : Under voltage selection

AD82589 support multi-level HV under voltage detection via bit3~ bit0, using this function, AD82589 will fade out signal to avoid pop sounds if high voltage supply disappear before low voltage supply.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	HVUV_EN	PVDD pin UVLO Enable	0	HVUVLO Disable
			1	HVUVLO Enable
B[6:3]	HV_UVSEL	PVDD pin UVLO(V_{HVUVL}) selection	0000	4.0V
			0001	7.0V
			0011	9.0V
			0100	12.0V
			1100	15.0V
			1101	Prohibited
			1110	Prohibited
			1111	Prohibited

- Address 0X0A : Dynamic temperature selection

AD82589 supports dynamic temperature control. The table describes the setting of DTC.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	DTC_TH	DTC attack and release threshold	00	110 deg
			01	120 deg
			10	130 deg
			11	140 deg
B[5:4]	DTC_RATE	DTC attack and release rate	00	1dB/sec
			01	0.5dB/sec
			10	0.33dB/sec
			11	0.25dB/sec

- Address 0X0E :Protection register

The protection registers will show what kind of protection occurs.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N	OCP error	0	Over current occurs
			1	No over current
B[6]	A_UVLO_N	Under voltage error	0	Under voltage occurs
			1	No under voltage
B[5]	A_LVDET_N	Bias error	0	Bias error occurs
			1	No bias error
B[4]	A_DC_ERR_N	DC error	0	DC error occurs
			1	No DC error
B[3]	A_CK_ERR_N	Clock error	0	Clock error occurs
			1	No clock error
B[2]	A_OTP_N	OTP error	0	Over temperature occurs
			1	No over temperature
B[1]	A_OVP_N	OVP error	0	Over voltage occurs
			1	No over voltage
B[0]	DAIF_ERR_N	DAIF error	0	DAIF error
			1	No DAIF error

- Address 0X0F : Protection latch register

The protection latch registers will show what kind of protection ever occurred.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N_LATCH	OCP error latch signal	0	Over current ever occurred
			1	No over current
B[6]	A_UVLO_N_LATCH	Under voltage error latch signal	0	Under voltage ever occurred
			1	No under voltage
B[5]	A_LVDET_N_LATCH	Bias error latch signal	0	Bias error ever occurred
			1	No bias error
B[4]	A_DC_ERR_N_LATCH	DC error latch signal	0	DC error ever occurred
			1	No DC error
B[3]	A_CK_ERR_N_LATCH	Clock error latch signal	0	Clock error ever occurred
			1	No clock error
B[2]	A_OTP_N_LATCH	OTP error latch signal	0	Over temperature ever occurred
			1	No over temperature
B[1]	A_OVP_N_LATCH	OVP error latch signal	0	Over voltage ever occurred
			1	No over voltage
B[0]	DAIF_ERR_N_LATCH	DAIF error latch signal	0	DAIF error ever occurred
			1	No DAIF error

- Address 0X10 : Protection clear register

The protection latch registers will show what kind of protection ever occurred.

Using the protection clear registers can clear the corresponding protection latch registers.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N_CLEAR	OCP latch clear signal	0	No clear
			1	Clear
B[6]	A_UVLO_N_CLEAR	Under voltage latch clear signal	0	No clear
			1	Clear
B[5]	A_LVDET_N_CLEAR	LVDET latch clear signal	0	No clear
			1	Clear
B[4]	A_DC_ERR_N_CLEAR	DC_ERR latch clear signal	0	No clear
			1	Clear
B[3]	A_CK_ERR_N_CLEAR	CK_ERR latch clear signal	0	No clear
			1	Clear
B[2]	A_OTP_N_CLEAR	OTP latch clear signal	0	No clear
			1	Clear
B[1]	A_OVP_N_ CLEAR	OVP latch clear signal	0	No clear
			1	Clear
B[0]	DAIF_ERR_N_CLEAR	DAIF latch clear signal	0	No clear
			1	Clear

- Address 0X11 and 0X12: Volume fine tune

AD82589 supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

Address 0X11

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MV_FT	Main Volume Fine tune	00	0 dB
			01	-0.125 dB
			10	-0.25 dB
			11	-0.375 dB
B[5:4]	C1V_FT	CH1 Volume Fine tune	00	0 dB
			01	-0.125 dB
			10	-0.25 dB
			11	-0.375 dB
B[3:2]	C2V_FT	CH2 Volume Fine tune	00	0 dB
			01	-0.125 dB
			10	-0.25 dB
			11	-0.375 dB
B[1:0]	C3V_FT	CH3 Volume Fine tune	00	0 dB
			01	-0.125 dB
			10	-0.25 dB
			11	-0.375 dB

Address 0X12

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	CH4_FT	CH4 Volume Fine tune	00	0 dB
			01	-0.125 dB
			10	-0.25 dB
			11	-0.375 dB

- Address 0X13 : Master Volume

AD82589 supports both master-volume (Address 0X13) and channel-volume control (Address 0x14, 0x15 ,0X16, and 0X17) modes. Both volume control settings range from +6dB ~ -103dB and 0.5dB per step. Note that the master volume control is added to the individual channel volume control as the total volume control. For example, if the master volume level is set at, Level A (in dB unit) and the channel volume level is set at Level B (in dB unit), the total volume control setting is equal to Level A plus with Level B.

-103dB ≦ Total volume (Level A + Level B) ≦ +12dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MV	Main Volume	00000000	+6 dB
			00000001	+5.5 dB
			…	…
			00001100	0 dB
			00001101	-0.5dB
			…	…
			11011010	-103dB
			11011011	-∞ dB
			…	
			11111111	-∞ dB

- Address 0X14 : Channel 1 Volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1V	Channel 1 Volume	00000000	+6 dB
			00000001	+5.5 dB
			…	…
			00001100	0 dB
			00001101	-0.5dB
			…	…
			11011010	-103dB
			11011011	-∞ dB
			…	
			11111111	-∞ dB

- Address 0X15 : Channel 2 Volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2V	Channel 2 Volume	00000000	+6 dB
			00000001	+5.5 dB
			…	…
			00001100	0 dB
			00001101	-0.5dB
			…	…
			11011010	-103dB
			11011011	-∞ dB
			…	
			11111111	-∞ dB

- Address 0X16 : Channel 3 Volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3V	Channel 3 Volume	00000000	+6 dB
			00000001	+5.5 dB
			…	…
			00001100	0 dB
			00001101	-0.5dB
			…	…
			11011010	-103dB
			11011011	-∞ dB
			…	
			11111111	-∞ dB

- Address 0X17 : Channel 4 Volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4V	Channel 4 Volume	00000000	+6 dB
			00000001	+5.5 dB
			…	…
			00001100	0 dB
			00001101	-0.5dB
			…	…
			11011010	-103dB
			11011011	-∞ dB
			…	
			11111111	-∞ dB

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- Address 0X18 : DRC1 Attack/Release control

AD82589 includes 2 bands DRC . DRC1 is used for L and R channel if two band DRC is disabled. When two band DRC is enabled, DRC1 is used for high frequnecy part of L and R channel, DRC2 is only used for low frequnecy part of L and R. When the input exceeds the programmable attack threshold value, the output power will be limited by this threshold value via gradual gain reduction. In DRC attack and release sequences, output is changed with attack rate and release rate. DRC1 attack rate and release rate are defined 4-bit of address 0X18. DRC2 attack rate and release rate are defined 4-bit of address 0X19.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	LA1	DRC1 Attack rate	0000	3 dB/msec
			0001	2.677 dB/msec
			0010	2.182 dB/msec
			0011	1.846 dB/msec
			0100	1.333 dB/msec
			0101	0.889 dB/msec
			0110	0.4528 dB/msec
			0111	0.2264 dB/msec
			1000	0.15 dB/msec
			1001	0.1121 dB/msec
			1010	0.0902 dB/msec
			1011	0.0752 dB/msec
			1100	0.0645 dB/msec
			1101	0.0563 dB/msec
			1110	0.0501 dB/msec
			1111	0.0451 dB/msec
B[3:0]	LR1	DRC1 Release rate	0000	0.5106 dB/msec
			0001	0.1371 dB/msec
			0010	0.0743 dB/msec
			0011	0.0499 dB/msec
			0100	0.0360 dB/msec
			0101	0.0299 dB/msec
			0110	0.0264 dB/msec
			0111	0.0208 dB/msec
			1000	0.0198 dB/msec
			1001	0.0172 dB/msec
			1010	0.0147 dB/msec
			1011	0.0137 dB/msec
			1100	0.0134 dB/msec
			1101	0.0117 dB/msec
			1110	0.0112 dB/msec
			1111	0.0104 dB/msec

- Address 0X19 : DRC2 Attack/Release control

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	LA2	DRC2 Attack rate	0000	3 dB/msec
			0001	2.677 dB/msec
			0010	2.182 dB/msec
			0011	1.846 dB/msec
			0100	1.333 dB/msec
			0101	0.889 dB/msec
			0110	0.4528 dB/msec
			0111	0.2264 dB/msec
			1000	0.15 dB/msec
			1001	0.1121 dB/msec
			1010	0.0902 dB/msec
			1011	0.0752 dB/msec
			1100	0.0645 dB/msec
			1101	0.0563 dB/msec
			1110	0.0501 dB/msec
			1111	0.0451 dB/msec
B[3:0]	LR2	DRC2 Release rate	0000	0.5106 dB/msec
			0001	0.1371 dB/msec
			0010	0.0743 dB/msec
			0011	0.0499 dB/msec
			0100	0.0360 dB/msec
			0101	0.0299 dB/msec
			0110	0.0264 dB/msec
			0111	0.0208 dB/msec
			1000	0.0198 dB/msec
			1001	0.0172 dB/msec
			1010	0.0147 dB/msec
			1011	0.0137 dB/msec
			1100	0.0134 dB/msec
			1101	0.0117 dB/msec
			1110	0.0112 dB/msec
			1111	0.0104 dB/msec

- Address 0x28,0x29 : Bass/Treble control

The EQ-8 and EQ-9 can be programmed as bass/treble tone boost and cut. When, register with address-0X2B, bit-6, BTE is set to high, the EQ-8 and EQ-9 will perform as bass and treble respectively. The -3dB corner frequency of bass is 360Hz, and treble is 7kHz. The gain range for both filters is +12db ~ -12dB with 1dB per step.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]		Reserved		
B[4:0]	BTC[4:0] / TTC[4:0]	The gain setting of boost and cut	00000	+12dB
			…	…
			00100	+12dB
			00101	+11dB
			00110	+10dB
			…	…
			01110	+2dB
			01111	+1dB
			10000	0dB
			10001	-1dB
			10010	-2dB
			…	…
			11010	-10dB
			11011	-11dB
			11100	-12dB
			…	…
			11111	-12dB

- Address 0X2B ~0X3B : User-defined coefficients registers

An on-chip RAM in AD82589 stores user-defined EQ and mixing coefficients. The content of this coefficient RAM is indirectly accessed via coefficient registers, which consist of one base address register (address 0X2B), five sets of registers (address 0X2C to 0X3A) of three consecutive 8-bit entries for each 24-bit coefficient, and one control register (address 0X3B) to control access of the coefficients in the RAM.

Base Address

Address 0X2B

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CFA[7:0]	Coefficient RAM base address	00000000	

Coefficient of A1

Address 0X2C,A1cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[23:16]	Top 8-bits of coefficients A1		

Address 0X2D, A1cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[15:8]	Middle 8-bits of coefficients A1		

Address 0X2E, A1cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[7:0]	Bottom 8-bits of coefficients A1		

Coefficient of A2

Address 0X2F, A2cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[23:16]	Top 8-bits of coefficients A2		

Address 0X30, A2cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[15:8]	Middle 8-bits of coefficients A2		

Address 0X31, A2cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[7:0]	Bottom 8-bits of coefficients A2		

Coefficient of B1

Address 0X32, B1cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[23:16]	Top 8-bits of coefficients B1		

Address 0X33, B1cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[15:8]	Middle 8-bits of coefficients B1		

Address 0X34, B1cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[7:0]	Bottom 8-bits of coefficients B1		

Coefficient of B2

Address 0X35,B2cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[23:16]	Top 8-bits of coefficients B2		

Address 0X36,B2cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[15:8]	Middle 8-bits of coefficients B2		

Address 0X37,B2cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[7:0]	Bottom 8-bits of coefficients B2		

Coefficient of A0

Address 0X38,A0cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[23:16]	Top 8-bits of coefficients A0		

Address 0X39,A0cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[15:8]	Middle 8-bits of coefficients A0		

Address 0X3A,A0cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[7:0]	Bottom 8-bits of coefficients A0		

Update Coefficient

Address 0X3B,CfRW

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3]	RA	Enable of reading a set of coefficients from RAM	0	Read complete
			1	Read enable
B[2]	R1	Enable of reading a single coefficients from RAM	0	Read complete
			1	Read enable
B[1]	WA	Enable of writing a set of coefficients to RAM	0	Write complete
			1	Write enable
B[0]	W1	Enable of writing a single coefficient to RAM	0	Write complete
			1	Write enable

- Address 0X47 : DRC/BEQ check setting

AD82589 provide DRC/BEQ checksum protection.The following is the setting of DRC/BEQ checksum protection.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CHK_DRC_P	PLOTN link DRC_CHK	0	No link
			1	PROTN linked
B[6]	CHK_DRC_AM	Auto mute DRC_CHK	0	Disable
			1	Enable
B[5]	CHK_DRC_R	Result DRC_CHK	0	No error
			1	Error occurred
B[4]	CHK_DRC_EN	Enable DRC_CHK	0	Disable
			1	Enable
B[3]	CHK_BEQ_P	PLOTN link BEQ_CHK	0	No link
			1	PROTN linked
B[2]	CHK_BEQ_AM	Auto mute BEQ_CHK	0	Disable
			1	Enable
B[1]	CHK_BEQ_R	Result BEQ_CHK	0	No error
			1	Error occurred
B[0]	CHK_BEQ_EN	Enable BEQ_CHK	0	Disable
			1	Enable

- Address 0X48 : Top 8 bits of DRC_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_V[23:16]	Top 8-bits of DRC_CHK set value	00000000	Initial value
			X	User programmed

- Address 0X49 : Middle 8 bits of DRC_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_V[15:8]	Middle 8-bits of DRC_CHK set value	00000000	Initial value
			X	User programmed

- Address 0X4A : Bottom 8 bits of DRC_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_V[7:0]	Bottom 8-bits of DRC_CHK set value	00000000	Initial value
			X	User programmed

- Address 0X4B : Top 8 bits of BEQ_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_V[23:16]	Top 8-bits of BEQ_CHK set value	00000000	Initial value
			X	User programmed

- Address 0X4C : Middle 8 bits of BEQ _CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_V[15:8]	Middle 8-bits of BEQ_CHK set value	00000000	Initial value
			X	User programmed

- Address 0X4D : Bottom 8 bits of BEQ_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_V[7:0]	Bottom 8-bits of BEQ_CHK set value	00000000	Initial value
			X	User programmed

- Address 0X4E : Top 8 bits of DRC_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_R[23:16]	Top 8-bits of DRC_CHK result	X	Result

- Address 0X4F : Middle 8 bits of DRC_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_R[15:8]	Middle 8-bits of DRC_CHK result	X	Result

- Address 0X50 : Bottom 8 bits of DRC_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_R[7:0]	Bottom 8-bits of DRC_CHK result	X	Result

- Address 0X51 : Top 8 bits of BEQ_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_R[23:16]	Top 8-bits of BEQ_CHK result	X	Result

- Address 0X52 : Middle 8 bits of BEQ _CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_R[15:8]	Middle 8-bits of BEQ_CHK result	X	Result

- Address 0X53 : Bottom 8 bits of BEQ_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_R[7:0]	Bottom 8-bits of BEQ_CHK result	X	Result

- Address 0X56 : Level meter clear

AD82589 has level meter function. AD82589 has 4 registers using 24bits data for C1, C2, C3, and C4 level meters. The registers are written to hold max level data before DRC function. When set CXDRCM=1, channel X level meter will hold max square value of all the sample points. On the other hand, when set CXDRCM=0, channel X level meter will hold max peak value of all the sample points. Level meter registers are cleared when user set level meter clear register high via I2C control.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	C1_CLR	Clear C1 level meter	0	Hold max value
			1	Clear
B[6]	C2_CLR	Clear C2 level meter	0	Hold max value
			1	Clear
B[5]	C3_CLR	Clear C3 level meter	0	Hold max value
			1	Clear
B[4]	C4_CLR	Clear C4 level meter	0	Hold max value
			1	Clear

- Address 0X57 : Top 8 bits of channel 1 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1_LEVEL[23:16]	Top 8-bits of CH1 MAX value	X	Result

- Address 0X58 : Middle 8 bits of channel 1 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1_LEVEL[15:8]	Middle 8-bits of CH1 MAX value	X	Result

- Address 0X59 : Bottom 8 bits of channel 1 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1_LEVEL[7:0]	Bottom 8-bits of CH1 MAX value	X	Result

- Address 0X5A : Top 8 bits of channel 2 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2_LEVEL[23:16]	Top 8-bits of CH2 MAX value	X	Result

- Address 0X5B : Middle 8 bits of channel 2 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2_LEVEL[15:8]	Middle 8-bits of CH2 MAX value	X	Result

- Address 0X5C : Bottom 8 bits of channel 2 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2_LEVEL[7:0]	Bottom 8-bits of CH2 MAX value	X	Result

- Address 0X5D : Top 8 bits of channel 3 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3_LEVEL[23:16]	Top 8-bits of CH3 MAX value	X	Result

- Address 0X5E : Middle 8 bits of channel 3 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3_LEVEL[15:8]	Middle 8-bits of CH3 MAX value	X	Result

- Address 0X5F : Bottom 8 bits of channel 3 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3_LEVEL[7:0]	Bottom 8-bits of CH3 MAX value	X	Result

- Address 0X60 : Top 8 bits of channel 4 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4_LEVEL[23:16]	Top 8-bits of CH4 MAX value	X	Result

- Address 0X61 : Middle 8 bits of channel 4 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4_LEVEL[15:8]	Middle 8-bits of CH4 MAX value	X	Result

- Address 0X62 : Bottom 8 bits of channel 4 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4_LEVEL[7:0]	Bottom 8-bits of CH4 MAX value	X	Result

RAM access

The procedure to read/write coefficient(s) from/to RAM is as followings:

Read a single coefficient from RAM:

1. Write 8-bis of address to I2C address-0X2B
2. Write 1 to R1 bit in address-0X3B
3. Read top 8-bits of coefficient in I2C address-0X2C
4. Read middle 8-bits of coefficient in I2C address-0X2D
5. Read bottom 8-bits of coefficient in I2C address-0X2E

Read a set of coefficients from RAM:

1. Write 8-bits of address to I2C address-0X2B
2. Write 1 to RA bit in address-0X3B
3. Read top 8-bits of coefficient A1 in I2C address-0X2C
4. Read middle 8-bits of coefficient A1in I2C address-0X2D
5. Read bottom 8-bits of coefficient A1 in I2C address-0X2E
6. Read top 8-bits of coefficient A2 in I2C address-0X2F
7. Read middle 8-bits of coefficient A2 in I2C address-0X30
8. Read bottom 8-bits of coefficient A2 in I2C address-0X31
9. Read top 8-bits of coefficient B1 in I2C address-0X32
10. Read middle 8-bits of coefficient B1 in I2C address-0X33
11. Read bottom 8-bits of coefficient B1 in I2C address-0X34
12. Read top 8-bits of coefficient B2 in I2C address-0X35
13. Read middle 8-bits of coefficient B2 in I2C address-0X36
14. Read bottom 8-bits of coefficient B2 in I2C address-0X37
15. Read top 8-bits of coefficient A0 in I2C address-0X38
16. Read middle 8-bits of coefficient A0 in I2C address-0X39
17. Read bottom 8-bits of coefficient A0 in I2C address-0X3A

Write a single coefficient from RAM:

1. Write 8-bis of address to I2C address-0X2B
2. Write top 8-bits of coefficient in I2C address-0X2C
3. Write middle 8-bits of coefficient in I2C address-0X2D
4. Write bottom 8-bits of coefficient in I2C address-0X2E
5. Write 1 to W1 bit in address-0X3B

Write a set of coefficients from RAM:

1. Write 7-bits of address to I2C address-0X2B
2. Write top 8-bits of coefficient A1 in I2C address-0X2C
3. Write middle 8-bits of coefficient A1 in I2C address-0X2D
4. Write bottom 8-bits of coefficient A1 in I2C address-0X2E
5. Write top 8-bits of coefficient A2 in I2C address-0X2F
6. Write middle 8-bits of coefficient A2 in I2C address-0X30
7. Write bottom 8-bits of coefficient A2 in I2C address-0X31
8. Write top 8-bits of coefficient B1 in I2C address-0X32
9. Write middle 8-bits of coefficient B1 in I2C address-0X33
10. Write bottom 8-bits of coefficient B1 in I2C address-0X34
11. Write top 8-bits of coefficient B2 in I2C address-0X35
12. Write middle 8-bits of coefficient B2 in I2C address-0X36
13. Write bottom 8-bits of coefficient B2 in I2C address-0X37
14. Write top 8-bits of coefficient A0 in I2C address-0X38
15. Write middle 8-bits of coefficient A0 in I2C address-0X39
16. Write bottom 8-bits of coefficient A0 in I2C address-0X3A
17. Write 1 to WA bit in address-0X3B

Note that: the read and write operation on RAM coefficients works any state exclude SLEEPN=low.

User-defined equalizer

The AD82589 provides 24 parametric Equalizer (EQ). Users can program suitable coefficients via I^2C control interface to program the required audio band frequency response for every EQ. The transfer function

$$H(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 + B_1 z^{-1} + B_2 z^{-2}}$$

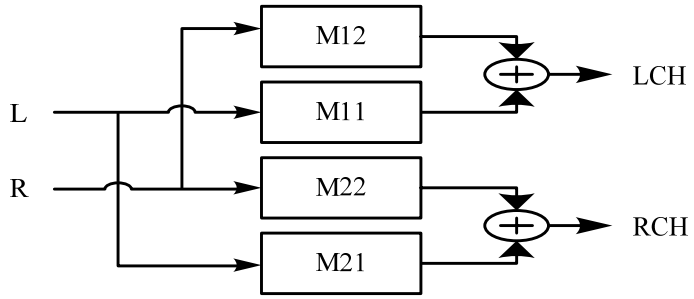
The data format of 2's complement binary code for EQ coefficient is 3.21. i.e., 3-bits for integer (MSB is the sign bit) and 21-bits for mantissa. Each coefficient range is from 0x800000 (-4) to 0x7FFFFF (+3.999999523). These coefficients are stored in User Defined RAM and are referenced in following manner:

$$CHxEQyA0 = A0$$
$$CHxEQyA1 = A1$$
$$CHxEQyA2 = A2$$
$$CHxEQyB1 = -B1$$
$$CHxEQyB2 = -B2$$

Where *x* and *y* represents the number of channel and the band number of EQ equalizer.
All user-defined filters are path-through, where all coefficients are defaulted to 0 after being powered up, except the A0 that is set to 0x200000 which represents 1.

Mixer

The AD82589 provides mixers to generate the extra audio source from the input left and right channels. The coefficients of mixers are defined in range from 0x800000 (-1) to 0x7FFFFF (0.9999998808). The function block diagram is as following:



Pre-scale

For each audio channel, AD82589 can scale input signal level prior to EQ processing which is realized by a 24-bit signed fractional multiplier. The pre-scale factor, ranging from -1 (0x800000) to 0.9999998808 (0x7FFFFF), for this multiplier, can be loaded into RAM. The default values of the pre-scaling factors are set to 0x7FFFFF. Programming of RAM is described in RAM access.

Post-scale

The AD82589 provides an additional multiplication after equalizing and before interpolation stage, which is realized by a 24-bit signed fractional multiplier. The post-scaling factor, ranging from -1 (0x800000) to 0.9999998808 (0x7FFFFF), for this multiplier, can be loaded into RAM. The default values of the post-scaling factors are set to 0x7FFFFF. All channels can use the channel-1 post-scale factor by setting the post-scale link. Programming of RAM is described in RAM access.

Power Clipping

The AD82589 provides power clipping function to avoid excessive signal that may destroy loud speaker. Two sets of power clipping are provided. One is used for both channel 1 and channel 2, while the other is used for channel 3. The power clipping level is defined by 24-bit representation and is stored in RAM address 0X80. The following table shows the power clipping level's numerical representation.

Max amplitude	dB	Linear	Decimal	Hex (1.23 format)
1.8*Gain	0	1	8388607	7FFFFF
1.8*0.707*Gain	-3	0.707	5930745	5A7EF9
1.8*0.5*Gain	-6	0.5	4194303	3FFFFF
1.8*L*Gain	x	$L=10^{(x/20)}$	D=8388607xL	H=dec2hex(D)

Note: Gain is the closed loop gain of AD82589, the value is 14.16(±5%) with 8ohm load. If the max amplitude is larger than PVDD, max amplitude change to PVDD.

Attack threshold for Dynamic Range control

The AD82589 provides dynamic range control (DRC) function. When the input RMS exceeds the programmable attack threshold value, the output power will be limited by this threshold power level via gradual gain reduction. Two sets of dynamic range control are provided. One is used of DRC1, while the other is used for. Attack threshold is defined by 24-bit representation and is stored in RAM address 0X81 and 0X83.

Release threshold for Dynamic Range control

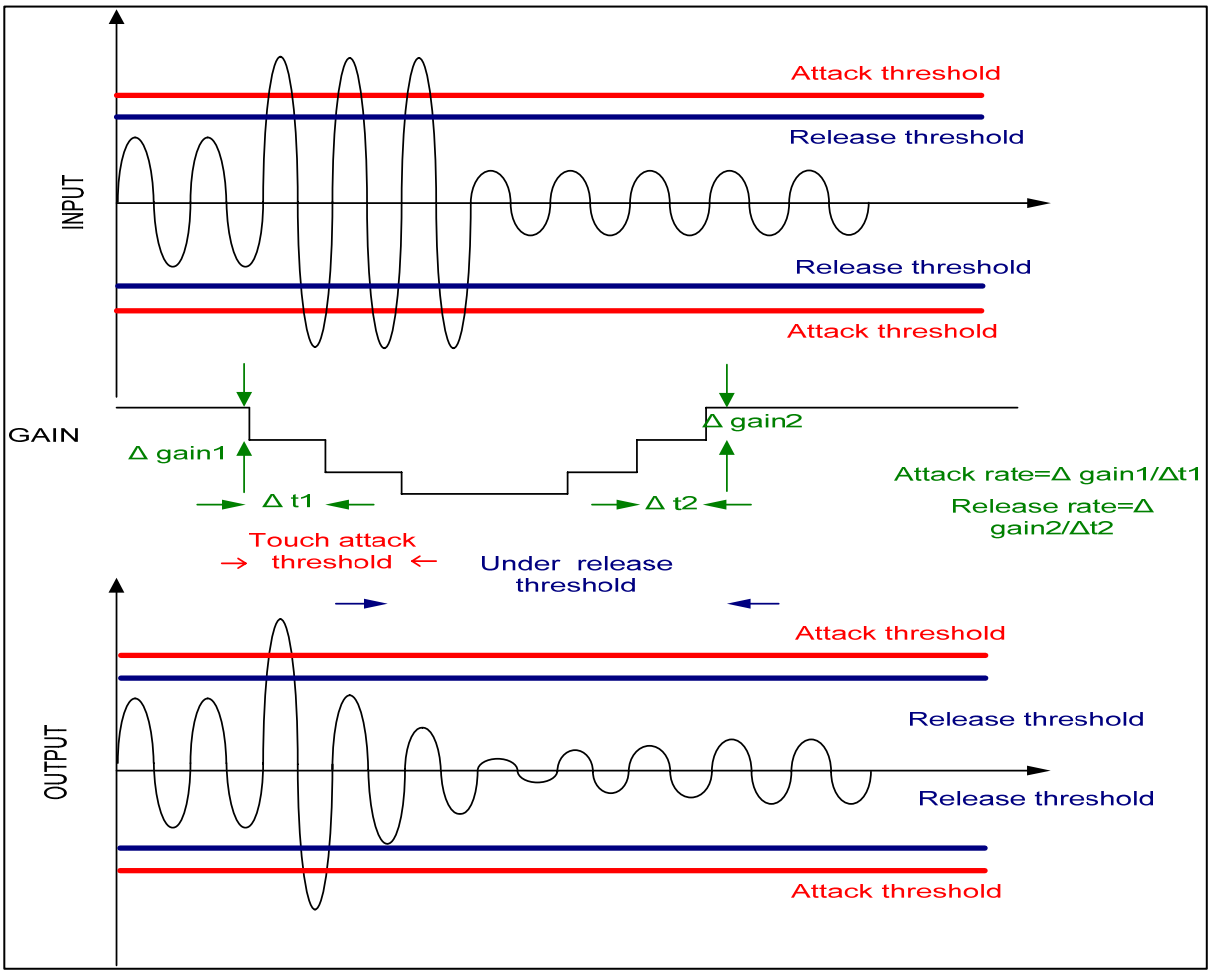
After AD82589 has reached the attack threshold, its output power will be limited to that level. The output power level will be gradually adjusted to the programmable release threshold level. Two sets of dynamic range control are provided. One is used of DRC1, while the other is used for DRC2. Release threshold is defined by 24-bit representation and is stored in RAM address 0X82 and 0X84. The following table shows the attack and release threshold's numerical representation with RMS mode.

Table 7 Sample calculation for attack and release threshold

Power	dB	Linear	Decimal	Hex (3.21 format)
(1.8*Gain)^2/R	0	1	2097152	200000
(1.8*Gain)^2/2R	-3	0.5	1048576	100000
(1.8*Gain)^2/4R	-6	0.25	524288	80000
((1.8*Gain)^2/R)*L	x	$L=10^{(x/10)}$	D=2097152xL	H=dec2hex(D)

Note: Gain is the closed loop gain of AD82589, the value is 14.16(±5%) with 8ohm load.

To best illustrate the dynamic range control, please refer to the following figure.



Noise Gate Attack level

When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or zero if the noise gate function is enabled. Noise gate attack level is defined by 24-bit representation and is stored in RAM address 0X85.

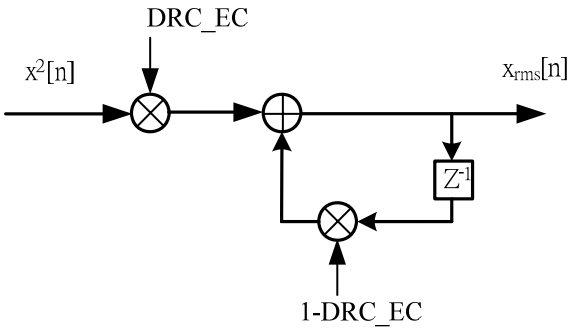
Noise Gate Release level

After entering the noise gating status, the noise gain will be removed whenever AD82589 receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 24-bit representation and is stored in RAM address 0X86. The following table shows the noise gate attack and release threshold level's numerical representation.

Table 8 Sample calculation for noise gate attack and release level

Input amplitude (dB)	Linear	Decimal	Hex (1.23 format)
0	1	8388607	7FFFFF
-100	10^{-5}	83	53
-110	$10^{-5.5}$	26	1A
x	$L=10^{(x/20)}$	D=8388607xL	H=dec2hex(D)

DRC energy coefficient



The above figure illustrates the digital processing of calculating RMS signal power. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Two sets of energy coefficients are provided. One is used of DRC1, while the other is used for DRC2. Energy coefficient is defined by 24-bit representation and is stored in RAM address 0X87 and 0X88. The following table shows the DRC energy coefficient numerical representation.

Table 9 Sample calculation for DRC energy coefficient

DRC energy coefficient	dB	Linear	Decimal	Hex (1.23 format)
1	0	1	8388607	7FFFFF
1/256	-48.2	1/256	32768	8000
1/1024	-60.2	1/1024	8192	2000
L	x	$L=10^{(x/20)}$	D=8388607xL	H=dec2hex(D)

BEQ and DRC Coeficient Protection

The AD82589 implements an automatic Check Sum (or CRC) calculation for the BEQ and DRC coefficient Register. The User define RAM contents from 0x00 to 0x77 will be calculated by adder (or CRC) to obtain the CHS_BEQ_R, and RAM from 0x81 to 0x84 will be calculated by adder (or CRC) to obtain the CHS_DRC_R. Both result (24bit) are exported on I^2C registers from 0x4E to 0x53. The calculation will start as soon as the CHK_BEQ_EN or the CHK_DRC_EN bit is set to 1.When CHK_BEQ_EN or CHK_DRC_EN is set to '1', the relative result is continuously compared. If the result matches its own reference value (set the CHS_BEQ_V or the CHS_DRC_V), the respective matching bits (CHK_BEQ_R and CHK_DRC_R) will be set to '0'. The compare bits have no effect if the respective GO bit is not set.

In case of errors (i.e. the internally calculated didn't match the reference), an automatic device mute action can be activated. This function is enabled when the CHK_BEQ_AM or CHK_DRC_AM bit is set to '1'. The automatic mute bits have no effect if the respective enable bits are not set.

The recommended procedure for automatic reset activation is the following:

- Download the set of coefficients (RAM locations 0x00...0x77)
- Download the externally callculated biquad checksum into registers *CHS_BEQ_V*
- Enable the checksum of the biquad coefficients by setting the *CHK_BEQ_EN* bit. The checksum will start to be automatically calculated and its value exposed on registers *CHS_BEQ_R.*
- It will start to be compared with the reference one and the result will be exposed on the *CHK_BEQ_R*. The following operation will be executed on each audio frame:

```
if ((CHS_BEQ_R == CHS_BEQ_V)) {
        CHK_BEQ_R = 0;// Check is ok, reset the error bit }
else {
        CHK_BEQ_R = 1;// Check failure detected, set the error bit and pull down /PROTN (if P_CHK_BEQ
= "1")
 }
```

- If the check failure detects , the CHK_BEQ_R will go to "1". If the CHK_BEQ_P is set to "1", the /PROTN goes to pull down.
- Enable automatic mute of the device in case of check failure by setting the *CHK_BEQ_AM* bit. The *CHK_BEQ_R* bit will then be automatically checked by the AD82589, on each audio frame, and a mute event will be triggered in case of check failure.
- After check failure occurred, If correct coefficient is sent, CHK_BEQ_R goes to "0" and un-mute.

The previous example is intended for biquad coefficient register calculation, but it can be easily extended to DRC register.

The user defined RAM

The contents of user defined RAM is represented in following table.

Address	NAME	Coefficient	Default
0x00	Channel-1 EQ0	CH1EQ0A1	0x000000
0x01		CH1EQ0A2	0x000000
0x02		CH1EQ0B1	0x000000
0x03		CH1EQ0B2	0x000000
0x04		CH1EQ0A0	0x200000
0x05	Channel-1 EQ1	CH1EQ1A1	0x000000
0x06		CH1EQ1A2	0x000000
0x07		CH1EQ1B1	0x000000
0x08		CH1EQ1B2	0x000000
0x09		CH1EQ1A0	0x200000
0x0A	Channel-1 EQ2	CH1EQ2A1	0x000000
0x0B		CH1EQ2A2	0x000000
0x0C		CH1EQ2B1	0x000000
0x0D		CH1EQ2B2	0x000000
0x0E		CH1EQ2A0	0x200000
0x0F	Channel-1 EQ3	CH1EQ3A1	0x000000
0x10		CH1EQ3A2	0x000000
0x11		CH1EQ3B1	0x000000
0x12		CH1EQ3B2	0x000000
0x13		CH1EQ3A0	0x200000
0x14	Channel-1 EQ4	CH1EQ4A1	0x000000
0x15		CH1EQ4A2	0x000000
0x16		CH1EQ4B1	0x000000
0x17		CH1EQ4B2	0x000000
0x18		CH1EQ4A0	0x200000
0x19	Channel-1 EQ5	CH1EQ5A1	0x000000
0x1A		CH1EQ5A2	0x000000
0x1B		CH1EQ5B1	0x000000
0x1C		CH1EQ5B2	0x000000
0x1D		CH1EQ5A0	0x200000
0x1E	Channel-1 EQ6	CH1EQ6A1	0x000000
0x1F		CH1EQ6A2	0x000000

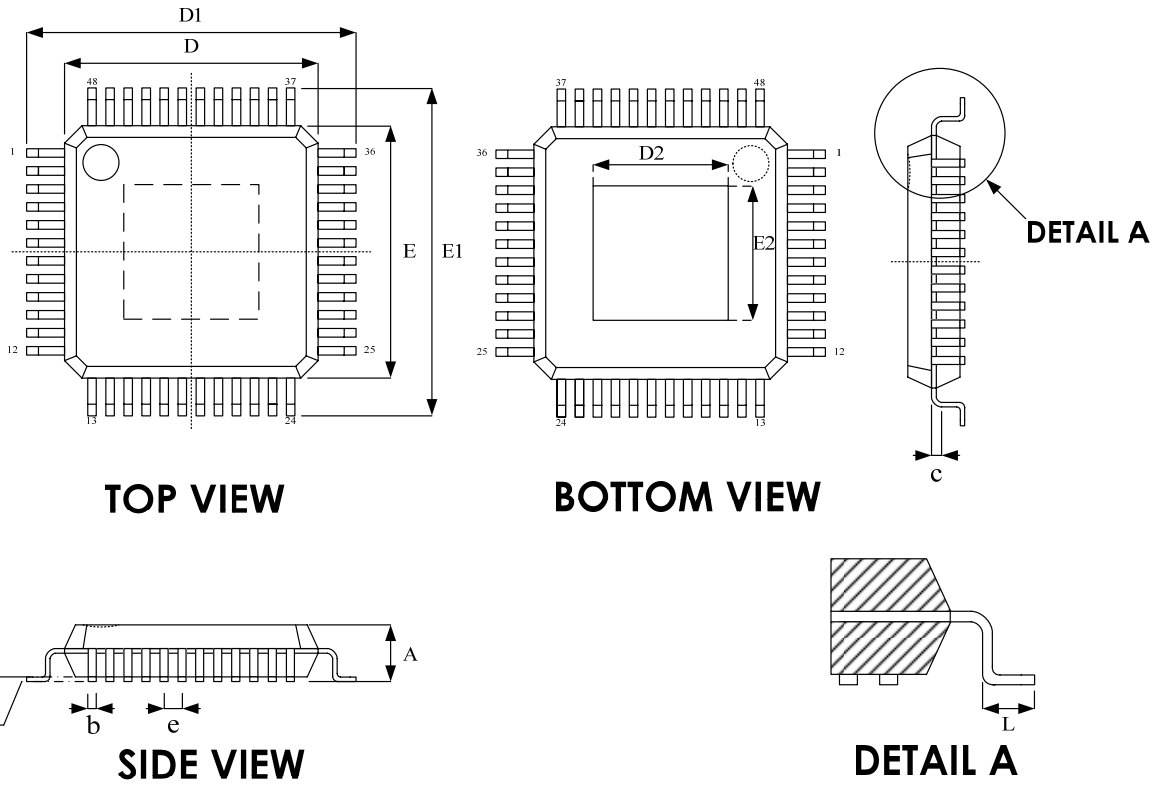
0x20		CH1EQ6B1	0x000000
0x21		CH1EQ6B2	0x000000
0x22		CH1EQ6A0	0x200000
0x23	Channel-1 EQ7	CH1EQ7A1	0x000000
0x24		CH1EQ7A2	0x000000
0x25		CH1EQ7B1	0x000000
0x26		CH1EQ7B2	0x000000
0x27		CH1EQ7A0	0x200000
0x28	Channel-1 EQ8	CH1EQ8A1	0x000000
0x29		CH1EQ8A2	0x000000
0x2A		CH1EQ8B1	0x000000
0x2B		CH1EQ8B2	0x000000
0x2C		CH1EQ8A0	0x200000
0x2D	Channel-1 EQ9	CH1EQ9A1	0x000000
0x2E		CH1EQ9A2	0x000000
0x2F		CH1EQ9B1	0x000000
0x30		CH1EQ9B2	0x000000
0x31		CH1EQ9A0	0x200000
0x32	Channel-1 EQ10 Channel-1 HPF0	CH1EQ10A1	0x000000
0x33		CH1EQ10A2	0x000000
0x34		CH1EQ10B1	0x000000
0x35		CH1EQ10B2	0x000000
0x36		CH1EQ10A0	0x200000
0x37	Channel-1 EQ11 Channel-1 HPF1	CH1EQ11A1	0x000000
0x38		CH1EQ11A2	0x000000
0x39		CH1EQ11B1	0x000000
0x3A		CH1EQ11B2	0x000000
0x3B		CH1EQ11A0	0x200000
0x3C	Channel-2 EQ0	CH2EQ0A1	0x000000
0x3D		CH2EQ0A2	0x000000
0x3E		CH2EQ0B1	0x000000
0x3F		CH2EQ0B2	0x000000
0x40		CH2EQ0A0	0x200000
0x41	Channel-2 EQ1	CH2EQ1A1	0x000000
0x42		CH2EQ1A2	0x000000
0x43		CH2EQ1B1	0x000000

0x44		CH2EQ1B2	0x000000
0x45		CH2EQ1A0	0x200000
0x46	Channel-2 EQ2	CH2EQ2A1	0x000000
0x47		CH2EQ2A2	0x000000
0x48		CH2EQ2B1	0x000000
0x49		CH2EQ2B2	0x000000
0x4A		CH2EQ2A0	0x200000
0x4B	Channel-2 EQ3	CH2EQ3A1	0x000000
0x4C		CH2EQ3A2	0x000000
0x4D		CH2EQ3B1	0x000000
0x4E		CH2EQ3B2	0x000000
0x4F		CH2EQ3A0	0x200000
0x50	Channel-2 EQ4	CH2EQ4A1	0x000000
0x51		CH2EQ4A2	0x000000
0x52		CH2EQ4B1	0x000000
0x53		CH2EQ4B2	0x000000
0x54		CH2EQ4A0	0x200000
0x55	Channel-2 EQ5	CH2EQ5A1	0x000000
0x56		CH2EQ5A2	0x000000
0x57		CH2EQ5B1	0x000000
0x58		CH2EQ5B2	0x000000
0x59		CH2EQ5A0	0x200000
0x5A	Channel-2 EQ6	CH2EQ6A1	0x000000
0x5B		CH2EQ6A2	0x000000
0x5C		CH2EQ6B1	0x000000
0x5D		CH2EQ6B2	0x000000
0x5E		CH2EQ6A0	0x200000
0x5F	Channel-2 EQ7	CH2EQ7A1	0x000000
0x60		CH2EQ7A2	0x000000
0x61		CH2EQ7B1	0x000000
0x62		CH2EQ7B2	0x000000
0x63		CH2EQ7A0	0x200000
0x64	Channel-2 EQ8	CH2EQ8A1	0x000000
0x65		CH2EQ8A2	0x000000
0x66		CH2EQ8B1	0x000000
0x67		CH2EQ8B2	0x000000

0x68		CH2EQ8A0	0x200000
0x69	Channel-2 EQ9	CH2EQ9A1	0x000000
0x6A		CH2EQ9A2	0x000000
0x6B		CH2EQ9B1	0x000000
0x6C		CH2EQ9B2	0x000000
0x6D		CH2EQ9A0	0x200000
0x6E	Channel-2 EQ10 Channel-2 HPF0	CH2EQ10A1	0x000000
0x6F		CH2EQ10A2	0x000000
0x70		CH2EQ10B1	0x000000
0x71		CH2EQ10B2	0x000000
0x72		CH2EQ10A0	0x200000
0x73	Channel-2 EQ11 Channel-2 HPF1	CH2EQ11A1	0x000000
0x74		CH2EQ11A2	0x000000
0x75		CH2EQ11B1	0x000000
0x76		CH2EQ11B2	0x000000
0x77		CH2EQ11A0	0x200000
0x78	Channel-1 Mixer1	M11	0x7FFFFF
0x79	Channel-1 Mixer2	M12	0x000000
0x7A	Channel-2 Mixer1	M21	0x000000
0x7B	Channel-2 Mixer2	M22	0x7FFFFF
0x7C	Channel-1 Prescale	C1PRS	0x7FFFFF
0x7D	Channel-2 Prescale	C2PRS	0x7FFFFF
0x7E	Channel-1 Postscale	C1POS	0x7FFFFF
0x7F	Channel-2 Postscale	C2POS	0x7FFFFF
0x80	CH1.2 Power Clipping	PC1	0x7FFFFF
0x81	DRC1 Attack threshold	DRC1_ATH	0x200000
0x82	DRC1 Release threshold	DRC1_RTH	0x80000
0x83	DRC2 Attack threshold	DRC2_ATH	0x200000
0x84	DRC2 Release threshold	DRC2_RTH	0x80000
0x85	Noise Gate Attack Level	NGAL	0x00001A
0x86	Noise Gate Release Level	NGRL	0x000053
0x87	DRC1 Energy Coefficient	DRC1_EC	0x8000
0x88	DRC2 Energy Coefficient	DRC2_EC	0x2000

Package Dimensions

- **E-LQFP 48L (7x7mm)**



Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.17	0.27
c	0.09	0.20
D	6.90	7.10
D1	8.90	9.10
E	6.90	7.10
E1	8.90	9.10
e	0.50 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	4.31	5.21
E2	4.31	5.21

Revision History

Revision	Date	Description
0.1	2015.08.31	Original
0.2	2016.01.18	Modify power clipping table.
0.3	2016.03.25	Add packing type : AD82589-LG48NRR
0.4	2016.04.22	Modify digital amplifier startup sequence. Modify CxDRCM register name.
0.5	2016.06.30	Add packing code in ordering information table.
1.0	2016.08.22	Modify packing code in ordering information table. Remove the word of preliminary.

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