2x25W Stereo / 1x 50W Mono Digital Audio Amplifier With 20 bands EQ Functions, DRC and 2.1CH Mode

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
  Loudspeaker: 98dB (PSNR), 108dB (DR) @24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
  3.3V for digital circuit
  8V~26V for loudspeaker driver
- Supports 2.0CH/2.1CH/Mono configuration
- Loudspeaker output power@24V for stereo
  10W x 2CH into 8Ω @0.09% THD+N
  15W x 2CH into 8Ω @0.15% THD+N
  25W x 2CH into 8Ω @0.28% THD+N
- Sound processing including：
  20 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Dual Band Dynamic range control
  Power Clipping
  3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  Bass/Treble tone control
  Bass management crossover filter
  DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- Supports I^2C control without MCLK
- I^2C control interface with selectable device address
- Support BCLK system
- Support hardware and software reset
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode

Applications

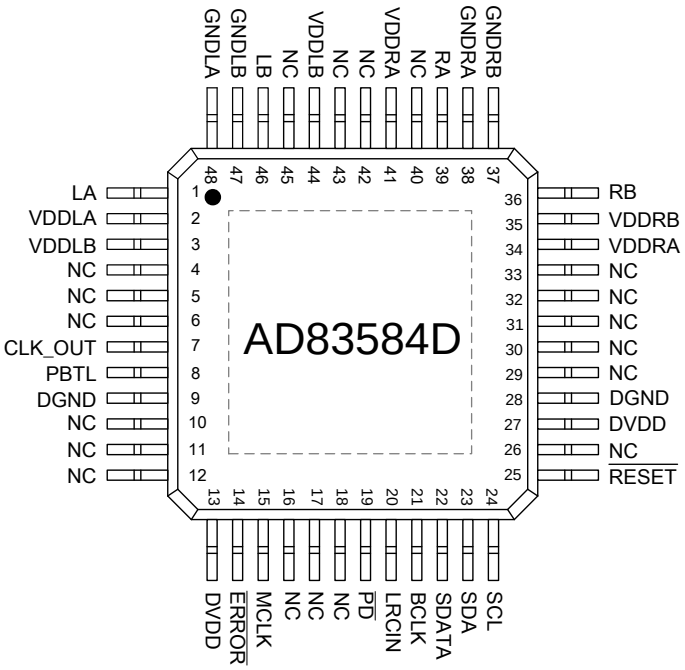
- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

AD83584D is a digital audio amplifier capable of driving 25W (BTL) each to a pair of 8Ω load speaker and 50W (PBTL) to a 4Ω load speaker operating at 24V supply without external heat-sink or fan requirement with play music. AD83584D is also capable of driving 4Ω, 12W (SE)x2 + 8Ω, 25W (BTL)x1 at 24V supply for 2.1CH application.

AD83584D can provide advanced audio processing functions, such as volume control, 20 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD83584D from damage due to accidental erroneous operating condition. The full digital circuit design of AD83584D is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog class-AB or class-D audio amplifier counterpart implemented by analog circuit design. AD83584D is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment



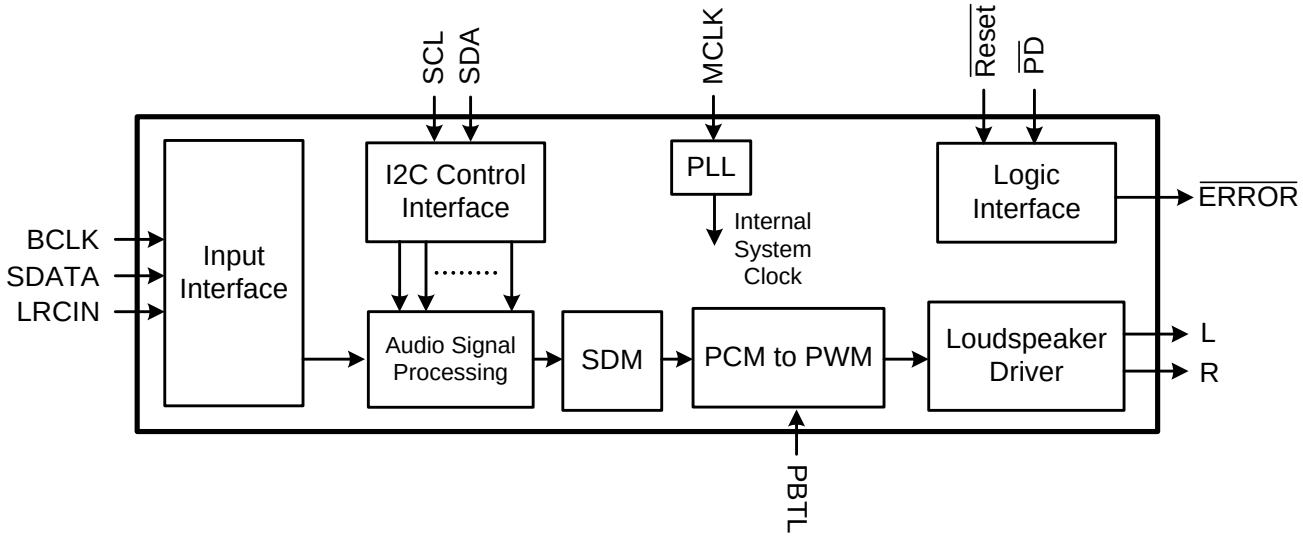
Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	LA	O	Left channel output A	
2	VDDLA	P	Left channel supply A	
3	VDDLB	P	Left channel supply B	
4	NC		Not connected	
5	NC		Not connected	
6	NC		Not connected	
7	CLK_OUT	I/O	PLL ratio setting pin during power up, this pin is monitored on the rising edge of reset. PMF register will be default set at 1 or 4 times PLL ratio. Low: PMF [3:0]=[0100], 4 time of PLL ratio to avoid system MCLK over flow. High: PMF [3:0]=[0000], 1 times of PLL ratio. This pin could be clock output pin also during normal operating if EN_CLK_OUT register bit is enabled.	TTL output buffer, internal pull Low with a 80Kohm resistor.
8	PBTL	I	Stereo/Mono configuration pin (Low: Stereo ; High: Mono)	
9	DGND	P	Digital Ground	

10	NC		Not connected	
11	NC		Not connected	
12	NC		Not connected	
13	DVDD	P	Digital Power	
14	$\overline{\text{ERROR}}$	O	$\overline{\text{ERROR}}$ pin is a dual function pin. One is I^2C address setting during power up. The other one is error status report (low active), It sets by register of A_SEL_FAULT at address 0x13 B[6] to enable it.	This pin is monitored on the rising edge of reset. A value of Low (15-kΩ pull down) sets the I^2C device address to 0x30 and a value of High (15-kΩ pull up) sets it to 0x31.
15	MCLK	I	Master clock input	Schmitt trigger TTL input buffer, internal pull Low with a 80Kohm resistor.
16	NC		Not connected	
17	NC		Not connected	
18	NC		Not connected	
19	$\overline{\text{PD}}$	I	Power down, low active	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
20	LRCIN	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer, internal pull Low with a 80Kohm resistor.
21	BCLK	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer, internal pull Low with a 80Kohm resistor.
22	SDATA	I	Serial audio data input	Schmitt trigger TTL input buffer
23	SDA	I/O	I^2C bi-directional serial data	Schmitt trigger TTL input buffer
24	SCL	I	I^2C serial clock input	Schmitt trigger TTL input buffer
25	$\overline{\text{RESET}}$	I	Reset, low active	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
26	NC		Not connected	
27	DVDD	P	Digital Power	
28	DGND	P	Digital Ground	
29	NC		Not connected	
30	NC		Not connected	
31	NC		Not connected	

32	NC		Not connected	
33	NC		Not connected	
34	VDDRA	P	Right channel supply A	
35	VDDRB	P	Right channel supply B	
36	RB	O	Right channel output B	
37	GNDRB	P	Right channel ground B	
38	GNDRA	P	Right channel ground A	
39	RA	O	Right channel output A	
40	NC		Not connected	
41	VDDRA	P	Right channel supply A	
42	NC		Not connected	
43	NC		Not connected	
44	VDDLB	P	Left channel supply B	
45	NC		Not connected	
46	LB	O	Left channel output B	
47	GNDLB	P	Left channel ground B	
48	GNDLA	P	Left channel ground A	

Functional Block Diagram



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD83584D-LG48NAY	E-LQFP-48L 7x7 mm	250 Units / Tray 2.5K Units / Box (10 Tray)	Green
AD83584D-LG48NAR	E-LQFP-48L 7x7 mm	2K Units / Reel	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jt}(℃/W)	Exposed Thermal Pad
7x7 48L E-LQFP	AD83584D	27.4	1.33	34.9	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja}, the junction-to-ambient thermal resistance is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The simulation is tested using the JESD51-5 thermal measurement standard.

Note 1.3: Ψ_{jt} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{ja}, using a procedure described in JESD51-2.

Note 1.4: θ_{jt} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

Marking Information

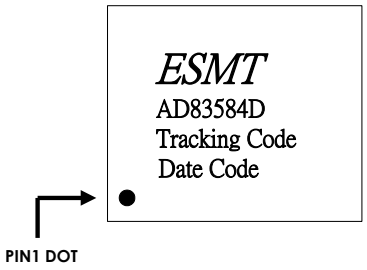
AD83584D

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code

Line 4 : Date Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	^oC
T_J	Junction Operating Temperature	0	150	^oC
R_L	Minimum Load Resistance for BTL, VDDL/R >13V	4.8	-	Ω
	Minimum Load Resistance for BTL, VDDL/R ≦13V	3.2	-	
L_O	Minimum Load Resistance for PBTL	3.2	-	uH
	Minimum Output Filter Inductor under Short-Circuit Condition	6		

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	8~26	V
T_J	Junction Operating Temperature	0~125	^oC
T_A	Ambient Operating Temperature	0~70	^oC

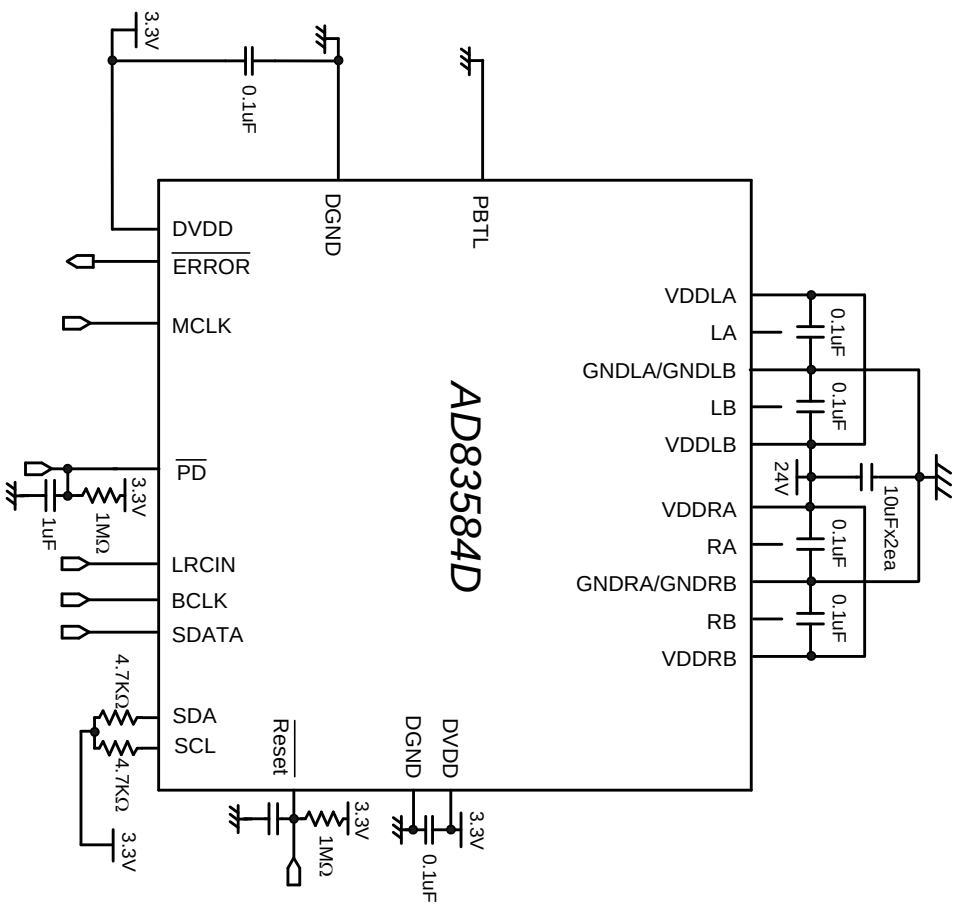
General Electrical Characteristics

Condition: T_A=25 °C (unless otherwise specified).

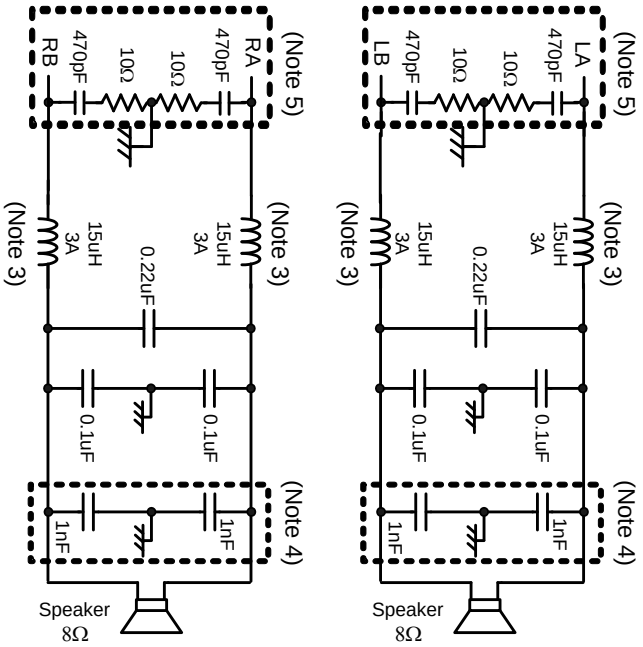
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}(HV)	PVDD Supply Current during Power Down	PVDD=24V		10	200	uA
I_{PD}(LV)	DVDD Supply Current during Power Down	DVDD=3.3V, PBTL=Low		13	20	uA
I_Q(HV)	Quiescent current for PVDD (50%/50% PWM duty)	PVDD=24V		37		mA
I_Q(LV)	Quiescent current for DVDD (Un-mute)	DVDD=3.3V, PBTL=Low		70		mA
T_{SENSOR}	Junction Temperature for Driver Shutdown			158		°C
	Temperature Hysteresis for Recovery from Shutdown			33		°C
UV_H	Under Voltage Disabled (For DVDD)			2.8		V
UV_L	Under Voltage Enabled (For DVDD)			2.7		V
Rds-on	Static Drain-to-Source On-state Resistor, PMOS	PVDD=24V, Id=500mA		260		mΩ
	Static Drain-to-Source On-state Resistor, NMOS			230		mΩ
I_{SC}	L(R) Channel Over-Current Protection (Note 2)	PVDD=24V		7		A
		PVDD=12V		3.5		
	Mono Channel Over-Circuit Protection (Note 2)	PVDD=24V		14		A
		PVDD=12V		7		
V_{IH}	High-Level Input Voltage	DVDD=3.3V	2.0			V
V_{IL}	Low-Level Input Voltage	DVDD=3.3V			0.8	V
V_{OH}	High-Level Output Voltage	DVDD=3.3V	2.4			V
V_{OL}	Low-Level Output Voltage	DVDD=3.3V			0.4	V
C_I	Input Capacitance			6.4		pF

Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Application Circuit Example for Stereo



Pin / Logic	0	1
PD	Power Down	Normal
Reset	Reset	Normal
PBTL	Stereo	Mono

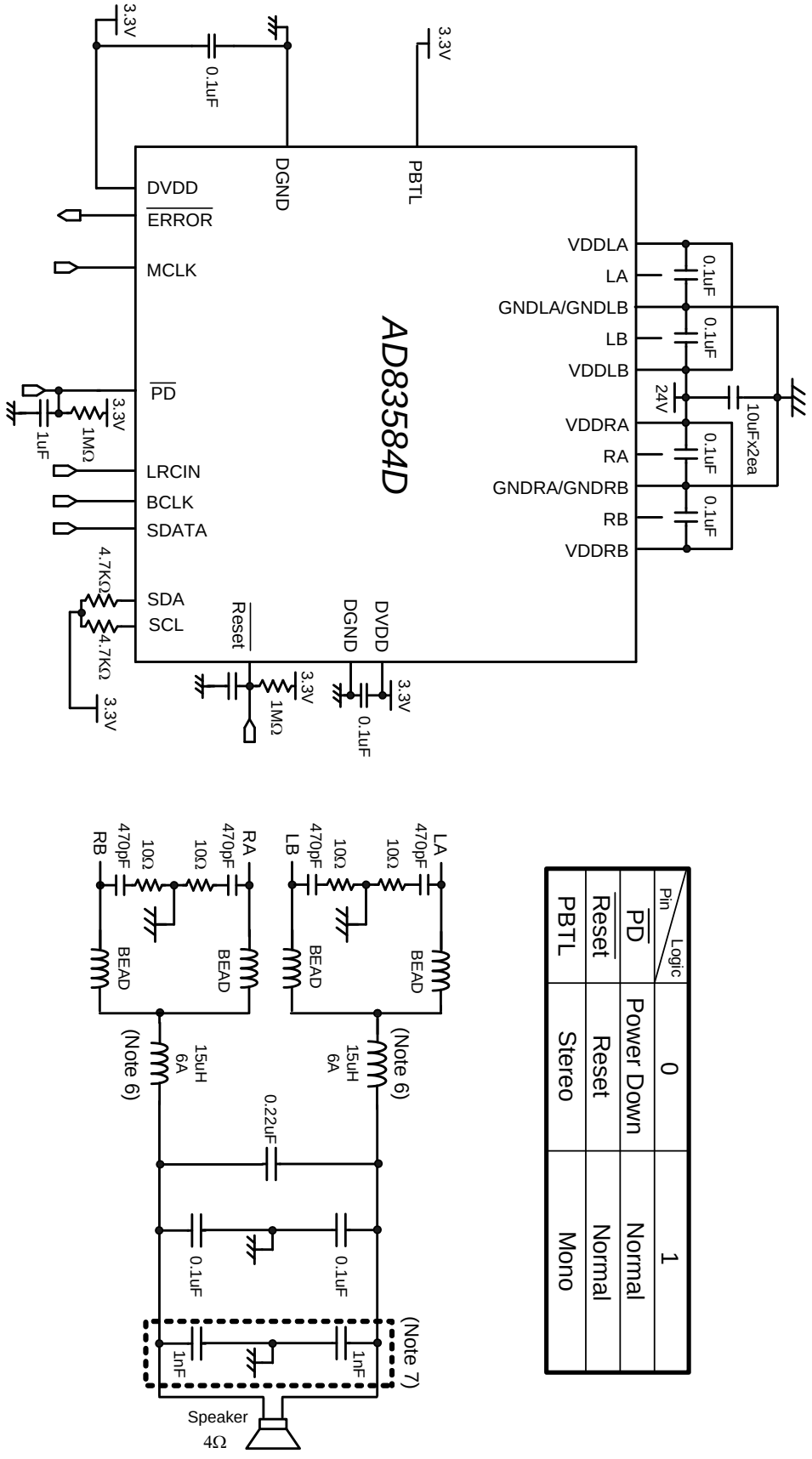


Note 3: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 7A.

Note 4: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 5: The snubber circuit can be removed while the PVDD <=20V.

Application Circuit Example for Mono

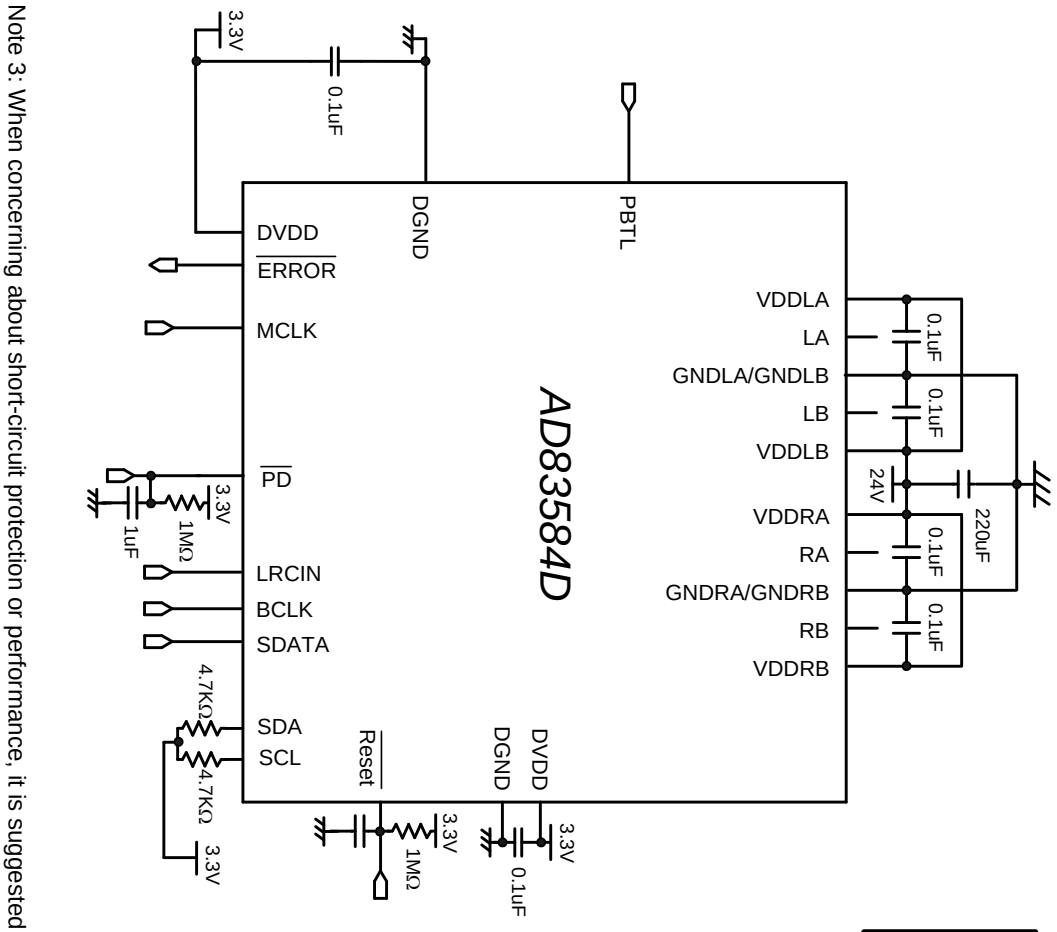


Pin / Logic	0	1
PD	Power Down	Normal
Reset	Reset	Normal
PBTL	Stereo	Mono

Note 6: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 14A.

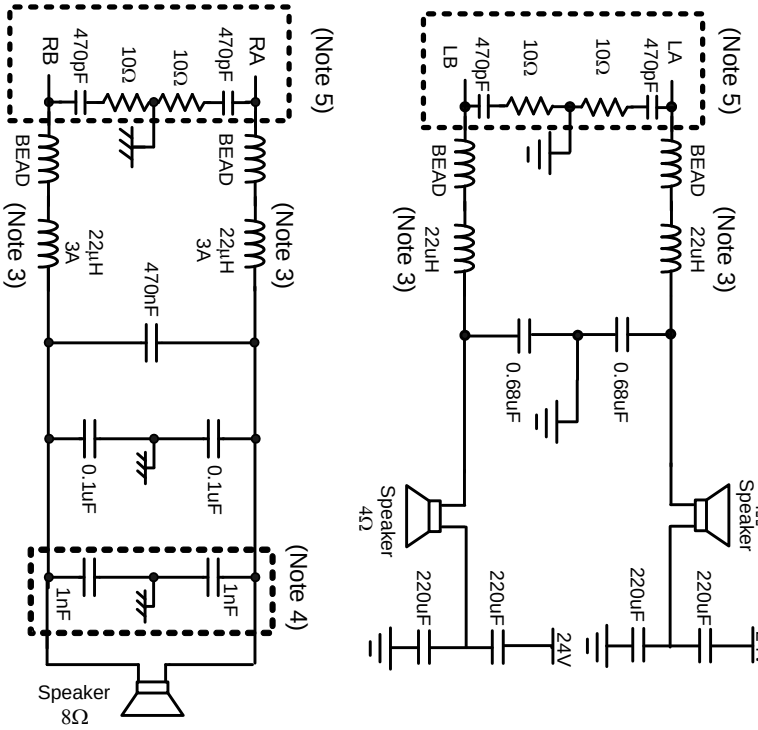
Note 7: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Application Circuit Example for 2.1CH



Pin / Logic	0	1
PD	Power Down	Normal
Reset	Reset	Normal
PBTL	X	X

Note : 2.1CH configuration, it programs by I2C via register address 0x11, B[4] SEM.



Note 3: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 7A.

Note 4: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 5: The snubber circuit can be removed while the PVDD <=20V.

Electrical Characteristics and Specifications for Loudspeaker

- **BTL (Bridge-Tied-Load) output for Stereo**

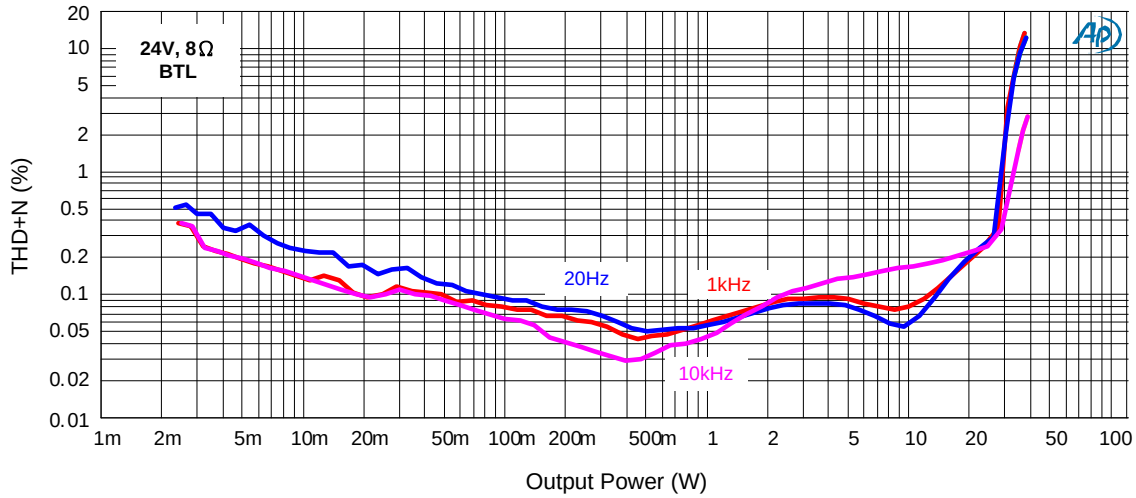
Condition: T_A=25 °C, DVDD =3.3V, VDDL=VDDR=24V, F_S=48kHz, Load=8Ω with passive LC lowpass filter (L=15μ H with R_{DC}=63mΩ , C=220nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N=0.28%)				25		W
	RMS Output Power (THD+N=0.15%)				15		W
	RMS Output Power (THD+N=0.09%)				10		W
THD+N	Total Harmonic Distortion + Noise	P_O=7.5W			0.1		%
SNR	Signal to Noise Ratio (Note 8)		-1dB		98		dB
DR	Dynamic Range (Note 8)		-60dB		108		dB
Vn	Output Noise (Note 8)	20Hz to 20kHz			110		uV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz			-72		dB
	Channel Separation	1W @1kHz			-81		dB

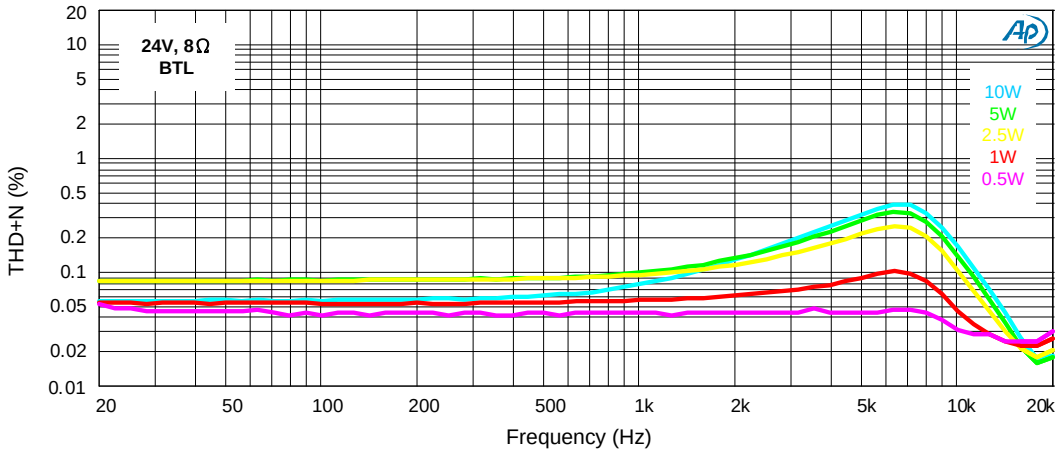
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

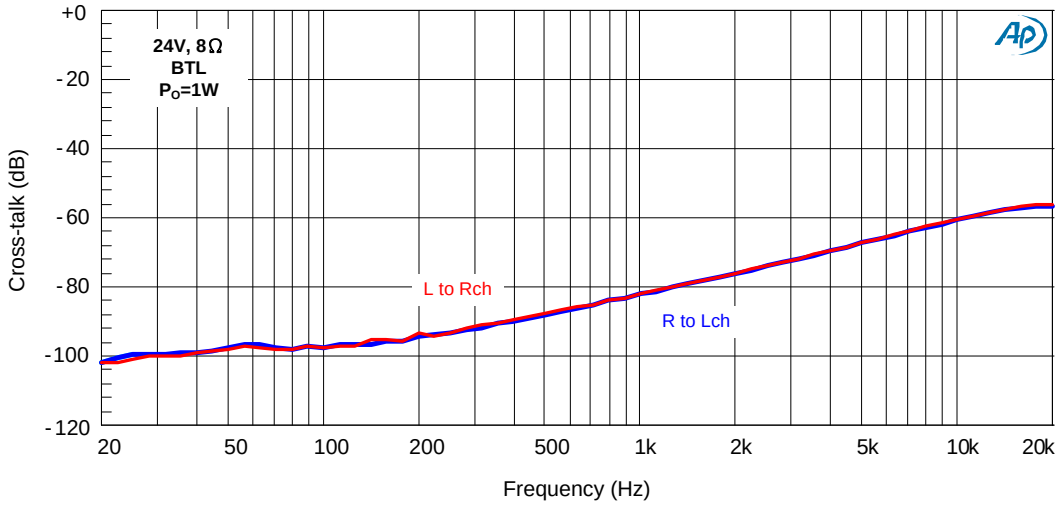
Total Harmonic Distortion + Noise vs. Output Power (BTL)



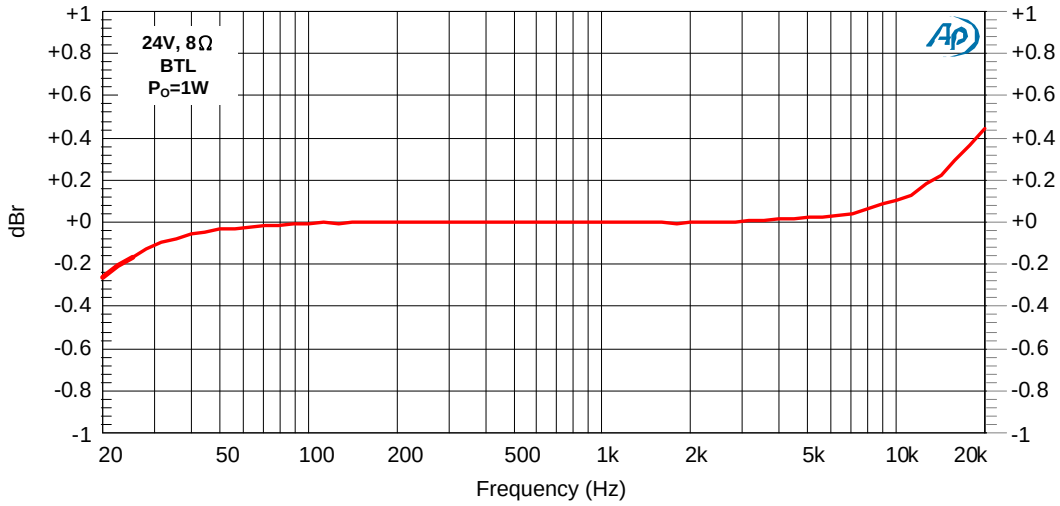
Total Harmonic Distortion + Noise vs. Frequency (BTL)



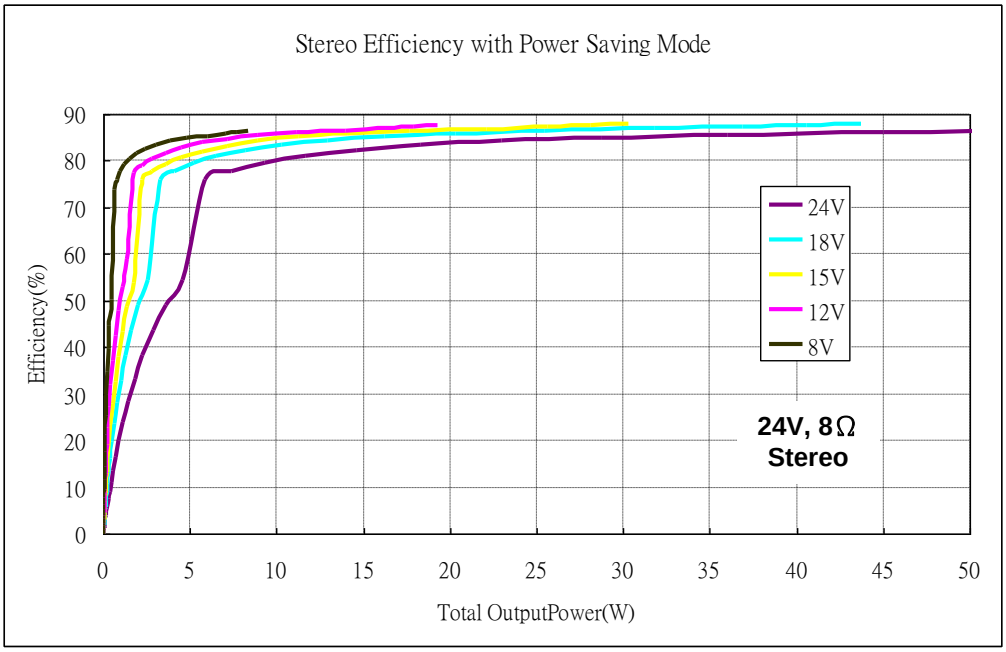
Cross-talk (Stereo, BTL)



Frequency Response (BTL)



Efficiency (Stereo, BTL) during Power Saving Mode



Electrical Characteristics and Specifications for Loudspeaker (cont.)

- **PBTL (Parallel-Bridge-Tied-Load) output for Mono**

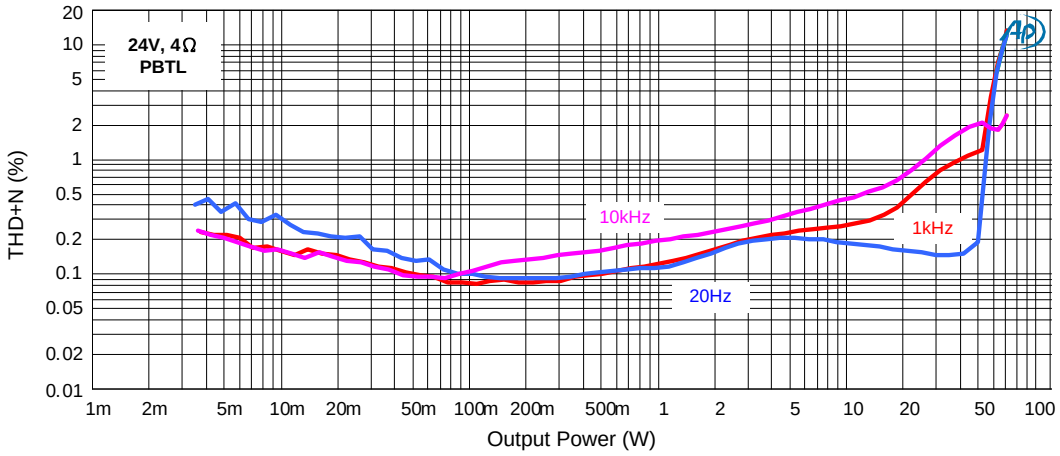
Condition: T_A=25 °C, DVDD= 3.3V, VDDL=VDDR=24V, F_S=48kHz, Load=4Ω with passive LC lowpass filter (L=15μ H with R_{DC}=63mΩ , C=220nF); Input is 1kHz sinewave.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N=1.3%)				50		W
	RMS Output Power (THD+N=0.85%)				30		W
	RMS Output Power (THD+N=0.55%)				20		W
THD+N	Total Harmonic Distortion + Noise	P_o=15W			0.4		%
SNR	Signal to Noise Ratio (Note 8)		-1dB		94		dB
DR	Dynamic Range (Note 8)		-60dB		106		dB
Vn	Output Noise (Note 8)	20Hz to 20kHz			85		uV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz			-79		dB

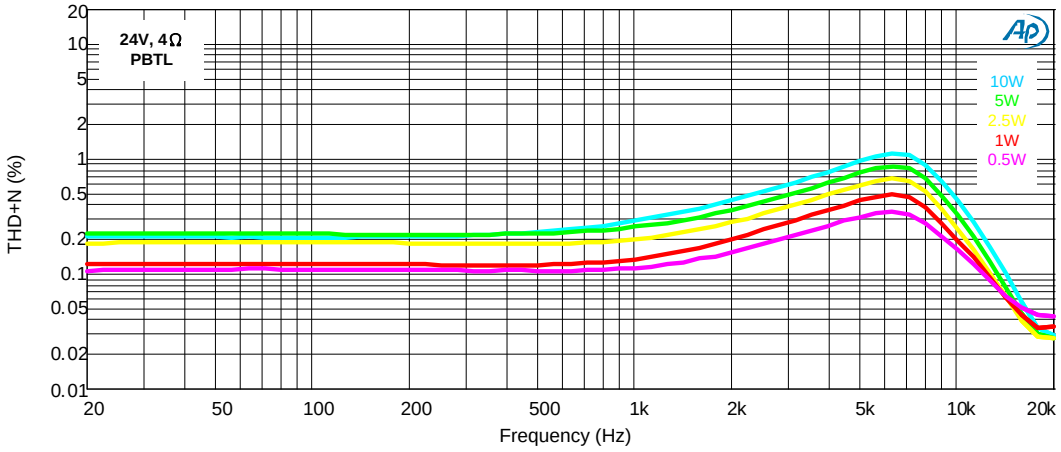
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

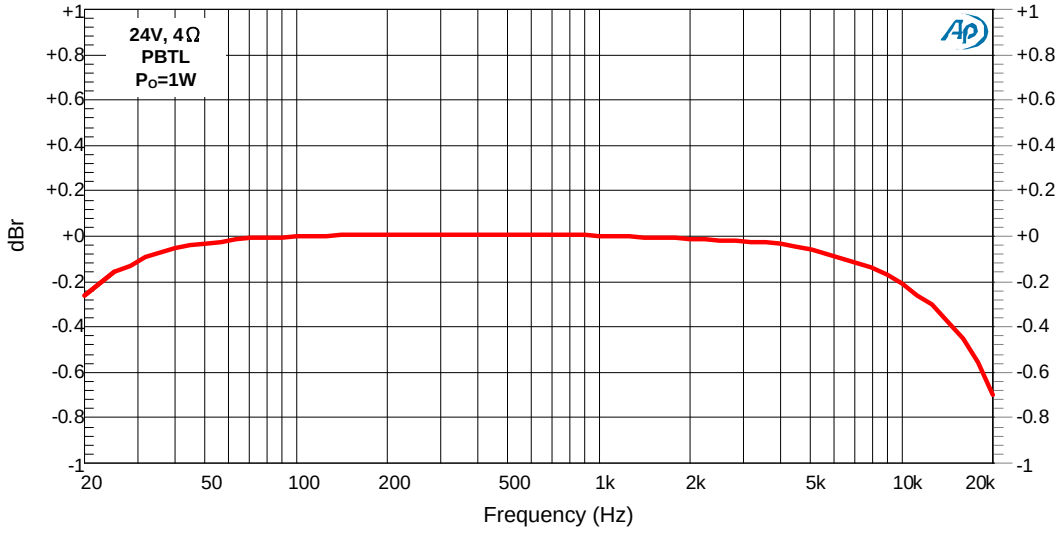
Total Harmonic Distortion + Noise vs. Output Power (PBTL)



Total Harmonic Distortion + Noise vs. Frequency (PBTL)



Frequency Response (PBTL)



Electrical Characteristics and Specifications for Loudspeaker (cont.)

- **SE (Single-ended) output for 2.1CH**

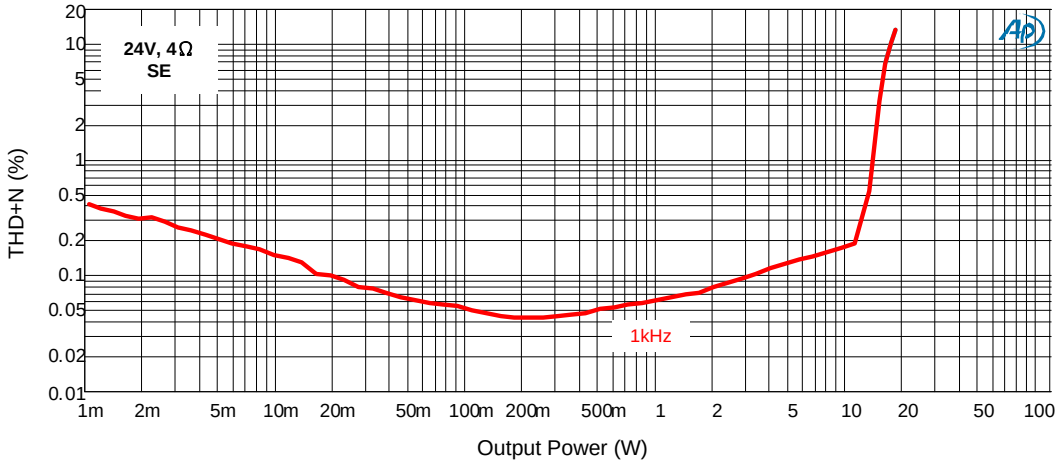
Condition: T_A=25 °C, DVDD =3.3V, VDDL=VDDR=24V, F_S=48kHz, Load=4Ω with passive LC lowpass filter (L=22μ H with R_{DC}=60mΩ , C=680nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N=0.3%)				12		W
THD+N	Total Harmonic Distortion + Noise	P_O=5W			0.14		%
SNR	Signal to Noise Ratio (Note 8)		-9dB		91		dB
DR	Dynamic Range (Note 8)		-68dB		98		dB
Vn	Output Noise (Note 8)	20Hz to 20kHz			132		uV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz			-71		dB
	Channel Separation	1W @1kHz			-62		dB

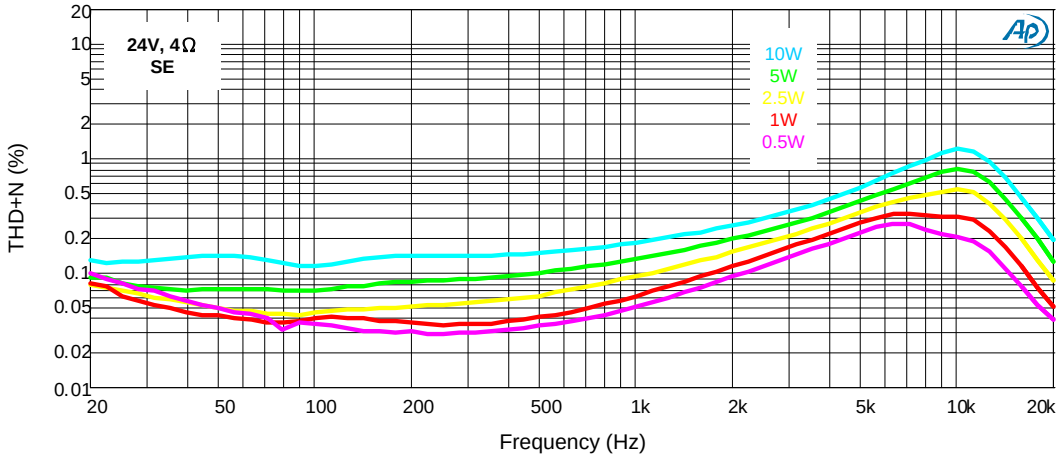
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

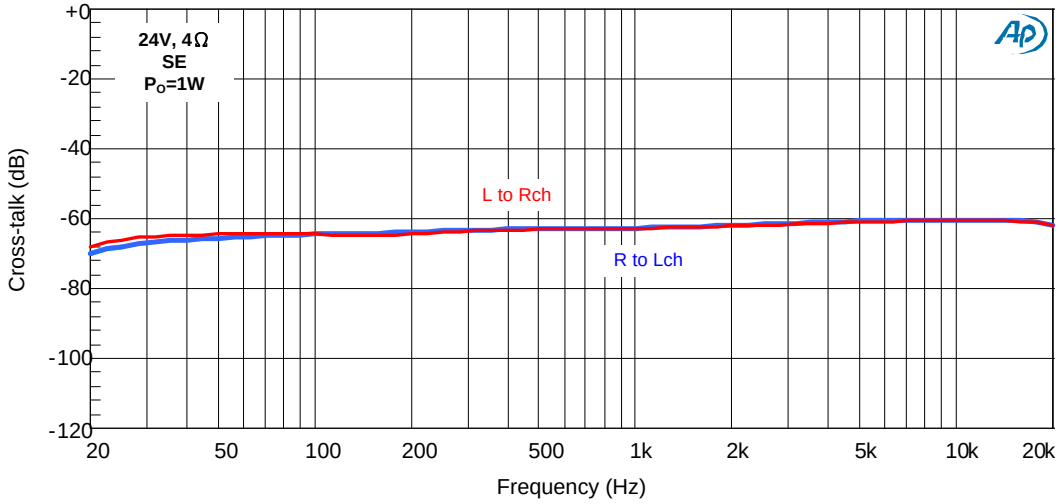
Total Harmonic Distortion + Noise vs. Output Power (SE)



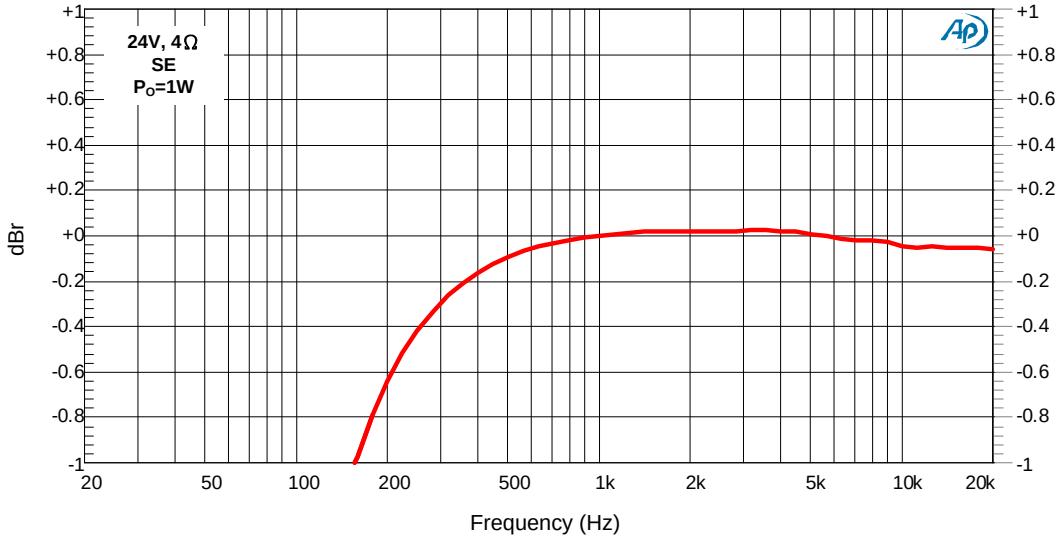
Total Harmonic Distortion + Noise vs. Frequency (SE)



Cross-talk (SE)

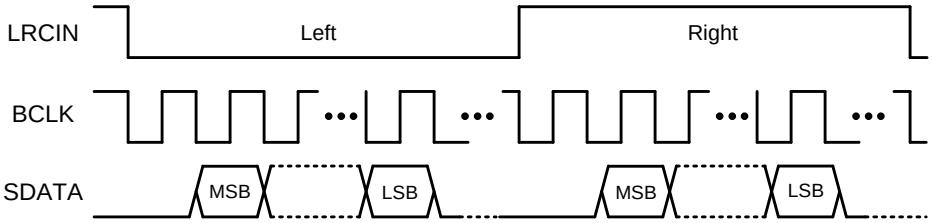


Frequency Response (SE)

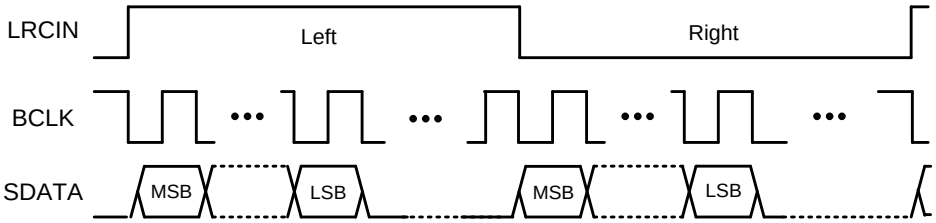


Interface configuration

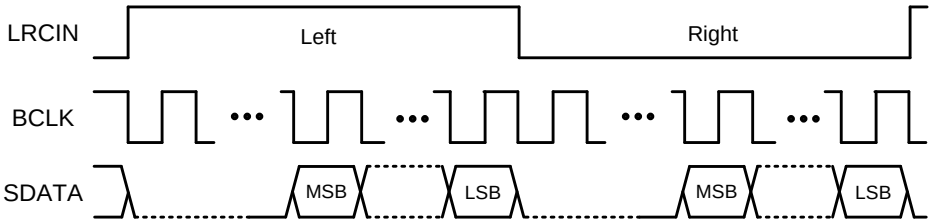
- I^2S



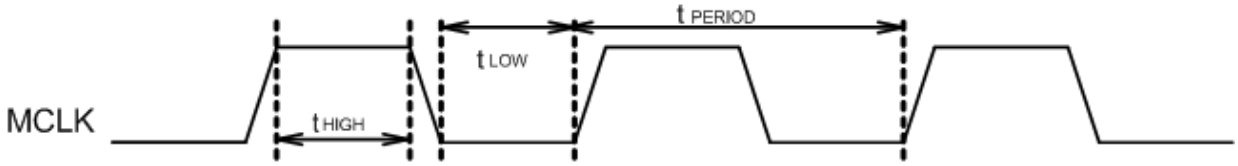
- Left-Alignment



- Right-Alignment

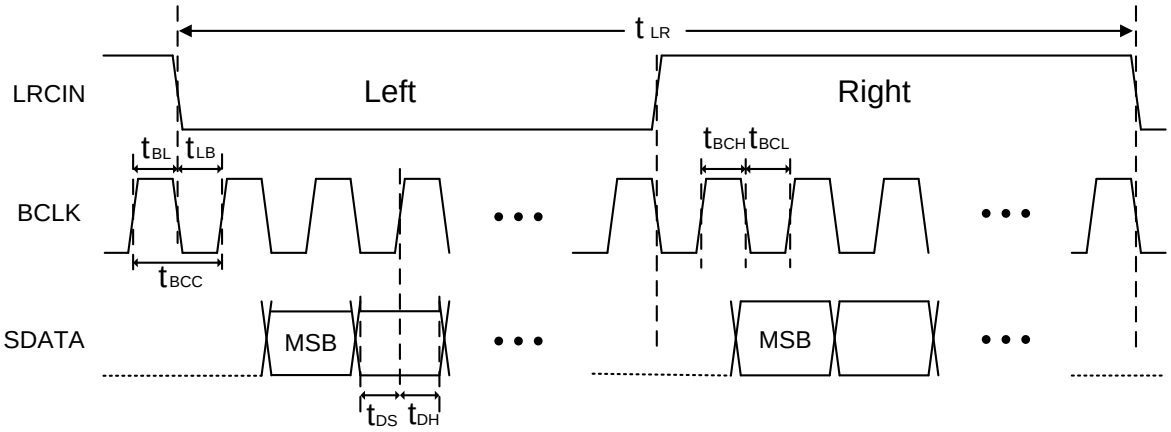


- System Clock Timing



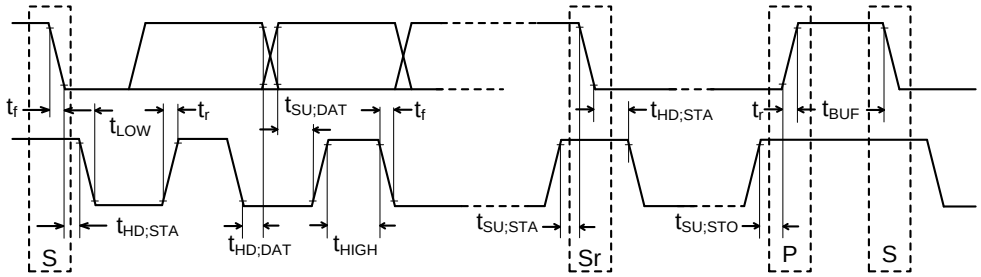
t_{HIGH} ≧ 40 .4 ns	t_{LOW} ≧ 40 .4 ns	t_{PERIOD} ≧ 80 .8 ns	CLK_OUT pin is pulled low or floating
t_{HIGH} ≧ 10 .1 ns	t_{LOW} ≧ 10 .1 ns	t_{PERIOD} ≧ 20 .2 ns	CLK_OUT pin is pulled high

- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	10.41		31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	50			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	50			ns
t_{BCC}	BCLK Period ($1/64F_S$)	162.76		488.3	ns
t_{BCH}	BCLK Pulse Width High	81.38		244	ns
t_{BCL}	BCLK Pulse Width Low	81.38		244	ns
t_{DS}	SDATA Set-Up Time	50			ns
t_{DH}	SDATA Hold Time	50			ns

- I^2C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time for repeated START condition	$t_{HD,STA}$	4.0	---	0.6	---	μs
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	μs
Setup time for repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	μs
Hold time for I^2C bus data	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Setup time for I^2C bus data	$t_{SU;DAT}$	250	---	100	---	Ns
Rise time of both SDA and SCL signals	t_r	---	1000	20+0.1Cb	300	Ns
Fall time of both SDA and SCL signals	t_f	---	300	20+0.1Cb	300	Ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	μs
Bus free time between STOP and the next START condition	t_{BUF}	4.7	---	1.3	---	μs
Capacitive load for each bus line	C_b		400		400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	---	$0.1V_{DD}$	---	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	---	$0.2V_{DD}$	---	V

Operation Description

AD83584D has a built-in PLL internally, the default volume is muted. AD83584D will activate while the de-mute command via I^2C is programmed.

- Operation modes

(i) Without I^2C control

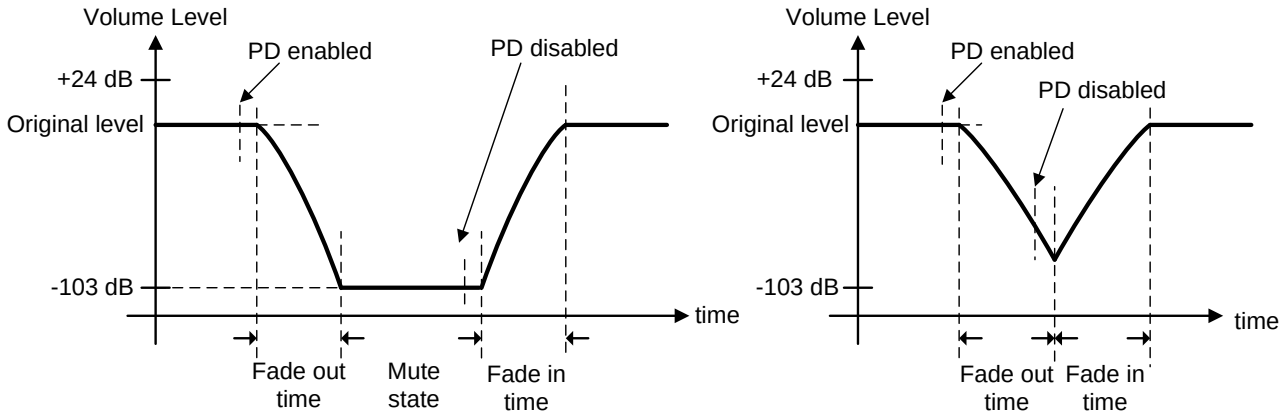
The default settings, Bass, Treble, EQ, Volume, DRC, PLL, Subwoofer Bandwidth, …, and Sub-woofer gain are applied to register table content when using AD83584D without I^2C control. The more information about default settings, please refer to the highlighted column of register table section.

(ii) With I^2C control

When using I^2C control, user can program suitable parameters into AD83584D for their specific applications. Please refer to the register table section to get the more detail.

- Power down control

AD83584D has a built-in volume fade-in/fade-out design for PD/Mute function. The relative PD timing diagrams for loudspeakers are shown below.



The volume level will be decreased to -∞dB in several LRCIN cycles. Once the fade-out procedure is finished, AD83584D will turn off the power stages, stop clock signals (MCLK, BCLK) from feeding into digital circuit and turn off the current of the internal analog circuits. After PD pin is pulled low, AD83584D needs up to 256 LRCIN clocks to finish the above works before entering power down state. Users can't program AD83584D during power down state, but all the settings of register table will still be kept except that DVDD is removed.

If the PD function is disabled in the midway of the fade-out procedure, AD83584D will also execute the fade-in procedure. In addition, AD83584D will establish the analog circuits' bias current and feed the clock signals (MCLK, BCLK) into digital circuits. Then, AD83584D will return to its normal operation without power down.

- Reset

When the $\overline{\text{RESET}}$ pin is lowered, AD83584D will clear the stored data and reset the register table to default values. AD83584D will exit reset state at the 256th MCLK cycle after the $\overline{\text{RESET}}$ pin is raised to high.

- Self-protection circuits

AD83584D has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

(i) When the internal junction temperature is higher than 150℃, power stages will be turned off and AD83584D will return to normal operation once the temperature drops to 120℃. The temperature values may vary around 10%.

(ii) The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or GND/VDD. For normal 24V operations, the current flowing through the power stage will be less than 7A for stereo configuration or less than 14A for mono configuration. Otherwise, the short-circuit detectors may pull the $\overline{\text{ERROR}}$ pin to DGND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain $\overline{\text{ERROR}}$ pin will be pulled low and latched into ERROR state.

Once the over-temperature or short-circuit condition is removed, AD83584D will exit ERROR state when one of the following conditions is met: (1) $\overline{\text{RESET}}$ pin is pulled low, (2) $\overline{\text{PD}}$ pin is pulled low, (3) Master mute is enabled through the I^2C interface.

(iii) Once the DVDD voltage is lower than 2.7V, AD83584D will turn off its loudspeaker power stages and cease the operation of digital processing circuits. When DVDD becomes higher than 2.8V, AD83584D will return to normal operation.

- Anti-pop design

AD83584D will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- 3D surround sound

AD83584D provides the virtual surround sound technology with greater separation and depth voice quality for stereo signals.

- I^2C Chip Select

$\overline{\text{ERROR}}$ is an input pin during power. It can be pulled High (15-kΩ pull up) or Low (15-kΩ pull down). Low indicates an I^2C address of 0x30, and high an address of 0x31.

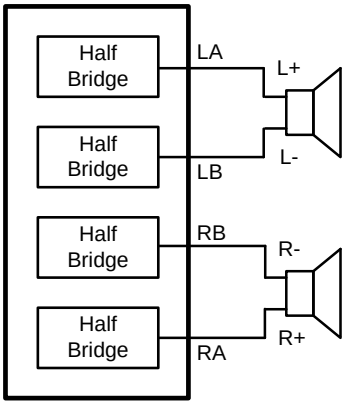
- Output configuration

The bit4 [SEM] of address 0X11 and PBTL pin defines the configuration mode. AD83584D can be configured to stereo, mono via PBTL pin (the bit4 [SEM] of address 0X11 default is low). 2.1CH output mode configuration, user can via I^2C to program it from the bit 4 [SEM] of address 0X11. Table1 provides a reference of available configuration.

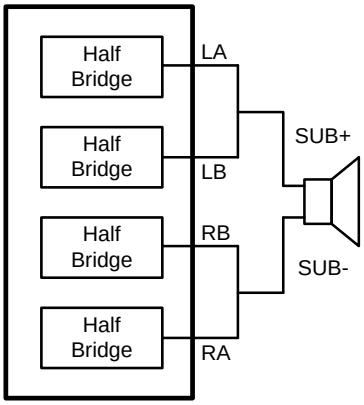
Table 1.

[SEM]	PBTL	Configuration Mode
0	0	Stereo
0	1	Mono
1	X	2.1CH

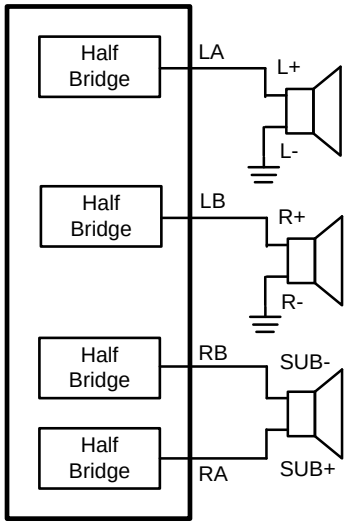
Configuration figures:



STEREO



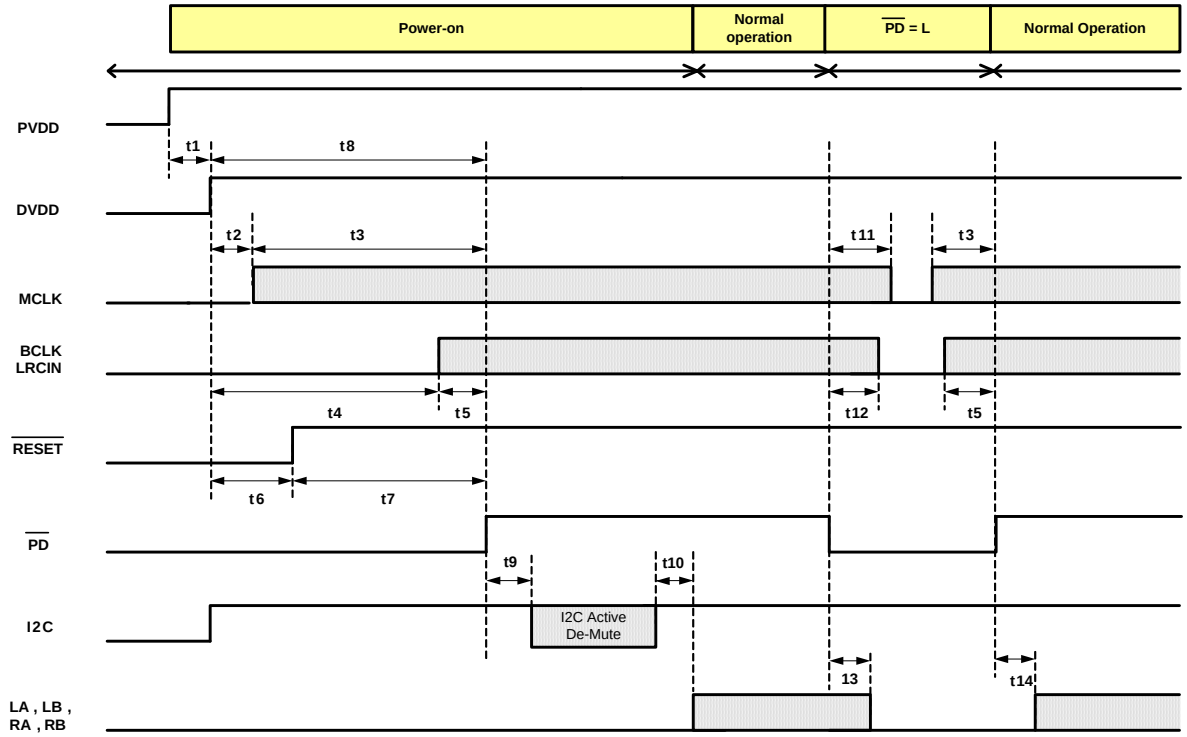
MONO



2.1CH

- Power on sequence

Hereunder is AD83584D's power on sequence. Give a de-mute command via I^2C when the whole system is stable.

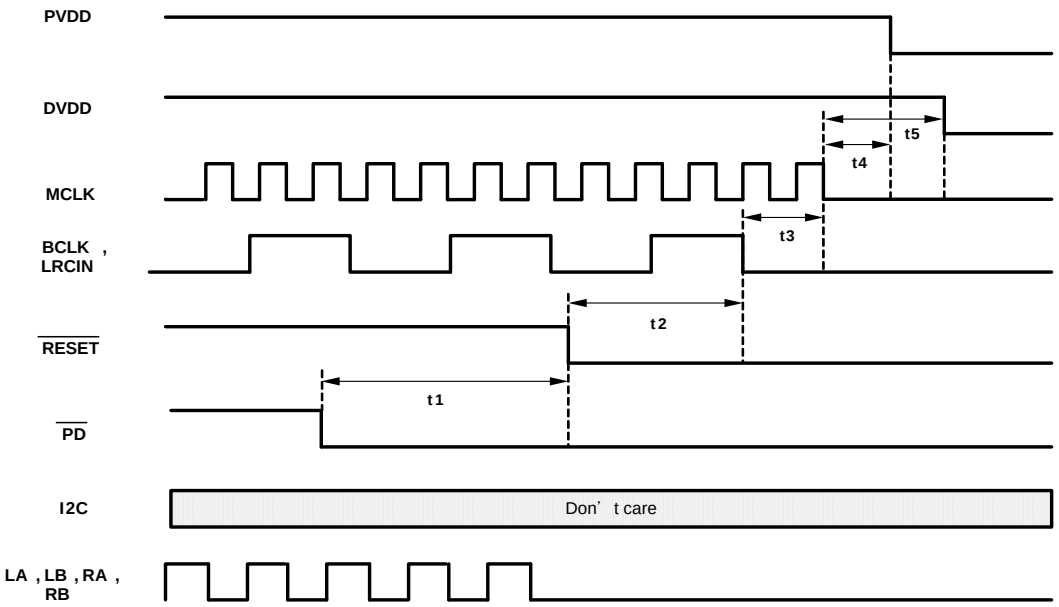


Symbol	Condition	Min	Max	Units
t1		0	-	msec
t2		0	-	msec
t3		10	-	msec
t4		0	-	msec
t5		10	-	msec
t6		10	-	msec
t7(Note 10)		0	-	msec
t8		200	-	msec
t9		20	-	msec
t10		-	0.1	msec
t11		25	-	msec
t12		25	-	msec
t13		-	22	msec
t14		-	0.1	Msec

Note 10: MCLK should meet timing spec before t7.

- Power off sequence

Hereunder is AD83584D's power off sequence.



Symbol	Condition	Min	Max	Units
t1		35	-	msec
t2		0.1	-	msec
t3		0	-	msec
t4		1	-	msec
t5		1	-	msec

I²C-Bus Transfer Protocol

- Introduction

AD83584D employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD83584D is always an I²C slave device.

- Protocol

  - START and STOP condition

START is identified by a high to low transition of the SDA signal. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD83584D and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

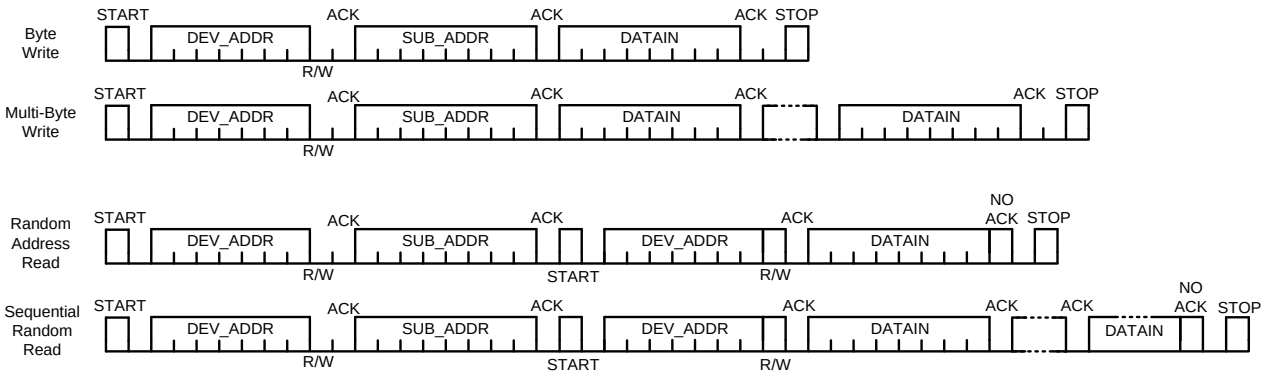
The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD83584D samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

The master generates 7-bit address to recognize slave devices. When AD83584D receives 7-bit address matched with 0110000 or 0110001 ($\overline{\text{ERROR}}$ pin state during power up), AD83584D will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD83584D internal sub-addresses.

  - Data transferring

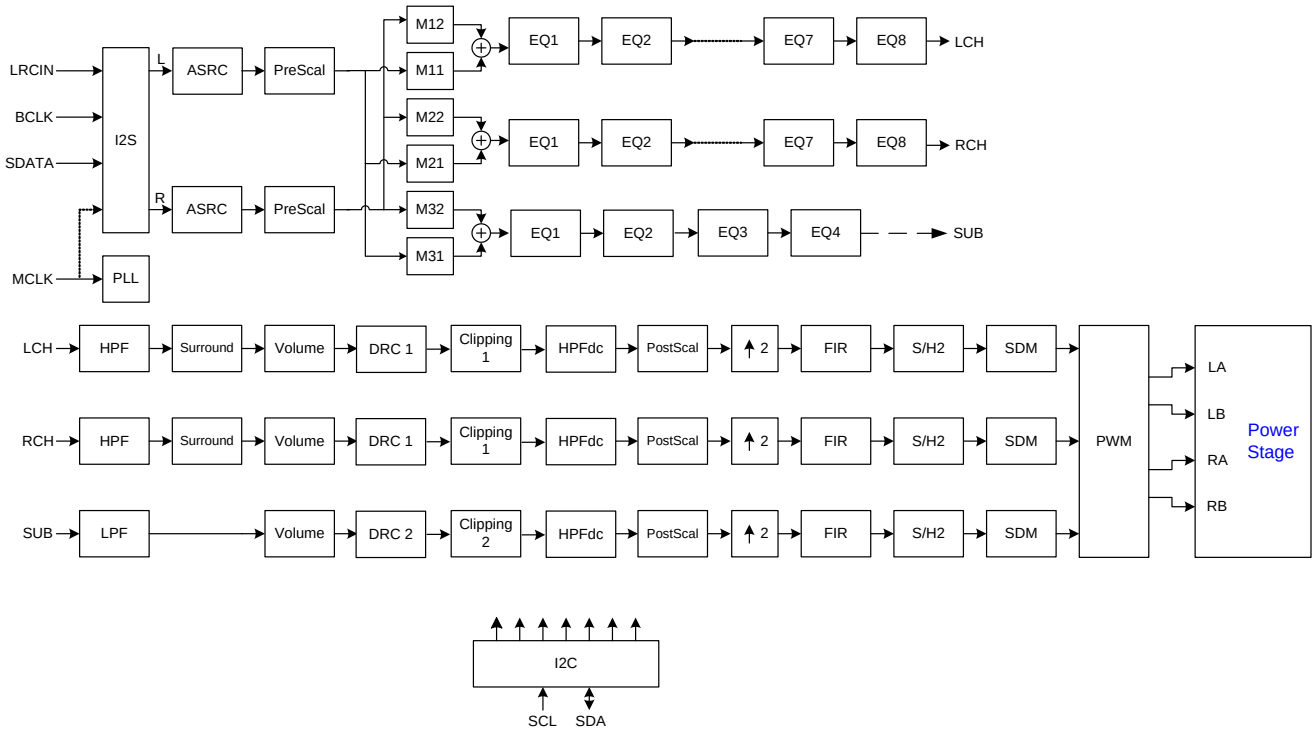
Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD83584D supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



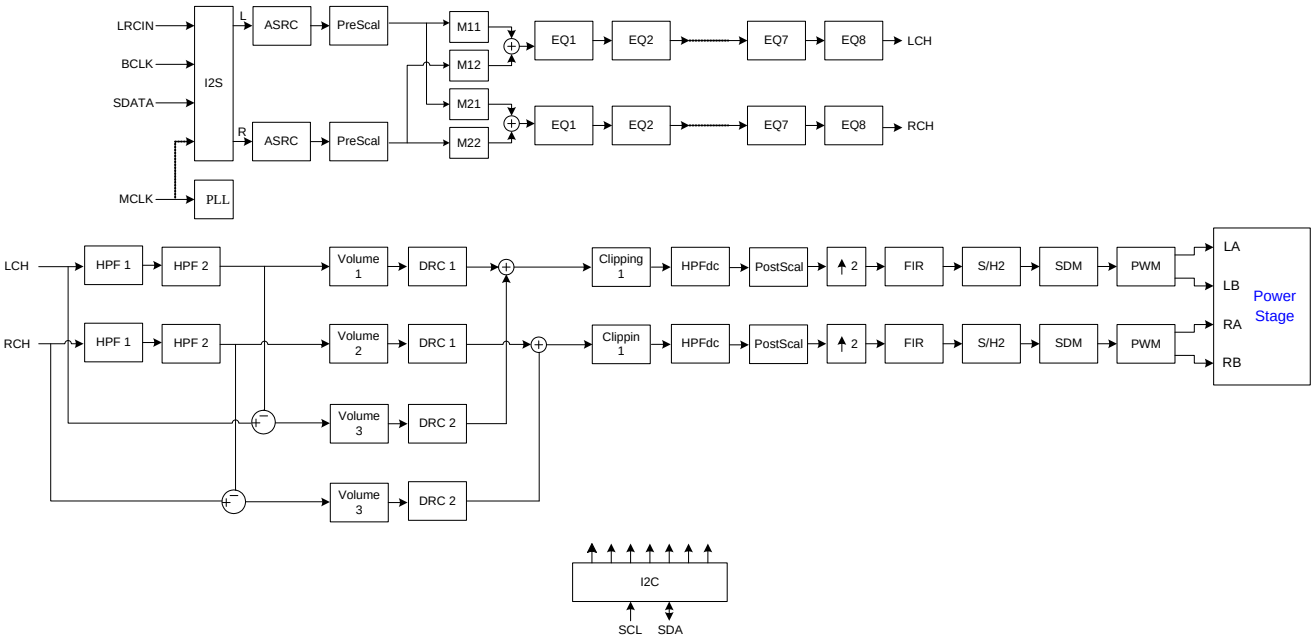
Register Table

The AD83584D's audio signal processing data flow is shown below. Users can control these functions by programming appropriate settings in the register table. In this section, the register table is summarized first. The definition of each register follows in the next section.

Dual bands DRC disable



Dual bands DRC enable (only for stereo mode, PBTL=Low)



Address	Name	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0X00	SCTL1	IF[2]	IF[1]	IF[0]	Reserved	PWML_X	PWMR_X	LV_UVSEL	LREXC
0X01	SCTL2	Reserved	BCLK_SEL	FS[1]	FS[0]	PMF[3]	PMF[2]	PMF[1]	PMF[0]
0X02	SCTL3	EN_CLK_OUT	Reserved			MUTE	CM1	CM2	CM3
0X03	MVOL	MV[7]	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]
0X04	C1VOL	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
0X05	C2VOL	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
0X06	C3VOL	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
0X07	BTONE	Reserved			BTC[4]	BTC[3]	BTC[2]	BTC[1]	BTC[0]
0X08	TTONE	Reserved			TTC[4]	TTC[3]	TTC[2]	TTC[1]	TTC[0]
0X09	XOF	Reserved				XO[3]	XO[2]	XO[1]	XO[0]
0X0A	SCTL4	SRBP	BTE	TBDRCE	NGE	EQL	PSL	DSPB	HPB
0X0B	C1CFG	Reserved				C1PCBP	C1DRCBP	C1HPFBP	C1VBP
0X0C	C2CFG	Reserved				C2PCBP	C2DRCBP	C2HPFBP	C2VBP
0X0D	C3CFG	Reserved				C3PCBP	C3DRCBP	C3HPFBP	C3VBP
0X0E	LAR	LA[3]	LA[2]	LA[1]	LA[0]	LR[3]	LR[2]	LR[1]	LR[0]
0X10	ERDLY	Reserved							
0X11	SCTL5	Reserved		SW_RSTB	LVUV_FADE	SEM	DIS_MCLK_DET	QT_EN	PWM_SEL
0X12	HVUV	DIS_HVUV	Reserved			HV_UVSEL [3]	HV_UVSEL [2]	HV_UVSEL [1]	HV_UVSEL [0]

0X13	NGCFG	Reserved	A_SEL_FAULT	D_MOD	DIS_NG_FADE	Reserved		NG_GAIN[1]	NG_GAIN[0]
0X14	CFADDR	Reserved	CFA[6]	CFA[5]	CFA[4]	CFA[3]	CFA[2]	CFA[1]	CFA[0]
0X15	A1CF1	C1B[23]	C1B[22]	C1B[21]	C1B[20]	C1B[19]	C1B[18]	C1B[17]	C1B[16]
0X16	A1CF2	C1B[15]	C1B[14]	C1B[13]	C1B[12]	C1B[11]	C1B[10]	C1B[9]	C1B[8]
0X17	A1CF3	C1B[7]	C1B[6]	C1B[5]	C1B[4]	C1B[3]	C1B[2]	C1B[1]	C1B[0]
0X18	A2CF1	C2B[23]	C2B[22]	C2B[21]	C2B[20]	C2B[19]	C2B[18]	C2B[17]	C2B[16]
0X19	A2CF2	C2B[15]	C2B[14]	C2B[13]	C2B[12]	C2B[11]	C2B[10]	C2B[9]	C2B[8]
0X1A	A2CF3	C2B[7]	C2B[6]	C2B[5]	C2B[4]	C2B[3]	C2B[2]	C2B[1]	C2B[0]
0X1B	B1CF1	C3B[23]	C3B[22]	C3B[21]	C3B[20]	C3B[19]	C3B[18]	C3B[17]	C3B[16]
0X1C	B1CF2	C3B[15]	C3B[14]	C3B[13]	C3B[12]	C3B[11]	C3B[10]	C3B[9]	C3B[8]
0X1D	B1CF3	C3B[7]	C3B[6]	C3B[5]	C3B[4]	C3B[3]	C3B[2]	C3B[1]	C3B[0]
0X1E	B2CF1	C4B[23]	C4B[22]	C4B[21]	C4B[20]	C4B[19]	C4B[18]	C4B[17]	C4B[16]
0X1F	B2CF2	C4B[15]	C4B[14]	C4B[13]	C4B[12]	C4B[11]	C4B[10]	C4B[9]	C4B[8]
0X20	B2CF3	C4B[7]	C4B[6]	C4B[5]	C4B[4]	C4B[3]	C4B[2]	C4B[1]	C4B[0]
0X21	A0CF1	C5B[23]	C5B[22]	C5B[21]	C5B[20]	C5B[19]	C5B[18]	C5B[17]	C5B[16]
0X22	A0CF2	C5B[15]	C5B[14]	C5B[13]	C5B[12]	C5B[11]	C5B[10]	C5B[9]	C5B[8]
0X23	A0CF3	C5B[7]	C5B[6]	C5B[5]	C5B[4]	C5B[3]	C5B[2]	C5B[1]	C5B[0]
0X24	CFUD	Reserved				RA	R1	WA	W1
0X25	FDCFG	Reserved							
0X26	MBIST	Reserved							
0X27	Status	Reserved							
0X28	PWM_CTRL	Reserved							
0X29	TM_CTRL	Reserved							
0X2A	QT_SW_LEVEL	SW_WINDOW[2]	SW_WINDOW[1]	SW_WINDOW[0]	QT_SW_LEVEL[4]	QT_SW_LEVEL[3]	QT_SW_LEVEL[2]	QT_SW_LEVEL[1]	QT_SW_LEVEL[0]
0X2B	VFT	MV_FT[1]	MV_FT[0]	C1V_FT[1]	C1V_FT[0]	C2V_FT[1]	C2V_FT[0]	C3V_FT[1]	C3V_FT[0]

Detail Description for Register

Note that the highlighted columns are default values of these tables. If there is no highlighted value, the default setting of this bit is determined by the external pin.

- Address 0X00 : State control 1

  AD83584D supports multiple serial data input formats including I^2S, Left-alignment and Right-alignment. These formats are selected by users via bit7~bit5 of address 0X00. The left/right channels can be exchanged to each other by programming to address 0/bit0, LREXC.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I^2S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
B[4]		Reserved		
B[3]	PWML_X	LA/LB exchange	0	No exchanged
			1	L/R exchanged
B[2]	PWMR_X	RA/RB exchange	0	L/R exchanged
			1	No exchanged
B[1]	LV_UVSEL	LV under voltage selection	0	2.7v
			1	3.0v
B[0]	LREXC	Left/Right (L/R) Channel exchanged	0	No exchanged
			1	L/R exchanged

- Address 0X01 : State control 2

AD83584D has a built-in PLL and supports multiple MCLK/Fs ratios. Detail setting is shown in the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]	BCLK_SEL	MCLK-less (BCLK system)	0	Disable
			1	Enable
B[5:4]	FS[1:0]	Sampling Frequency	00	32/44.1/48kHz
			01	64/88.2/96kHz
			1x	128/176.4/192kHz

Multiple MCLK/FS ratio setting table

BIT	NAME	DESCRIPTION	VALUE	B[5:4]=00	B[5:4]=01	B[5:4]=1x
B[3:0]	PMF[3:0]	MCLK/Fs setup	0000	1024x	512x	256x
			0001	64x	64x	64x
			0010	128x	128x	128x
			0011	192x	192x	192x
			0100	Reset Default (256x)	Reset Default (256x)	Reset Default (256x)
			0101	384x	384x	Reserved
			0110	512x	512x	
			0111	576x	Reserved	
			1000	768x		
			1001	1024x		

- Address 0X02 : State control 3

AD83584D has mute function including master mute and channel mute. When master mute is enabled, all 3 processing channels are muted. User can mute these 3 channels individually by channel mute. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	EN_CLK_OUT	PLL Clock Output	0	Disabled
			1	Enabled
B[6]		Reserved		
B[5]		Reserved		
B[4]		Reserved		
B[3]	MUTE	Master Mute	0	All channel not muted
			1	All channel muted
B[2]	CM1	Channel 1 Mute	0	Ch1 not muted
			1	Only Ch1 muted
B[1]	CM2	Channel 2 Mute	0	Ch2 not muted
			1	Only Ch2 muted
B[0]	CM3	Channel 3 Mute	0	Ch3 not muted
			1	Only Ch3 muted

- Address 0X03 : Master volume control

AD83584D supports both master-volume (Address 0X03) and channel-volume control (Address 0X04, 0X05 and 0X06) modes. Both volume control settings range from +12dB ~ -103dB and 0.5dB per step. Note that the master volume control is added to the individual channel volume control as the total volume control. For example, if the master volume level is set at, Level A (in dB unit) and the channel volume level is set at Level B (in dB unit), the total volume control setting is equal to Level A plus with Level B.

-103dB ≦ Total volume (Level A + Level B) ≦ +24dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	MV[7:0]	Master Volume	00000000	+12.0dB
			00000001	+11.5dB
			00000010	+11.0dB
			:	:
			00010111	+0.5dB
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X04 : Channel 1 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C1V[7:0]	Channel1 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X05 : Channel 2 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C2V[7:0]	Channel2 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X06 : Channel 3 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C3V[7:0]	Channel3 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X07/0X08 : Bass/Treble tone boost and cut

  Last two sets of EQ can be programmed as bass/treble tone boost and cut. When, register with address-0X0A, bit-6, BTE is set to high, the EQ-7 and EQ-8 will perform as bass and treble respectively. The -3dB corner frequency of bass is 360Hz, and treble is 7kHz. The gain range for both filters is +12db ~ -12dB with 1dB per step.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]		Reserved		
B[4:0]	BTC[4:0] / TTC[4:0]	The gain setting of boost and cut	00000	+12dB
			…	…
			00100	+12dB
			00101	+11dB
			00110	+10dB
			…	…
			01110	+2dB
			01111	+1dB
			10000	0dB
			10001	-1dB
			10010	-2dB
			…	…
			11010	-10dB
			11011	-11dB
			11100	-12dB
			…	…
			11111	-12dB

- Address 0X09 : Bass management crossover frequency

The AD83584D provides bass management crossover frequency selection. A 1st order high-pass filter (channel 1 and 2) and a 2nd order low-pass filter (channel 3) at selected frequency are performed.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3:0]	XO[3:0]	Bass management crossover frequency	0000	80Hz
			0001	100Hz
			0010	120Hz
			0011	140Hz
			0100	160Hz
			0101	180Hz
			0110	200Hz
			0111	300Hz
			1000	400Hz
			1001	500Hz
			1010	600Hz
			1011	700Hz
			1100	800Hz
			1101	900Hz
			1110	1000Hz
			1111	Reserved

- Address 0X0A : State control 4

The AD83584D provides several DSP setting as following.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	SRBP	Surround bypass	0	Surround enable
			1	Surround bypass
B[6]	BTE	Bass/Treble Selection bypass	0	Bass/Treble Disable
			1	Bass/Treble Enable
B[5]	TBDRCE	Two Band DRC Enable	0	Two Band DRC Disable
			1	Two Band DRC Enable
B[4]	NGE	Noise gate enable	0	Noise gate disable
			1	Noise gate enable
B[3]	EQL	EQ Link	0	Each channel uses individual EQ
			1	Channel-2 uses channel-1 EQ
B[2]	PSL	Post-scale link	0	Each channel uses individual post-scale
			1	Use channel-1 post-scale
B[1]	DSPB	EQ bypass	0	EQ enable
			1	EQ bypass
B[0]	HPB	DC blocking HPF bypass	0	HPF dc enable
			1	HPF dc bypass

- Address 0X0B, 0X0C and 0X0D : Channel configuration registers

The AD83584D can configure each channel to enable or bypass DRC and channel volume and select the limiter set.

Address 0X0B and 0X0C; where x=1 or 2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]		Reserved		
B[5]		Reserved		
B[4]		Reserved		
B[3]	CxPCBP	Channel x Power Clipping bypass	0	Channel x PC enable
			1	Channel x PC bypass
B[2]	CxDRCBP	Channel x DRC bypass	0	Channel x DRC enable
			1	Channel x DRC bypass
B[1]	CxHPFBP	Channel x bass management HPF bypass	0	Channel x HPF enable
			1	Channel x HPF bypass
B[0]	CxVBP	Channel x Volume bypass	0	Channel x's master volume operation
			1	Channel x's master volume bypass

Address 0X0D

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]		Reserved		
B[5]		Reserved		
B[4]		Reserved		
B[3]	C3PCBP	Channel 3 Power Clipping bypass	0	Channel 3 PC enable
			1	Channel 3 PC bypass
B[2]	C3DRCBP	Channel 3 DRC bypass	0	Channel 3 DRC enable
			1	Channel 3 DRC bypass
B[1]	C3HPFBP	Channel 3 bass management LPF bypass	0	Channel 3 LPF enable
			1	Channel 3 LPF bypass
B[0]	C3VBP	Channel 3 Volume bypass	0	Channel 3 volume operation
			1	Channel 3 volume bypass

- Address 0X0E : DRC limiter attack/release rate

The AD83584D defines a set of limiter. The attack/release rates are defines as following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	LA[3:0]	DRC attack rate	0000	3 dB/ms
			0001	2.667 dB/ms
			0010	2.182 dB/ms
			0011	1.846 dB/ms
			0100	1.333 dB/ms
			0101	0.889 dB/ms
			0110	0.4528 dB/ms
			0111	0.2264 dB/ms
			1000	0.15 dB/ms
			1001	0.1121 dB/ms
			1010	0.0902 dB/ms
			1011	0.0752 dB/ms
			1100	0.0645 dB/ms
			1101	0.0563 dB/ms
			1110	0.0501 dB/ms
			1111	0.0451 dB/ms
B[3:0]	LR[3:0]	DRC release rate	0000	0.5106 dB/ms
			0001	0.1371 dB/ms
			0010	0.0743 dB/ms
			0011	0.0499 dB/ms
			0100	0.0360 dB/ms
			0101	0.0299 dB/ms
			0110	0.0264 dB/ms
			0111	0.0208 dB/ms
			1000	0.0198 dB/ms
			1001	0.0172 dB/ms
			1010	0.0147 dB/ms
			1011	0.0137 dB/ms
			1100	0.0134 dB/ms
			1101	0.0117 dB/ms
			1110	0.0112 dB/ms
			1111	0.0104 dB/ms

- Address 0X11 : State control 5

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]		Reserved		
B[5]	SW_RSTB	Software reset	0	Reset
			1	Normal operation
B[4]	LVUV_FADE	Low Under Voltage Fade	0	No Fade
			1	Fade
B[3]	SEM	Single End Mode	0	2.0 mode (2BTL or 1PBTL)
			1	2.1 mode (2SE + 1BTL)
B[2]	DIS_MCLK_DET	Disable MCLK detect circuit	0	Enable MCLK detect circuit
			1	Disable MCLK detect circuit
B[1]	QT_EN	Power saving mode	0	Disable
			1	Enable
B[0]	PWM_SEL	PWM modulation	0	Qua-ternary
			1	Ternary

- Address 0X12 : PVDD under voltage selection

AD83584D can disable HV under voltage detection via bit 7.

AD83584D support multi-level HV under voltage detection via bit3~ bit0, using this function, AD83584D will fade out signal to avoid pop sounds if high voltage supply disappear before low voltage supply.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	DIS_HVUV	Disable HV under voltage selection	0	Enable
			1	Disable
B[6:4]		Reserved		
B[3:0]	HV_UV SEL	UV detection level	0000	8.2V
			0001	9.7V
			0011	13.2 V
			0100	15.5 V
			1100	19.5 V
			Others	9.7V

Note: Under voltage range has +/-10% max variation due to process window.

- Address 0X13 : I^{2}C address selection and Noise gate gain

The $\overline{\text{ERROR}}$ pin of AD83584D is a dual function pin. It is treated as a I^{2}C device address selection input when B[6] is set as low. It will become as an ERROR output pin when B[6] is set as high.

AD83584D provide noise gate function if receiving 2048 signal sample points smaller than noise gate attack level. User can change noise gate gain via bit1~ bit0. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, x0). User can select fade out or not via bit 4.

AD83584D provides a new modulation scheme, delta quaternary.
At zero input, it is like quaternary and will have PWM in A side and B side, but not 50% duty.
It will have smaller inrush current when power up.

At large input, it is like ternary, but the difference is both A side and B side have PWM.
It will have better performance than ternary.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	X	Reserved		
B[6]	A_SEL_FAULT	I2C address selection or ERROR output	0	I2C device address selection
			1	ERROR output
B[5]	D_MOD	Delta quaternary modulation	0	Disable
			1	enable
B[4]	DIS_NG_FADE	Disable noise gate fade	0	Fade
			1	No fade
B[3:2]	X	Reserved		
B[1:0]	NG_GAIN[1:0]	Noise gate gain	00	x1/8
			01	x1/4
			10	x1/2
			11	Mute

- Address 0X14 ~0X24 : User-defined coefficients registers

An on-chip RAM in AD83584D stores user-defined EQ and mixing coefficients. The content of this coefficient RAM is indirectly accessed via coefficient registers, which consist of one base address register (address 0X14), five sets of registers (address 0X15 to 0X23) of three consecutive 8-bit entries for each 24-bit coefficient, and one control register (address 0X24) to control access of the coefficients in the RAM..

Address 0X14

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6:0]	CFA[6:0]	Coefficient RAM base address	0000000	

Address 0X15, A1cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[23:16]	Top 8-bits of coefficients A1		

Address 0X16, A1cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[15:8]	Middle 8-bits of coefficients A1		

Address 0X17, A1cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[7:0]	Bottom 8-bits of coefficients A1		

Address 0X18, A2cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[23:16]	Top 8-bits of coefficients A2		

Address 0X19, A2cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[15:8]	Middle 8-bits of coefficients A2		

Address 0X1A, A2cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[7:0]	Bottom 8-bits of coefficients A2		

Address 0X1B, B1cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[23:16]	Top 8-bits of coefficients B1		

Address 0X1C, B1cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[15:8]	Middle 8-bits of coefficients B1		

Address 0X1D, B1cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[7:0]	Bottom 8-bits of coefficients B1		

Address 0X1E, B2cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[23:16]	Top 8-bits of coefficients B2		

Address 0X1F, B2cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[15:8]	Middle 8-bits of coefficients B2		

Address 0X20, B2cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[7:0]	Bottom 8-bits of coefficients B2		

Address 0X21, A0cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[23:16]	Top 8-bits of coefficients A0		

Address 0X22, A0cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[15:8]	Middle 8-bits of coefficients A0		

Address 0X23, A0cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[7:0]	Bottom 8-bits of coefficients A0		

Address 0X24, CfRW

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3]	RA	Enable of reading a set of coefficients from RAM	0	Read complete
			1	Read enable
B[2]	R1	Enable of reading a single coefficients from RAM	0	Read complete
			1	Read enable
B[1]	WA	Enable of writing a set of coefficients to RAM	0	Write complete
			1	Write enable
B[0]	W1	Enable of writing a single coefficient to RAM	0	Write complete
			1	Write enable

- Address 0X2A : Power saving mode switching level

If the PWM exceeds the programmed switching power level (default 26*40ns), the modulation algorithm will change from quaternary or delta quaternary into power saving mode (ternary). It results in higher power efficiency during larger power output operations. If the PWM drops below the programmed switching power level - programmed switching window (default (26-5)*40ns), the modulation algorithm will change back to quaternary or delta quaternary modulation.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	SW_WINDOW	Power saving mode switching window	111	9
			110	8
			101	7
			100	6
			011	5
			010	4
			001	3
			000	2
B[4:0]	QT_SW_LEVEL	Power saving mode switching level	11111	62
			11110	60
			:	:
			10000	32
			01111	30
			01110	28
			01101	26
			:	:
			00001	4
			00000	4

Note: QT_SW_LEVEL should be larger than SW_WINDOW.

- Address 0X2B : Volume fine tune

AD83584D supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MV_FT	Master Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C1V_FT	Channel 1 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C2V_FT	Channel 2 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]	C3V_FT	Channel 3 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB

- RAM access

The procedure to read/write coefficient(s) from/to RAM is as followings:

Read a single coefficient from RAM:

1. Write 7-bis of address to I2C address-0X14
2. Write 1 to R1 bit in address-0X24
3. Read top 8-bits of coefficient in I2C address-0X15
4. Read middle 8-bits of coefficient in I2C address-0X16
5. Read bottom 8-bits of coefficient in I2C address-0X17

Read a set of coefficients from RAM:

1. Write 7-bits of address to I2C address-0X14
2. Write 1 to RA bit in address-0X24
3. Read top 8-bits of coefficient A1 in I2C address-0X15
4. Read middle 8-bits of coefficient A1in I2C address-0X16
5. Read bottom 8-bits of coefficient A1 in I2C address-0X17
6. Read top 8-bits of coefficient A2 in I2C address-0X18
7. Read middle 8-bits of coefficient A2 in I2C address-0X19
8. Read bottom 8-bits of coefficient A2 in I2C address-0X1A
9. Read top 8-bits of coefficient B1 in I2C address-0X1B
10. Read middle 8-bits of coefficient B1 in I2C address-0X1C
11. Read bottom 8-bits of coefficient B1 in I2C address-0X1D
12. Read top 8-bits of coefficient B2 in I2C address-0X1E
13. Read middle 8-bits of coefficient B2 in I2C address-0X1F
14. Read bottom 8-bits of coefficient B2 in I2C address-0X20
15. Read top 8-bits of coefficient A0 in I2C address-0X21
16. Read middle 8-bits of coefficient A0 in I2C address-0X22
17. Read bottom 8-bits of coefficient A0 in I2C address-0X23

Write a single coefficient from RAM:

1. Write 7-bis of address to I2C address-0X14
2. Write top 8-bits of coefficient in I2C address-0X15
3. Write middle 8-bits of coefficient in I2C address-0X16
4. Write bottom 8-bits of coefficient in I2C address-0X17
5. Write 1 to W1 bit in address-0X24

Write a set of coefficients from RAM:

1. Write 7-bits of address to I2C address-0X14
2. Write top 8-bits of coefficient A1 in I2C address-0X15
3. Write middle 8-bits of coefficient A1 in I2C address-0X16
4. Write bottom 8-bits of coefficient A1 in I2C address-0X17
5. Write top 8-bits of coefficient A2 in I2C address-0X18
6. Write middle 8-bits of coefficient A2 in I2C address-0X19
7. Write bottom 8-bits of coefficient A2 in I2C address-0X1A
8. Write top 8-bits of coefficient B1 in I2C address-0X1B
9. Write middle 8-bits of coefficient B1 in I2C address-0X1C
10. Write bottom 8-bits of coefficient B1 in I2C address-0X1D
11. Write top 8-bits of coefficient B2 in I2C address-0X1E
12. Write middle 8-bits of coefficient B2 in I2C address-0X1F
13. Write bottom 8-bits of coefficient B2 in I2C address-0X20
14. Write top 8-bits of coefficient A0 in I2C address-0X21
15. Write middle 8-bits of coefficient A0 in I2C address-0X22
16. Write bottom 8-bits of coefficient A0 in I2C address-0X23
17. Write 1 to WA bit in address-0X24

Note that: the read and write operation on RAM coefficients works only if LRCIN (pin-15) switching on rising edge. And, before each writing operation, it is necessary to read the address-0X24 to confirm whether RAM is writable current in first. If the logic of W1 or WA is high, the coefficient writing is prohibited.

- User-defined equalizer

The AD83584D provides 20 parametric Equalizer (EQ). Users can program suitable coefficients via I^2C control interface to program the required audio band frequency response for every EQ. The transfer function

$$H(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 + B_1 z^{-1} + B_2 z^{-2}}$$

The data format of 2's complement binary code for EQ coefficient is 3.21. i.e., 4-bits for integer (MSB is the sign bit) and 21-bits for mantissa. Each coefficient range is from 0x800000 (-4) to 0x7FFFFF (+3.999999523). These coefficients are stored in User Defined RAM and are referenced in following manner:

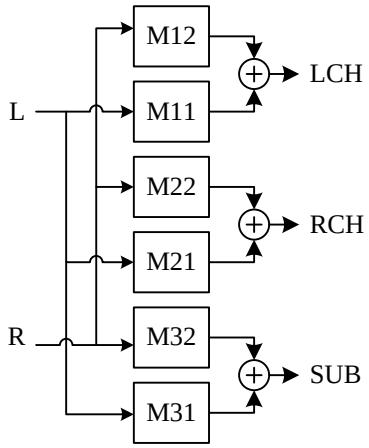
$$CHxEQyA0 = A0$$
$$CHxEQyA1 = A1$$
$$CHxEQyA2 = A2$$
$$CHxEQyB1 = -B1$$
$$CHxEQyB2 = -B2$$

Where *x* and *y* represents the number of channel and the band number of EQ biquard.

All user-defined filters are path-through, where all coefficients are defaulted to 0 after being powered up, except the A0 that is set to 0x200000 which represents 1.

- Mixer

The AD83584D provides mixers to generate the extra audio source from the input left and right channels. The coefficients of mixers are defined in range from 0x800000 (-1) to 0x7FFFFF (0.9999998808). The function block diagram is as following:



- Pre-scale

For each audio channel, AD83584D can scale input signal level prior to EQ processing which is realized by a 24-bit signed fractional multiplier. The pre-scale factor, ranging from -1 (0x800000) to 0.9999998808 (0x7FFFFF), for this multiplier, can be loaded into RAM. The default values of the pre-scaling factors are set to 0x7FFFFF. Programming of RAM is described in RAM access.

- Post-scale

The AD83584D provides an additional multiplication after equalizing and before interpolation stage, which is realized by a 24-bit signed fractional multiplier. The post-scaling factor, ranging from -1 (0x800000) to 0.9999998808 (0x7FFFFF), for this multiplier, can be loaded into RAM. The default values of the post-scaling factors are set to 0x7FFFFF. All channels can use the channel-1 post-scale factor by setting the post-scale link. Programming of RAM is described in RAM access.

- Power Clipping

The AD83584D provides power clipping function to avoid excessive signal that may destroy loud speaker. Two sets of power clipping are provided. One is used for both channel 1 and channel 2, while the other is used for channel 3. The power clipping level is defined by 24-bit representation and is stored in RAM address 0X6F and 0X70. The following table shows the power clipping level's numerical representation.

Sample calculation for power clipping

Max amplitude	dB	Linear	Decimal	Hex (3.21 format)
PVDD	0	1	2097152	200000
PVDD*0.707	-3	0.707	1482686	169FBE
PVDD*0.5	-6	0.5	1048576	100000
PVDD*L	x	$L=10^{(x/20)}$	D=2097152xL	H=dec2hex(D)

- Attack threshold

The AD83584D provides power limited function. When the input RMS exceeds the programmable attack threshold value, the output power will be limited by this threshold power level via gradual gain reduction. Two sets of power limit are provided. One is used of channel 1 and channel 2, while the other is used for channel3.Attack threshold is defined by 24-bit representation and is stored in RAM address 0X71 and 0X72.

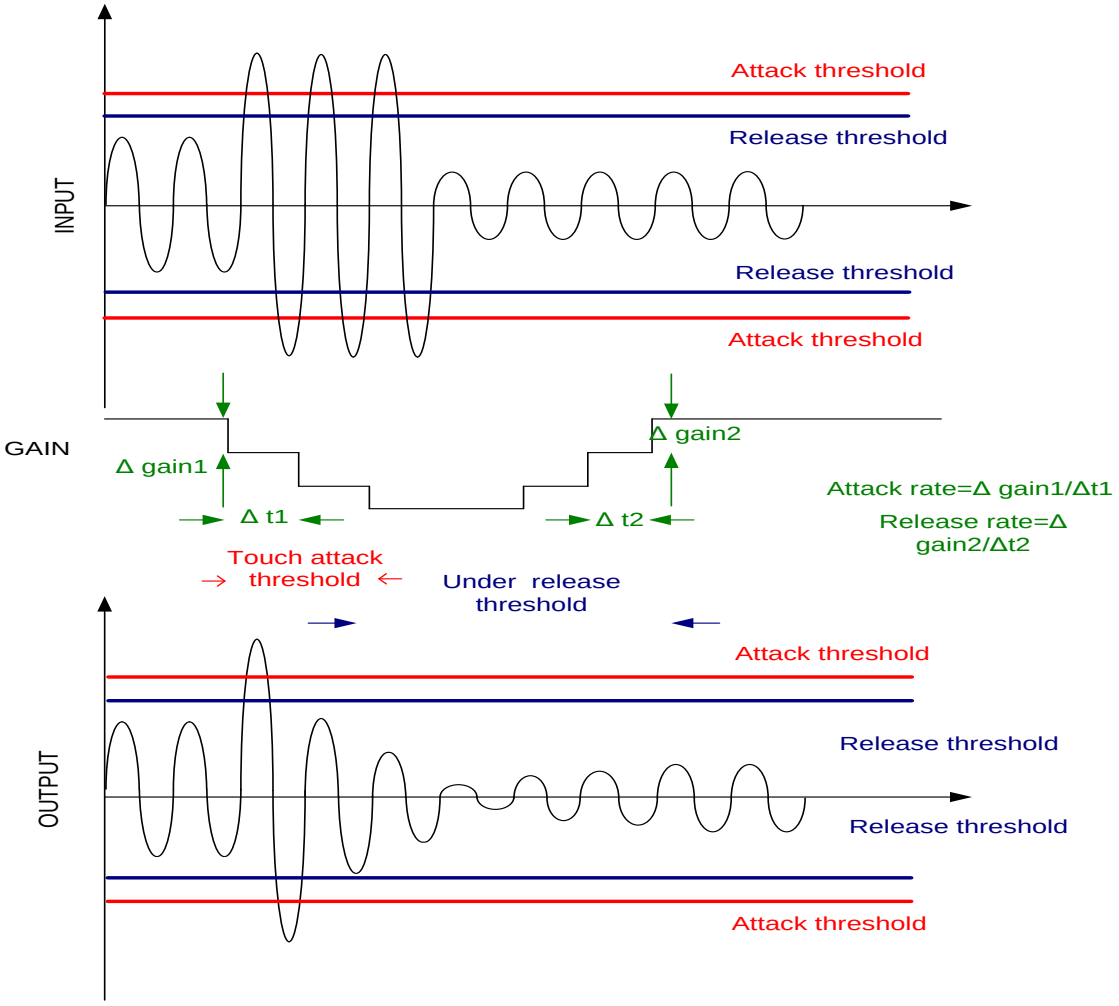
- Release threshold

After AD83584D has reached the attack threshold, its output power will be limited to that level. The output power level will be gradually adjusted to the programmable release threshold level. Two sets of power limit are provided. One is used of channel 1 and channel 2, while the other is used for channel3. Release threshold is defined by 24-bit representation and is stored in RAM address 0X73 and 0X74. The following table shows the attack and release threshold's numerical representation.

Sample calculation for attack and release threshold

Power	dB	Linear	Decimal	Hex (3.21 format)
(PVDD^2)/R	0	1	2097152	200000
(PVDD^2)/2R	-3	0.5	1048576	100000
(PVDD^2)/4R	-6	0.25	524288	80000
((PVDD^2)/R)*L	x	$L=10^{(x/10)}$	D=2097152xL	H=dec2hex(D)

To best illustrate the power limit function, please refer to the following figure.



- Noise Gate Attack Level

When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or zero if the noise gate function is enabled. Noise gate attack level is defined by 24-bit representation and is stored in RAM address 0X75.

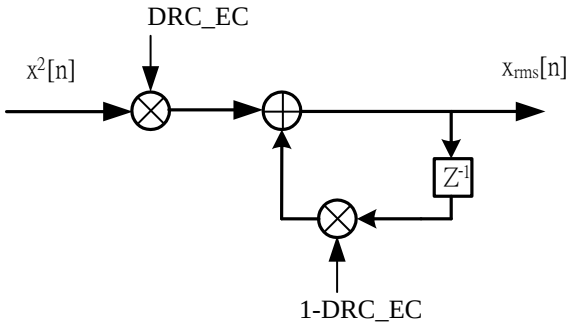
- Noise Gate Release Level

After entering the noise gating status, the noise gain will be removed whenever AD83584D receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 24-bit representation and is stored in RAM address 0X76. The following table shows the noise gate attack and release threshold level's numerical representation.

Sample calculation for noise gate attack and release level

Input amplitude (dB)	Linear	Decimal	Hex (1.23 format)
0	1	8388607	7FFFFF
-100	10^{-5}	83	53
-110	$10^{-5.5}$	26	1A
x	$L=10^{(x/20)}$	D=8388607xL	H=dec2hex(D)

- DRC Energy Coefficient



The above figure illustrates the digital processing of calculating RMS signal power. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Two sets of energy coefficients are provided. One is used of channel 1 and channel 2, while the other is used for channel3. Energy coefficient is defined by 24-bit representation and is stored in RAM address 0X77 and 0X78. The following table shows the DRC energy coefficient numerical representation.

Sample calculation for DRC energy coefficient

DRC energy coefficient	dB	Linear	Decimal	Hex (1.23 format)
1	0	1	8388607	7FFFFF
1/256	-48.2	1/256	32768	8000
1/1024	-60.2	1/1024	8192	2000
L	x	$L=10^{(x/20)}$	D=8388607xL	H=dec2hex(D)

The user defined RAM

The contents of user defined RAM is represented in following table.

Address	NAME	Coefficient	Default
0x00	Channel-1 EQ1	CH1EQ1A1	0x000000
0x01		CH1EQ1A2	0x000000
0x02		CH1EQ1B1	0x000000
0x03		CH1EQ1B2	0x000000
0x04		CH1EQ1A0	0x200000
0x05	Channel-1 EQ2	CH1EQ2A1	0x000000
0x06		CH1EQ2A2	0x000000
0x07		CH1EQ2B1	0x000000
0x08		CH1EQ2B2	0x000000
0x09		CH1EQ2A0	0x200000
0x0A	Channel-1 EQ3	CH1EQ3A1	0x000000
0x0B		CH1EQ3A2	0x000000
0x0C		CH1EQ3B1	0x000000
0x0D		CH1EQ3B2	0x000000
0x0E		CH1EQ3A0	0x200000
0x0F	Channel-1 EQ4	CH1EQ4A1	0x000000
0x10		CH1EQ4A2	0x000000
0x11		CH1EQ4B1	0x000000
0x12		CH1EQ4B2	0x000000
0x13		CH1EQ4A0	0x200000
0x14	Channel-1 EQ5	CH1EQ5A1	0x000000
0x15		CH1EQ5A2	0x000000
0x16		CH1EQ5B1	0x000000
0x17		CH1EQ5B2	0x000000
0x18		CH1EQ5A0	0x200000
0x19	Channel-1 EQ6	CH1EQ6A1	0x000000
0x1A		CH1EQ6A2	0x000000
0x1B		CH1EQ6B1	0x000000
0x1C		CH1EQ6B2	0x000000
0x1D		CH1EQ6A0	0x200000
0x1E	Channel-1 EQ7	CH1EQ7A1	0x000000
0x1F		CH1EQ7A2	0x000000
0x20		CH1EQ7B1	0x000000

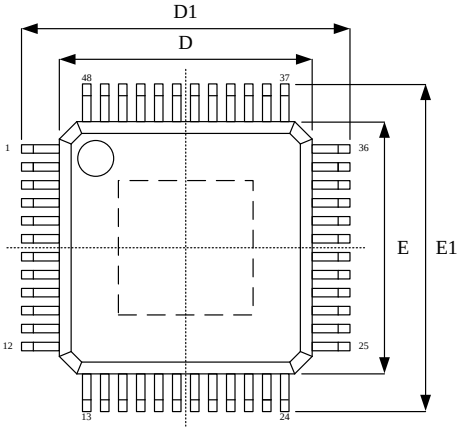
0x21		CH1EQ7B2	0x000000
0x22		CH1EQ7A0	0x200000
0x23	Channel-1 EQ8	CH1EQ8A1	0x000000
0x24		CH1EQ8A2	0x000000
0x25		CH1EQ8B1	0x000000
0x26		CH1EQ8B2	0x000000
0x27		CH1EQ8A0	0x200000
0x28	Channel-3 EQ1	CH3EQ1A1	0x000000
0x29		CH3EQ1A2	0x000000
0x2A		CH3EQ1B1	0x000000
0x2B		CH3EQ1B2	0x000000
0x2C		CH3EQ1A0	0x200000
0x2D	Channel-3 EQ3	CH3EQ3A1	0x000000
0x2E		CH3EQ3A2	0x000000
0x2F		CH3EQ3B1	0x000000
0x30		CH3EQ3B2	0x000000
0x31		CH3EQ3A0	0x200000
0x32	Channel-2 EQ1	CH2EQ1A1	0x000000
0x33		CH2EQ1A2	0x000000
0x34		CH2EQ1B1	0x000000
0x35		CH2EQ1B2	0x000000
0x36		CH2EQ1A0	0x200000
0x37	Channel-2 EQ2	CH2EQ2A1	0x000000
0x38		CH2EQ2A2	0x000000
0x39		CH2EQ2B1	0x000000
0x3A		CH2EQ2B2	0x000000
0x3B		CH2EQ2A0	0x200000
0x3C	Channel-2 EQ3	CH2EQ3A1	0x000000
0x3D		CH2EQ3A2	0x000000
0x3E		CH2EQ3B1	0x000000
0x3F		CH2EQ3B2	0x000000
0x40		CH2EQ3A0	0x200000
0x41	Channel-2 EQ4	CH2EQ4A1	0x000000
0x42		CH2EQ4A2	0x000000
0x43		CH2EQ4B1	0x000000
0x44		CH2EQ4B2	0x000000
0x45		CH2EQ4A0	0x200000

0x46	Channel-2 EQ5	CH2EQ5A1	0x000000
0x47		CH2EQ5A2	0x000000
0x48		CH2EQ5B1	0x000000
0x49		CH2EQ5B2	0x000000
0x4A		CH2EQ5A0	0x200000
0x4B	Channel-2 EQ6	CH2EQ6A1	0x000000
0x4C		CH2EQ6A2	0x000000
0x4D		CH2EQ6B1	0x000000
0x4E		CH2EQ6B2	0x000000
0x4F		CH2EQ6A0	0x200000
0x50	Channel-2 EQ7	CH2EQ7A1	0x000000
0x51		CH2EQ7A2	0x000000
0x52		CH2EQ7B1	0x000000
0x53		CH2EQ7B2	0x000000
0x54		CH2EQ7A0	0x200000
0x55	Channel-2 EQ8	CH2EQ8A1	0x000000
0x56		CH2EQ8A2	0x000000
0x57		CH2EQ8B1	0x000000
0x58		CH2EQ8B2	0x000000
0x59		CH2EQ8A0	0x200000
0x5A	Channel-3 EQ2	CH3EQ2A1	0x000000
0x5B		CH3EQ2A2	0x000000
0x5C		CH3EQ2B1	0x000000
0x5D		CH3EQ2B2	0x000000
0x5E		CH3EQ2A0	0x200000
0x5F	Channel-3 EQ4	CH3EQ4A1	0x000000
0x60		CH3EQ4A2	0x000000
0x61		CH3EQ4B1	0x000000
0x62		CH3EQ4B2	0x000000
0x63		CH3EQ4A0	0x200000
0x64	Channel-1 Mixer1	M11	0x7FFFFF
0x65	Channel-1 Mixer2	M12	0x000000
0x66	Channel-2 Mixer1	M21	0x000000
0x67	Channel-2 Mixer2	M22	0x7FFFFF
0x68	Channel-3 Mixer1	M31	0x400000
0x69	Channel-3 Mixer2	M32	0x400000
0x6A	Channel-1 Prescale	C1PRS	0x7FFFFF

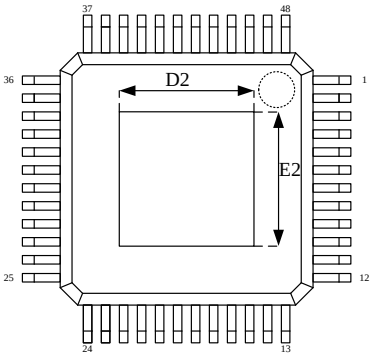
0x6B	Channel-2 Prescale	C2PRS	0x7FFFFF
0x6C	Channel-1 Postscale	C1POS	0x7FFFFF
0x6D	Channel-2 Postscale	C2POS	0x7FFFF
0x6E	Channel-3 Postscale	C3POS	0x7FFFFF
0x6F	CH1.2 Power Clipping	PC1	0x200000
0x70	CH3 Power Clipping	PC2	0x200000
0x71	CH1.2 DRC Attack threshold	DRC1_ATH	0x200000
0x72	CH1.2 DRC Release threshold	DRC1_RTH	0x80000
0x73	CH3 DRC Attack threshold	DRC2_ATH	0x200000
0x74	CH3 DRC Release threshold	DRC2_RTH	0x80000
0x75	Noise Gate Attack Level	NGAL	0x00001A
0x76	Noise Gate Release Level	NGRL	0x000053
0x77	DRC1 Energy Coefficient	DRC1_EC	0x8000
0X78	DRC2 Energy Coefficient	DRC2_EC	0x2000

Package Dimensions

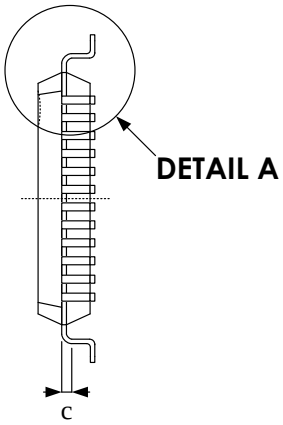
E-LQFP-48L (7mm x 7mm)

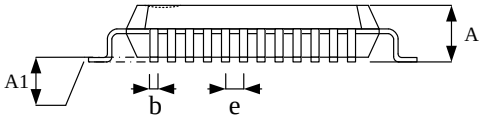


TOP VIEW

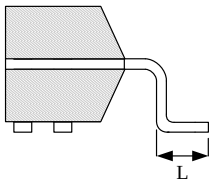


BOTTOM VIEW





SIDE VIEW



DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.17	0.27
c	0.09	0.20
D	6.90	7.10
D1	8.90	9.10
E	6.90	7.10
E1	8.90	9.10
e	0.50 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	4.31	5.21
E2	4.31	5.21

Revision History

Revision	Date	Description
0.1	2014.10.03	Original.
0.2	2014.11.27	1. Modify the description of address 0X01. 2. Modify the snubbers of Application Circuit Example. 3. Modify the power on / off sequence.
0.3	2015.02.03	Modify the output power for stereo, mono and 2.1CH.
1.0	2015.02.16	1. Remove preliminary word and modify version to 1.0. 2. Modify pin assignment.
1.1	2015.12.02	Update for the pin description of CLK_OUT.
1.2	2016.04.18	1. Remove DRC Mode. 2. Add Class-D HVUV range information into.
1.3	2016.06.29	Add packing code in ordering information table.
1.4	2016.08.10	1. Modify the Range of Recommend PVDD. 2. Update for the pin description of CLK_OUT. 3. Add note for power saving mode 4. Update figure for power limit. 5. Remove packing code in ordering information table.
1.5	2016.11.22	1. Modify the condition of System Clock Timing in Interface configuration. 2. Add a Note in Power on sequence.
1.6	2018.08.23	1. Update minimum load resistance information in AMR. 2. Update the level of over-current protection at 12V in General Electrical Characteristics.

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