2x60W Stereo / 1x120W Mono / 2x30W+1x60W 2.1CH Digital Audio Amplifier with 36 bands EQ and DRC Functions

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment and TDM data format
- PSNR & DR(A-weighting)
  Loudspeaker: 130dB (PSNR), 106dB (DR)@24V
- Multiple sampling frequencies (Fs)
  8kHz, 16kHz and 32kHz / 44.1kHz / 48kHz and 88.2k / 96kHz
- System clock = 32x,48x, 64x,96x, 128x,192x, 256x, 384x, 512 Fs
  MCLK system:
  32x~512x Fs for 8kHz, 16kHz and 32kHz / 44.1kHz / 48kHz and 88.2kHz / 96kHz
  BCLK system:
  32x~256x Fs for 8kHz, 16kHz and 32kHz / 44.1kHz / 48kHz and 88.2kHz / 96kHz
- Supply voltage
  3.3V for digital circuit
  1.65~3.6V for DVDDIO
  4.5V~26V for loudspeaker driver
- Speaker peak output power at 24V
  60W x 2CH into 4Ω @ 0.4% THD+N
  120W x 1CH into 2Ω @ 0.9% THD+N
- Speaker peak output power for 2.1CH at 24V
  30W x 2CH into 8Ω @ 0.3% THD+N
  60W x 1CH into 4Ω @ 0.4% THD+N
- Sound processing including：
  36 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  DRC, AGC and Power Clipping
  Programmed 3D surround sound
  Channel mixing
  Compensate filter
  DC-blocking high-pass filter
  Pre-scale/post-scale
  I^2S output with user programmed gain
  Crossover filter for twitter and woofer
- Anti-pop design
- Power meter
- I^2S output with selectable Audio DSP point
- Short circuit and over-temperature protection
- Supports I^2C control without clock
- I^2C control with 4 selectable device address
- Support hardware and software reset
- Internal PLL
- LV & HV Under-voltage detection
- Over voltage protection
- Auto clock detection
- Power saving mode
- DTC

Applications

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

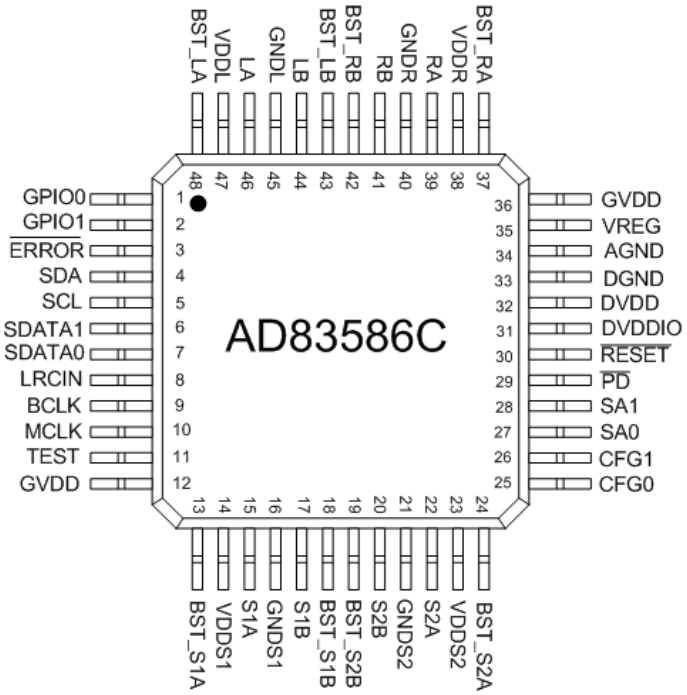
Description

AD83586C is a digital audio amplifier capable of driving a pair of 8Ω, 25W (30W peak) plus a single 4Ω, 50W (60W peak), or a pair of 4Ω, 50W (60W peak) or a single 2Ω, 100W (120W peak) speaker operating at 24V supply with proper cooling method.

AD83586C can provide advanced audio processing capabilities, such as volume control, 36 bands speaker EQ, audio mixing, 3D surround and Dynamic Range Control (DRC). These functions are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD83586C from damage due to accidental erroneous operating condition. AD83586C is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. AD83586C is pop free during instantaneous power switch because of its built-in, robust anti-pop circuit.

The output stage is flexibly configurable for 2.1 channel, stereo or mono applications. Furthermore, it is possible to use two pieces of AD83586C to realize 5.1 channels for home theater applications.

Pin Assignment



Pin Description (E-LQFP 48L)

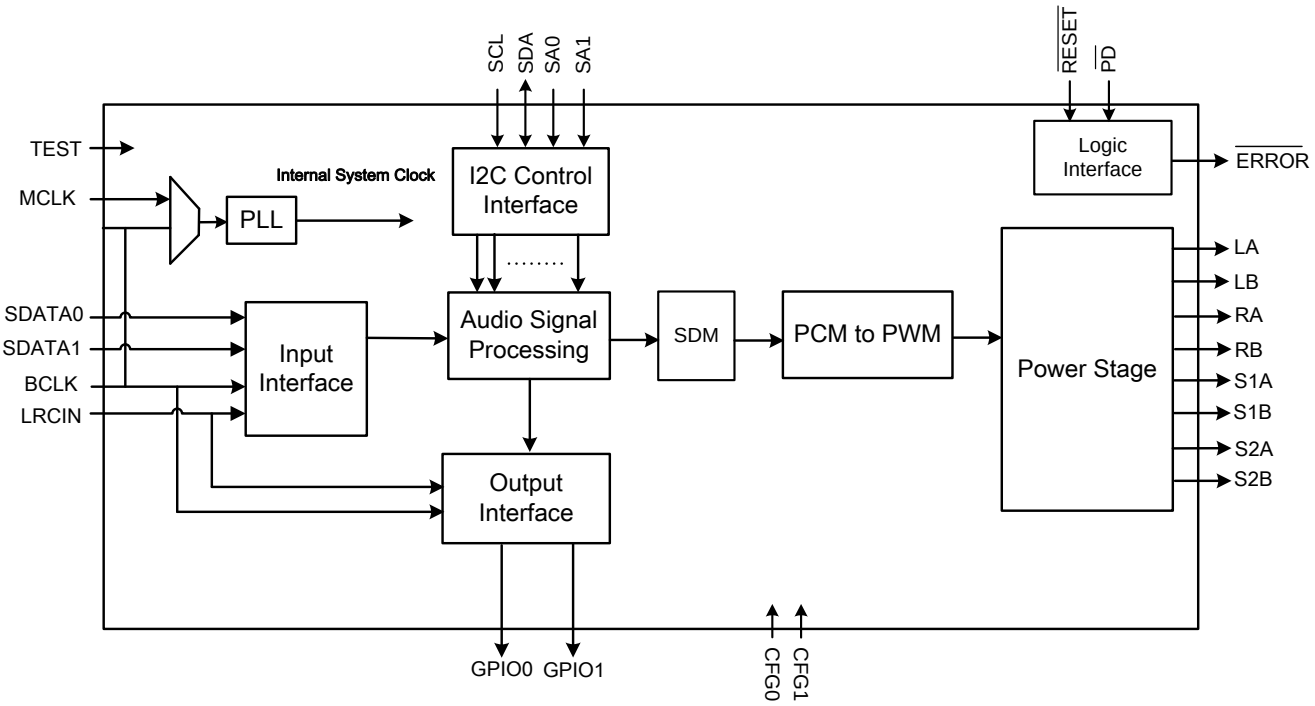
PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	GPIO0	DI/O	General purpose input0/output0.	
2	GPIO1	DI/O	General purpose input1/output1.	
3	$\overline{\text{ERROR}}$	DO	$\overline{\text{ERROR}}$ pin is an error status report (low active), It sets by register of A_SEL_FAULT at address 0x0C B[7] to enable it.	Schmitt trigger TTL input buffer.
4	SDA	DI/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer.
5	SCL	DI	I^2C serial clock input.	Schmitt trigger TTL input buffer.
6	SDATA1	DI	Serial audio data1 input.	Schmitt trigger TTL input buffer.
7	SDATA0	DI	Serial audio data0 input.	Schmitt trigger TTL input buffer.
8	LRCIN	DI	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
9	BCLK	DI	Bit clock input.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
10	MCLK	DI	Master clock input.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.

11	TEST	DI	This pin must connect to GND.	
12	GVDD	P	5V Regulator voltage output. This pin must not be used to drive external devices.	
13	BST_S1A	P	Bootstrap supply for sub channel1 output A.	
14	VDDS1	P	Sub1 channel supply.	
15	S1A	O	Sub1 channel output A.	
16	GNDS1	P	Sub1 channel ground.	
17	S1B	O	Sub1 channel output B.	
18	BST_S1B	P	Bootstrap supply for sub channel1 output B.	
19	BST_S2B	P	Bootstrap supply for sub channel2 output B.	
20	S2B	O	Sub2 channel output B.	
21	GNDS2	P	Sub2 channel ground.	
22	S2A	O	Sub2 channel output A.	
23	VDDS2	P	Sub2 channel supply.	
24	BST_S2B	P	Bootstrap supply for sub channel2 output A.	
25	CFG0	DI	Mono/Stereo/2.1 configuration pin.	
26	CFG1	DI	Mono/Stereo/2.1 configuration pin.	
27	SA0	DI	I^2C select address 0.	
28	SA1	DI	I^2C select address 1.	
29	$\overline{PD}$	DI	Power down, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
30	$\overline{RESET}$	DI	Reset, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
31	DVDDIO	P	Digital Power for I/O circuit.	
32	DVDD	P	Digital Power.	
33	DGND	P	Digital Ground.	
34	AGND.	P	Analog Ground.	
35	VREG	P	1.8V Regulator voltage output.	
36	GVDD	P	5V Regulator voltage output. This pin must not be used to drive external devices.	
37	BST_RA	P	Bootstrap supply for right channel output A.	
38	VDDR	P	Right channel supply.	
39	RA	O	Right channel output A.	
40	GNDR	P	Right channel ground.	
41	RB	O	Right channel output B.	

42	BST_RB	P	Bootstrap supply for right channel output B.	
43	BST_LB	P	Bootstrap supply for left channel output B.	
44	LB	O	Left channel output B.	
45	GNDL	P	Left channel ground.	
46	LA	O	Left channel output A.	
47	VDDL	P	Left channel supply.	
48	BST_LA	P	Bootstrap supply for left channel output A.	

Note: AI=Analog input; AO=Analog output; AI/O = Analog Bi-directional (input and output); DI=Digital Input; DO=Digital Output; DI/O = Digital Bi-directional (input and output); P=Power or Ground; O: PWM output

Functional Block Diagram



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD83586C-LG48NRY	E-LQFP 48L (7mmx7mm)	250 Units / Tray 2.5K Units / Box (10 Trays)	Green
AD83586C-LG48NRR		2K Units / Reel 1 Reel / Small box	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jt}(℃/W)	Exposed Thermal Pad
E-LQFP 48L	AD83586C	23.8	1.39	36.8	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja}, the junction-to-ambient thermal resistance is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The simulation is tested using the JESD51-5 thermal measurement standard.

Note 1.3: Ψ_{jt} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{ja}, using a procedure described in JESD51-2.

Note 1.4: θ_{jt} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

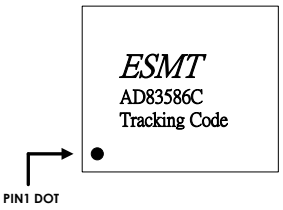
Marking Information

AD83586C

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code



Absolute Maximum Ratings (AMR)

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter		Min	Max	Units
DVDD	Supply for Digital Circuit		-0.3	3.6	V
DVDDIO	Supply for Digital I/O Circuit		-0.3	3.6	V
PVDD	Supply for Driver Stage (VDDL/VDDR/VDDS1/VDDS2)		-0.3	30	V
	Output Pin (LA/LB/RA/RB/S1A/S1B/S2A/S2B) to GND			32	V
V_i	Input Voltage		-0.3	3.6	V
T_{stg}	Storage Temperature		-65	150	°C
T_J	Junction Operating Temperature		-40	150	°C
ESD	Human Body Model			±2K	V
	Charged Device Model			±750	V
R_L	Minimum Load Resistance	BTL	4.8		Ω
		PBTL	3.2		Ω
		Two PBTL parallel	1.6		Ω

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.0~3.6	V
DVDDIO	Supply for Digital I/O Circuit for 1.8V	1.65~1.95	V
	Supply for Digital I/O Circuit for 3.3V	3.0~3.6	
PVDD	Supply for Driver Stage (VDDL/VDDR/VDDS1/VDDS2)	4.5~26	V
T_J	Junction Operating Temperature	-40~125	^oC
T_A	Ambient Operating Temperature	-40~85	^oC

General Electrical Characteristics

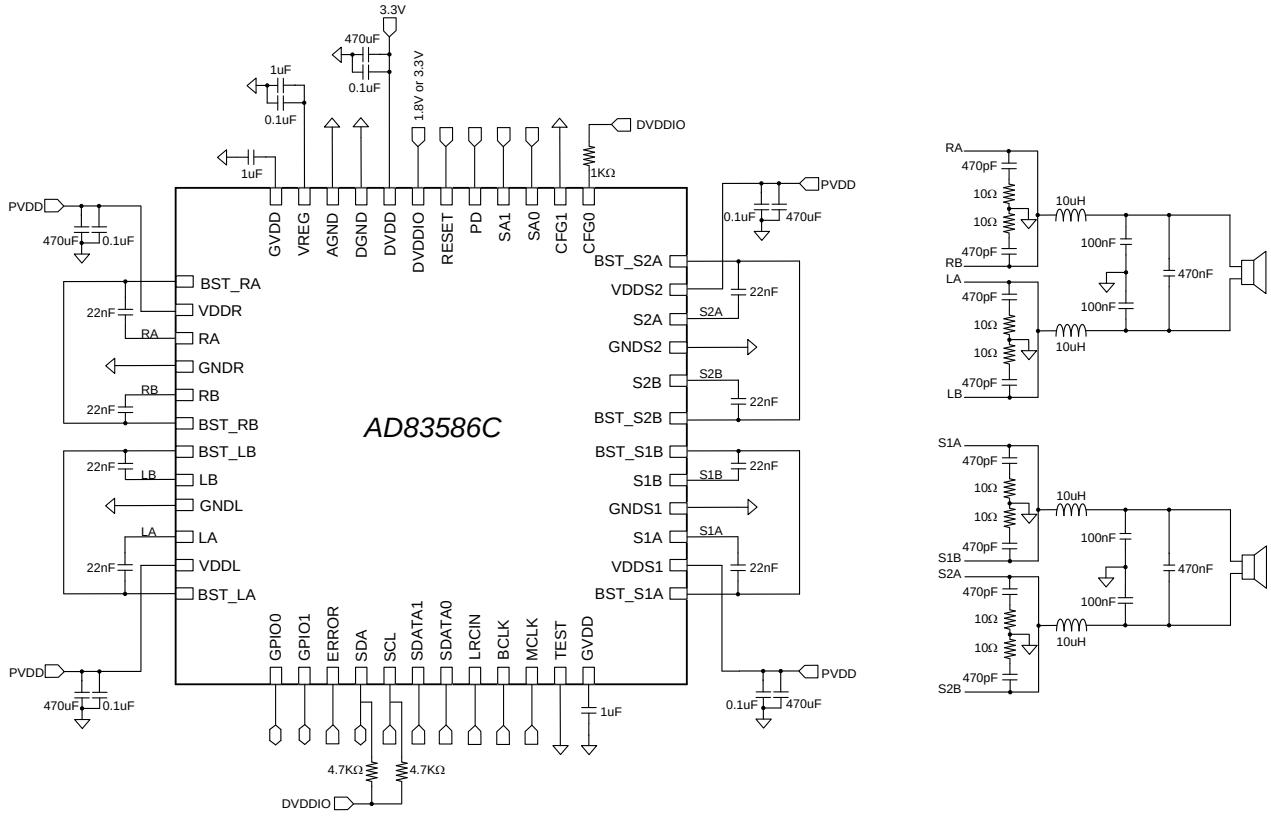
Condition: T_A=25 ^oC (unless otherwise specified).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}(HV)	PVDD Supply Current during Power Down	PVDD=24V		40		uA
I_Q(HV)	Quiescent current for PVDD (PWM duty in idle pulse)	PVDD=24V		40		mA
I_Q(LV)	Quiescent current for DVDD (Un-mute)	DVDD=3.3V, PBTL=Low		37		mA
T_{SENSOR}	Junction Temperature for Driver Shutdown			160		^oC
	Temperature Hysteresis for Recovery from Shutdown			35		^oC
UV_{DVDDH}	DVDD Under Voltage Release			2.99		V
UV_{DVDDL}	DVDD Under Voltage Active			2.89		V
UV_{PVDDH}	VDDL/VDDR/VDDS1/VDDS2 Under Voltage Release			4.23		V
UV_{PVDDL}	VDDL/VDDR/VDDS1/VDDS2 Under Voltage Active			4		V
OV_H	VDDL/VDDR/VDDS1/VDDS2 Over Voltage Active			29.2		V
OV_L	VDDL/VDDR/VDDS1/VDDS2 Under Voltage Release			28.5		V
$R_{DS(on)}$	Static Drain-to-Source On-state Resistor, NMOS	PVDD=24V, Id=500mA Not including bond wire and package resistance.		120		mΩ

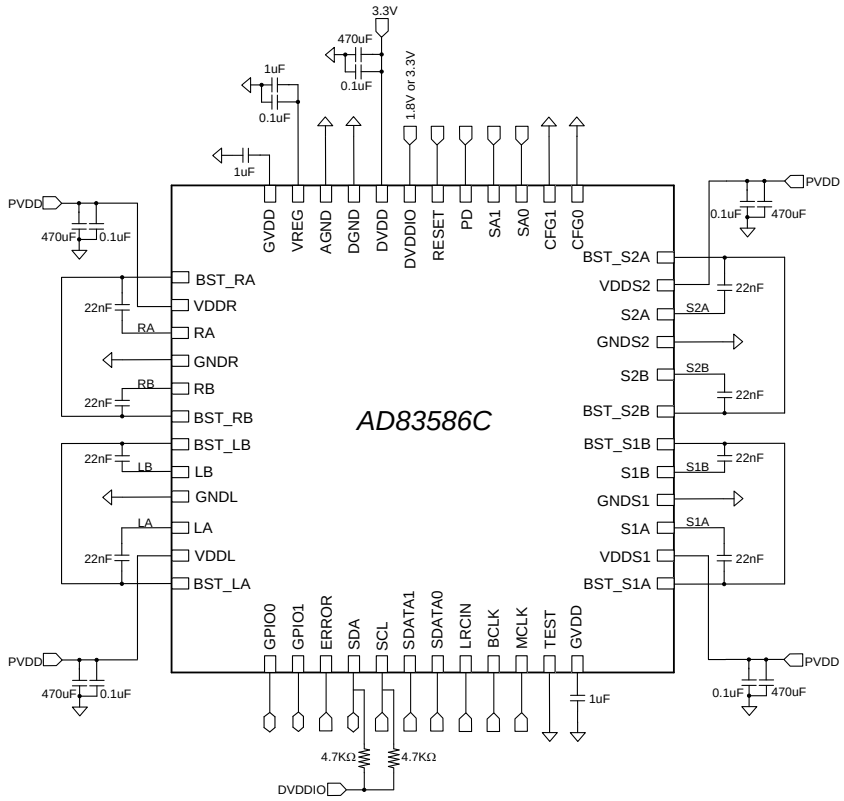
I_{SC}	L(R) Channel Over-Current Protection (Note 2)	PVDD=24V		9		A
		PVDD=12V		8.5		A
	Mono Over-Current Protection (Note 2)	PVDD=24V		18		A
		PVDD=12V		17		A
V_{IH}	High-Level Input Voltage for DVDD/DVDDIO	3.3V	2.0			V
	High-Level Input Voltage for DVDDIO	1.8V	1.26			V
V_{IL}	Low-Level Input Voltage for DVDD/DVDDIO	3.3V			0.8	V
	Low-Level Input Voltage for DVDDIO	1.8V			0.54	V
V_{OH}	High-Level Output Voltage for DVDD/DVDDIO	3.3V	2.4			V
	High-Level Output Voltage for DVDDIO	1.8V	1.44			V
V_{OL}	Low-Level Output Voltage for DVDD/DVDDIO	3.3V			0.4	V
	Low-Level Output Voltage for DVDDIO	1.8V			0.4	V
C_I	Input Capacitance			6.4		pF

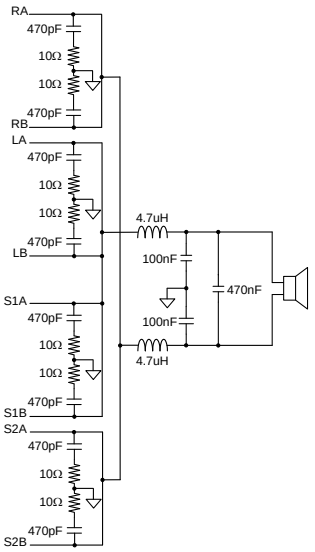
Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Application Circuit Example for Stereo

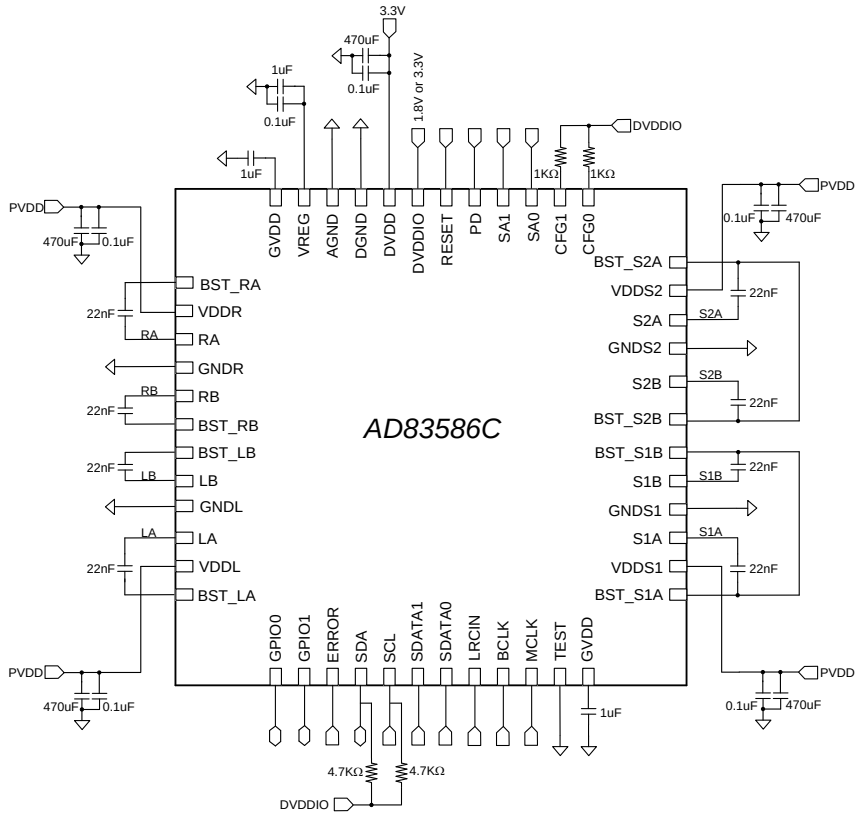


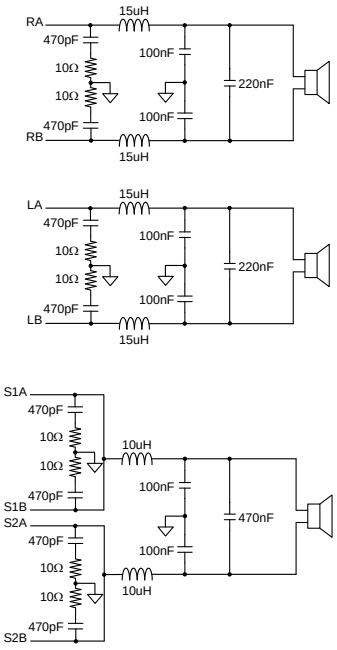
Application Circuit Example for Mono





Application Circuit Example for 2.1CH





Electrical Characteristics and Specifications for Loudspeaker

- **Stereo output (PBTL)**

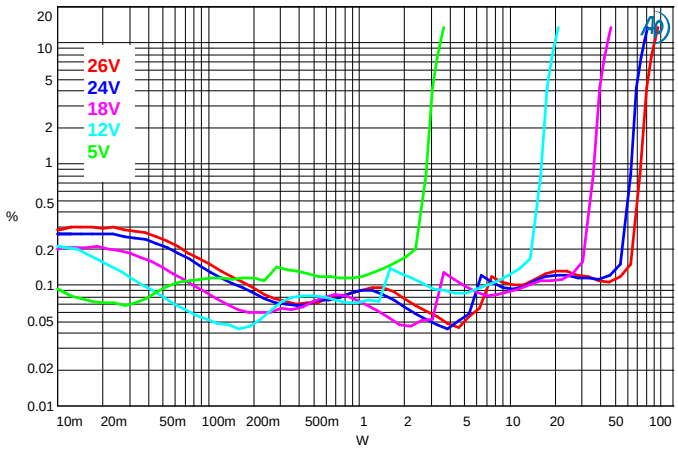
Condition: T_A=25°C, DVDD=3.3V, PVDD=24V, F_S=48kHz, Load=4Ω with passive LC low-pass filter (L=10μ H with R_{DC}=27mΩ , C=470nF); Input is 1kHz sine-wave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N=0.4%)	Instantaneous output power			60		W
	RMS Output Power (THD+N=0.18%)	Continuous output power			50		W
	RMS Output Power (THD+N=0.15%)				40		W
	RMS Output Power (THD+N=0.12%)				30		W
THD+N	Total Harmonic Distortion + Noise	P_O=25W			0.11		%
SNR	Signal to Noise Ratio (Note 8)	Maximum power at THD < 1% @1kHz			130		dB
DR	Dynamic Range (Note 8)		-60		102		dB
Vn	Output Noise (Note 8)	20Hz to 20kHz			5		uV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz			75		dB
X-talk	Channel Separation	1W @1kHz			97		dB

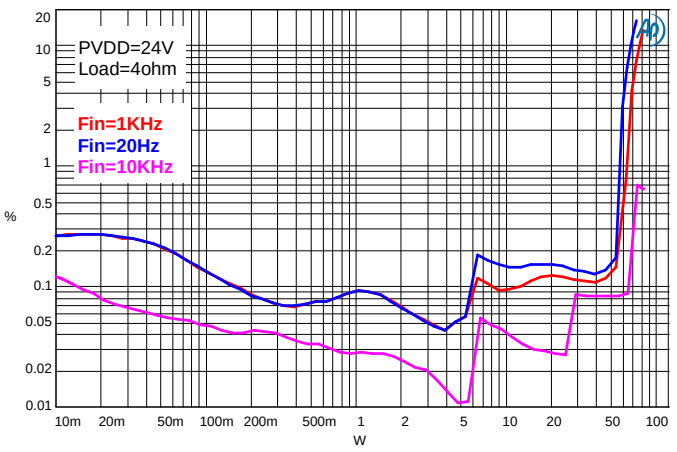
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

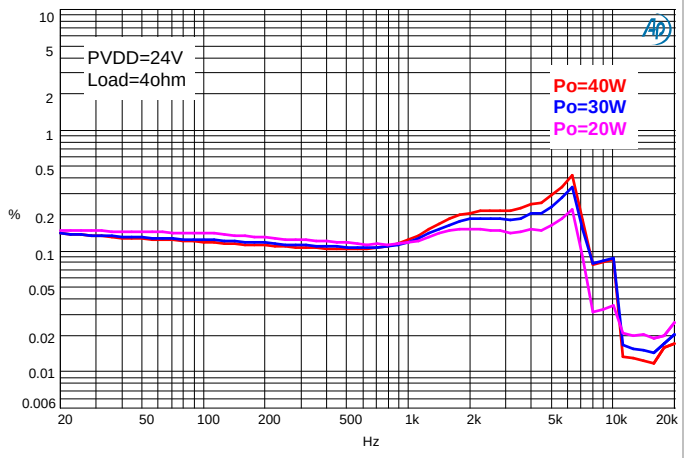
THD+N vs. Output Power, 4Ω load (PBTL)



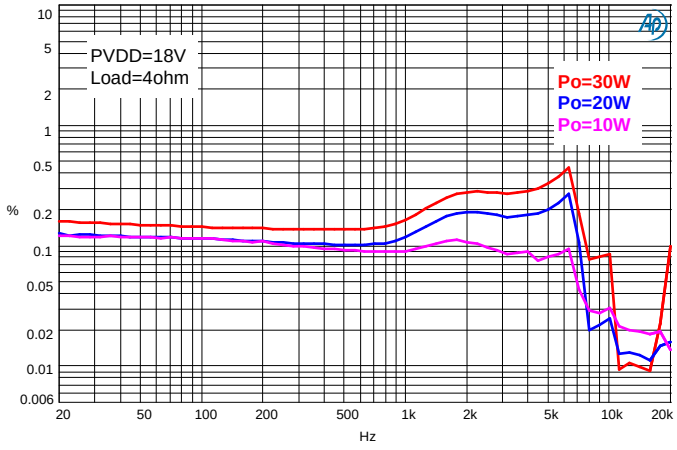
THD+N vs. Output Power, 4Ω load (PBTL)



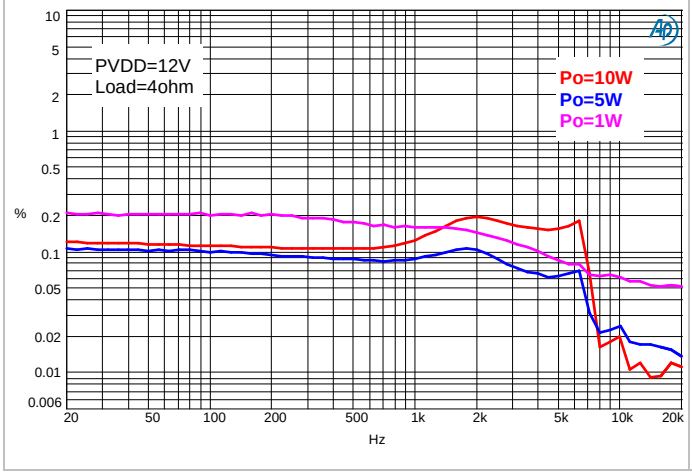
THD+N vs. Frequency, 4Ω load (PBTL)



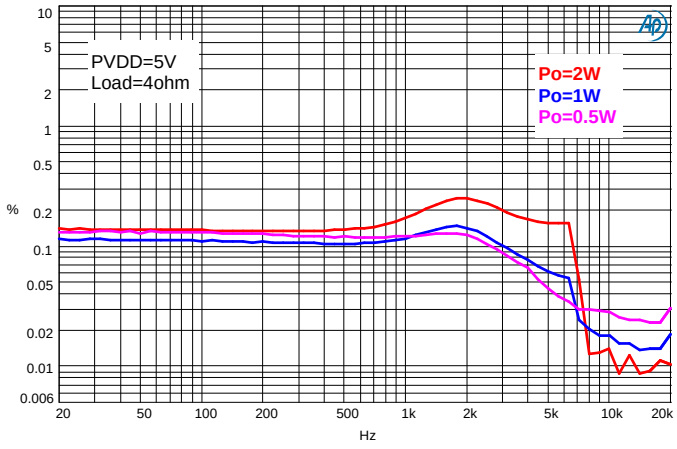
THD+N vs. Frequency, 4Ω load (PBTL)



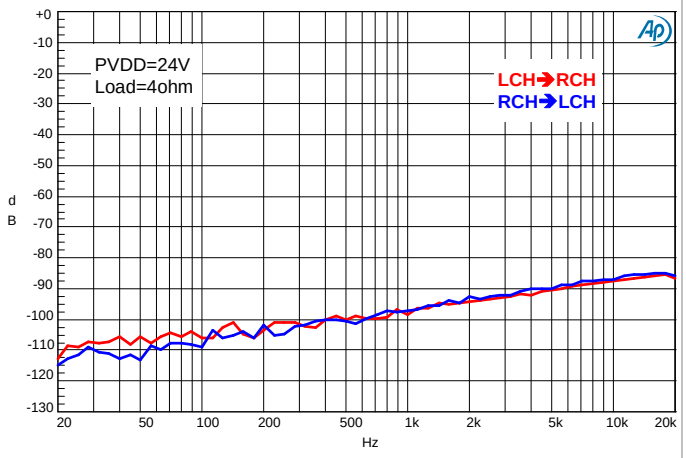
THD+N vs. Frequency, 4Ω load (PBTL)



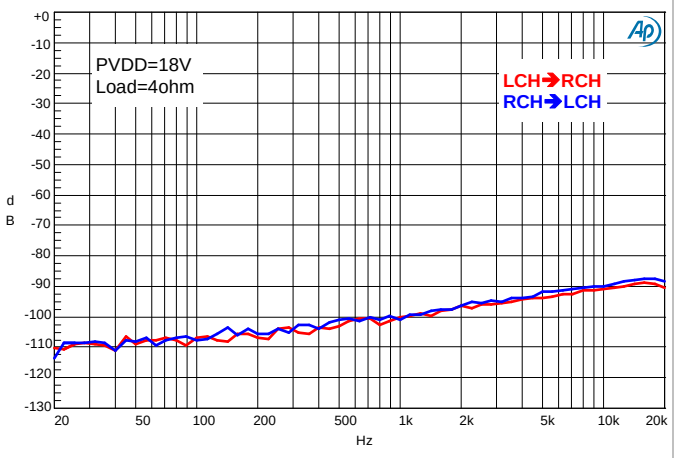
THD+N vs. Frequency, 4Ω load (PBTL)



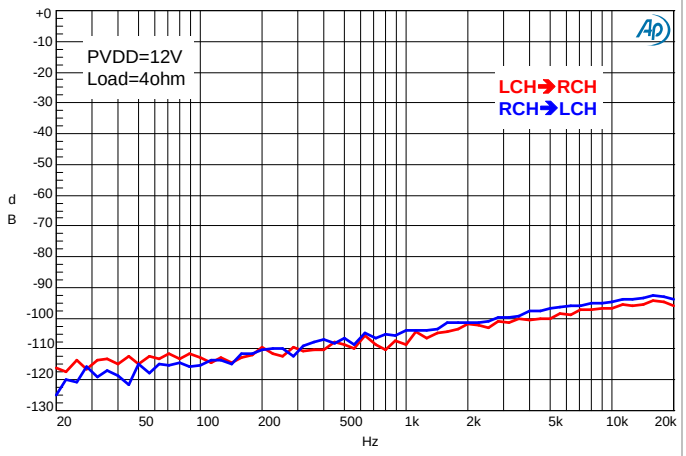
Crosstalk, 4Ω load (PBTL)



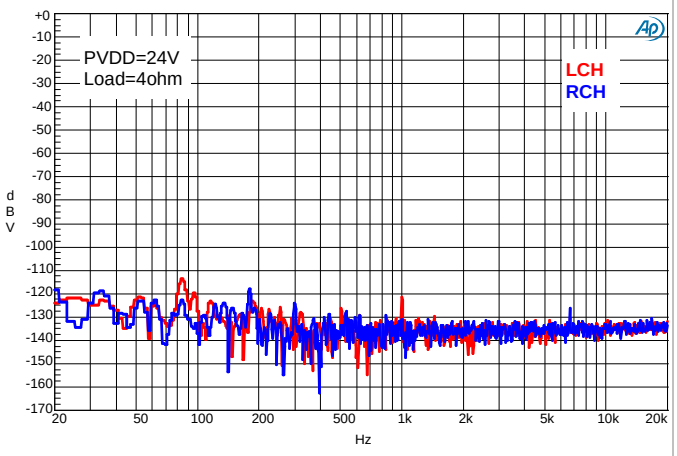
Crosstalk, 4Ω load (PBTL)



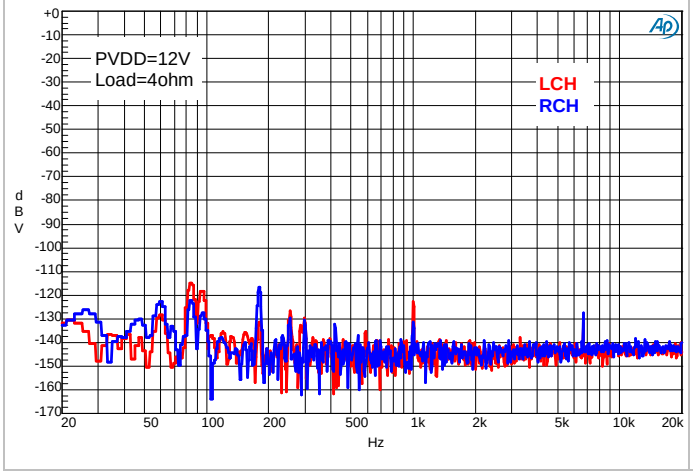
Crosstalk, 4Ω load (PBTL)



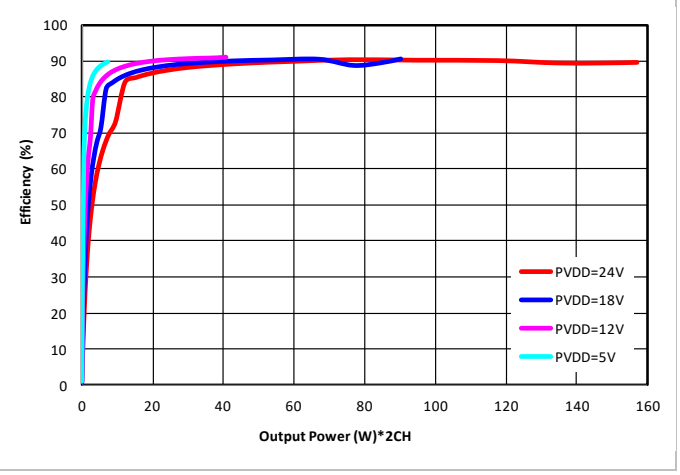
Noise FFT, 4Ω load (PBTL)



Noise FFT, 4Ω load (BTL)



Efficiency, 4Ω load (BTL)



Electrical Characteristics and Specifications for Loudspeaker (cont.)

- **MONO output (two PBTL parallel) output for Mono**

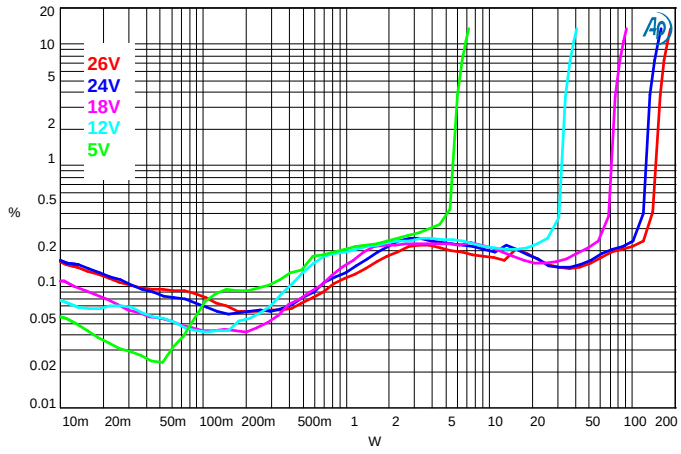
Condition: T_A=25°C, DVDD= 3.3V, PVDD=24V, F_S=48kHz, Load=2Ω with passive LC low-pass filter (L=4.7μ H with R_{DC}=8.4mΩ , C=470nF); Input is 1kHz sine-wave.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N=0.9%)	Instantaneous output power			120		W
	RMS Output Power (THD+N=0.24%)	Continuous output power			100		W
	RMS Output Power (THD+N=0.21%)				80		W
	RMS Output Power (THD+N=0.2%)				70		W
THD+N	Total Harmonic Distortion + Noise	P_o=50W			0.16		%
SNR	Signal to Noise Ratio (Note 8)	Maximum power at THD < 1% @1kHz			130		dB
DR	Dynamic Range (Note 8)		-60		106		dB
Vn	Output Noise (Note 8)	20Hz to 20kHz			5		uV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz			75		dB

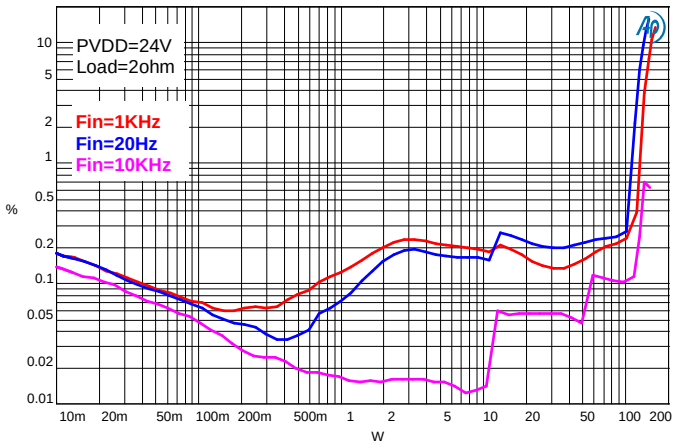
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

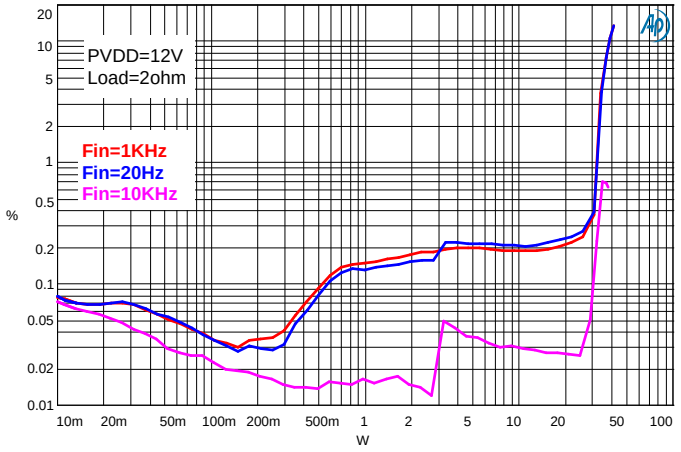
THD+N vs. Output Power, 2Ω load (Two PBTL Parallel)



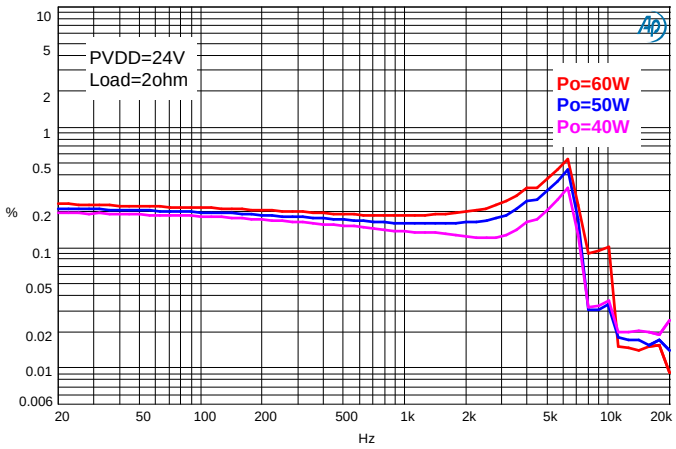
THD+N vs. Output Power, 2Ω load (Two PBTL Parallel)



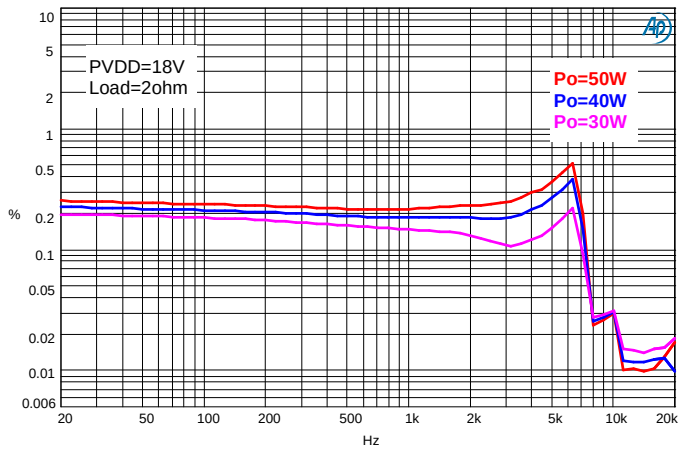
THD+N vs. Output Power, 2Ω load (Two PBTL Parallel)



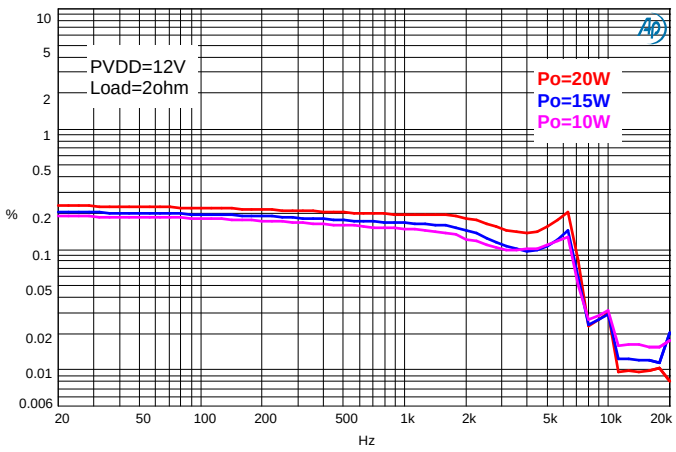
THD+N vs. Frequency, 2Ω load (Two PBTL Parallel)



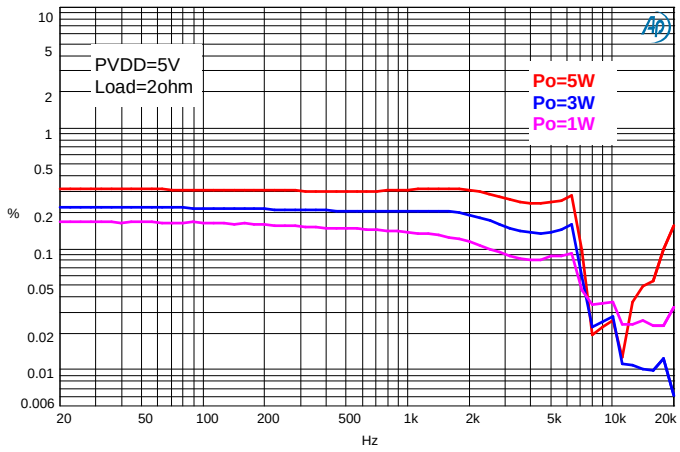
THD+N vs. Frequency, 2Ω load (Two PBTL Parallel)



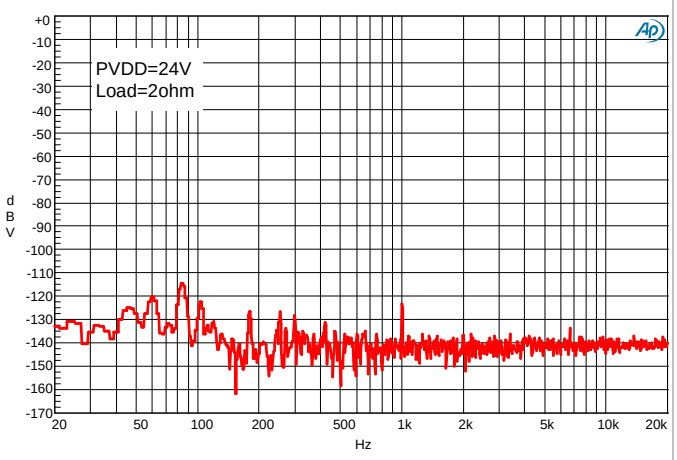
THD+N vs. Frequency, 2Ω load (Two PBTL Parallel)



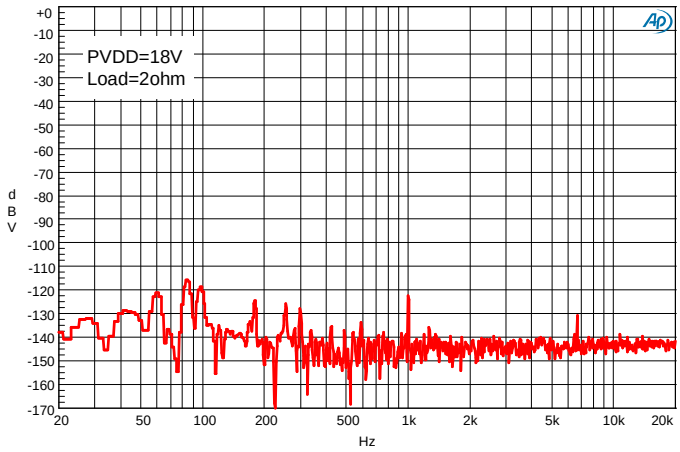
THD+N vs. Frequency, 2Ω load (Two PBTL Parallel)



Noise FFT , 2Ω load (Two PBTL Parallel)



Noise FFT , 2Ω load (Two PBTL Parallel)



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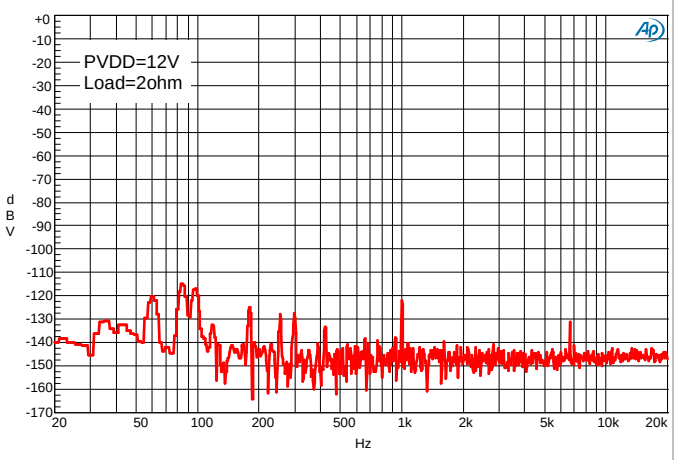
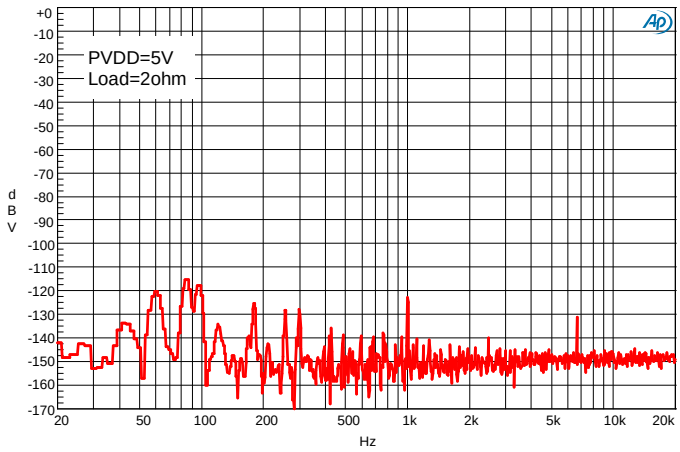
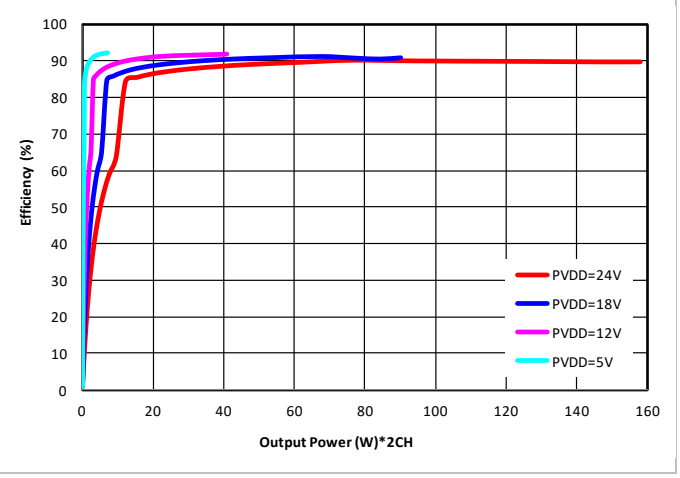


Noise FFT , 2Ω load (Two PBTL Parallel)



Efficiency, 2Ω load (Two PBTL Parallel)



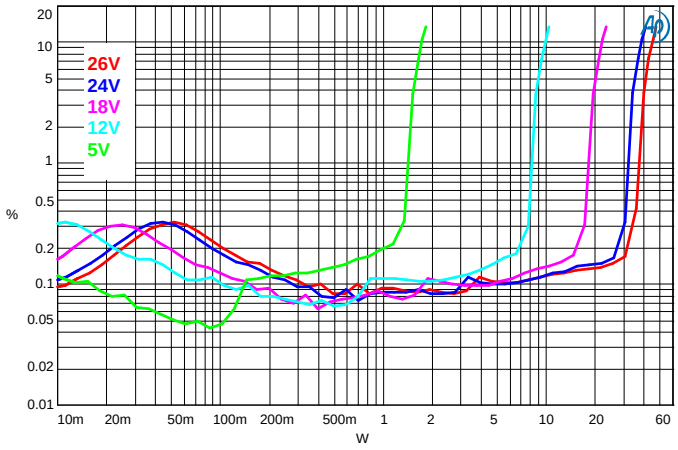
Electrical Characteristics and Specifications for Loudspeaker (cont.)

- **2.1CH output (BTL)**

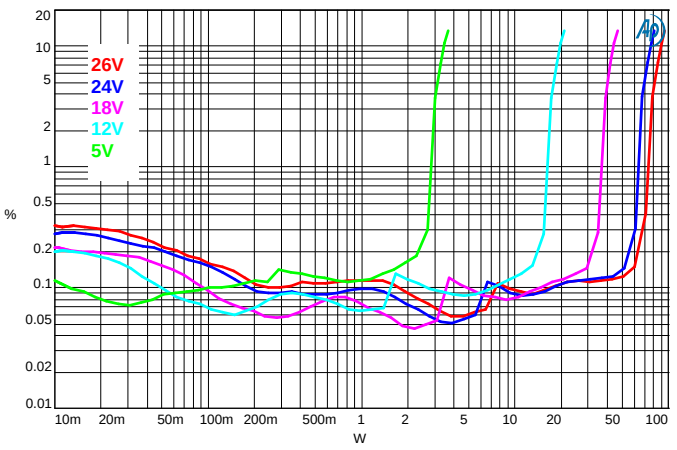
Condition: T_A=25°C, DVDD=3.3V, PVDD=24V, F_S=48kHz, Load=8Ω with passive LC low-pass filter (L=15μ H with R_{DC}=63mΩ , C=220nF); Input is 1kHz sine-wave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N=0.3%)	Instantaneous output power			30		W
	RMS Output Power (THD+N=0.17%)	Continuous output power			25		W
	RMS Output Power (THD+N=0.15%)				20		W
	RMS Output Power (THD+N=0.14%)				15		W
THD+N	Total Harmonic Distortion + Noise	P_o=12.5W			0.14		%
SNR	Signal to Noise Ratio (Note 8)	Maximum power at THD < 1% @1kHz			129		dB
DR	Dynamic Range (Note 8)		-60		106		dB
Vn	Output Noise (Note 8)	20Hz to 20kHz			5		uV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz			75		dB
X-talk	Channel Separation	1W @1kHz			70		dB

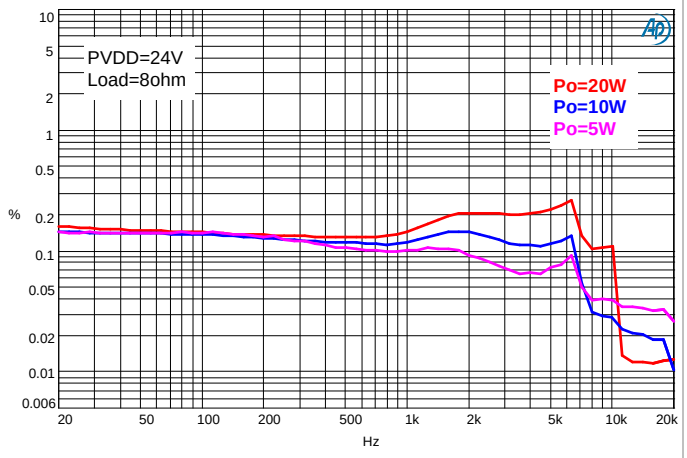
THD+N vs. Output Power, 8Ω load (BTL)



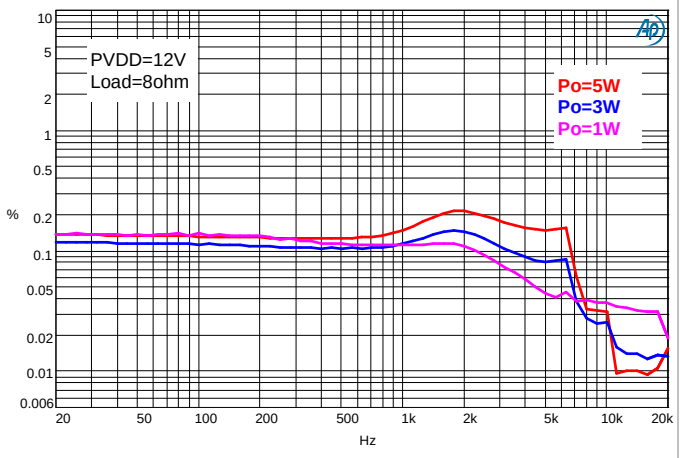
THD+N vs. Output Power, 4Ω load (PBTL)



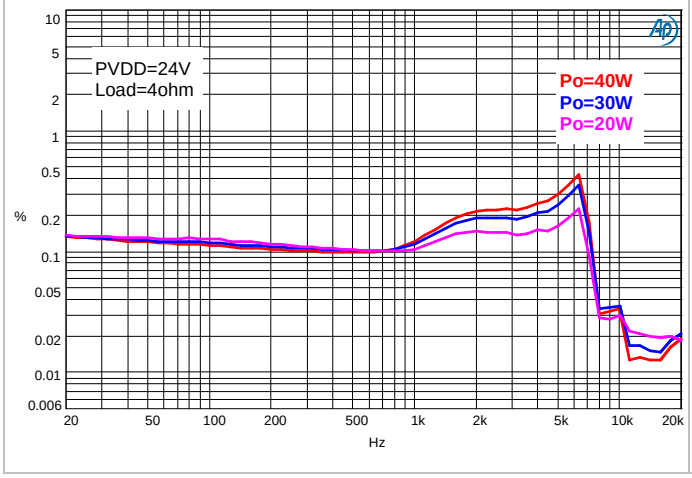
THD+N vs. Frequency, 8Ω load (BTL)



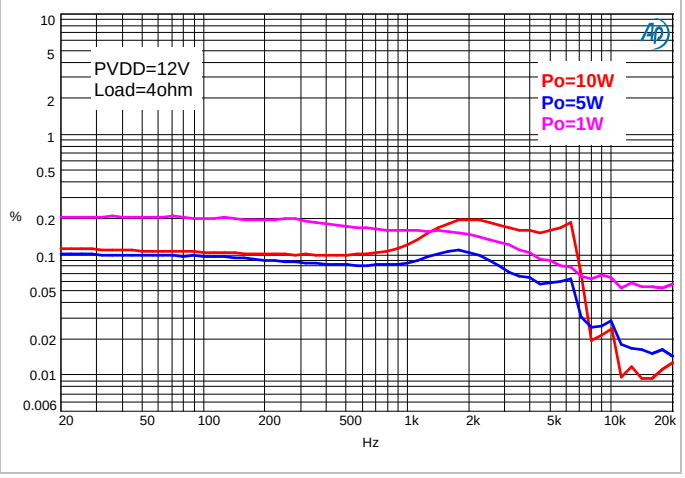
THD+N vs. Frequency, 8Ω load (BTL)



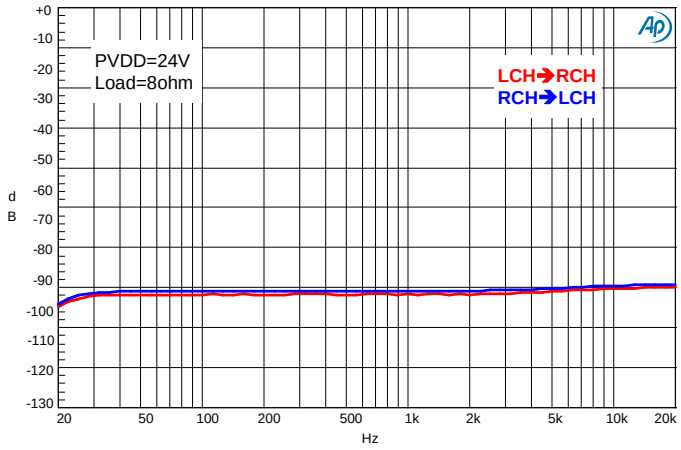
THD+N vs. Frequency, 4Ω load (PBTL)



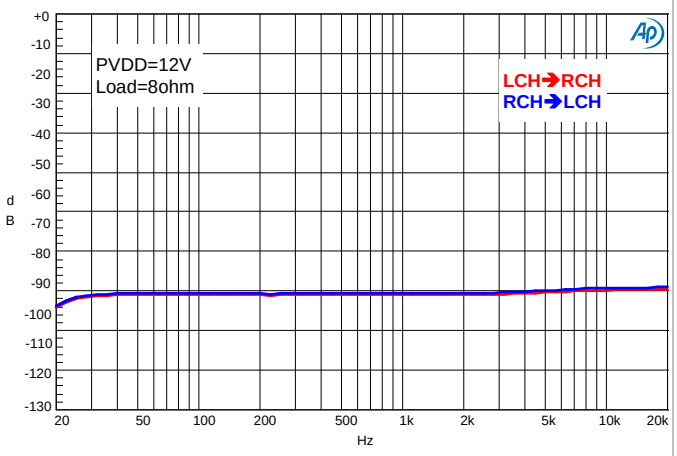
THD+N vs. Frequency, 4Ω load (PBTL)



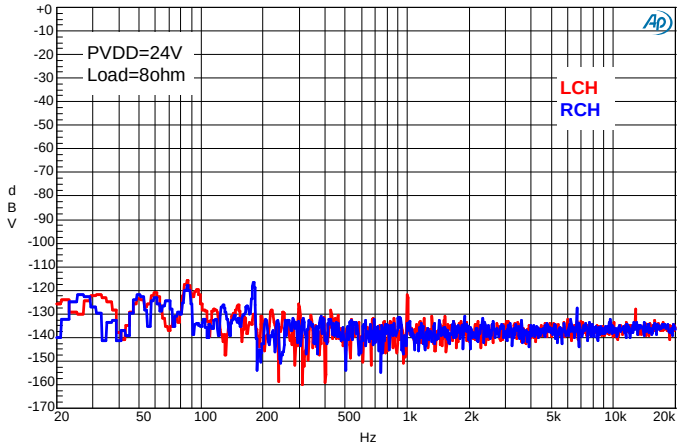
Crosstalk, 8Ω load (BTL)



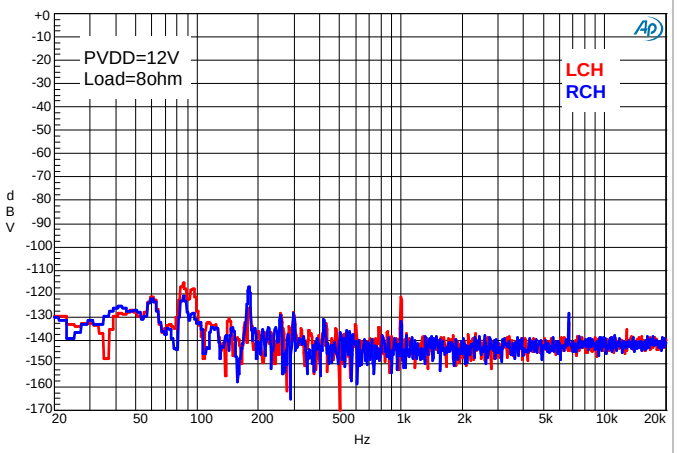
Crosstalk, 8Ω load (BTL)



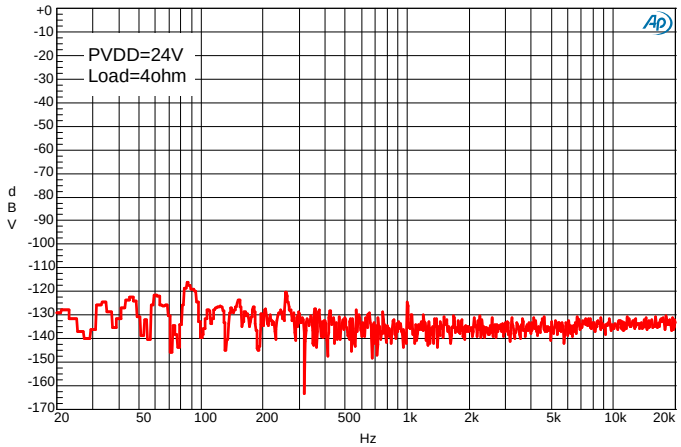
Noise FFT, 8Ω load (BTL)



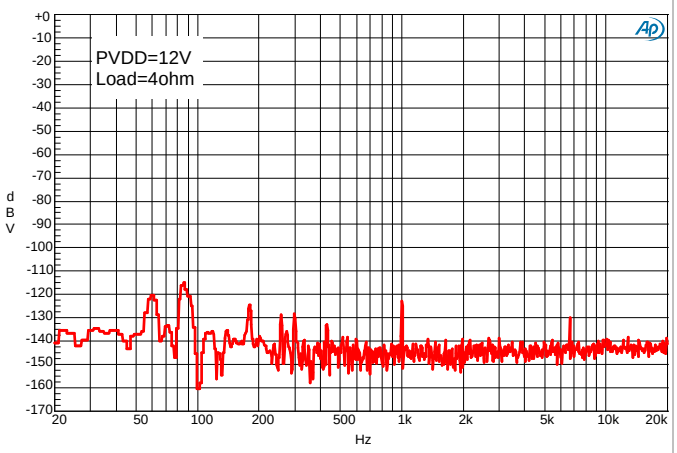
Noise FFT, 8Ω load (BTL)



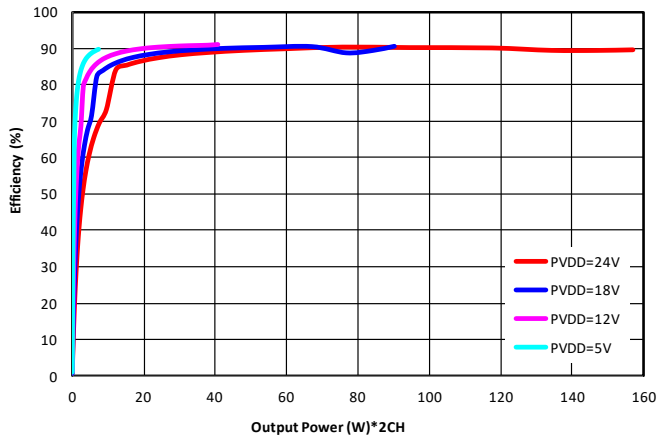
Noise FFT, 4Ω load (PBTL)



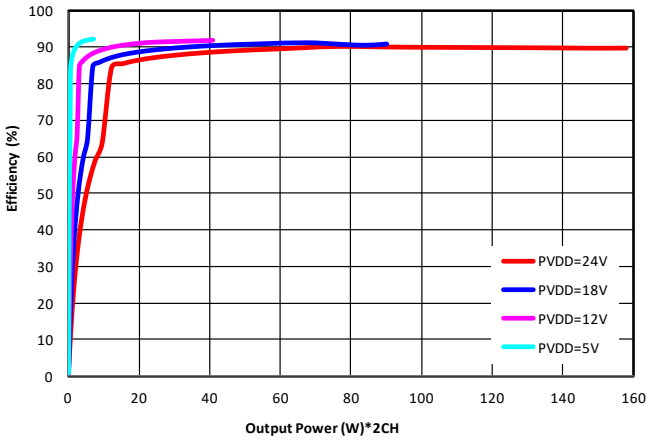
Noise FFT, 4Ω load (PBTL)



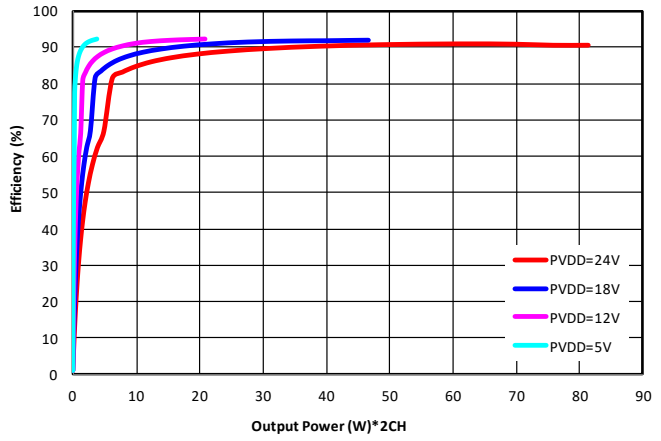
Efficiency (stereo, PBTL), 4Ω load



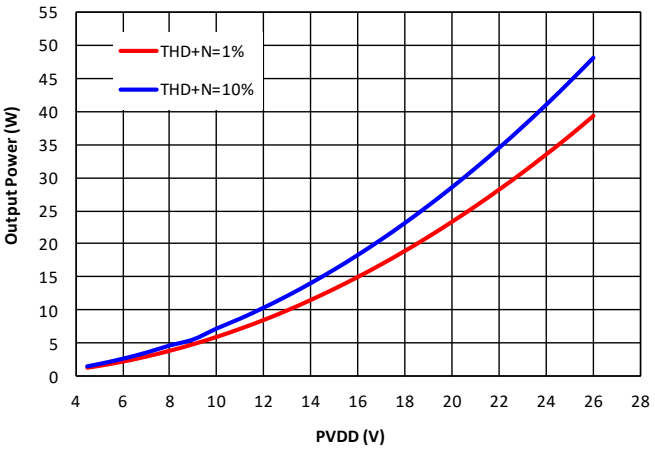
Efficiency (Mono, two PBTL), 2Ω load



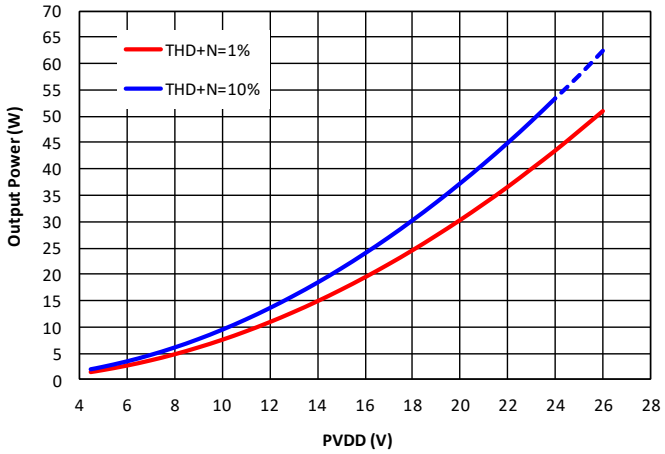
Efficiency (2.1CH, BTL), 8Ω load



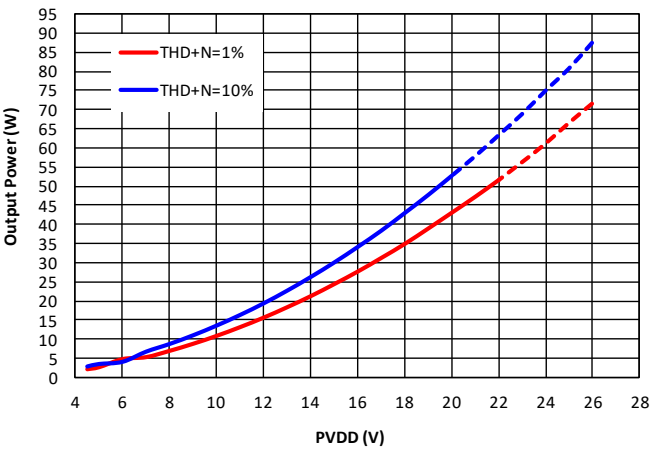
Output Power vs. PVDD @8ohm (Stereo PBTL)



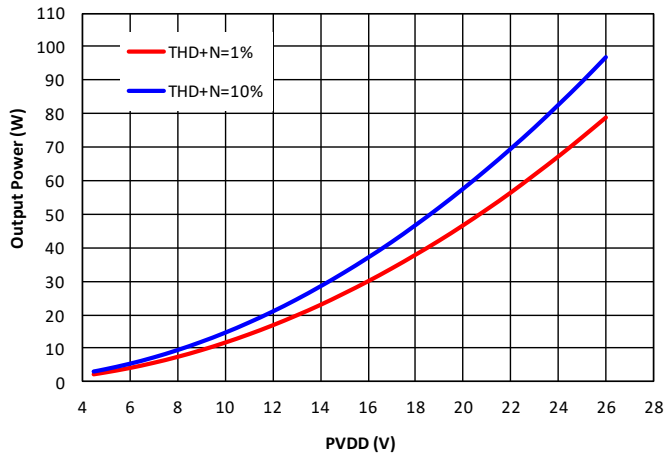
Output Power vs. PVDD @6ohm (Stereo PBTL)



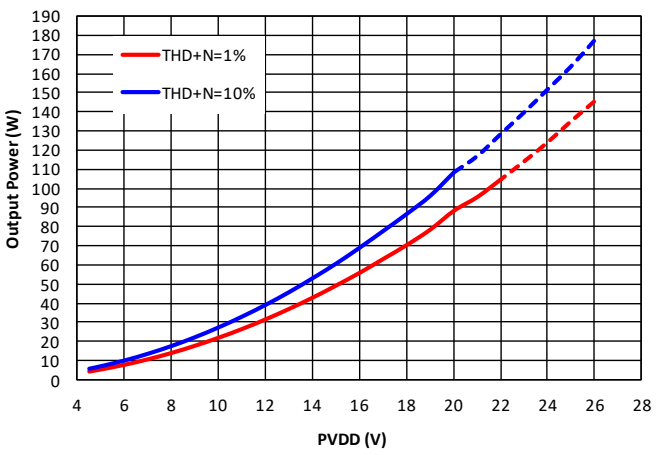
Output Power vs. PVDD @4ohm (Stereo PBTL)



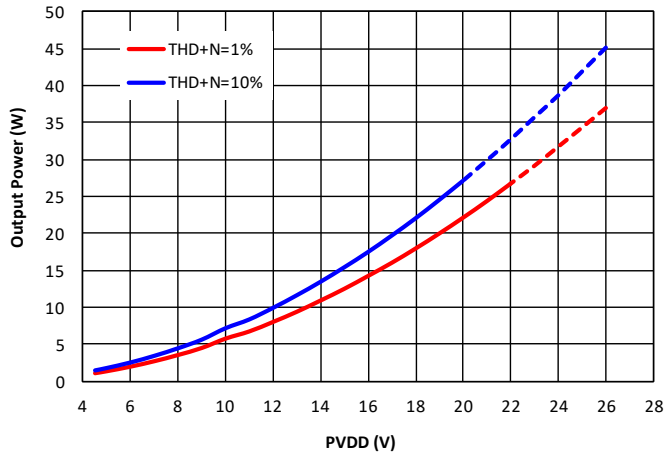
Output Power vs. PVDD @4ohm (Mono two PBTL)



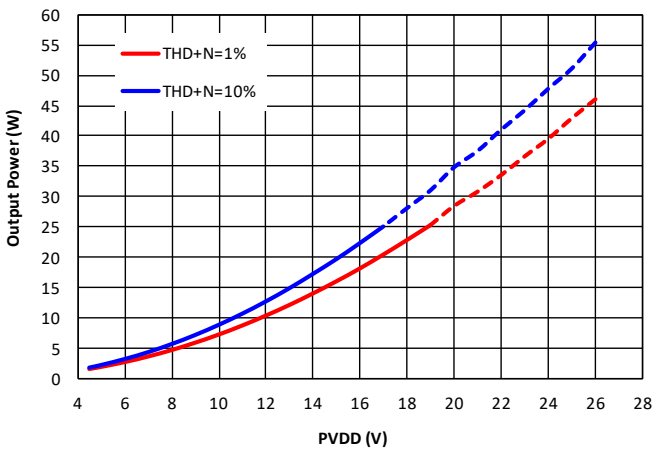
Output Power vs. PVDD @2ohm (Mono two PBTL)



Output Power vs. PVDD @8ohm (2.1ch BTL)

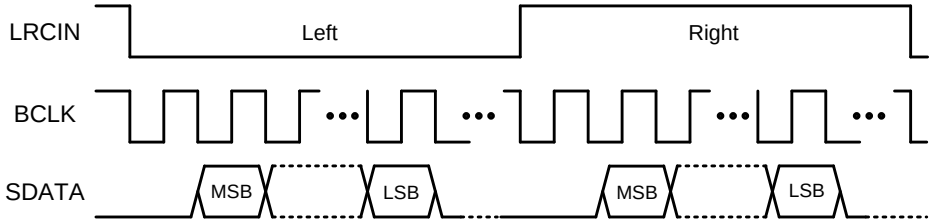


Output Power vs. PVDD @6ohm (2.1ch BTL)

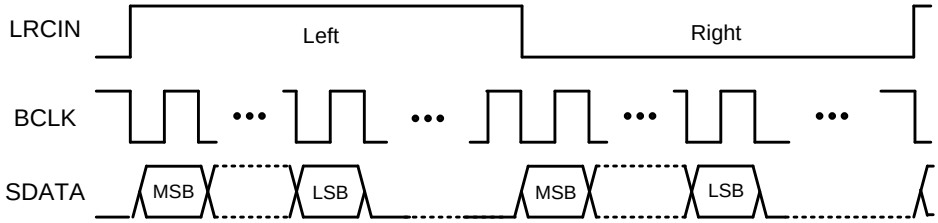


Interface configuration

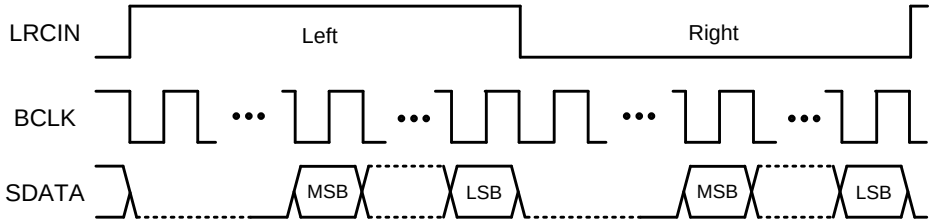
- I^2S



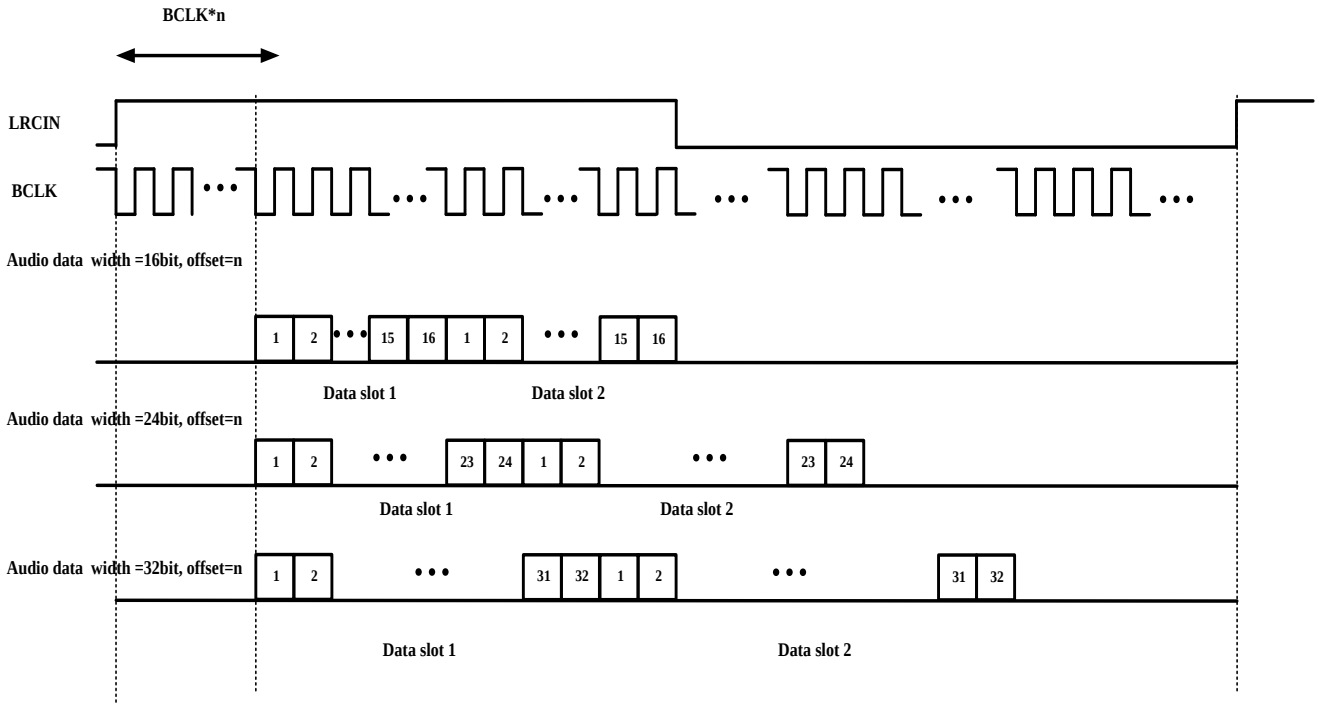
- Left-Alignment



- Right-Alignment



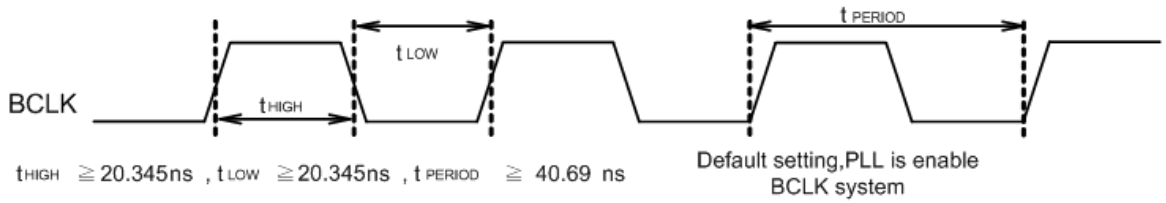
- TDM



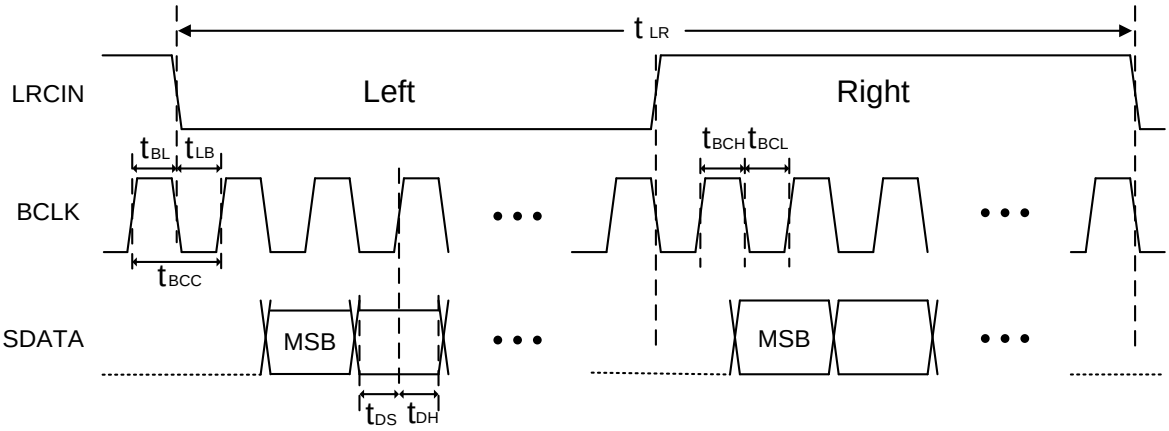
AD83586C device Audio Data Formats, Bit Depths, Clock Rates, and channel numbers (BCLK system)

Format	Data Bits	LRCIN Frequency (KHz)	BCLK Rate (FS)	Channel Numbers
I^2S/LJ/RJ	32, 24,16	48, 96	64x,48x,and 32x	2
	32, 24	16	64x and 48x	2
TDM	32	8	256X	8
	32, 24, 16	16	64x, 128x,192x, and 256x for 32 data bits 48x, 96x,and 192X for 24bits 64x,96x, and 128x for 16 data bits	2, 4, 6,8 channels for 32 data bits 2, 4, 8 channels for 24 data bits 4, 6,8 channel for 16 data bits
	32, 24,16	48, 96	64x, 128x, 192x, and 256x for 32 data bits 48x,96x,and 192X for 24bits 32x,64x,128x,192x,and256x for 16 data bits	2,4,6,8 channels for 32 data bits 2,4,8 channels for 24 data bits 2,4,6,8,16 channels for 16 data bits

- System Clock Timing

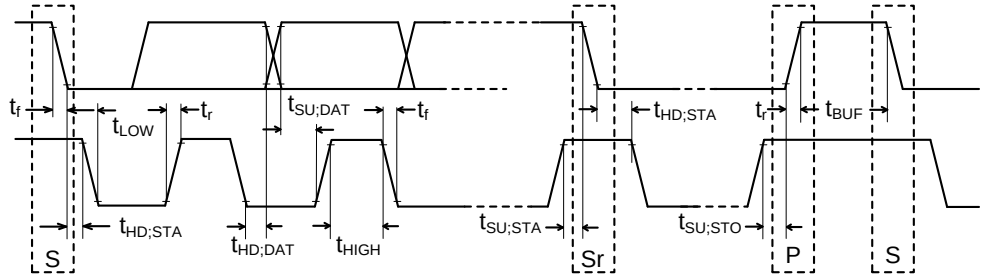


- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	10.4		31.25	us
t_{BL}	BCLK Rising Edge to LRCIN Edge	12.5			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	12.5			ns
t_{BCC}	BCLK Period ($1/64F_S$)	40.69		3906	ns
t_{BCH}	BCLK Pulse Width High	20.35		1953	ns
t_{BCL}	BCLK Pulse Width Low	20.35		1953	ns
t_{DS}	SDATA Set-Up Time	12.5			ns
t_{DH}	SDATA Hold Time	12.5			ns

- I^2C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time for repeated START condition	$t_{HD,STA}$	4.0	---	0.6	---	us
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	us
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	us
Setup time for repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	us
Hold time for I^2C bus data	$t_{HD;DAT}$	0	3.45	0	0.9	us
Setup time for I^2C bus data	$t_{SU;DAT}$	250	---	100	---	ns
Rise time of both SDA and SCL signals	t_r	---	1000	---	300	ns
Fall time of both SDA and SCL signals	t_f	---	300	---	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	us
Bus free time between STOP and the next START condition	t_{BUF}	4.7	---	1.3	---	us
Capacitive load for each bus line	C_b		400		400	pF

Operation Description

The default volume of AD83586C is muted. AD83586C will be activated while the de-mute command via I^2C is programmed.

- Internal PLL

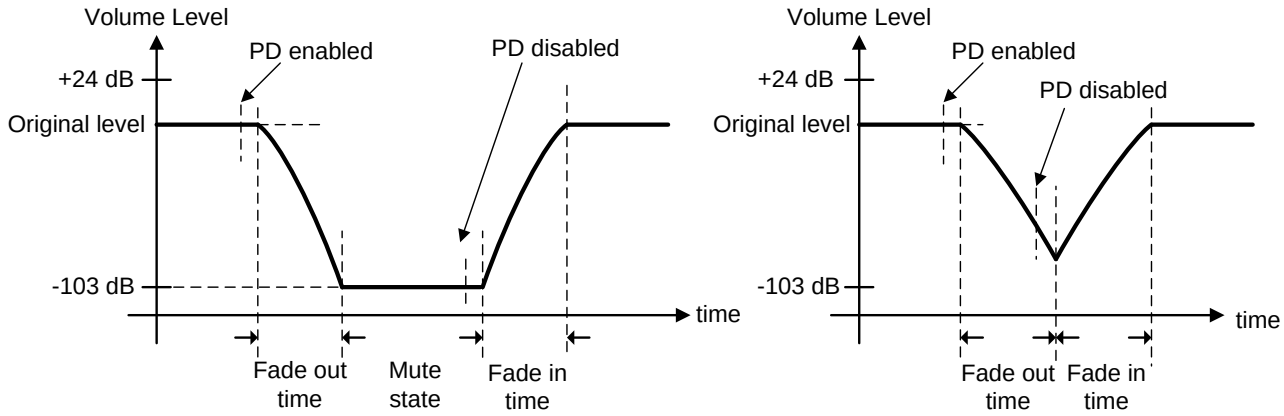
  AD83586C has a built-in PLL internally, the BCLK/FS or MCLK/FS ratio, which is selected by I^2C control interface. The clock inputted into the BCLK or MCLK pin becomes the frequency of multiple edge evaluation in chip internally.

- Reset

  When the $\overline{\text{RESET}}$ pin is lowered, AD83586C will clear the stored data and reset the register table to default values. AD83586C will exit reset state at the 512th internal clock cycle after the $\overline{\text{RESET}}$ pin is raised to high.

- Power down control

  AD83586C has a built-in volume fade-in/fade-out design for PD/Mute function. The relative PD timing diagrams for loudspeakers are shown below.



$$(10^{\frac{target(dB)}{20}} - 10^{\frac{original(dB)}{20}}) x 128 x (1/96K)$$

(Note: Address 0x0C B[6:5] = 00)

The volume level will be decreased to -∞dB in several LRCIN cycles. Once the fade-out procedure is finished, AD83586C will turn off the power stages, clock signals (for digital circuits) and current (for analog circuits). After PD pin is pulled low, AD83586C requires T_{fade} to finish the forementioned work before entering power down state. User can not program AD83586C during power down state. Also, all settings in the registers will remain intact unless DVDD is removed.

If the PD signal is removed during the fade-out procedure (above, right figure), AD83586C will still execute the fade-in procedure. In addition, AD83586C will establish the analog circuits' bias current and send the clock signals to digital circuits. Afterwards, AD83586C will return to its normal status.

- Self-protection circuits

AD83586C has built-in protection circuits including thermal, short-circuit, under-voltage detection, and over voltage circuits.

(i) When the internal junction temperature is higher than 160℃, power stages will be turned off and AD83586C will return to normal operation once the temperature drops to 125℃. The temperature values may vary around 10%.

(ii) The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or GND/PVDD. For normal 24V operations, the current flowing through the power stage will be less than 9A for stereo configuration. Otherwise, the short-circuit detectors may pull the $\overline{\text{ERROR}}$ pin to DGND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain $\overline{\text{ERROR}}$ pin will be pulled low and latched into ERROR state.

Once short-circuit condition is removed, AD83586C will exit ERROR state when one of the following conditions is met: (1) $\overline{\text{RESET}}$ pin is pulled low, (2) $\overline{\text{PD}}$ pin is pulled low, (3) Master mute is enabled through the I^2C interface.

(iii) Once the DVDD voltage is lower than 2.89V, AD83586C will turn off its loudspeaker power stages. When DVDD becomes higher than 2.99V, AD83586C will return to normal operation.

(iv) Once the PVDD voltage is higher than 29.2V, AD83586C will turn off its loudspeaker power stages. When PVDD becomes lower than 28.5V, AD83586C will return to normal operation.

(v) Once the PVDD voltage is lower than 4V, AD83586C will turn off its loudspeaker power stages. When PVDD becomes higher than 4.23V, AD83586C will return to normal operation.

- Anti-pop design

AD83586C will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- 3D surround sound

AD83586C provides the virtual surround sound technology with greater separation and depth voice quality for stereo signals.

- Error indicator

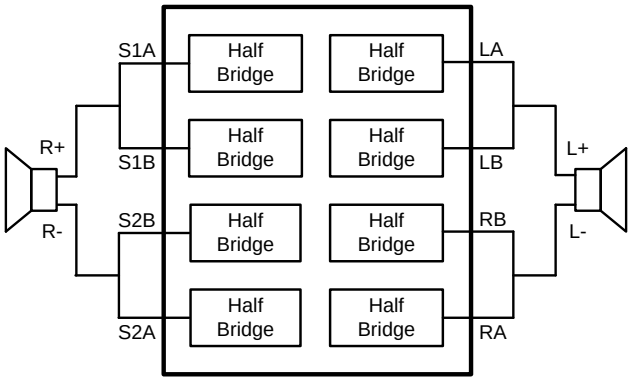
  $\overline{\text{ERROR}}$ is a protection indicator when A_SEL_FAULT(0X0C,B[7]) register is setting high. If OCP/OVP/OTP occur, ERROR pin will be low.

- Output configuration

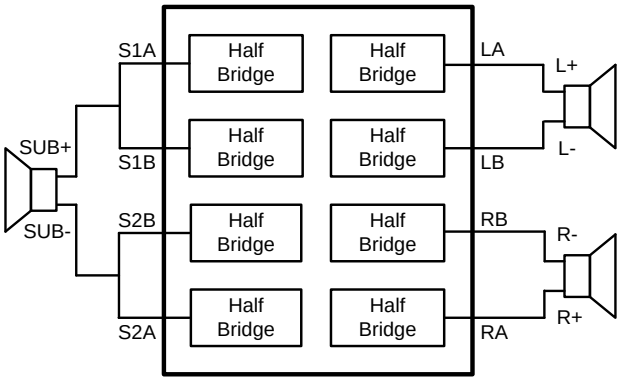
  AD83586C can be configured to Stereo or Mono mode by the pin of CFG0. If 2.1channel configuration is required on your applications, you can select it from the pin of CFG1 to enable it.

CFG1	CFG0	Configuration Mode
0	0	Mono
0	1	Stereo
1	x	2.1 Channel

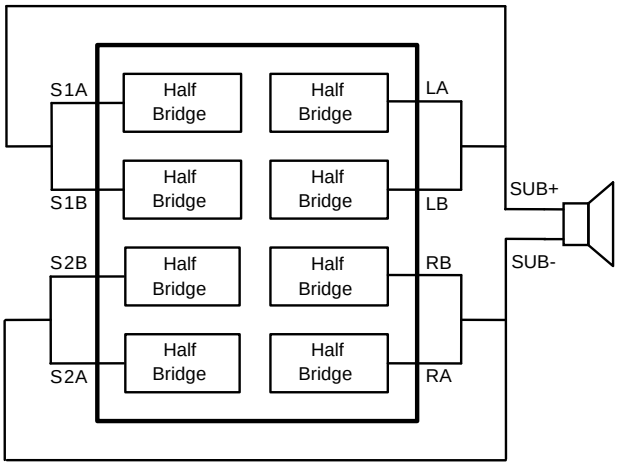
Configuration figures:



STEREO



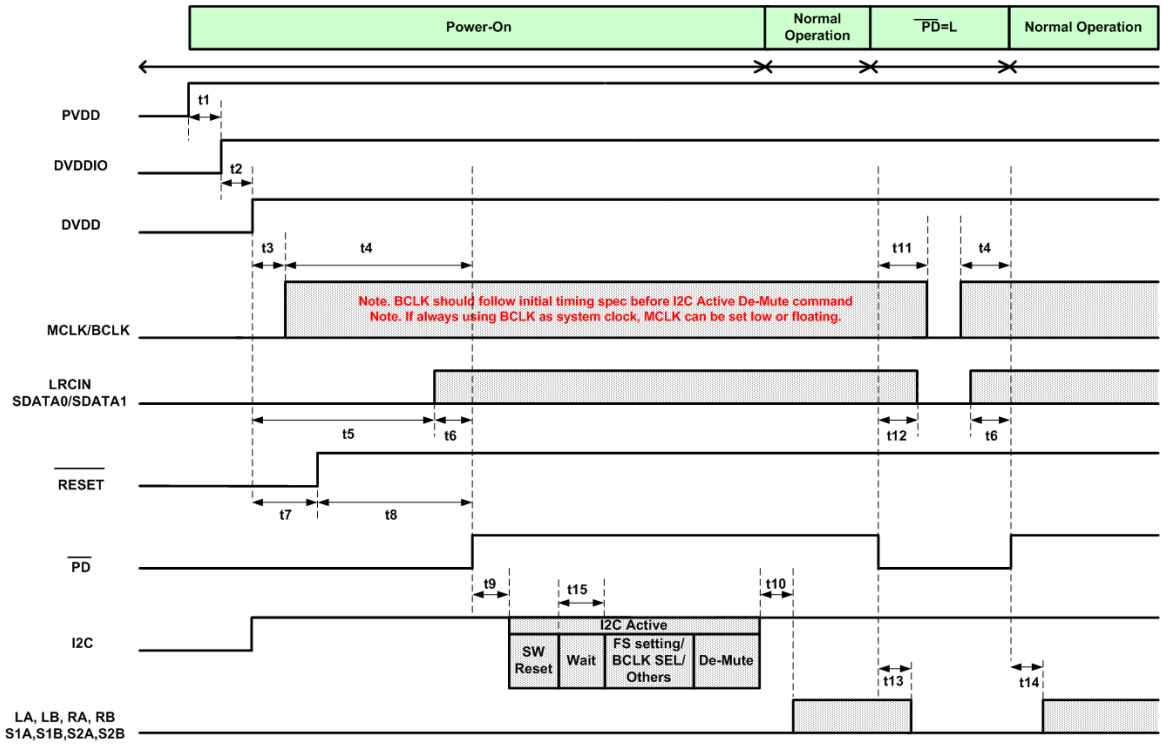
2.1CH



MONO

- Power on sequence

  Hereunder is AD83586C's power on sequence. Give a de-mute command via I^2C when the whole system is stable.



Note:

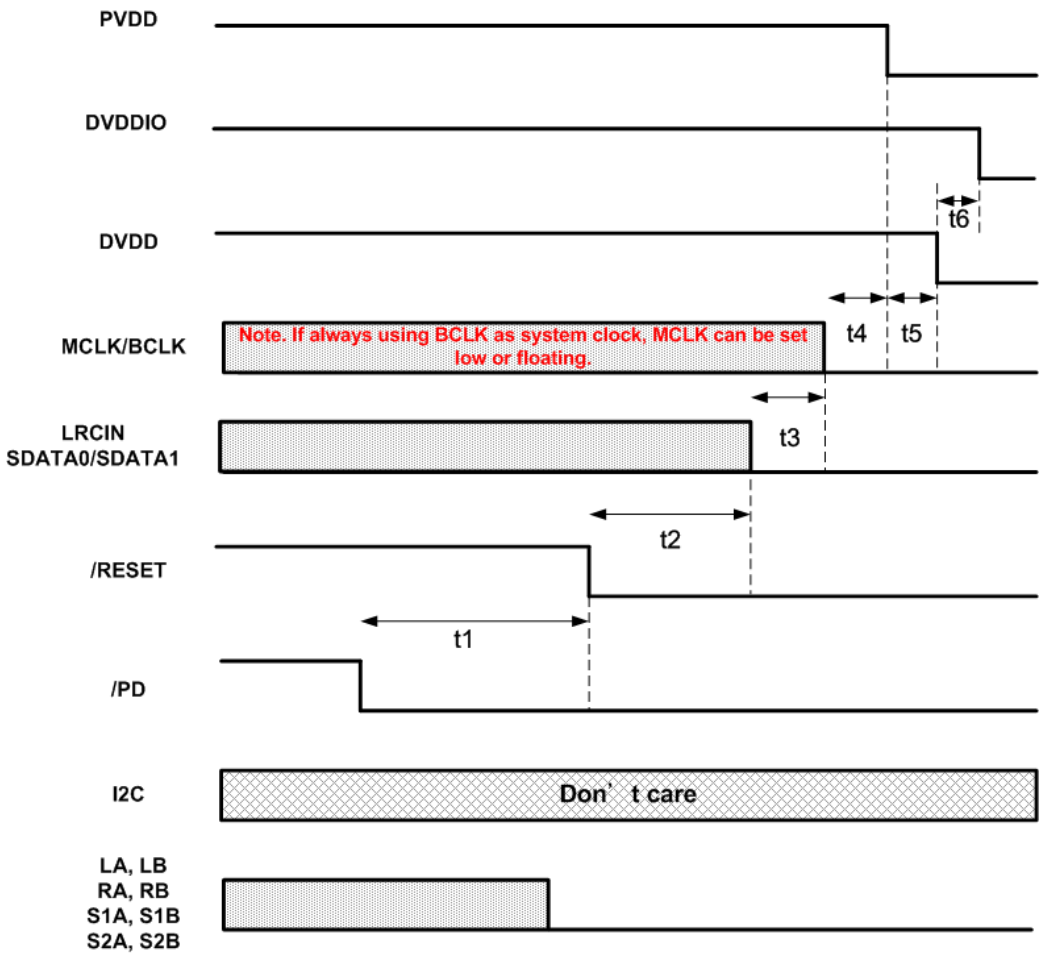
Please be noted below sequence shall be follow up with "I2C Active" processing,

(1) Set S/W reset bit = 0 → (2) Delay 5ms → (3) Set S/W reset bit = 1 → (4) Delay 20ms → (5) Set all channels = mute (setting address 0X02 = 0X7F) → (6) Set sampling frequency and other registers (except setting address 0X02) → (7) Set all channels = de-mute (setting address 0X02 = 0X00)

Symbol	Condition	Min	Max	Units
t1		0	-	msec
t2		0	-	msec
t3		0	-	msec
t4		10	-	msec
t5		0	-	msec
t6		10	-	msec
t7		10	-	msec
t8		0	-	msec
t9		20	-	msec
t10		-	0.1	msec
t11		25	-	msec
t12		25	-	msec
t13		-	22(FADE_SPEED=00) 88(FADE_SPEED=01) 176(FADE_SPEED=10) 352(FADE_SPEED=11)	msec
t14		-	20	msec
t15		20		msec

- Power off sequence

Hereunder is AD83586C's power off sequence.

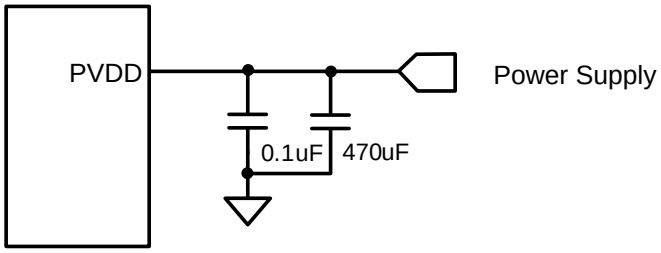


Symbol	Condition	Min	Max	Units
t1		35(FADE_SPEED=00) 140(FADE_SPEED=01) 280(FADE_SPEED=10) 560(FADE_SPEED=11)	-	msec
t2		0.1	-	msec
t3		0	-	msec
t4		1	-	msec
t5		1	-	msec
t6		0	-	msec

Application information

- Power supply decoupling capacitor (Cs)

Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVDD and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 0.1uF, is suggested for high frequency noise rejection. For low frequency noise filtering, a 470uF or greater capacitor (tantalum or electrolytic type) is suggested.



Recommended Power Supply Decoupling Capacitors.

- Boot-strap Capacitor

The output stage of the AD83586C uses a high-side NMOS driver. To generate the gate driver voltage for the high-side NMOS, a boot-strap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 22nF~220nF capacitors to connect the appropriate output pin to the boot-strap pin in BTL application and use 44nF~440nF boot-strap capacitor in PBTL application.

- Inductor Selection

The inductance vs. current profile for the inductor used in the output LC filter of a class-D amplifier can significantly impact the total harmonic distortion (THD) performance. The inductors always have decreasing inductance with increasing operating current. The inductance falls off severely, which induce inductor distortion is higher during lower-impedance loads. The effective inductance at the peak current is required to be at least 80% of the inductance value

In addition, it is required that the peak current is smaller than the OCP trigger threshold. Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation. The inductor's saturation current Isat > the amplifier's operating peak current is necessary. To operating safe considering, the inductor’s saturation current >1.35 times of the peak current of maximum output power is suggested.

$$Inductor\_Ipeak\_selection \geq \sqrt{2 \times \frac{Maximum\_output\_power}{Rload}} \times 1.35$$

I²C-Bus Transfer Protocol

- Introduction

AD83586C employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD83586C is always an I²C slave device.

- Protocol

  - START and STOP condition

START is identified by a high to low transition of the SDA signal. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD83586C and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

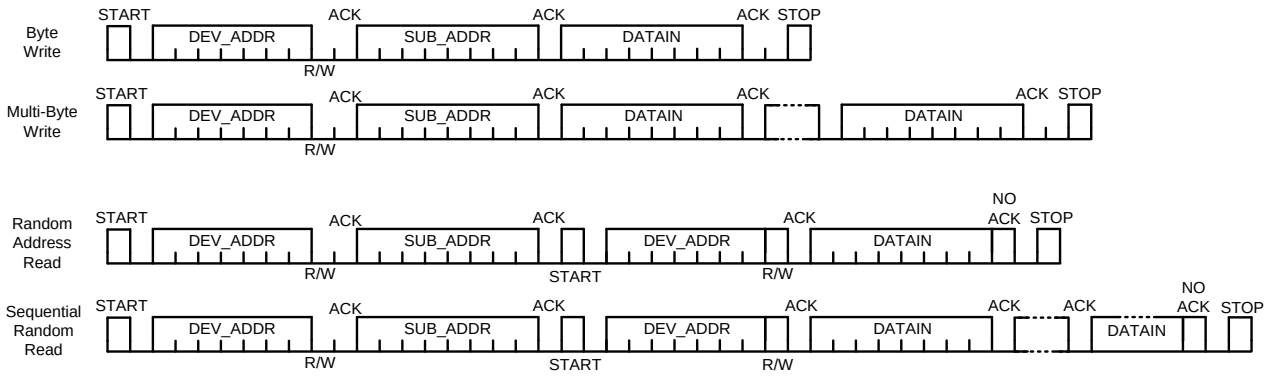
The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD83586C samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

The master generates 7-bit address to recognize slave devices. When AD83586C receives 7-bit address matched with 0111x0y (where x and y can be selected by external SA0 and SA1 pins, respectively), AD83586C will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD83586C internal sub-addresses.

  - Data transferring

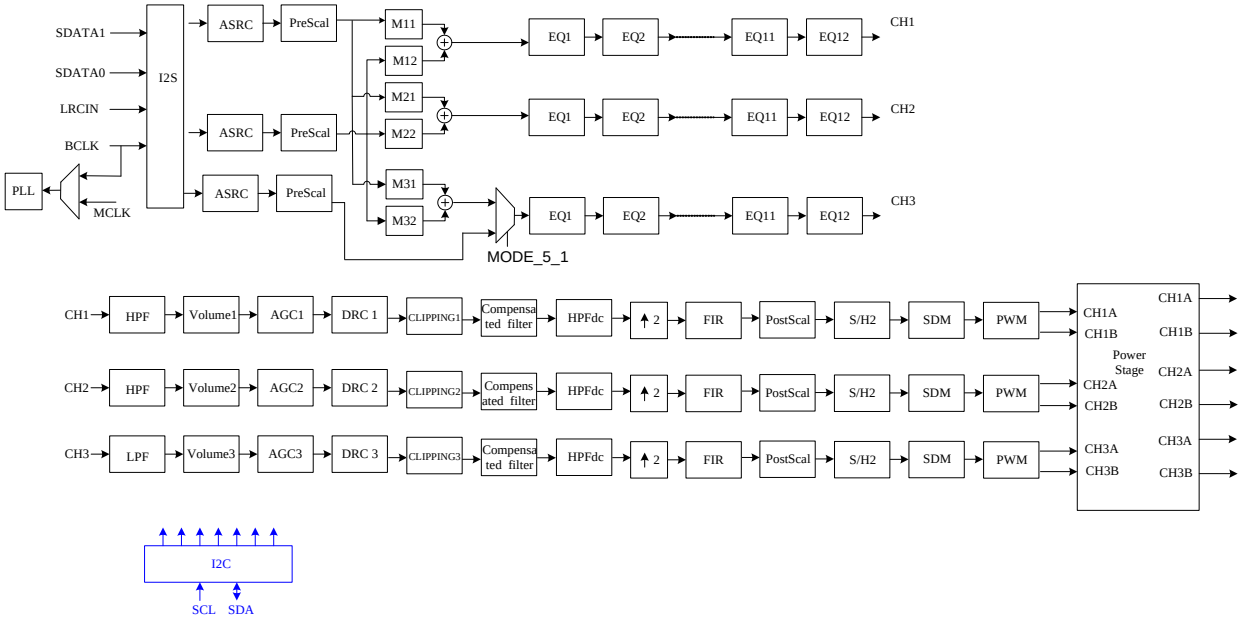
Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD83586C supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



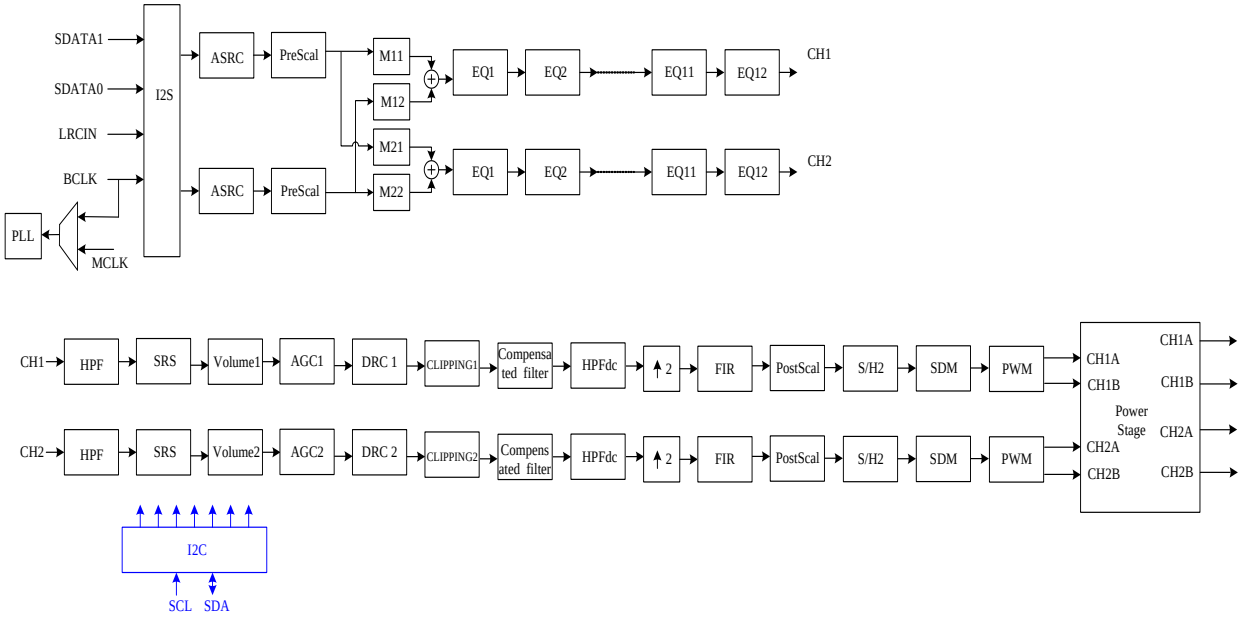
Register Table

The AD83586C's audio signal processing data flow is shown below. User can control these functions by programming appropriate settings in the register table. In this section, the register table is summarized first. The definition of each register follows in the next section.

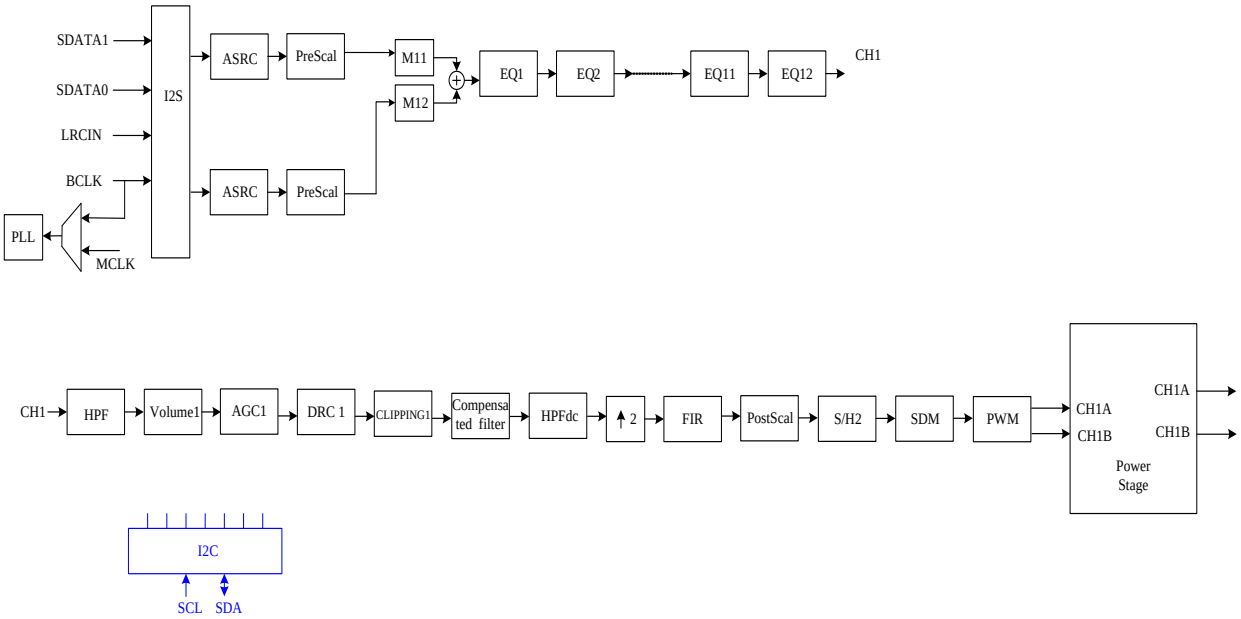
2.1 Application: CH1/CH2/CH3 has 12 EQs.



2.0 & 1.1 Application: CH1/CH2 has 12 EQs.



Mono Application: CH1 has 12 EQs.



Address	Name	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0X00	SCTL1	IF[2]	IF[1]	IF[0]	Reserved	Reserved	Reserved	LV_UVSEL	LREXC
0X01	SCTL2	BCLK_SEL	FS[1]	FS[0]	Reserved	PMF[3]	PMF[2]	PMF[1]	PMF[0]
0X02	SCTL3	Reserved	MUTE	CM1	CM2	CM3	Reserved	Reserved	Reserved
0X03	MVOL	MV[7]	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]
0X04	C1VOL	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
0X05	C2VOL	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
0X06	C3VOL	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
0X07	VFT	MV_FT[1]	MV_FT[0]	C1V_FT[1]	C1V_FT[0]	C2V_FT[1]	C2V_FT[0]	C3V_FT[1]	C3V_FT[0]
0X08	SCTL4	SRBP	SRS_dly	PWM_768K_EN	NGE	EQL	PSL	COMPEN_EN	HPB
0X09	SCTL5	EQL_EN	EQR_EN	EQS_EN	HPFL_EN	HPFR_EN	LPF_EN	Reserved	Reserved
0X0A	SCTL6	Reserved	Reserved	SW_RSTB	LVUV_FADE	OV_FADE	CLKDET_FADE	CHIP_SYNC_EN	Reserved
0X0B	SCTL7	CH3_DIN_SEL	DRCM	MODE_5_1	CH3_DIN_SEL	DIS_HVUV	HV_UVSEL[2]	HV_UVSEL[1]	HV_UVSEL[0]
0X0C	SCTL8	A_SEL_FAULT	FADE_SPEED[1]	FADE_SPEED[0]	PDB_DOPS	Reserved	DIS_NG_FADE	NG_GAIN[1]	NG_GAIN[0]
0X0D	GPIO0	Reserved		MTDMOC	GPIO0_status	GPIO0_CTRL[3]	GPIO0_CTRL[2]	GPIO0_CTRL[1]	GPIO0_CTRL[0]
0X0E	GPIO1	Reserved			GPIO1_status	GPIO1_CTRL[3]	GPIO1_CTRL[2]	GPIO1_CTRL[1]	GPIO1_CTRL[0]
0X0F	SCTL9	QT_EN_LR	PWM_SEL_LR	QT_EN_SUB	PWM_SEL_SUB	Reserved	Reserved	Reserved	Reserved
0X10	AGC	CH1_AGCEN	CH2_AGCEN	CH3_AGCEN	CH1_AGC_SHIFT	CH2_AGC_SHIFT	CH3_AGC_SHIFT	Reserved	Reserved
0X11	ATTACK_HOLD_Time	ATTACK_HOLD_TIME [7]	ATTACK_HOLD_TIME [6]	ATTACK_HOLD_TIME [5]	ATTACK_HOLD_TIME [4]	ATTACK_HOLD_TIME [3]	ATTACK_HOLD_TIME [2]	ATTACK_HOLD_TIME [1]	ATTACK_HOLD_TIME [0]

0X12	I2S_OUT	Reserved	SUB_I2S_DO_SEL_LR[2]	SUB_I2S_DO_SEL[1]	SUB_I2S_DO_SEL[0]	Reserved	LR_I2S_DO_SEL_LR[2]	LR_I2S_DO_SEL[1]	LR_I2S_DO_SEL[0]
0X13	C1CFG	C1DRCGS[1]	C1DRCGS[0]	Reserved	Reserved	C1PCBP	C1DRCBP	Reserved	C1VBP
0X14	C2CFG	C2DRCGS[1]	C2DRCGS[0]	Reserved	Reserved	C2PCBP	C2DRCBP	Reserved	C2VBP
0X15	C3CFG	C3DRCGS[1]	C3DRCGS[0]	Reserved	Reserved	C3PCBP	C3DRCBP	Reserved	C3VBP
0X16	TDM_W	Reserved	Reserved	Reserved	TDM_CH1_EN	TDM_CH2_EN	TDM_CH3_EN	WORD_WIDTH_SEL[1]	WORD_WIDTH_SEL[0]
0X17	TDM_O	TDM_OFFSET[7]	TDM_OFFSET[6]	TDM_OFFSET[5]	TDM_OFFSET[4]	TDM_OFFSET[3]	TDM_OFFSET[2]	TDM_OFFSET[1]	TDM_OFFSET[0]
0X18	PWM_MODE	D_MOD_LR	QD_EN_LR	DUTY_PWM_EN_LR	D_MOD_SUB	QD_EN_SUB	DUTY_PWM_EN_SUB	Reserved	Reserved
0X19	QT_SW_LEVEL_LR	QT_SW_WINDOW_LR [2]	QT_SW_WINDOW_LR [1]	QT_SW_WINDOW_LR [0]	QT_SW_LEVEL_LR[4]	QT_SW_LEVEL_LR [3]	QT_SW_LEVEL_LR[2]	QT_SW_LEVEL_LR [1]	QT_SW_LEVEL_LR[0]
0X1A	QT_SW_LEVEL_SUB	QT_SW_WINDOW_SUB [2]	QT_SW_WINDOW_SUB [1]	QT_SW_WINDOW_SUB [0]	QT_SW_LEVEL_SUB[4]	QT_SW_LEVEL_SUB[3]	QT_SW_LEVEL_SUB[2]	QT_SW_LEVEL_SUB[1]	QT_SW_LEVEL_SUB[0]
0X1B	Q_DUTY_LR	Q_DUTY_LR[7]	Q_DUTY_LR[6]	Q_DUTY_LR[5]	Q_DUTY_LR[4]	Q_DUTY_LR[3]	Q_DUTY_LR[2]	Q_DUTY_LR[1]	Q_DUTY_LR[0]
0X1C	Q_DUTY_SUB	Q_DUTY_SUB[7]	Q_DUTY_SUB[6]	Q_DUTY_SUB[5]	Q_DUTY_SUB[4]	Q_DUTY_SUB[3]	Q_DUTY_SUB[2]	Q_DUTY_SUB[1]	Q_DUTY_SUB[0]
0X1D	CFADDR	CFA[7]	CFA[6]	CFA[5]	CFA[4]	CFA[3]	CFA[2]	CFA[1]	CFA[0]
0X1E	A1CF1	Reserved	Reserved	Reserved	Reserved	C1B[27]	C1B[26]	C1B[25]	C1B[24]
0X1F	A1CF2	C1B[23]	C1B[22]	C1B[21]	C1B[20]	C1B[19]	C1B[18]	C1B[17]	C1B[16]
0X20	A1CF3	C1B[15]	C1B[14]	C1B[13]	C1B[12]	C1B[11]	C1B[10]	C1B[9]	C1B[8]
0X21	A1CF4	C1B[7]	C1B[6]	C1B[5]	C1B[4]	C1B[3]	C1B[2]	C1B[1]	C1B[0]
0X22	A2CF1	Reserved	Reserved	Reserved	Reserved	C2B[27]	C2B[26]	C2B[25]	C2B[24]
0X23	A2CF2	C2B[23]	C2B[22]	C2B[21]	C2B[20]	C2B[19]	C2B[18]	C2B[17]	C2B[16]
0X24	A2CF3	C2B[15]	C2B[14]	C2B[13]	C2B[12]	C2B[11]	C2B[10]	C2B[9]	C2B[8]
0X25	A2CF4	C2B[7]	C2B[6]	C2B[5]	C2B[4]	C2B[3]	C2B[2]	C2B[1]	C2B[0]
0X26	B1CF1	Reserved	Reserved	Reserved	Reserved	C3B[27]	C3B[26]	C3B[25]	C3B[24]
0X27	B1CF2	C3B[23]	C3B[22]	C3B[21]	C3B[20]	C3B[19]	C3B[18]	C3B[17]	C3B[16]
0X28	B1CF3	C3B[15]	C3B[14]	C3B[13]	C3B[12]	C3B[11]	C3B[10]	C3B[9]	C3B[8]
0X29	B1CF4	C3B[7]	C3B[6]	C3B[5]	C3B[4]	C3B[3]	C3B[2]	C3B[1]	C3B[0]
0X2A	B2CF1	Reserved	Reserved	Reserved	Reserved	C4B[27]	C4B[26]	C4B[25]	C4B[24]
0X2B	B2CF2	C4B[23]	C4B[22]	C4B[21]	C4B[20]	C4B[19]	C4B[18]	C4B[17]	C4B[16]
0X2C	B2CF3	C4B[15]	C4B[14]	C4B[13]	C4B[12]	C4B[11]	C4B[10]	C4B[9]	C4B[8]
0X2D	B2CF4	C4B[7]	C4B[6]	C4B[5]	C4B[4]	C4B[3]	C4B[2]	C4B[1]	C4B[0]
0X2E	A0CF1	Reserved	Reserved	Reserved	Reserved	C5B[27]	C5B[26]	C5B[25]	C5B[24]

0X2F	A0CF2	C5B[23]	C5B[22]	C5B[21]	C5B[20]	C5B[19]	C5B[18]	C5B[17]	C5B[16]
0X30	A0CF3	C5B[15]	C5B[14]	C5B[13]	C5B[12]	C5B[11]	C5B[10]	C5B[9]	C5B[8]
0X31	A0CF4	C5B[7]	C5B[6]	C5B[5]	C5B[4]	C5B[3]	C5B[2]	C5B[1]	C5B[0]
0X32	CFRW	Reserved	RSB	R3	W3	RA	R1	WA	W1
0X33	HI_RES	Reserved							FIR2_EN
0X34	ID	DN[3]	DN[2]	DN[1]	DN[0]	VN[3]	VN[2]	VN[1]	VN[0]
0X35	ERR1_STATUS	A_OCP1_N	A_OTP_N	A_UV1_N	A_BSUV1_N	A_BSOV1_N	D_CKERR_N	A_OVP1_N	A_GVDD1UV_N
0X36	ERR1_LATCH	A_OCP1_N_LATCH	A_OTP_N_LATCH	A_UV1_N_LATCH	A_BSUV1_N_LATCH	A_BSOV1_N_LATCH	D_CKERR_N_LATCH	A_OVP1_N_LATCH	A_GVDD1UV_N_LATCH
0X37	ERR1_CLEAR	A_OCP1_N_CLEAR	A_OTP_N_CLEAR	A_UV1_N_CLEAR	A_BSUV1_N_CLEAR	A_BSOV1_N_CLEAR	D_CKERR_N_CLEAR	A_OVP1_N_CLEAR	A_GVDD1UV_N_CLEAR
0X38	ERR2_STATUS	A_OCP2_N	Reserved	A_UV2_N	A_BSUV2_N	A_BSOV2_N	A_CKERR_N	A_OVP2_N	A_GVDD2UV_N
0X39	ERR2_LATCH	A_OCP2_N_LATCH	Reserved	A_UV2_N_LATCH	A_BSUV2_N_LATCH	A_BSOV2_N_LATCH	A_CKERR_N_LATCH	A_OVP2_N_LATCH	A_GVDD2UV_N_LATCH
0X3A	ERR2_CLEAR	A_OCP2_N_CLEAR	Reserved	A_UV2_N_CLEAR	A_BSUV2_N_CLEAR	A_BSOV2_N_CLEAR	A_CKERR_N_CLEAR	A_OVP2_N_CLEAR	A_GVDD2UV_N_CLEAR
0X3B	FREQBUF	Reserved	Reserved	Reserved	FS_BUF	PMF_BUF[3]	PMF_BUF[2]	PMF_BUF[1]	PMF_BUF[0]
0X3C	CLK_FS_ERR	ASR_ERR	BCLK_FS_RATIO_ERR	MCLK_FS_RATIO_ERR	Reserved	Reserved	Reserved	Reserved	CLK_ERROR_METHOD
0X3D	CLK_DET	ASR_DET	BCLK_FS_RATIO_DET	MCLK_FS_RATIO_DET	D_CLK_DET	FS_PMF_AUTO_EN	A_CKDET_EN	CKDET_SEL	CLK_ERROR_FADE_EN
0X3E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0X3F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0X40	Reserved	DTC	DTC_TH[1]	DTC_TH[0]	DTC_Rate[1]	DTC_Rate[0]	Reserved	Reserved	Reserved

Detail Description for Register

Note that the highlighted columns are default values of these tables. If there is no highlighted value, the default setting of this bit is determined by the external pin.

- Address 0X00 : State control 1

  AD83586C supports multiple serial data input formats including I^2S, Left-alignment and Right-alignment. These formats are selected by user via bit7~bit5 of address 0X00. The left/right channels can be exchanged to each other by programming to address 0/bit0, LREXC.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I^2S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
			110	TDM
B[4:2]		Reserved		
B[1]	LV_UVSEL	LV under voltage selection	0	2.9V
			1	2.7V
B[0]	LREXC	Left/Right (L/R) Channel exchanged	0	No exchanged
			1	L/R exchanged

- Address 0X01 : State control 2

AD83586C has a built-in PLL and supports multiple MCLK/Fs or BCLK/Fs ratios.

If BCLK_SEL is high, the ratio is changed to BCLK/FS ratios.

On the contrary, the ratio is changed to MCLK/FS ratios.

AD83586C has 8K and16K sample rate.

Detail setting is shown in the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	BCLK_SEL	MCLK-less (BCLK system)	0	Disable
			1	Enable
B[6:5]	FS[1:0]	Sampling Frequency	00	32/44.1/48kHz
			01	88.2/96kHz
			10	8kHz
			11	16kHz
B[4]		Reserved		

Multiple MCLK/FS in MCLK system or BCLK/FS in BCLK system ratio setting table

BIT	NAME	DESCRIPTION	VALUE	B[6:5]=00	B[6:5]=01	B[6:5]=10	B[6:5]=11
B[3:0]	PMF[3:0]	MCLK/Fs or BCLK/Fs Setup	0000	32X	32X	32X	32X
			0001	48X	48X	Reserved	48X
			0010	64X	64X	64X	64X
			0011	96X	96X	96X	96X
			0100	128X	128X	128X	128X
			0101	192X	192X	192X	192X
			0110	256X	256X	256X	256X
			0111	384X	384X	384X	384X
			1000	512X	512X	512X	512X

- Address 0X02 : State control 3

AD83586C has mute function including master mute and channel mute.

When master mute is enabled, all 3 processing channels are muted. User can mute these 3 channels individually by channel mute. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]	MMUTE	Master Mute	0	All channel not muted
			1	All channel muted
B[5]	CM1	Channel 1 Mute	0	Ch1 not muted
			1	Only Ch1 muted
B[4]	CM2	Channel 2 Mute	0	Ch2 not muted
			1	Only Ch2 muted
B[3]	CM3	Channel 3 Mute	0	Ch3 not muted
			1	Only Ch3 muted
B[2:0]		Reserved		

- Address 0X03 : Master volume control

AD83586C supports both master-volume (Address 0X03) and channel-volume control (Address 0X04, 0X05, 0X06) modes. Both volume control settings range from +12dB ~ -103dB and 0.5dB per step. Note that the master volume control is added to the individual channel volume control as the total volume control. For example, if the master volume level is set at, Level A (in dB unit) and the channel volume level is set at Level B (in dB unit), the total volume control setting is equal to Level A plus with Level B.

-103dB ≦ Total volume (Level A + Level B) ≦ +24dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	MV[7:0]	Master Volume	00000000	+12.0dB
			00000001	+11.5dB
			00000010	+11.0dB
			:	:
			00010111	+0.5dB
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X04 : Channel 1 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C1V[7:0]	Channel1 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X05 : Channel 2 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C2V[7:0]	Channel2 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X06 : Channel 3 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C3V[7:0]	Channel3 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X07: Volume fine tune

AD83586C supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MV_FT	Master Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C1V_FT	Channel 1 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C2V_FT	Channel 2 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]	C3V_FT	Channel 3 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB

- Address 0X08 : State control 4

The AD83586C provides several DSP setting as following.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	SRBP	Surround bypass	0	Surround enable
			1	Surround bypass
B[6]	SRS_dly	Surround Delay	0	No Delay
			1	Delay 1 Fs
B[5]	PWM_768K_EN	PWM switching rate	0	384KHz
			1	768KHz
B[4]	NGE	Noise gate enable	0	Noise gate disable
			1	Noise gate enable
B[3]	EQL	EQ Link	0	Each channel uses individual EQ
			1	Channel-2 uses channel-1 EQ
B[2]	PSL	Post-scale link	0	Each channel uses individual post-scale
			1	Use channel-1 post-scale
B[1]	COMPEN_EN	Compensate filter enable	0	Disable
			1	Enable
B[0]	HPB	DC blocking HPF bypass	0	HPF dc enable
			1	HPF dc bypass

- Address 0X09 : State control 5

L channel, R channel and sub channel EQs of AD83586C can be enable or disable via bit 7, 6 and 5.

Cross over filter of each channel can be enable or disable via bit 4, 3 and 2.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	EQL_EN	L channel EQ enable	0	Bypass
			1	Enable
B[6]	EQR_EN	R channel EQ enable	0	Bypass
			1	Enable
B[5]	EQS_EN	S channel EQ enable	0	Bypass
			1	Enable
B[4]	HPFL_EN	L channel XO HPF enable	0	Bypass
			1	Enable
B[3]	HPFR_EN	R channel XO HPF enable	0	Bypass
			1	Enable
B[2]	LPF_EN	S channel XO LPF enable	0	Bypass
			1	Enable
B[1:0]		Reseved		

- Address 0X0A : State control 6

AD83586C has software reset for initial power on via bit5.

When LVUV, OV, and CKDET detection occurs, AD83586C can directly be Hi-Z state or fade out via bit4,3, and2.

If using 2 AD83586C for stereo application, setting CHIP_SYNC_EN can minimum two AD83586C phase shift.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]		Reserved		
B[5]	SW_RSTB	Software reset	0	Reset
			1	Normal operation
B[4]	LVUV_FADE	Low under voltage fade	0	No Fade
			1	Fade
B[3]	OV_FADE	Over voltage fade	0	No Fade
			1	Fade
B[2]	CLKDET_FADE	Clock detection fade	0	No Fade
			1	Fade
B[1]	CHIP_SYNC_EN	Chip sync enable	0	No sync
			1	Sync
B[0]		Reserved		

- Address 0X0B : State control 7

AD83586C can disable HV under voltage detection via bit 3.

AD83586C support multi-level HV under voltage detection via bit2~ bit0, using this function, AD83586C will fade out signal to avoid pop sounds if high voltage supply disappear before low voltage supply.

When MODE_5_1 is high, AD83586C CH3 input will select I^2S data from SDATA1. On the contrary, when MODE_5_1 is low, EQ input of CH3 will select from the mixing output from left and right channel.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]	DRCM	DRC MODE	0	PEAK
			1	RMS
B[5]	MODE_5_1	5.1 application mode	0	Disable
			1	Enable
B[4]	CH3_DIN_SEL	Channel 3 data input selection in 5.1 application	0	Select L of SDATA1
			1	Select R of SDATA1
B[3]	DIS_HVUV	Disable HV under voltage selection	0	Enable
			1	Disable
B[2:0]	HV_UV SEL	UV detection level	000	4V
			001	7.2V
			010	9.7 V
			011	13.2V
			100	15.5 V
			101	19.5 V
			Others	7.2V

- Address 0X0C: State control 8

The $\overline{\text{ERROR}}$ pin of AD83586C is a dual function pin. It is treated as a I^2C device address selection input when B[6] is set as low. It will become as an ERROR output pin when B[7] is set as high.

AD83586C can turn on delta quaternary modulation via bit 5.
AD83586C provide 4 kind of fade in/out speed via bit 6 and bit 5, which are 1.25ms, 5ms, 10ms, 20ms from mute to 0dB.

When power down, AD83586C provide immediately turns off power stage or fade out via be 4.
AD83586C provide noise gate function if receiving 2048 signal sample points smaller than noise gate attack level. User can change noise gate gain via bit1~ bit0. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, Mute). User can select fade out or not via bit 2.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_SEL_FAULT	I2C address selection or ERROR output	0	I2C device address selection
			1	ERROR output
B[6:5]	FADE_SPEED	Fade in/out speed selection	00	1.25ms
			01	5ms
			10	10ms
			11	20ms
B[4]	PDB_DOPS	Power down direct off power stage	0	Fade out when PD
			1	Power stage direct off when PD
B[3]		Reserved		
B[2]	DIS_NG_FADE	Disable noise gate fade	0	Fade
			1	No fade
B[1:0]	NG_GAIN[1:0]	Noise gate gain	00	x1/8
			01	x1/4
			10	x1/2
			11	Mute

- Address 0X0D : GPIO0 control

GPIO0 of AD83586C is input or output via bit 4. Select output types of GPIO0 by setting bit 3-0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]		Reserved		
B[5]	MTDMOC	Multi TDM output connection	0	Disable
			1	Enable
B[4]	GPIO0_STATUS	GPIO0_status	0	GPIO0 act as input (initial MCLK/Fs setting)
			1	GPIO0 act as output
B[3:0]	GPIO0_CTRL	GPIO0 Control	0000	GND
			0001	CH1/CH2 STATAO(I2S) CH1/CH2/CH3 STATAO(TDM 4 channel)
			0010	CH3 STATAO(I2S)
			Others	Prohibited

- Address 0X0E : GPIO1 control

GPIO1 of AD83586C is input or output via bit 4. Select output types of GPIO1 by setting bit 3-0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]		Reserved		
B[4]	GPIO1_STATUS	GPIO1_status	0	Hi-z
			1	GPIO1 act as output
B[3:0]	GPIO1_CTRL	GPIO1 Control	0000	GND
			0001	CH1/CH2 STATAO(I2S) CH1/CH2/CH3 STATAO(TDM 4 channel)
			0010	CH3 STATAO(I2S)

- Address 0X0F : State control 9

AD83586C provides power saving mode for L/R channel and sub-woofer channel via bit 7 and bits5.

AD83586C ternary and quaternary modulation for L/R channel and sub-woofer channel via bit 6 and bits4.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	QT_EN_LR	LR channel power saving mode	0	Disable
			1	Enable
B[6]	PWM_SEL_LR	LR channel PWM modulation	0	Qua-ternary
			1	Ternary
B[5]	QT_EN_SUB	SUB channel power saving mode	0	Disable
			1	Enable
B[4]	PWM_SEL_SUB	SUB channel PWM modulation	0	Qua-ternary
			1	Ternary
B[3:0]		Reserved		

- Address 0X10 : AGC control

AD83586C provides AGC function for each channel via bit 7, 6 and 5.

And AGC gain step can be select via bit 4, 3 and 2.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CH1_AGCEN	Channel 1 AGC enable	0	Disable
			1	Enable
B[6]	CH2_AGCEN	Channel 2 AGC enable	0	Disable
			1	Enable
B[5]	CH3_AGCEN	Channel 3 AGC enable	0	Disable
			1	Enable
B[4]	CH1_AGC_SHIFT	Channel 1 AGC gain step	0	0.125dB
			1	0.25dB
B[3]	CH2_AGC_SHIFT	Channel 2 AGC gain step	0	0.125dB
			1	0.25dB
B[2]	CH3_AGC_SHIFT	Channel 3 AGC gain step	0	0.125dB
			1	0.25dB
B[1:0]		Reserved		

- Address 0X11 : AGC ATTACK_HOLD_SET

AGC attack hold time is defined continuously compress audio amplitude when signal is less than attack threshold. Fine tune this register can avoid audio amplitude change a lot when AGC is active.

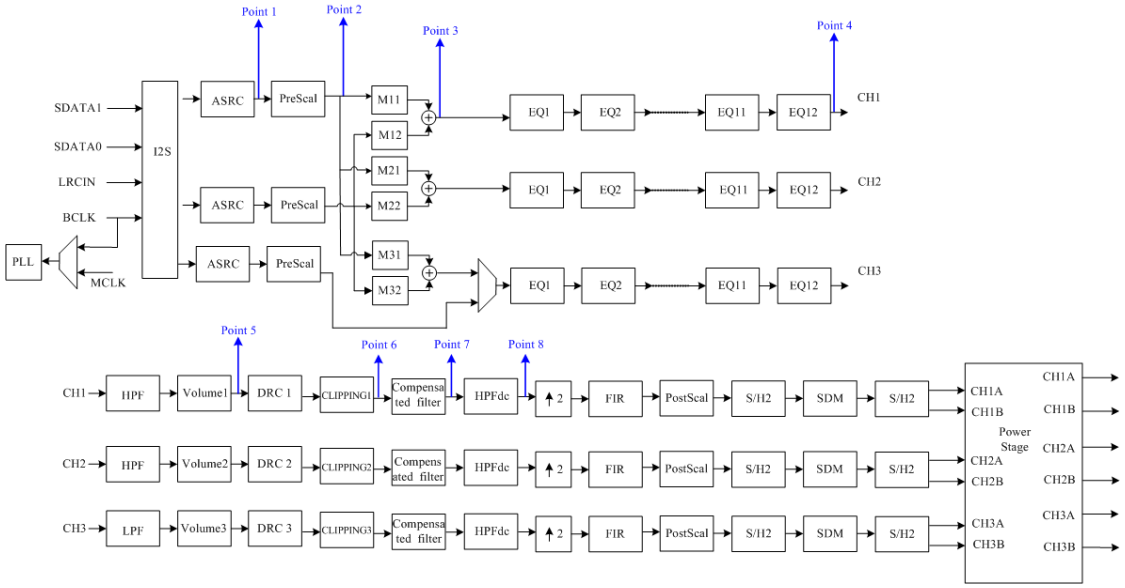
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	ATTACK_HOLD_TIME	ATTACK_HOLD_Time	00000000	0us
			00000001	20us
			00000010	40us
			…	
			11111110	5080us
			11111111	5100us

- Address 0X12 : I2S output selection

  AD83586C provide I2S output function and the output point of sub channel can be selected via bit 6~bit 4.

  AD83586C provide I2S output function and the output point of L/R channel can be selected via bit 2~bit 0

BIT	NAME	DESCRIPTION	VALUE	FUNCTION (2.1 mode)	FUNCTION (5.1 mode)
B[7]		Reserved			
B[6:4]	SUB_ I2S_DO_SEL	SUB I2S DATA OUTPUT selection	000	Prohibited	Ponit1 : ASRC output
			001	Prohibited	Point2 : pre-scale output
			010	Point3 : Mixer output	Prohibited
			011	Point4 : EQ12 output	Point4 : EQ12 output
			100	Point5 : volume output	Point5 : volume output
			101	Point6 : clipping output	Point6 : clipping output
			110	Point7 : compensate filter output	Point7 : compensate filter output
			111	Point8 : DC blocking output	Point8 : DC blocking output
B[3]		Reserved			
B[2:0]	LR I2S_DO_SEL	LR I2S DATA OUTPUT selection	000	Ponit1 : ASRC output	
			001	Point2 : pre-scale output	
			010	Point3 : Mixer output	
			011	Point4 : EQ12 output	
			100	Point5 : volume output	
			101	Point6 : clipping output	
			110	Point7 : compensate filter output	
			111	Point8 : DC blocking output	



- Address 0X13,0X14,0X15 : Channel configuration registers

AD83586C can configure each channel to enable or bypass DRC and channel volume and select the limiter set.

Address 0X13, 0X14, 0X15; where x=1, 2, 3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	CXDRCGS	Channel X DRC gain step	00	DRC gain step =0.5dB
			01	DRC gain step =0.25dB
			1x	DRC gain step =0.125dB
B[5:4]		Reserved		
B[3]	CxPCBP	Channel x Power Clipping bypass	0	Channel x PC enable
			1	Channel x PC bypass
B[2]	CxDRCBP	Channel x DRC bypass	0	Channel x DRC enable
			1	Channel x DRC bypass
B[1]		Reserved		
B[0]	CxVBP	Channel x Volume bypass	0	Channel x's master volume operation
			1	Channel x's master volume bypass

- Address 0X16 : TDM word length selection

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]		Reserved		
B[4]	TDM_CH1	TDM channel output	0	Disable
			1	Enable
B[3]	TDM_CH2	TDM channel output	0	Disable
			1	Enable
B[2]	TDM_CH3	TDM channel output	0	Disable
			1	Enable
B[1:0]	WORD_WIDTH_SEL	TDM word length selection	00	32 bits
			01	24 bits
			10	20 bits
			11	16 bits

- Address 0X17 : TDM offset

These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCLK from the starting (MSB) of audio frame to the starting of the desired audio sample

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	TDM_OFFSET	TDM offset bits	00000000	Offset is 0 BCLK
			00000001	Offset is 1 BCLK
			00000010	Offset is 2 BCLK
			…	
			11111101	Offset is 253 BCLK
			11111110	Offset is 254 BCLK
			11111111	Offset is 255 BCLK

- Address 0X18 : PWM mode

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	D_MOD_LR	LR channel Delta quaternary modulation	0	Disable
			1	Enable
B[6]	QD_EN_LR	LR channel Quaternary and delta quaternary switching	0	Disable
			1	Enable
B[5]	AQ_EN_LR	LR channel AQ enable	0	Disable
			1	Enable
B[4]	D_MOD_SUB	SUB channel Delta quaternary modulation	0	Disable
			1	Enable
B[3]	QD_EN_SUB	SUB channel Quaternary and delta quaternary switching	0	Disable
			1	Enable
B[2]	AQ_EN_SUB	SUB channel AQ enable	0	Disable
			1	Enable
B[1:0]		Reserve		

- Address 0X19 : L/R channel Power saving mode switching level

If the PWM exceeds the programmed switching power level (default 20*40ns), the modulation algorithm will change from default modulation scheme into power saving mode scheme. It results in higher power efficiency during larger power output operations. If the PWM drops below the programmed switching power level - programmed switching window (default (20-5)*40ns), the modulation algorithm will change back to default modulation scheme.

Switching scheme is related to QT_EN_LR (address0X0F, B[7]), D_MOD_LR (address0X18, B[7]), QD_EN_LR (address0X18, B[6]), and Advanced quaternary_EN_LR(address0X18, B[5]).

AD83586C has three type switching schemes and they share the same switching scheme.

One time will only have one switching scheme.

Case1: QT_EN_LR =1, D_MOD_LR =0, QD_EN_LR =0, Advanced quaternary_EN_LR=0

The default modulation scheme is quaternary and power saving mode scheme is ternary.

Case2: QT_EN_LR =1, D_MOD_LR =1, QD_EN_LR =0, Advanced quaternary_EN_LR=0.

The default modulation scheme is delta quaternary and power saving mode scheme is ternary.

Case3: QT_EN_LR =1, D_MOD_LR =0, QD_EN_LR =0, Advanced quaternary_EN_LR=1.

The default modulation scheme is duty quaternary and power saving mode scheme is ternary.

Case4: QT_EN_LR =0, D_MOD_LR =0, QD_EN_LR =1, Advanced quaternary_EN_LR=0.

The default modulation scheme is quaternary and power saving mode scheme is delta quaternary.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	SW_WINDOW_LR	LR channel Power saving mode switching window	000	2
			001	3
			010	4
			011	5
			100	6
			101	7
			110	8
			111	9
B[4:0]	QT_SW_LEVEL_LR	LR channel Power saving mode switching level	00000	4
			00001	4
			:	:
			01010	20
			:	:
			01101	26
			01110	28
			01111	30
			:	:
			11110	60
			11111	62

- Address 0X1A : SUB channel Power saving mode switching level

If the PWM exceeds the programmed switching power level (default 20*40ns), the modulation algorithm will change from default modulation scheme into power saving mode scheme. It results in higher power efficiency during larger power output operations. If the PWM drops below the programmed switching power level - programmed switching window (default (20-5)*40ns), the modulation algorithm will change back to default modulation scheme.

Switching scheme is related to QT_EN_SUB (address0X0F, B[5]), D_MOD_ SUB (address0X18, B[4]), and QD_EN_SUB (address0X18, B[3]) , and Advanced quaternary_EN_SUB(address0X18, B[2]).

AD83586C has four type switching schemes and they share the same switching scheme.

One time will only have one switching scheme.

Case1: QT_EN_SUB =1, D_MOD_SUB=0, QD_EN_SUB=0, Advanced quaternary_EN_SUB=0.

The default modulation scheme is quaternary and power saving mode scheme is ternary.

Case2: QT_EN_SUB =1, D_MOD_SUB=1, QD_EN_SUB=0, Advanced quaternary_EN_SUB=0.

The default modulation scheme is delta quaternary and power saving mode scheme is ternary.

Case3: QT_EN_SUB =1, D_MOD_SUB=0, QD_EN_SUB=0, Advanced quaternary_EN_SUB=1.

The default modulation scheme is delta quaternary and power saving mode scheme is ternary.

Case4: QT_EN_SUB =0, D_MOD_SUB=0, QD_EN_SUB=1, Advanced quaternary_EN_SUB=1.

The default modulation scheme is quaternary and power saving mode scheme is delta quaternary.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	SW_WINDOW_SUB	SUB channel Power saving mode switching window	000	2
			001	3
			010	4
			011	5
			100	6
			101	7
			110	8
			111	9
B[4:0]	QT_SW_LEVEL_SUB	SUB channel Power saving mode switching level	00000	4
			00001	4
			:	:
			01010	20
			:	:
			01101	26
			01110	28
			01111	30
			:	:
			11110	60
			11111	62

- Address 0X1D ~0X32 : User-defined coefficients registers

An on-chip RAM in AD83586C stores user-defined EQ, mixing, pre-scale, post-scale coefficients…etc. The content of this coefficient RAM is indirectly accessed via coefficient registers, which consist of one base address register (address 0X1D), five sets of registers (address 0X1E to 0X31) of three consecutive 8-bit entries for each 28-bit coefficient, and one control register (address 0X32) to control access of the coefficients in the RAM..

Address 0X1D

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CFA[7:0]	Coefficient RAM base address	00000000	

Address 0X1E, A1cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	Reserved			
B[3:0]	C1B[27:24]	First 4-bits of coefficients A1		

Address 0X1F, A1cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[23:16]	Second 8-bits of coefficients A1		

Address 0X20, A1cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[15:8]	Third 8-bits of coefficients A1		

Address 0X21, A1cf4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[7:0]	Fourth 8-bits of coefficients A1		

Address 0X22, A2cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	Reserved			
B[3:0]	C2B[27:24]	First 4-bits of coefficients A2		

Address 0X23, A2cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[23:16]	Second 8-bits of coefficients A2		

Address 0X24, A2cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[15:8]	Third 8-bits of coefficients A2		

Address 0X25, A2cf4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[7:0]	Fourth 8-bits of coefficients A2		

Address 0X26, B1cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	Reserved			
B[3:0]	C3B[27:24]	First 4-bits of coefficients B1		

Address 0X27, B1cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[23:16]	Second 8-bits of coefficients B1		

Address 0X28, B1cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[15:8]	Third 8-bits of coefficients B1		

Address 0X29, B1cf4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[7:0]	Fourth 8-bits of coefficients B1		

Address 0X2A, B2cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	Reserved			
B[3:0]	C4B[27:24]	First 4-bits of coefficients B2		

Address 0X2B, B2cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[23:16]	Second 8-bits of coefficients B2		

Address 0X2C, B2cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[15:8]	Third 8-bits of coefficients B2		

Address 0X2D, B2cf4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[7:0]	Fourth 8-bits of coefficients B2		

Address 0X2E, A0cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	Reserved			
B[3:0]	C5B[27:24]	First 4-bits of coefficients A0		

Address 0X2F, A0cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[23:16]	Second 8-bits of coefficients A0		

Address 0X30, A0cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[15:8]	Third 8-bits of coefficients A0		

Address 0X31, A0cf4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[7:0]	Fourth 8-bits of coefficients A0		

Address 0X32, CfRW

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]	RBS	RAM bank selection	0	Select RAM bank 0
			1	Select RAM bank 1
B[5]	R3	Enable of reading three coefficients from RAM	0	Read complete
			1	Read enable
B[4]	W3	Enable of writing three coefficients to RAM	0	Write complete
			1	Write enable
B[3]	RA	Enable of reading a set of coefficients from RAM	0	Read complete
			1	Read enable
B[2]	R1	Enable of reading a single coefficients from RAM	0	Read complete
			1	Read enable
B[1]	WA	Enable of writing a set of coefficients to RAM	0	Write complete
			1	Write enable
B[0]	W1	Enable of writing a single coefficient to RAM	0	Write complete
			1	Write enable

- Address 0X33 : Wide band setting register

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:1]		Reserved		
B[0]	FIR2_EN	Enable FIR2	0	Disabled
			1	Enable

Fs=96KHz input, please set address 0X33=”0X01” to extend frequency response from 20kHz to 40KHz if Wide Band Setting spec. is request. We called this “Wide Band Setting enable”.

- Address 0X34 : Device number and Version number

Device number and version number are the ID for the device.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	DN	Device number	1000	Identification code
B[3:0]	VN	Version number	0111	Identification code

- Address 0X35 : Protection register1

The protection registers will show what kind of protection occurs from LA/LB/RA/RB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP1_N	OCP1 register	0	OCP1 occur
			1	Normal
B[6]	A_OTP_N	OTP register	0	OT occur
			1	Normal
B[5]	A_UV1_N	UV1 register	0	UV1 occur
			1	Normal
B[4]	A_BSUV1_N	BSUV1 register	0	BSUV1 occur
			1	Normal
B[3]	A_BSOV1_N	BSOV1 register	0	BSOV1 occur
			1	Normal
B[2]	D_CKERR_N	CKERR register	0	CKERR occur
			1	Normal
B[1]	A_OVP1_N	OVP1 register	0	OVP1 occur
			1	Normal
B[0]	A_GVDD1UV_N	GVDDUV1 register	0	GVDDUV1 occur
			1	Normal

- Address 0X36 : Protection latch register1

The protection registers will show what kind of protection ever occurred from LA/LB/RA/RB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP1_N_LATCH	OCP1 latch register	0	OCP1 ever occur
			1	Normal
B[6]	A_OTP_N_LATCH	OTP latch register	0	OT ever occur
			1	Normal
B[5]	A_UV1_N_LATCH	UV1 latch register	0	UV1 ever occur
			1	Normal
B[4]	A_BSUV1_N_LATCH	BSUV1 latch register	0	BSUV1 ever occur
			1	Normal
B[3]	A_BSOV1_N_LATCH	BSOV1 latch register	0	BSOV1 ever occur
			1	Normal
B[2]	D_CKERR_N_LATCH	CKERR latch register	0	CKERR ever occur
			1	Normal
B[1]	A_OVP1_N_LATCH	OVP1 latch register	0	OVP1 ever occur
			1	Normal
B[0]	A_GVDD1UV_N_LATCH	GVDDUV1 latch register	0	GVDDUV1 ever occur
			1	Normal

- Address 0X37 : Protection clear register1

The protection latch registers will show what kind of protection ever occurred from LA/LB/RA/RB..

Using the protection clear registers can clear the corresponding protection latch registers.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP1_N_CLEAR	OCP1 latch clear register	0	No clear
			1	Clear
B[6]	A_OTP_N_CLEAR	OTP latch clear register	0	No clear
			1	Clear
B[5]	A_UV1_N_CLEAR	UV1 latch clear register	0	No clear
			1	Clear
B[4]	A_BSUV1_N_CLEAR	BSUV1 latch clear register	0	No clear
			1	Clear
B[3]	A_BSOV1_N_CLEAR	BSOV1 latch clear register	0	No clear
			1	Clear
B[2]	D_CKERR_N_CLEAR	CLOCK ERROR latch clear register	0	No clear
			1	Clear
B[1]	A_OVP1_N_CLEAR	OVP1 latch clear register	0	No clear
			1	Clear
B[0]	A_GVDD1UV_N_CLEAR	GVDDUV1 latch clear register	0	No clear
			1	Clear

- Address 0X38 : Protection register2

The protection registers will show what kind of protection occurs from S1A/S1B/S2A/S2B.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP2_N	OCP2 register	0	OCP2 occur
			1	Normal
B[6]		reserved		
B[5]	A_HVUV2_N	HVUV2 register	0	HVUV2 occur
			1	Normal
B[4]	A_BSUV2_N	BSUV2 register	0	BSUV2 occur
			1	Normal
B[3]	A_BSOV2_N	BSOV2 register	0	BSOV2 occur
			1	Normal
B[2]	A_CKERR_N	Analog CKERR register	0	Analog CKERR occur
			1	Normal
B[1]	A_OVP2_N	OVP2 register	0	OVP2 occur
			1	Normal
B[0]	A_GVDD2UV_N	GVDDUV2 register	0	GVDDUV2 occur
			1	Normal

- Address 0X39 : Protection latch register2

The protection registers will show what kind of protection ever occurred S1A/S1B/S2A/S2B.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP2_N_LATCH	OCP2 latch register	0	OCP2 ever occur
			1	Normal
B[6]		reserved		
B[5]	A_HVUV2_N__LATCH	HVUV2 latch register	0	UV2 ever occur
			1	Normal
B[4]	A_BSUV2_N_LATCH	BSUV2 latch register	0	BSUV2 ever occur
			1	Normal
B[3]	A_BSOV2_N_LATCH	BSOV2 latch register	0	BSOV2 ever occur
			1	Normal
B[2]	A_CKERR_N_LATCH	Analog CKERR latch register	0	CKERR ever occur
			1	Normal
B[1]	A_OVP2_N_LATCH	OVP2 latch register	0	OVP2 ever occur
			1	Normal
B[0]	A_GVDD2UV_N_LATCH	GVDDUV2 latch register	0	GVDDUV2 ever occur
			1	Normal

- Address 0X3A : Protection clear register2

The protection latch registers will show what kind of protection ever occurred S1A/S1B/S2A/S2B.

Using the protection clear registers can clear the corresponding protection latch registers.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP2_N_CLEAR	OCP2 latch clear register	0	No clear
			1	Clear
B[6]		reserved		
B[5]	A_HVUV2_N_CLEAR	HVUV2 latch clear register	0	No clear
			1	Clear
B[4]	A_BSUV2_N_CLEAR	BSUV latch clear register	0	No clear
			1	Clear
B[3]	A_BSOV2_N_CLEAR	BSOV latch clear register	0	No clear
			1	Clear
B[2]	A_CKERR_N_CLEAR	ANA CLCOK ERROR latch clear register	0	No clear
			1	Clear
B[1]	A_OVP2_N_CLEAR	OVP latch clear register	0	No clear
			1	Clear
B[0]	A_GVDD2UV_N_CLEAR	GVDDUV2 latch clear register	0	No clear
			1	Clear

- Address 0X3C : clock and FS detection

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	ASR_ERR	Auto sample rate detection error	0	Normal
			1	FS ERROR
B[6]	BCLK_FS_RATIO_ERR	BCLK/FS ratio error	0	Normal
			1	BCLK/FS ratio ERROR
B[5]	MCLK_FS_RATIO_ERR	MCLK/FS ratio error	0	Normal
			1	MCLK/FS ratio ERROR
B[4:1]		reserved		
B[0]	CLK_ERROR_METHOD	Clock error PD PLL	0	No PD PLL
			1	PD PLL

- Address 0X3D : Auto clock detection control

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	ASR_DET	Auto sample rate detection	0	Disable
			1	Enable
B[6]	BCLK_FS_RATIO_DET	Bit Clock/FS Ratio detection	0	Disable
			1	Enable
B[5]	MCLK_FS_RATIO_DET	Master Clock/FS Ratio detection	0	Disable
			1	Enable
B[4]	D_CKDET_EN	Digital Clock detection	0	Disable
			1	Enable
B[3]	FS_PMF_AUTO_EN	Sample rate and PMF auto change enable	0	Disable
			1	Enable
B[2]	A_CKDET_EN	Analog Clock detection	0	Disable
			1	Enable
B[1]	CKDET_SEL	Select A_CKDET or D_CKDET	0	D_CKDET
			1	A_CKDET
B[0]	CLK_ERROR_FADE_EN	Clock error fade	0	Disable
			1	Enable

RAM access

The procedure to read/write coefficient(s) from/to RAM is as followings:

Read a single coefficient from RAM:

1. Write 7-bis of address to I2C address-0X1D
2. Write 1 to R1 bit and write 1/0 to RBS in address-0X32
3. Read first 4-bits of coefficient in I2C address-0X1E
4. Read second 8-bits of coefficient in I2C address-0X1F
5. Read third 8-bits of coefficient in I2C address-0X20
6. Read fourth 8-bits of coefficient in I2C address-0X21

Read a set of coefficients from RAM:

1. Write 7-bits of address to I2C address-0X1D
2. Write 1 to RA bit and write 1/0 to RBS in address-0X32
3. Read first 4-bits of coefficient A1 in I2C address-0X1E
4. Read second 8-bits of coefficient A1 in I2C address-0X1F
5. Read third 8-bits of coefficient A1in I2C address-0X20
6. Read fourth 8-bits of coefficient A1 in I2C address-0X21
7. Read first 4-bits of coefficient A2 in I2C address-0X22
8. Read second 8-bits of coefficient A2 in I2C address-0X23
9. Read third 8-bits of coefficient A2 in I2C address-0X24
10. Read fourth 8-bits of coefficient A2 in I2C address-0X25
11. Read first 4-bits of coefficient B1 in I2C address-0X26
12. Read second 8-bits of coefficient B1 in I2C address-0X27
13. Read third 8-bits of coefficient B1 in I2C address-0X28
14. Read fourth 8-bits of coefficient B1 in I2C address-0X29
15. Read first 4-bits of coefficient B2 in I2C address-0X2A
16. Read second 8-bits of coefficient B2 in I2C address-0X2B
17. Read third 8-bits of coefficient B2 in I2C address-0X2C
18. Read fourth 8-bits of coefficient B2 in I2C address-0X2D
19. Read first 4-bits of coefficient A0 in I2C address-0X2E
20. Read second 8-bits of coefficient A0 in I2C address-0X2F
21. Read third 8-bits of coefficient A0 in I2C address-0X30
22. Read fourth 8-bits of coefficient A0 in I2C address-0X31

Write a single coefficient from RAM:

1. Write 7-bis of address to I2C address-0X1D
2. Write first 4-bits of coefficient in I2C address-0X1E
3. Write second 8-bits of coefficient in I2C address-0X1F
4. Write third 8-bits of coefficient in I2C address-0X20
5. Write fourth 8-bits of coefficient in I2C address-0X21
6. Write 1 to W1 bit and write 1/0 to RBS in address-0X32

Write a set of coefficients from RAM:

1. Write 7-bits of address to I2C address-0X1D
2. Write first 4-bits of coefficient A1 in I2C address-0X1E
3. Write second 8-bits of coefficient A1 in I2C address-0X1F
4. Write third 8-bits of coefficient A1 in I2C address-0X20
5. Write fourth 8-bits of coefficient A1 in I2C address-0X21
6. Write first 4-bits of coefficient A2 in I2C address-0X22
7. Write second 8-bits of coefficient A2 in I2C address-0X23
8. Write third 8-bits of coefficient A2 in I2C address-0X24
9. Write fourth 8-bits of coefficient A2 in I2C address-0X25
10. Write first 4-bits of coefficient B1 in I2C address-0X26
11. Write second 8-bits of coefficient B1 in I2C address-0X27
12. Write third 8-bits of coefficient B1 in I2C address-0X28
13. Write fourth 8-bits of coefficient B1 in I2C address-0X29
14. Write first 4-bits of coefficient B2 in I2C address-0X2A
15. Write second 8-bits of coefficient B2 in I2C address-0X2B
16. Write third 8-bits of coefficient B2 in I2C address-0X2C
17. Write fourth 8-bits of coefficient B2 in I2C address-0X2D
18. Write first 4-bits of coefficient A0 in I2C address-0X2E
19. Write second 8-bits of coefficient A0 in I2C address-0X2F
20. Write third 8-bits of coefficient A0 in I2C address-0X30
21. Write fourth 8-bits of coefficient A0 in I2C address-0X31
22. Write 1 to WA bit and write 1/0 to RBS in address-0X32

Note that: the read and write operation on RAM coefficients works only if LRCIN (pin-8) switching on rising edge. And, before each writing operation, it is necessary to read the address-0X32 to confirm whether RAM is writable current in first. If the logic of W1 or WA is high, the coefficient writing is prohibited.

- User-defined equalizer

The AD83586C provides 36 parametric Equalizer (EQ). User can program suitable coefficients via I^2C control interface to program the required audio band frequency response for every EQ. The transfer function

$$H(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 + B_1 z^{-1} + B_2 z^{-2}}$$

The data format of 2's complement binary code for EQ coefficient is 3.25. i.e., 3-bits for integer (MSB is the sign bit) and 25-bits for mantissa. Each coefficient range is from 0x8000000 (-4) to 0x7FFFFFF (+3.99999997). These coefficients are stored in User Defined RAM and are referenced in following manner:

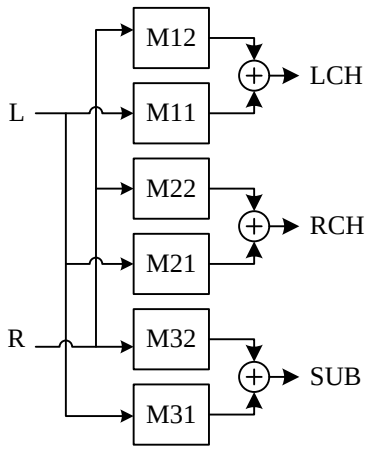
$$CHxEQyA0 = A0$$
$$CHxEQyA1 = A1$$
$$CHxEQyA2 = A2$$
$$CHxEQyB1 = -B1$$
$$CHxEQyB2 = -B2$$

Where *x* and *y* represents the number of channel and the band number of EQ biquard.

All user-defined filters are path-through, where all coefficients are defaulted to 0 after being powered up, except the A0 that is set to 0x2000000 which represents 1.

- Mixer

The AD83586C provides mixers to generate the extra audio source from the input left and right channels. The coefficients of mixers are defined in range from 0x8000000 (-1) to 0x7FFFFFF (0.9999998808). The function block diagram is as following:



- Pre-scale

For each audio channel, AD83586C can scale input signal level prior to mixing processing which is realized by a 28-bit signed fractional multiplier. The pre-scale factor, ranging from -16 (0x8000000) to 15.99999988(0x7FFFFFF), for this multiplier, can be loaded into RAM. The default values of the pre-scaling factors are set to 0x07e88e0. Programming of RAM is described in RAM access.

- Post-scale

The AD83586C provides an additional multiplication after equalizing and before interpolation stage, which is realized by a 28-bit signed fractional multiplier. The post-scaling factor, ranging from -4 (0x8000000) to 3.99999997 (0x7FFFFFF), for this multiplier, can be loaded into RAM. The default values of the post-scaling factors are set to 0x2000000. Left and right channels can use the channel-1 post-scale factor by setting the post-scale link. Programming of RAM is described in RAM access.

- Power Clipping

The AD83586C provides power clipping function to avoid excessive signal that may destroy loud speaker. 3. The power clipping level is defined by 28-bit representation and is stored in RAM address 0X54, 0XD4 of RAM bank 0, and 0X54 of RAM bank 1 respectively. The following table shows the power clipping level's numerical representation.

Sample calculation for power clipping

Max amplitude	dB	Linear	Decimal	Hex (3.25 format)
GAIN	0	1	33554432	2000000
GAIN *0.707	-3	0.707	23722976	169FBE0
GAIN *0.5	-6	0.5	16777216	1000000
GAIN *L	x	$L=10^{(x/20)}$	D=33554432xL	H=dec2hex(D)

- DRC threshold

The AD83586C provides DRC function. When the input RMS exceeds the programmable DRC threshold value, the output power will be limited by this threshold power level via gradual gain reduction. Three sets of DRC are provided, which are used of channel 1, channel 2, and channel3. DRC threshold is defined by 28-bit presentation and is stored in RAM address 0X4C, 0XCC of RAM bank 0, and RAM address 0X4C of RAM bank 1.

The following table shows the DRC threshold's numerical representation. "T" is the threshold of DRC.

The equation is

$$T_{dB} = (T - 24) / 6.0206(dB)$$

Ex: T=-6 db, TdB=(-6-24)/6.0206=-4.982892(dB)

T_{Dec}=-41799528

T_{Hex}=0XD823098

Vp=5*[10^((T+4)/20)]

Sample calculation for DRC threshold

Power	T	TdB	Decimal	Hex (5.23 format)
(Vp^2)/2R	-4	-4.65	-39012893	DACB5E3
	-7	-5.149	-43192845	D6CEDF3
	X	(x-24)/6.0206	D=2^23*TdB	H=dec2hex(D)

- DRC slope

The AD83586C DRC provides limiter and compressor. Using slope to decide compression factor. The relationship between the ratio R and the slope S is

$$S = 1 - \frac{1}{R}$$

$$R = \frac{1}{1-S} = \frac{x - Threshold(dB)}{y - Threshold(dB)}$$

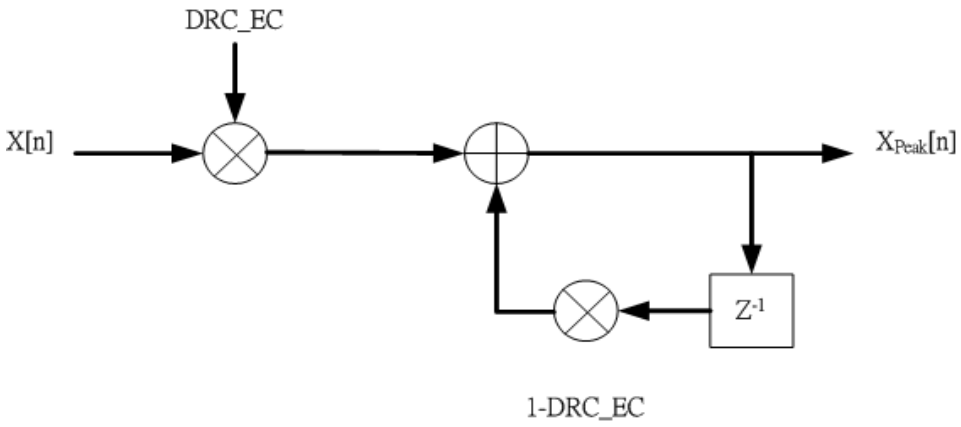
DRC slope is defined by 28bit and is stored in RAM address 0x4D, 0xCD of bank 0, and 0x4Dof bank 1

Ex: Setting DRC is limiter, S=1 (R=∞).

S_DEC=1*2^25 = 33554432

S_HEX = 0X2000000

- DRC Energy Coefficient



The above figure illustrates the digital processing of calculating Peak signal average. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Three sets of energy coefficients are provided and used for respective DRC. Energy coefficient is defined by 28-bit representation and is stored in RAM address 0X57, 0XD7 of RAM bank 0, and RAM address 0X57 of RAM bank 1. The following table shows the DRC energy coefficient numerical representation.

Sample calculation for DRC energy coefficient

DRC energy coefficient	dB	Linear	Decimal	Hex (1.27 format)
1	0	1	134217712	7FFFFF0
1/256	-48.2	1/256	524288	80000
1/1024	-60.2	1/1024	131072	20000
L	x	$L=10^{(x/20)}$	D=134217712xL	H=dec2hex(D)

- Noise Gate Attack Level

When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or mute if the noise gate function is enabled. Noise gate attack level is defined by 28-bit representation and is stored in RAM address 0X55 of RAM bank 0 and bank 1.

- Noise Gate Release Level

After entering the noise gating status, the noise gain will be removed whenever AD83586C receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 28-bit representation and is stored in RAM address 0X56 of RAM bank 0 and bank 1. The following table shows the noise gate attack and release threshold level's numerical representation.

Sample calculation for noise gate attack and release level

Input amplitude (dB)	Linear	Decimal	Hex (1.27 format)
0	1	134217712	7FFFFF0
-100	10^{-5}	1328	530
-110	$10^{-5.5}$	416	1A0
x	$L=10^{(x/20)}$	D=134217712xL	H=dec2hex(D)

The user defined RAM

The contents of user defined RAM is represented in following table.

RAM Bank selection = 0

Address	NAME	Coefficient	Default
0x00	1st SET Channel-1 EQ1	CH1EQ1A1	0x0000000
0x01		CH1EQ1A2	0x0000000
0x02		CH1EQ1B1	0x0000000
0x03		CH1EQ1B2	0x0000000
0x04		CH1EQ1A0	0x2000000
0x05	1st SET Channel-1 EQ2	CH1EQ2A1	0x0000000
0x06		CH1EQ2A2	0x0000000
0x07		CH1EQ2B1	0x0000000
0x08		CH1EQ2B2	0x0000000
0x09		CH1EQ2A0	0x2000000
0x0A	1st SET	CH1EQ3A1	0x0000000

0x0B	Channel-1 EQ3	CH1EQ3A2	0x0000000
0x0C		CH1EQ3B1	0x0000000
0x0D		CH1EQ3B2	0x0000000
0x0E		CH1EQ3A0	0x2000000
0x0F	1st SET Channel-1 EQ4	CH1EQ4A1	0x0000000
0x10		CH1EQ4A2	0x0000000
0x11		CH1EQ4B1	0x0000000
0x12		CH1EQ4B2	0x0000000
0x13		CH1EQ4A0	0x2000000
0x14	1st SET Channel-1 EQ5	CH1EQ5A1	0x0000000
0x15		CH1EQ5A2	0x0000000
0x16		CH1EQ5B1	0x0000000
0x17		CH1EQ5B2	0x0000000
0x18		CH1EQ5A0	0x2000000
0x19	1st SET Channel-1 EQ6	CH1EQ6A1	0x0000000
0x1A		CH1EQ6A2	0x0000000
0x1B		CH1EQ6B1	0x0000000
0x1C		CH1EQ6B2	0x0000000
0x1D		CH1EQ6A0	0x2000000
0x1E	1st SET Channel-1 EQ7	CH1EQ7A1	0x0000000
0x1F		CH1EQ7A2	0x0000000
0x20		CH1EQ7B1	0x0000000
0x21		CH1EQ7B2	0x0000000
0x22		CH1EQ7A0	0x2000000
0x23	1st SET Channel-1 EQ8	CH1EQ8A1	0x0000000
0x24		CH1EQ8A2	0x0000000
0x25		CH1EQ8B1	0x0000000
0x26		CH1EQ8B2	0x0000000
0x27		CH1EQ8A0	0x2000000
0x28	1st SET Channel-1 EQ9	CH1EQ9A1	0x0000000
0x29		CH1EQ9A2	0x0000000
0x2A		CH1EQ9B1	0x0000000
0x2B		CH1EQ9B2	0x0000000
0x2C		CH1EQ9A0	0x2000000
0x2D	1st SET Channel-1 EQ10	CH1EQ10A1	0x0000000
0x2E		CH1EQ10A2	0x0000000
0x2F		CH1EQ10B1	0x0000000

0x30		CH1EQ10B2	0x0000000
0x31		CH1EQ10A0	0x2000000
0x32	1st SET Channel-1 EQ11	CH1EQ11A1	0x0000000
0x33		CH1EQ11A2	0x0000000
0x34		CH1EQ11B1	0x0000000
0x35		CH1EQ11B2	0x0000000
0x36		CH1EQ11A0	0x2000000
0x37	1st SET Channel-1 EQ12	CH1EQ12A1	0x0000000
0x38		CH1EQ12A2	0x0000000
0x39		CH1EQ12B1	0x0000000
0x3A		CH1EQ12B2	0x0000000
0x3B		CH1EQ12A0	0x2000000
0x3C	HPF (for 2.1 filter)	CH1HPFA1	0xC05BA70
0x3D		CH1HPFA2	0x1FD22C0
0x3E		CH1HPFB1	0x3FA4190
0x3F		CH1HPFB2	0xE05B660
0x40		CH1HPFA0	0x1FD22C0
0x41	SRS EQ	CH1SRSA1	0x0000000
0x42		CH1SRSA2	0x0000000
0x43		CH1SRSB1	0x0000000
0x44		CH1SRSB2	0x0000000
0x45		CH1SRSA0	0x2000000
0x46	Channel-1 Mixer1	M11	0x7FFFFFF
0x47	Channel-1 Mixer2	M12	0x0000000
0x48	Channel-1 Prescale	C1PRS	0x07E88E0
0x49	Channel-1 Postscale	C1POS	0x2000000
0x4A	Channel-3 Mixer1	M31	0x3FFFFFF
0x4B	Channel-3 Mixer2	M32	0x3FFFFFF
0x4C	DRC1 FF threshold	DRC1TH	0xE01C070
0x4D	DRC1 FF Slope	DRC1_Slope	0X2000000
0x4E	DRC1 FF aa	DRC1_AA	0X0004000
0X4F	DRC1 FF da	DRC1_DA	0X0004000
0X50	SRS GAIN	SRS_GAIN	0X2000000
0X51	CH1 COMPEN_FILTER A0	CH1_COMP_A0	0x1D7E6E0
0X52	CH1 COMPEN_FILTER A1	CH1_COMP_A1	0x02E7740
0X53	CH1 COMPEN_FILTER B1	CH1_COMP_B1	0x FF9A1E0
0X54	CH1 Power Clipping	PC1	0x20000000

0x55	CH12 Noise Gate Attack Level	CH12_NGAL	0x00001A0
0X56	CH12 Noise Gate Release Level	CH12_NGRL	0x0000530
0X57	DRC1 Energy Coefficient	DRC1_EC	0x0010000
0X58	DRC1 GAIN	C1_GAIN	Read only
0X59	DRC1 Power Meter	C1_RMS	Read only
0x5A	I2SO LCH GAIN	I2SO_L_GAIN	0X0800000
0x5B	AGC1 Attack threshold	AGC1_ATH	0X05A9DF0
0x5C	AGC1 Release threshold	AGC_RTH	0X047FAD0
0x5D	AGC1 Attack Rate	AGC1_AR	0X0000001
0x5E	AGC1 Release Rate	AGC1_RR	0X0000064
0x5F	AGC1 Attack Time	AGC1_AT	0X0000001
0x60	AGC1 Release Time	AGC1_RT	0X0000064
0X61-0x7F	Reserved		
0x80	1st SET Channel-2 EQ1	CH2EQ1A1	0x000000
0x81		CH2EQ1A2	0x000000
0x82		CH2EQ1B1	0x000000
0x83		CH2EQ1B2	0x000000
0x84		CH2EQ1A0	0x200000
0x85	1st SET Channel-2 EQ2	CH2EQ2A1	0x000000
0x86		CH2EQ2A2	0x000000
0x87		CH2EQ2B1	0x000000
0x88		CH2EQ2B2	0x000000
0x89		CH2EQ2A0	0x200000
0x8A	1st SET Channel-2 EQ3	CH2EQ3A1	0x000000
0x8B		CH2EQ3A2	0x000000
0x8C		CH2EQ3B1	0x000000
0x8D		CH2EQ3B2	0x000000
0x8E		CH2EQ3A0	0x200000
0x8F	1st SET Channel-2 EQ4	CH2EQ4A1	0x000000
0x90		CH2EQ4A2	0x000000
0x91		CH2EQ4B1	0x000000
0x92		CH2EQ4B2	0x000000
0x93		CH2EQ4A0	0x200000
0x94	1st SET Channel-2 EQ5	CH2EQ5A1	0x000000
0x95		CH2EQ5A2	0x000000
0x96		CH2EQ5B1	0x000000
0x97		CH2EQ5B2	0x000000

0x98		CH2EQ5A0	0x200000
0x99	1st SET Channel-2 EQ6	CH2EQ6A1	0x000000
0x9A		CH2EQ6A2	0x000000
0x9B		CH2EQ6B1	0x000000
0x9C		CH2EQ6B2	0x000000
0x9D		CH2EQ6A0	0x200000
0x9E	1st SET Channel-2 EQ7	CH2EQ7A1	0x000000
0x9F		CH2EQ7A2	0x000000
0xA0		CH2EQ7B1	0x000000
0xA1		CH2EQ7B2	0x000000
0xA2		CH2EQ7A0	0x200000
0xA3	1st SET Channel-2 EQ8	CH2EQ8A1	0x000000
0xA4		CH2EQ8A2	0x000000
0xA5		CH2EQ8B1	0x000000
0xA6		CH2EQ8B2	0x000000
0xA7		CH2EQ8A0	0x200000
0xA8	1st SET Channel-2 EQ9	CH2EQ9A1	0x000000
0xA9		CH2EQ9A2	0x000000
0xAA		CH2EQ9B1	0x000000
0xAB		CH2EQ9B2	0x000000
0xAC		CH2EQ9A0	0x200000
0xAD	1st SET Channel-2 EQ10	CH2EQ10A1	0x000000
0xAE		CH2EQ10A2	0x000000
0xAF		CH2EQ10B1	0x000000
0xB0		CH2EQ10B2	0x000000
0xB1		CH2EQ10A0	0x200000
0xB2	1st SET Channel-2 EQ11	CH2EQ11A1	0x000000
0xB3		CH2EQ11A2	0x000000
0xB4		CH2EQ11B1	0x000000
0xB5		CH2EQ11B2	0x000000
0xB6		CH2EQ11A0	0x200000
0xB7	1st SET Channel-2 EQ12	CH2EQ12A1	0x000000
0xB8		CH2EQ12A2	0x000000
0xB9		CH2EQ12B1	0x000000
0xBA		CH2EQ12B2	0x000000
0xBB		CH2EQ12A0	0x200000
0xBC	HPF	CH2HPFA1	0xC05BA70

0xBD	(for 2.1 filter)	CH2HPFA2	0x1FD22C0
0xBE		CH2HPFB1	0x3FA4190
0xBF		CH2HPFB2	0xE05B660
0xC0		CH2HPFA0	0x1FD22C0
0xC1	SRS EQ	CH2SRSA1	0x0000000
0xC2		CH2SRSA2	0x0000000
0xC3		CH2SRSB1	0x0000000
0xC4		CH2SRSB2	0x0000000
0xC5		CH2SRSA0	0x2000000
0xC6	Channel-2 Mixer1	M21	0x000000
0xC7	Channel-2 Mixer2	M22	0x7FFFFF
0xC8	Channel-2 Prescale	C2PRS	0x07E88E0
0xC9	Channel-2 Postscale	C2POS	0x2000000
0xCA	Reserved		
0xCB	Reserved		
0xCC	DRC2 FF threshold	DRC2TH	0xe01c070
0xCD	DRC2 FF Slope	DRC2_Slope	0X2000000
0xCE	DRC2 FF aa	DRC2_AA	0X0004000
0xCF	DRC2 FF da	DRC2_DA	0X0004000
0xD0	Reserved		
0xD1	CH2 COMPEN_FILTER A0	CH2_COMP_A0	0x1D7E6E0
0xD2	CH2 COMPEN_FILTER A1	CH2_COMP_A1	0x02E7740
0xD3	CH2 COMPEN_FILTER B1	CH2_COMP_B1	0x FF9A1E0
0xD4	CH2 Power Clipping	PC2	0x2000000
0XD5	Reserved		
0XD6	Reserved		
0XD7	DRC2 Energy Coefficient	DRC2_EC	0x0010000
0XD8	DRC2 GAIN	C2_GAIN	Read only
0xD9	DRC2 Power Meter	C2_RMS	Read only
0xDA	I2SO RCH GAIN	I2SO_R_GAIN	0X0800000
0xDB	AGC2 Attack threshold	AGC2_ ATH	0X05A9DF0
0xDC	AGC2 Release threshold	AGC2_RTH	0X047FAD0
0xDD	AGC2 Attack Rate	AGC2_AR	0X0000001
0xDE	AGC2 Release Rate	AGC2_RR	0X0000064
0xDF	AGC2 Attack Time	AGC2_AT	0X0000001
0xE0	AGC2 Release Time	AGC2_RT	0X0000064
0XE1~FF	Reserved		

RAM Bank selection = 1

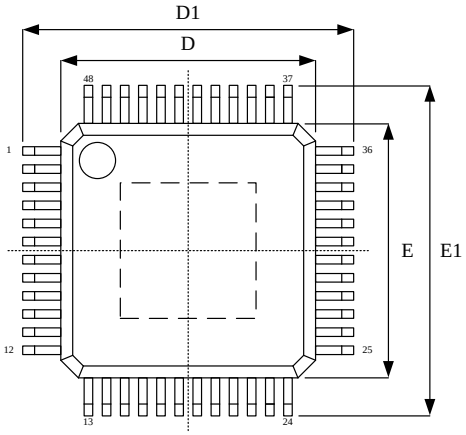
Address	NAME	Coefficient	Default
0x00	1st SET Channel-3 EQ1	CH3EQ1A1	0x0000000
0x01		CH3EQ1A2	0x0000000
0x02		CH3EQ1B1	0x0000000
0x03		CH3EQ1B2	0x0000000
0x04		CH3EQ1A0	0x2000000
0x05	1st SET Channel-3 EQ2	CH3EQ2A1	0x0000000
0x06		CH3EQ2A2	0x0000000
0x07		CH3EQ2B1	0x0000000
0x08		CH3EQ2B2	0x0000000
0x09		CH3EQ2A0	0x2000000
0x0A	1st SET Channel-3 EQ3	CH3EQ3A1	0x0000000
0x0B		CH3EQ3A2	0x0000000
0x0C		CH3EQ3B1	0x0000000
0x0D		CH3EQ3B2	0x0000000
0x0E		CH3EQ3A0	0x2000000
0x0F	1st SET Channel-3 EQ4	CH3EQ4A1	0x0000000
0x10		CH3EQ4A2	0x0000000
0x11		CH3EQ4B1	0x0000000
0x12		CH3EQ4B2	0x0000000
0x13		CH3EQ4A0	0x2000000
0x14	1st SET Channel-3 EQ5	CH3EQ5A1	0x0000000
0x15		CH3EQ5A2	0x0000000
0x16		CH3EQ5B1	0x0000000
0x17		CH3EQ5B2	0x0000000
0x18		CH3EQ5A0	0x2000000
0x19	1st SET Channel-3 EQ6	CH3EQ6A1	0x0000000
0x1A		CH3EQ6A2	0x0000000
0x1B		CH3EQ6B1	0x0000000
0x1C		CH3EQ6B2	0x0000000
0x1D		CH3EQ6A0	0x2000000
0x1E	1st SET Channel-3 EQ7	CH3EQ7A1	0x0000000
0x1F		CH3EQ7A2	0x0000000
0x20		CH3EQ7B1	0x0000000
0x21		CH3EQ7B2	0x0000000
0x22		CH3EQ7A0	0x2000000

0x23	1st SET Channel-3 EQ8	CH3EQ8A1	0x0000000
0x24		CH3EQ8A2	0x0000000
0x25		CH3EQ8B1	0x0000000
0x26		CH3EQ8B2	0x0000000
0x27		CH3EQ8A0	0x2000000
0x28	1st SET Channel-3 EQ9	CH3EQ9A1	0x0000000
0x29		CH3EQ9A2	0x0000000
0x2A		CH3EQ9B1	0x0000000
0x2B		CH3EQ9B2	0x0000000
0x2C		CH3EQ9A0	0x2000000
0x2D	1st SET Channel-3 EQ10	CH3EQ10A1	0x0000000
0x2E		CH3EQ10A2	0x0000000
0x2F		CH3EQ10B1	0x0000000
0x30		CH3EQ10B2	0x0000000
0x31		CH3EQ10A0	0x2000000
0x32	1st SET Channel-3 EQ11	CH3EQ11A1	0x0000000
0x33		CH3EQ11A2	0x0000000
0x34		CH3EQ11B1	0x0000000
0x35		CH3EQ11B2	0x0000000
0x36		CH3EQ11A0	0x2000000
0x37	1st SET Channel-3 EQ12	CH3EQ12A1	0x0000000
0x38		CH3EQ12A2	0x0000000
0x39		CH3EQ12B1	0x0000000
0x3A		CH3EQ12B2	0x0000000
0x3B		CH3EQ12A0	0x2000000
0x3C	LPF (for 2.1 filter)	CH3LPFA1	0x0000400
0x3D		CH3LPFA2	0x0000200
0x3E		CH3LPFB1	0x3FA4190
0x3F		CH3LPFB2	0xE05B660
0x40		CH3LPFA0	0x0000200
0x41	Reserved		
0x42	Reserved		
0x43	Reserved		
0x44	Reserved		
0x45	Reserved		
0x46	Reserved		
0x47	Reserved		

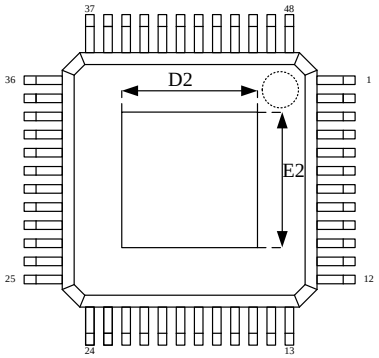
0x48	Channel-3 Prescale	C3PRS	0x07E88E0
0x49	Channel-3 Postscale	C3POS	0x2000000
0x4A	Reserved		
0x4B	Reserved		
0x4C	DRC3 FF threshold	DRC3_TH	0xe01c070
0x4D	DRC3 FF Slope	DRC3_Slope	0X2000000
0x4E	DRC3 FF aa	DRC3_AA	0X0004000
0X4F	DRC3 FF da	DRC3_DA	0X0004000
0X50	Reserved		
0X51	CH3 COMPEN_FILTER A0	CH3_COMP_A0	0x1D7E6E0
0X52	CH3 COMPEN_FILTER A1	CH3_COMP_A1	0x02E7740
0X53	CH3 COMPEN_FILTER B1	CH3_COMP_B1	0x FF9A1E0
0X54	CH3 Power Clipping	PC3	0x2000000
0x55	CH3 Noise Gate Attack Level	CH3_NGAL	0x00001A0
0X56	CH3 Noise Gate Release Level	CH3_NGRL	0x0000530
0X57	DRC3 Energy Coefficient	DRC3_EC	0x0010000
0X58	DRC3 GAIN	C3_GAIN	Read only
0X59	DRC3 Power Meter	C3_RMS	Read only
0x5A	I2SO SUB GAIN	I2SO_S_GAIN	0X0800000
0x5B	AGC3 Attack threshold	AGC3_ATH	0X05A9DF0
0x5C	AGC3 Release threshold	AGC3_RTH	0X047FAD0
0x5D	AGC3 Attack Rate	AGC3_AR	0X0000001
0x5E	AGC3 Release Rate	AGC3_RR	0X0000064
0x5F	AGC3 Attack Time	AGC3_AT	0X0000001
0x60	AGC3 Release Time	AGC3_RT	0X0000064
0X61-0x7F	Reserved		

Package Dimensions

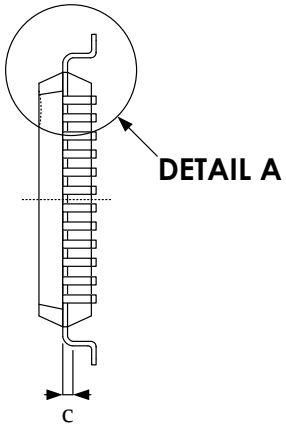
- E-LQFP-48L (7mm x 7mm)

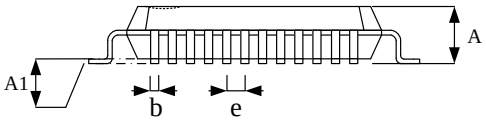


TOP VIEW

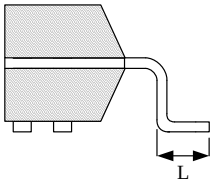


BOTTOM VIEW





SIDE VIEW



DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.17	0.27
c	0.09	0.20
D	6.90	7.10
D1	8.90	9.10
E	6.90	7.10
E1	8.90	9.10
e	0.50 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	4.31	5.21
E2	4.31	5.21

Revision History

Revision	Date	Description
0.1	2024.01.30	Original.
1.0	2024.03.01	Modify reversion to 1.0 from 0.1 for RP

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