Fast, High Voltage Drive, 6-Channel Output DecDriver® Decimating LCD Panel Driver

AD8381

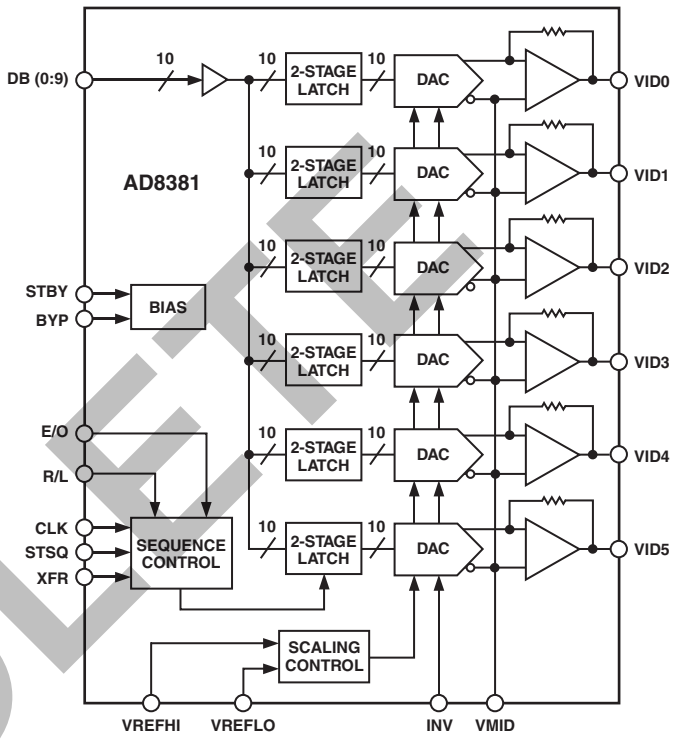
FEATURES

- High Voltage Drive:
  - Rated Settling Time to within 1.3 V of Supply Rails
- Output Overload Protection
- High Update Rates:
  - Fast, 100 Ms/s 10-Bit Input Word Rate
- Low Power Dissipation: 570 mW
  - Includes STBY Function
- Voltage Controlled Video Reference (Brightness) and Full-Scale (Contrast) Output Levels
- 3.3 V or 5 V Logic and 9 V to 18 V Analog Supplies
- High Accuracy:
  - Laser Trimming Eliminates External Calibration
- Flexible Logic:
  - INV Reverses Polarity of Video Signal
  - STSQ/XFR for Parallel AD8381 Operation in 12-Channel Systems
- Drives Capacitive Loads:
  - 27 ns Settling Time to 1% into 150 pF Load
  - Slew Rate 265 V/μs with 150 pF Load
- Available in 48-Lead LQFP

APPLICATIONS

- LCD Analog Column Driver

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD8381 provides a fast, 10-bit latched decimating digital input, which drives six high voltage outputs. Ten-bit input words are sequentially loaded into six separate high speed, bipolar DACs. Flexible digital input format allows several AD8381s to be used in parallel for higher resolution displays. STSQ synchronizes sequential input loading, XFR controls synchronous output updating and R/L controls the direction of loading as either left-to-right or right-to-left. Six channels of high voltage output drivers drive to within 1.3 V of the rail in rated settling time. The output signal can be adjusted for brightness, signal inversion, and contrast for maximum flexibility.

The AD8381 is fabricated on ADI's proprietary, fast bipolar 24 V process, providing fast input logic, bipolar DACs with trimmed accuracy and fast settling, high voltage precision drive amplifiers on the same chip.

The AD8381 dissipates 570 mW nominal static power. The STBY pin reduces power to a minimum, with fast recovery.

The AD8381 is offered in a 48-lead 7 mm × 7 mm × 1.4 mm LQFP package and operates over the commercial temperature range of 0°C to 85°C.

REV. B

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AD8381* Product Page Quick Links

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Comparable Parts

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Documentation

Data Sheet

- AD8381: Fast, High Voltage Drive, 6-Channel Output DecDriver™ Decimating LCD Panel Driver Data Sheet

Design Resources

- AD8381 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all AD8381 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

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AD8381–SPECIFICATIONS (@ 25°C, AVCC = 15.5 V, DVCC = 3.3 V, VREFLO = VMID = 7 V, VREFHI = 9.5 V, T_{MIN} = 0°C, T_{MAX} = 85°C, unless otherwise noted.)

Model	Conditions	Min	Typ	Max	Unit
VIDEO DC PERFORMANCE[1]	T_{MIN} to T_{MAX}				
VDE	DAC Code 450 to 800	–7.5	+1.0	+7.5	mV
VCME	DAC Code 450 to 800	–3.5	+0.5	+3.5	mV
REFERENCE INPUTS	(VREFHI – VREFLO) = 2.5 V				
VMID Range[2]		6.25		9.25	V
VMID Bias Current			35	77	µA
VREFHI		VREFLO		AVCC	V
VREFLO		VMID – 0.5		VREFHI	V
VREFHI Input Resistance	to VREFLO		20		kΩ
VREFLO Bias Current			0.01	0.07	µA
VREFHI Input Current			125	165	µA
VFS Range[3]		0		5.75	V
RESOLUTION					
Coding	Binary	10			Bits
DIGITAL INPUT CHARACTERISTICS	CLK Rise and Fall Time = 5 ns				
Input Data Update Rate	NRZ			100	Ms/s
CLK to Data Setup Time: t_1		0			ns
CLK to STSQ Setup Time: t_3		0			ns
CLK to XFR Setup Time: t_5		0			ns
CLK to Data Hold Time: t_2		5			ns
CLK to STSQ Hold Time: t_4		5			ns
CLK to XFR Hold Time: t_6		5			ns
$t_{CLK\ HIGH}$	E/O = HIGH	4.5			ns
$t_{CLK\ LOW}$		3.5			ns
C_{IN}				3	pF
I_{IH}			0.6	0.7	µA
I_{IL}			0.05	0.16	µA
V_{IH}		2.0			V
V_{IL}				0.8	V
V_{TH}	Threshold Voltage		1.4		V
VIDEO OUTPUT CHARACTERISTICS					
Output Voltage Swing	AVCC – VOH, VOL – AGND		1	1.3	V
CLK to VID Delay[4]: t_7	50% of VIDx	13.5	15.5	17.5	ns
INV to VID Delay	50% of VIDx	12	14	16	ns
Output Current		30	75		mA
Output Resistance			29		Ω
VIDEO OUTPUT DYNAMIC PERFORMANCE	T_{MIN} to T_{MAX}, V_O = 5 V Step, C_L = 150 pF				
Data Switching Slew Rate			265		V/µs
Invert Switching Slew Rate			410		V/µs
Data Switching Settling Time to 1%			27	32	ns
Data Switching Settling Time to 0.25%			50	75	ns
Invert Switching Settling Time to 1%			33	40	ns
Invert Switching Settling Time to 0.25%			55	100	ns
CLK and Data Feedthrough[5]			5		mV p-p
All-Hostile Crosstalk[6]					
Amplitude			50		mV p-p
Glitch Duration			45		ns
POWER SUPPLY					
Supply Rejection (VDE)	AVCCx = +15.5 V ± 1 V		0.6		mV/V
DVCC, Operating Range		3		5.5	V
DVCC, Quiescent Current			18	25	mA
AVCC, Operating Range		9		18	V
Total AVCC Quiescent Current			33	40	mA
STBY AVCC Current	STBY = H		1.8	3	mA
STBY DVCC Current	STBY = H		0.03	0.1	mA
OPERATING TEMPERATURE RANGE		0		85	°C

NOTES
[1]VDE = Differential error voltage. VCME = Common-mode error voltage. See the Theory of Operation section.
[2]See Figure 6 in Theory of Operation section.
[3]VFS = 2 × (VREFHI – VREFLO). See the Theory of Operation section.
[4]Measured from 50% of falling CLK edge to 50% of output change. Measurement is made for both states of INV.
[5]Measured on one output as CLK is driven and STSQ and XFR are held low.
[6]Measured on one output as the other five are changing from 0x000 to 0x3FF for both states of INV.

Specifications subject to change without notice.

TIMING CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Unit
t_1 CLK to Data Setup Time	CLK Rise and Fall Time = 5 ns	0			ns
t_2 CLK to Data Hold Time	CLK Rise and Fall Time = 5 ns	5			ns
t_3 CLK to STSQ Setup Time	CLK Rise and Fall Time = 5 ns	0			ns
t_4 CLK to STSQ Hold Time	CLK Rise and Fall Time = 5 ns	5			ns
t_5 CLK to XFR Setup Time	CLK Rise and Fall Time = 5 ns	0			ns
t_6 CLK to XFR Hold Time	CLK Rise and Fall Time = 5 ns	5			ns
t_7 CLK to VID Delay		13.5	15.5	17.5	ns

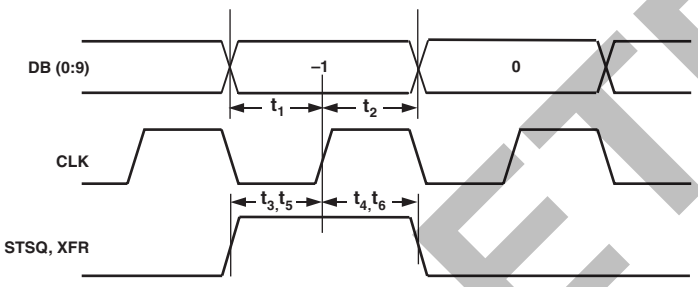


Figure 1. Timing Requirement E/O = High

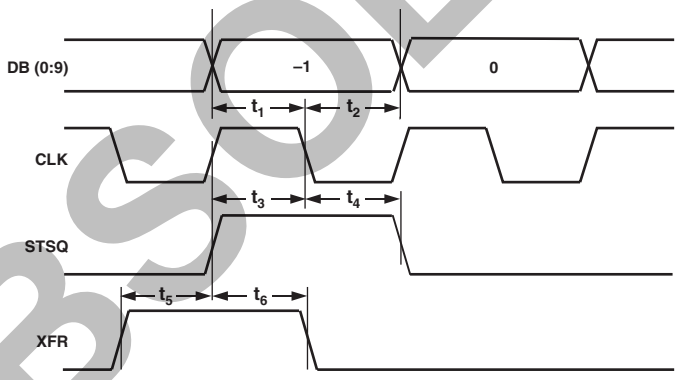


Figure 2. Timing Requirements E/O = Low

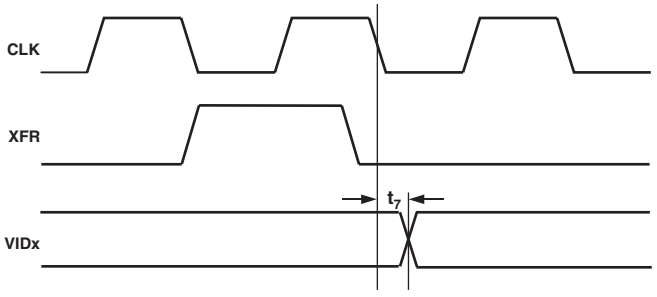


Figure 3. Output Timing

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages
- AVCCx – AGND . . . . . 19 V
- DVCC – DGND . . . . . 5.5 V

Input Voltages
- Maximum Digital Input Voltages . . . . . DVCC + 0.5 V
- Minimum Digital Input Voltages . . . . . DGND – 0.5 V
- Maximum Analog Input Voltages . . . . . AVCC + 0.5 V
- Minimum Analog Input Voltages . . . . . AGND – 0.5 V

Internal Power Dissipation[2]
- LQFP Package @ 25°C Ambient . . . . . 2.7 W

Output Short Circuit Duration . . . . . Infinite
Operating Temperature Range . . . . . 0°C to 85°C
Storage Temperature Range . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES

[1]Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings for extended periods may reduce device reliability.

[2]48-lead LQFP Package:
- θ_{JA} = 45°C/W (Still Air, 4-Layer PCB)
- θ_{JC} = 19°C/W

Overload Protection

The AD8381 employs a two-stage overload protection circuit that consists of an output current limiter and a thermal shutdown.

The maximum current at any one output of the AD8381 is internally limited to 100 mA average. In the event of a momentary short circuit between a video output and a power supply rail (VCC or AGND), the output current limit is sufficiently low to provide temporary protection.

The thermal shutdown debiases the output amplifier when the junction temperature reaches the internally set trip point. In the event of an extended short circuit between a video output and a power supply rail, the output amplifier current continues to switch between 0 mA and 100 mA typ with a period determined by the thermal time constant and the hysteresis of the thermal trip point. The thermal shutdown provides long term protection by limiting the average junction temperature to a safe level.

Recovery from a momentary short circuit is fast, approximately 100 ns. Recovery from a thermal shutdown is slow and is dependent on the ambient temperature.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8381 is limited by its junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

To ensure proper operation within the specified operating temperature range, it is necessary to limit the maximum power dissipation as follows:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$$

where:

T_{JMAX} = 150°C.

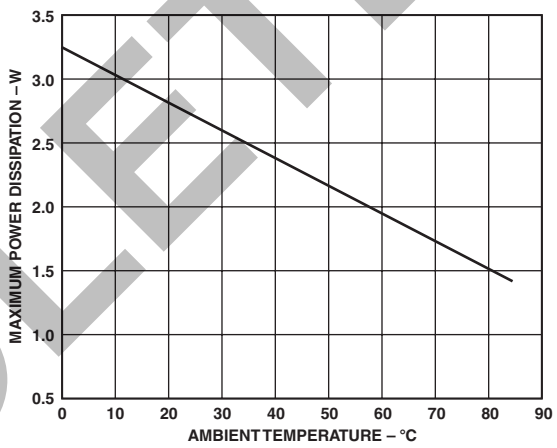


Figure 4. Maximum Power Dissipation vs. Temperature

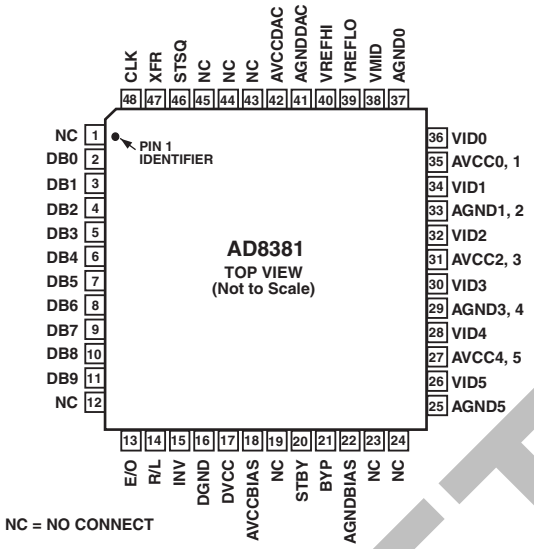
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8381JST	0°C to 85°C	48-Lead LQFP	ST-48
AD8381-EB		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8381 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

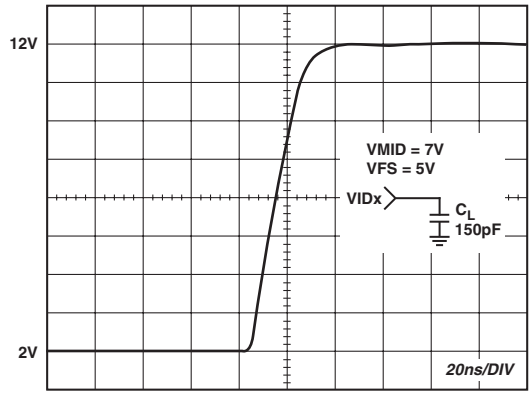
PIN CONFIGURATION



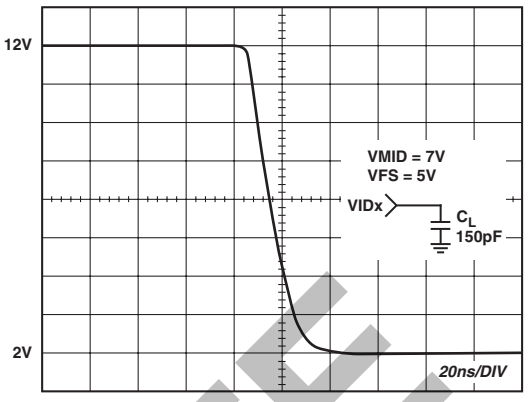
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function	Description
1, 12, 19, 23, 24, 43–45	NC	No Connect	
2–11	DB (0:9)	Data Input	10-Bit Data Input MSB = DB (9).
13	E/O	Even/Odd Select	The active CLK edge is the rising edge when this input is held high, and it is the falling edge when this input is held low. Data is loaded sequentially on the rising edges of CLK when this input is high and loaded on the falling edges when this input is low.
14	R/L	Right/Left Select	A new data loading sequence begins on the left, with Channel 0, when this input is low, and on the right, with Channel 5, when this input is high.
15	INV	Invert	When this pin is high, the analog output voltages are above VMID. When low, the analog output voltages are below VMID.
16	DGND	Digital Supply Return	This pin is normally connected to the analog ground plane.
17	DVCC	Digital Power Supply	Digital Power Supply.
18, 27, 31 35, 42	AVCCx	Analog Power Supplies	Analog Power Supplies.
20	STBY	Standby	When high, the internal circuits are debiased and the power dissipation drops to a minimum.
21	BYP	Bypass	A 0.1 µF capacitor connected between this pin and AGND ensures optimum settling time.
22, 25, 29 33, 37, 41	AGNDx	Analog Supply Returns	These pins are normally connected to the analog ground plane.
26, 28, 30, 32, 34, 36	VID5, VID4, VID3, VID2, VID1, VID0	Analog Outputs	These pins are directly connected to the analog inputs of the LCD panel.
38	VMID	Midpoint Reference	The voltage applied between this pin and AGND sets the midpoint reference of the analog outputs. This pin is normally connected to VCOM.
39	VREFLO	Full-Scale Reference	The voltage applied between Pins 39 and 40 sets the full-scale output voltage.
40	VREFHI	Full-Scale Reference	The voltage applied between Pins 39 and 40 sets the full-scale output voltage.
46	STSQ	Start Sequence	A new data loading sequence begins on the rising edge of CLK when this input was high on the preceding rising edge of CLK and the E/O input is held high. A new data loading sequence begins on the falling edge of CLK when this input was high on the preceding falling edge of CLK and the E/O input is held low.
47	XFR	Data Transfer	Data is transferred to the outputs on the immediately following falling edge of CLK when this input is high on the rising edge of CLK.
48	CLK	Clock	Clock Input.

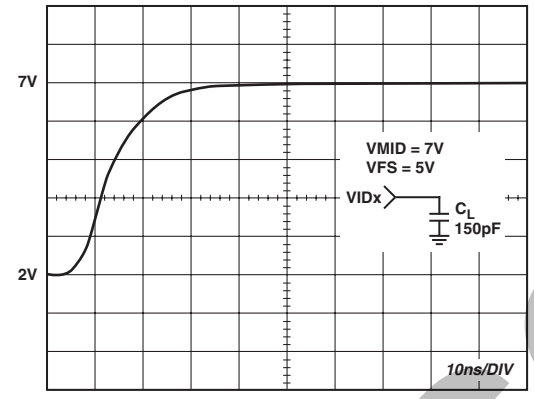
AD8381–Typical Performance Characteristics



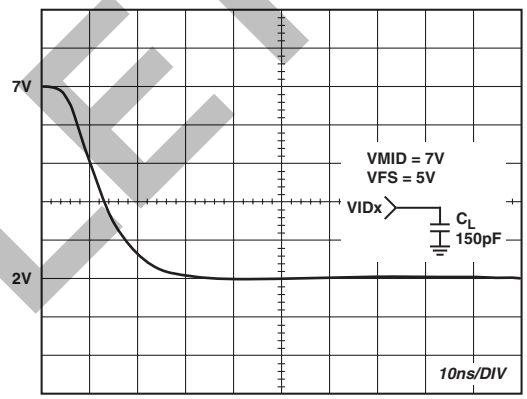
TPC 1. Invert Switching 10 V Step Response (Rise) at C_L



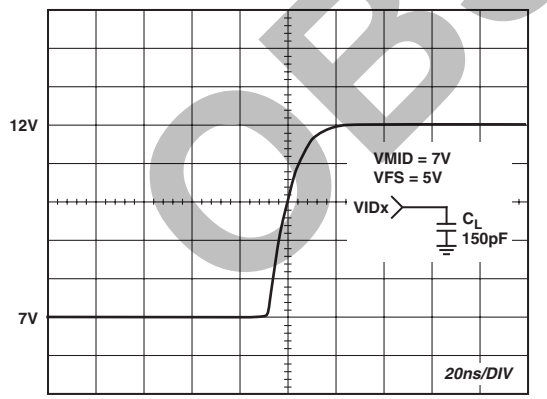
TPC 4. Invert Switching 10 V Step Response (Fall) at C_L



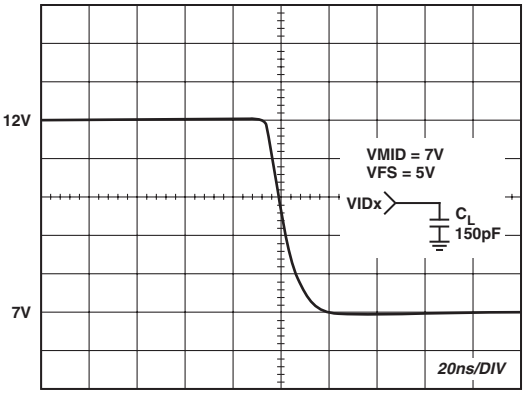
TPC 2. Data Switching 5 V Step Response (Rise) at C_L, INV = L



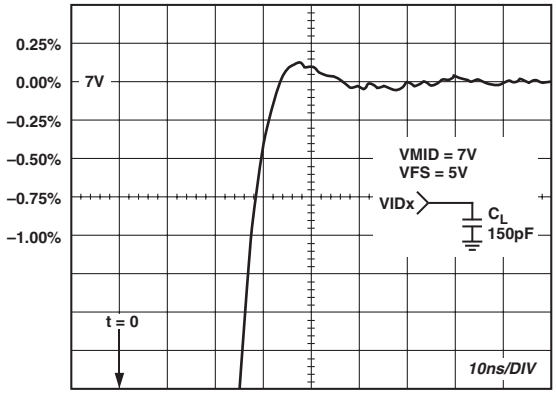
TPC 5. Data Switching 5 V Step Response (Fall) at C_L, INV = L



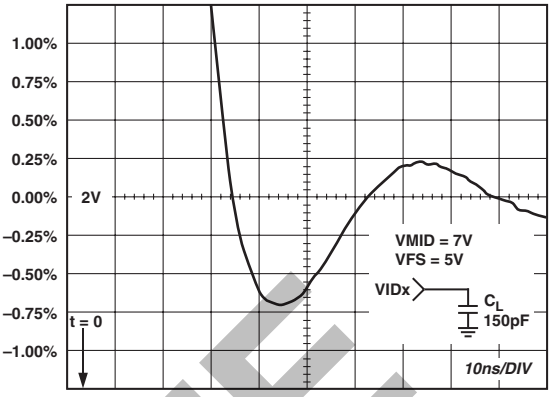
TPC 3. Data Switching 5 V Step Response (Rise) at C_L, INV = H



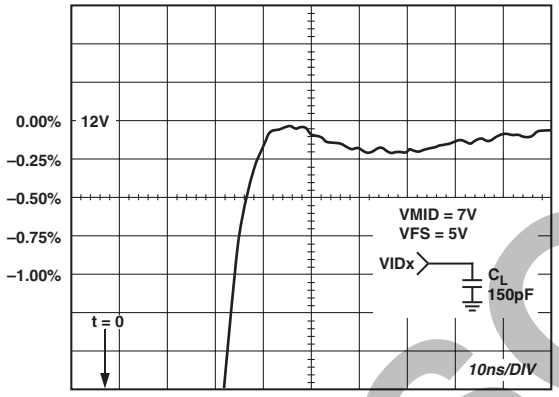
TPC 6. Data Switching 5 V Step Response (Fall) at C_L, INV = H



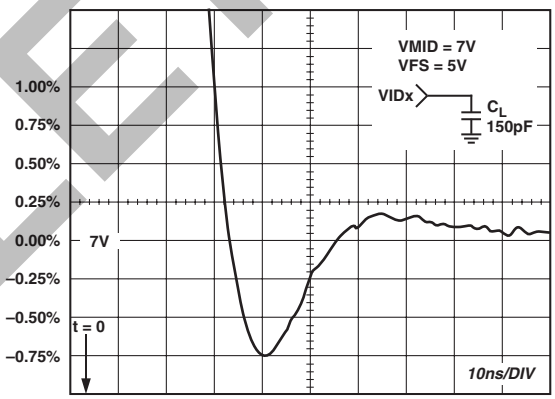
TPC 7. Output Settling Time (Rising Edge) at C_L, 5 V Step, INV = Low



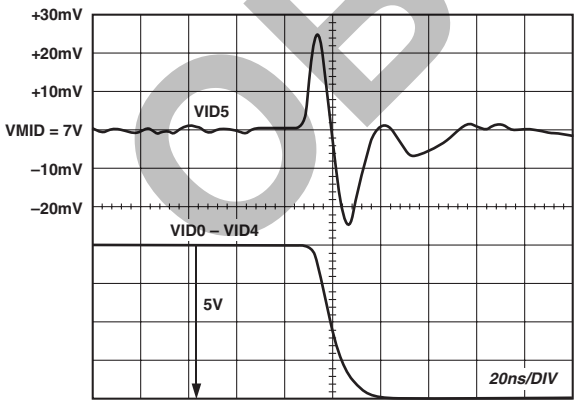
TPC 10. Output Settling Time (Falling Edge) at C_L, 5 V Step, INV = Low



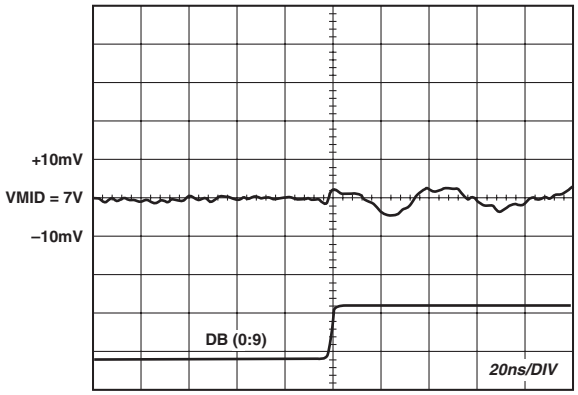
TPC 8. Output Settling Time (Rising Edge) at C_L, 5 V Step, INV = High



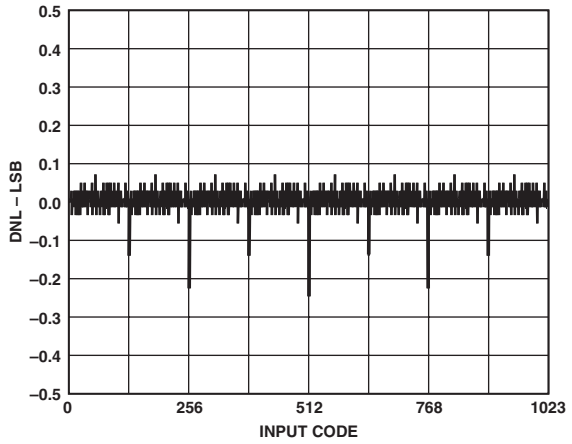
TPC 11. Output Settling Time (Falling Edge) at C_L, 5 V Step, INV = High



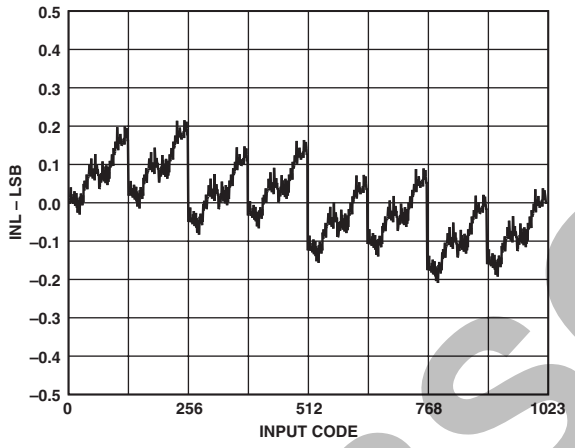
TPC 9. All-Hostile Crosstalk at C_L



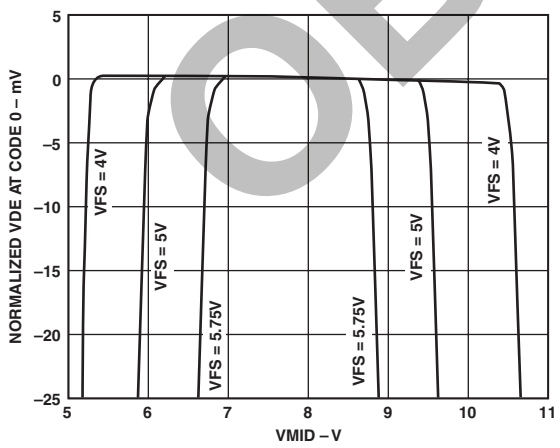
TPC 12. Data Switching Transient (Feedthrough) at C_L



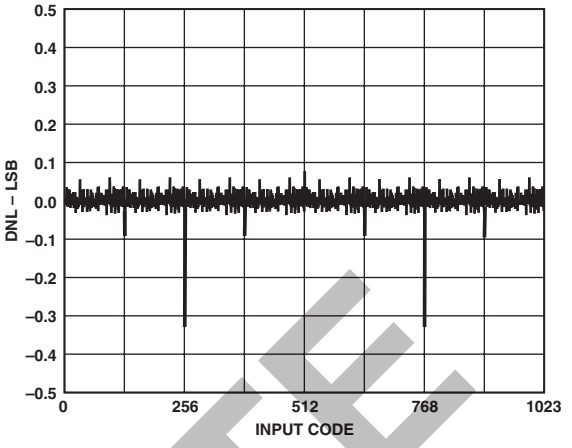
TPC 13. Differential Nonlinearity (DNL) vs. Code, INV = H



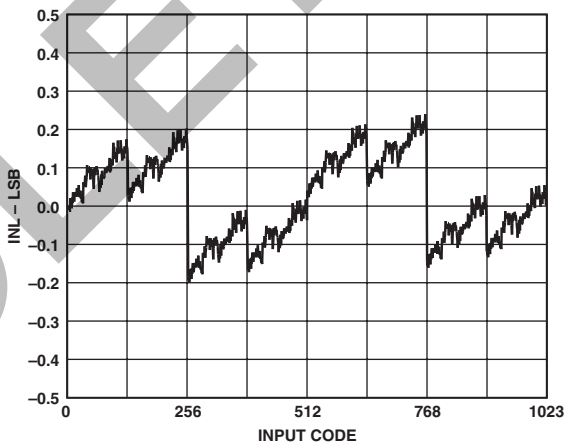
TPC 14. Integral Nonlinearity (INL) vs. Code, INV = H



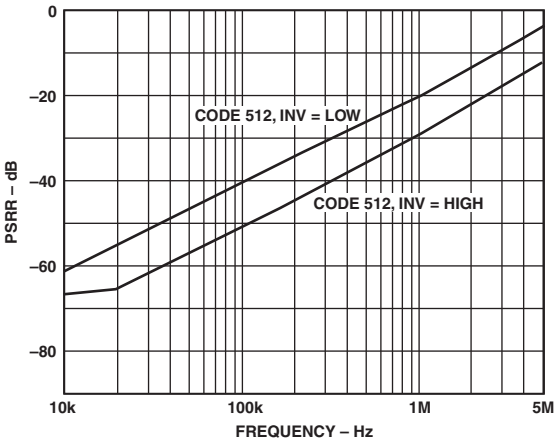
TPC 15. Normalized VDE at Code 0 vs. VMID, AVCC = 15.5 V



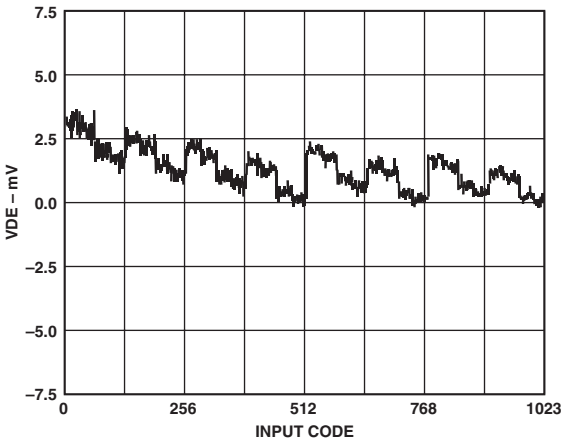
TPC 16. Differential Nonlinearity (DNL) vs. Code, INV = L



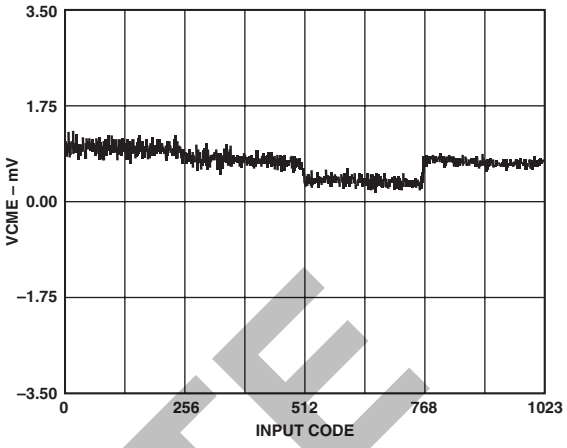
TPC 17. Integral Nonlinearity (INL) vs. Code, INV = L



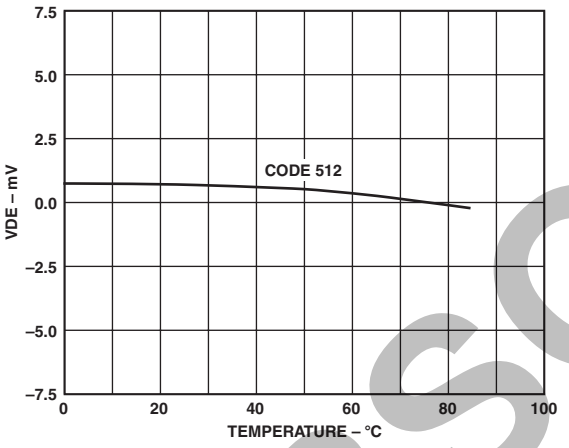
TPC 18. AVCC Power Supply Rejection vs. Frequency



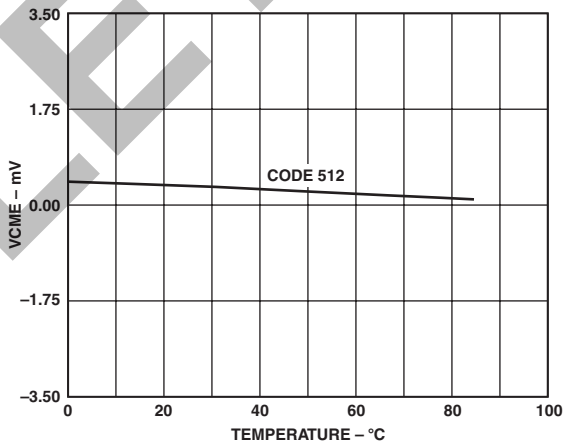
TPC 19. Differential Error Voltage (VDE) vs. Code



TPC 21. Common-Mode Error Voltage (VCME) vs. Code



TPC 20. Differential Error Voltage (VDE) vs. Temperature



TPC 22. Common-Mode Error (VCME) vs. Temperature

FUNCTIONAL DESCRIPTION

The AD8381 is a system building block designed to directly drive the columns of LCD panels of the type popularized for use in data projectors. It comprises six channels of precision 10-bit digital-to-analog converters loaded from a single, high speed, 10-bit-wide input. Precision current feedback amplifiers, providing well-damped pulse response and rapid voltage settling into large capacitive loads, buffer the six outputs. Laser trimming at the wafer level ensure low absolute output errors and tight channel-to-channel matching. In addition, tight part-to-part matching in high channel count systems is guaranteed by the use of an external voltage reference.

Input Data Loading (STart SeQuence Control—STSQ)
A valid STSQ control input initiates a new six-clock pulse loading cycle, during which six input data words are loaded sequentially into six internal channels. A new loading sequence begins on the current active CLK edge only when STSQ was held high at the preceding active CLK edge.

Data Loading—Expanded Systems (Even/Odd Control)
To facilitate expanded, even/odd systems, the active CLK edge, at which input data is loaded, is set with the E/O control input.

Input data is loaded on rising CLK edges while the E/O input is held high and loaded on falling CLK edges while the E/O input is held low.

Data Loading—Inverted Images (Right/Left Control)
To facilitate image mirroring, the order in which input data is loaded is set with the R/L input.

A new loading sequence begins at Channel 0 and proceeds to Channel 5 when the R/L input is held high and begins at Channel 5 and proceeding to Channel 0 when the R/L input is held low.

Data Transfer to Outputs (XFR Control)
Data transfer to all outputs is initiated by the XFR control input. When XFR is held high during a rising CLK edge, data is simultaneously transferred to all outputs on the immediately following falling CLK edge.

VCOM Reference (VMID Reference Input)
An external analog reference voltage connected to this input sets the reference level at the outputs. This input is normally connected to VCOM.

Full-Scale Output (VREFHI, VREFLO Reference Inputs)
The difference between two external analog reference voltages, connected to these inputs, sets the full-scale output voltage at the outputs. VREFLO is normally tied to VMID.

Analog Voltage Inversion (INVert Control)
To facilitate systems that use column, row or pixel inversion, the analog output voltage inversion is controlled by the INV control input. While INV is high, the analog voltage equivalent of the input code is subtracted from (VMID + VFS) at each output. While INV is low, the analog voltage equivalent of the input code is added to (VMID – VFS) at each output.

Standby Mode (STBY Control)
A high applied to the STBY input debiases the internal circuitry, dropping the quiescent power dissipation to a few milliwatts. Since both digital and analog circuits are debiased, all stored data will be lost. Upon returning STBY to low, normal operation is restored.

TRANSFER FUNCTION

The AD8381 has two regions of operation, selected by the INV input, where the video output voltages are either above or below a reference voltage, applied externally at the VMID input.

The transfer function defines the analog output voltage as the function of the digital input code as follows:

$$VOUT = VMID \pm VFS \times \left(1 - \frac{n}{1023}\right)$$

where:

n = input code

VFS = 2 × (VREFHI – VREFLO)

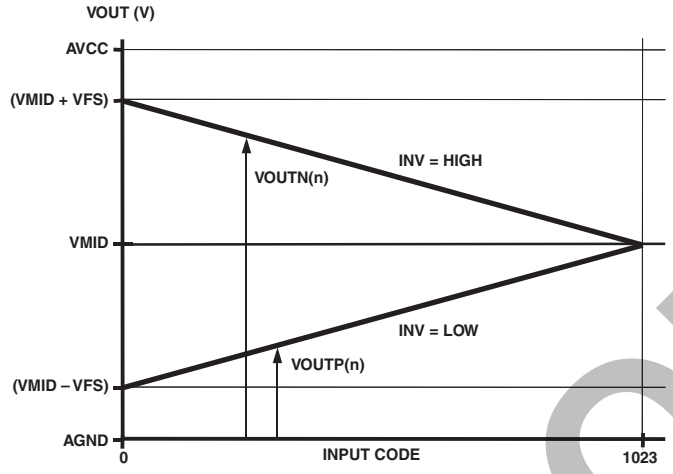


Figure 5. Transfer Function

The region over which the output voltage varies with input code is selected by the INV input. When INV is low, the output voltage increases from (VMID – VFS), (where VFS = the full-scale output voltage), to VMID as the input code increases from 0 to 1023. When INV is high, the output voltage decreases from (VMID + VFS) to VMID with increasing input code.

For each value of input code there are then two possible values of output voltage. When INV is low, the output is defined as VOUTP(n) where n is the input code and P indicates the operating region where the slope of the transfer function is positive. When INV is high, the output is defined as VOUTN(n) where N indicates the operating region where the slope of the transfer function is negative.

ACCURACY

To best correlate transfer function errors to image artifacts, the overall accuracy of the AD8381 is defined by two parameters, VDE and VCME.

VDE, the differential error voltage, measures the deviation of the rms value of the output from the rms value of the ideal. It is dependent on the difference between the output amplitudes VOUTN(n) and VOUTP(n) at a particular code. The defining expression is

$$VDE = \frac{1}{2} \times \left(VOUTN(n) - VOUTP(n)\right) - \left(VFS \times \left(1 - \frac{n}{1023}\right)\right)$$

where:

$\frac{1}{2} \times \left(VOUTN(n) - VOUTP(n)\right)$ is the rms value of the output.

$(VFS \times (1 - n/1023))$ is the rms value of the ideal.

VCME, the common-mode error voltage, measures the deviation of the average value of the output from the average value of the ideal. It is dependent on the average between the output amplitudes VOUTN(n) and VOUTP(n) at a particular code.

The defining expression is:

$$VCME = \frac{1}{2} \times \left(\frac{1}{2} \times \left(VOUTN(n) + VOUTP(n)\right) - VMID\right)$$

where:

$\frac{1}{2} \times \left(VOUTN(n) + VOUTP(n)\right)$ is the average value of the output.

$VMID$ is the average value of the ideal.

MAXIMUM FULL-SCALE OUTPUT VOLTAGE

The following conditions limit the range of usable output voltages:

- The internal DACs limit the minimum allowed voltage at the VMID input to 5.3 V.
- The scale factor control loop limits the maximum full-scale output voltage to 5.75 V.
- The output amplifiers settle cleanly at voltages within 1.3 V from the supply rails.
- The common-mode range of the output amplifiers limit the maximum value of VMID to AVCC – 3.

At any given valid value of VMID, the voltage required to reach any one of the above limits defines the maximum usable full-scale output voltage VFSMAX.

VFSMAX is the envelope in Figure 6. The valid range of VMID is the shaded area.

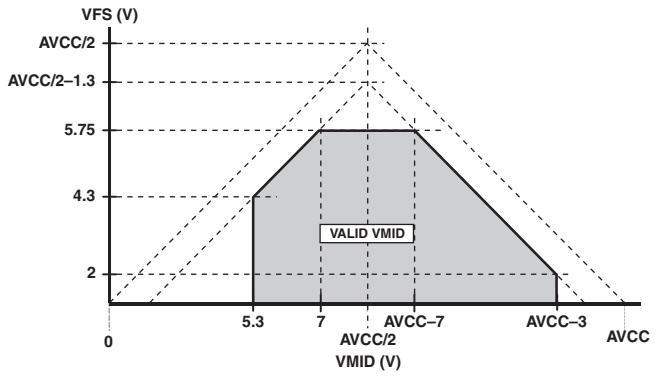


Figure 6. VFSMAX vs. VMID

Operating Modes—6-Channel Systems

The simplest full color LCD based system is characterized by an image processor with a single 10-bit-wide data bus and a 6-channel LCD per color.

Such systems usually have VGA or SVGA resolution and require a single AD8381 per color.

The INV input facilitates column and row inversion for these systems.

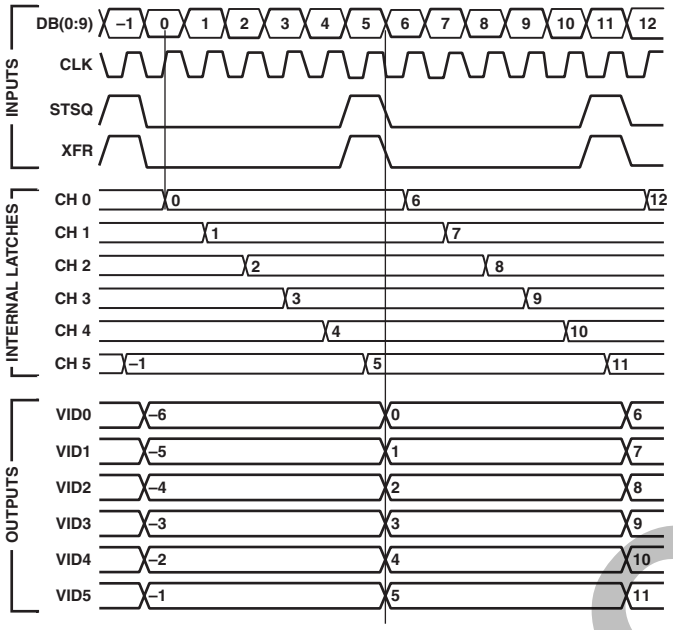


Figure 7. 6-Channel System Timing Diagram, E/O = H, R/L = Low

Operating Modes—12-Channel Systems

Single and dual data bus type 12-channel systems are commonly in use.

The single data bus 12-channel system is characterized by an image processor with a single, 10-bit data bus and a 12-channel LCD per color. The maximum resolution of such a system is usually up to 85 Hz XGA or 75 Hz SXGA and requires two AD8381s per color.

One AD8381 is set to run in even mode while the other is in odd mode. Both AD8381s share the same data bus and CLK. The timing diagram of such system is shown in Figure 8.

The dual data bus 12-channel system is characterized by an image processor with two 10-bit parallel data buses and a 12-channel LCD. The maximum resolution of such system is usually up to 75 Hz UXGA and requires two AD8381s per color.

Both AD8381s may be set to run in Even mode and may share the same CLK. The timing diagram of each AD8381 in such system is identical to that of the 6-channel system.

The INV input facilitates column, row, and pixel inversion for both types of 12-channel systems.

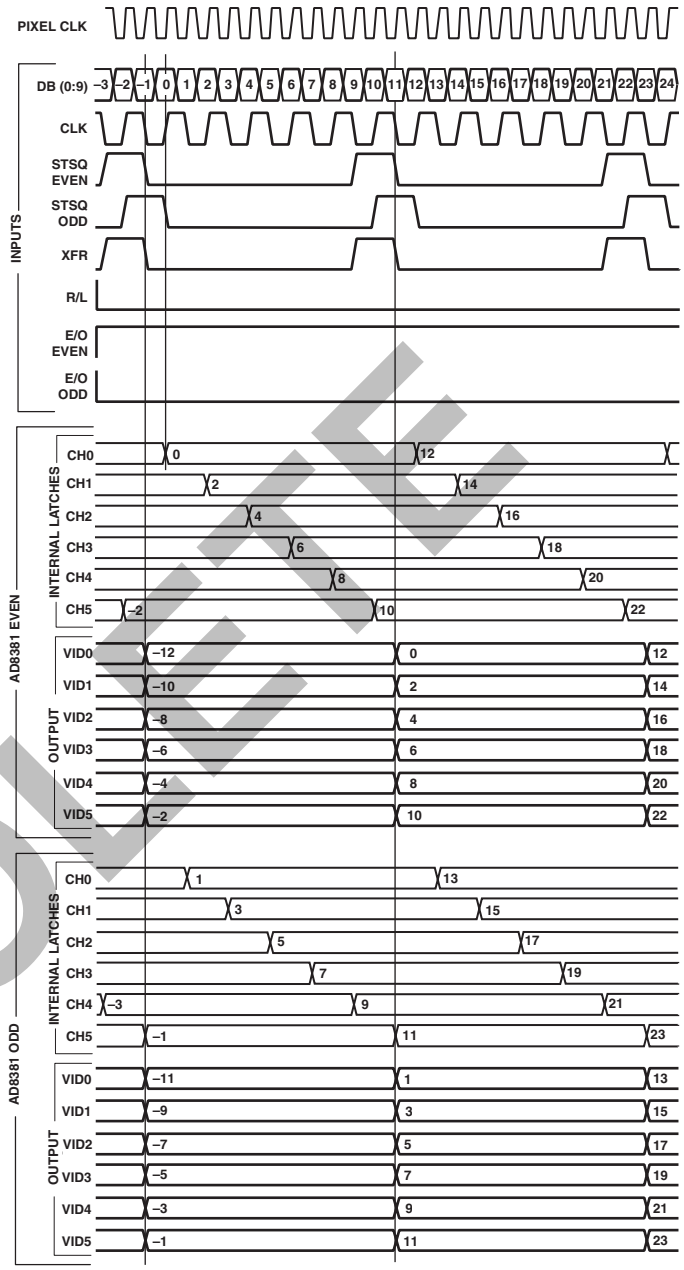


Figure 8. Twelve-Channel Even/Odd System Timing Diagram

Operating Modes—Large Channel Count Systems

To facilitate 18, 24, or higher channel systems, any number of required AD8381s may be cascaded.

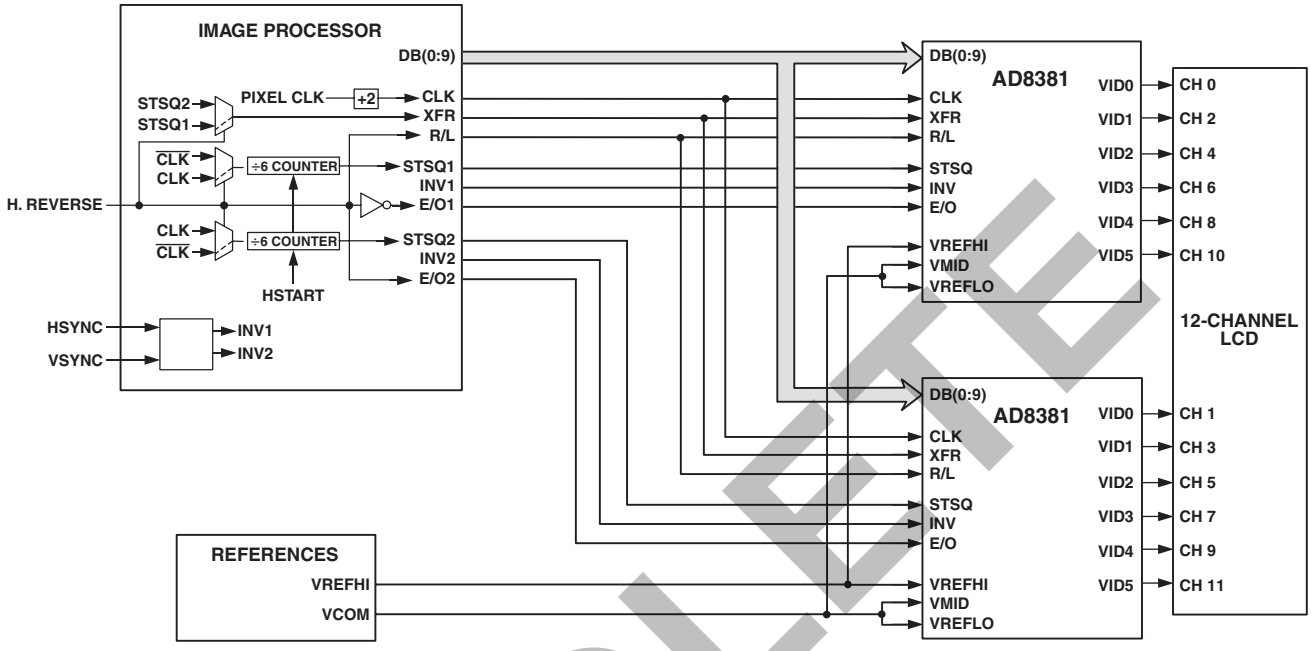


Figure 9. Single Data Bus 12-Channel Even/Odd System Block Diagram

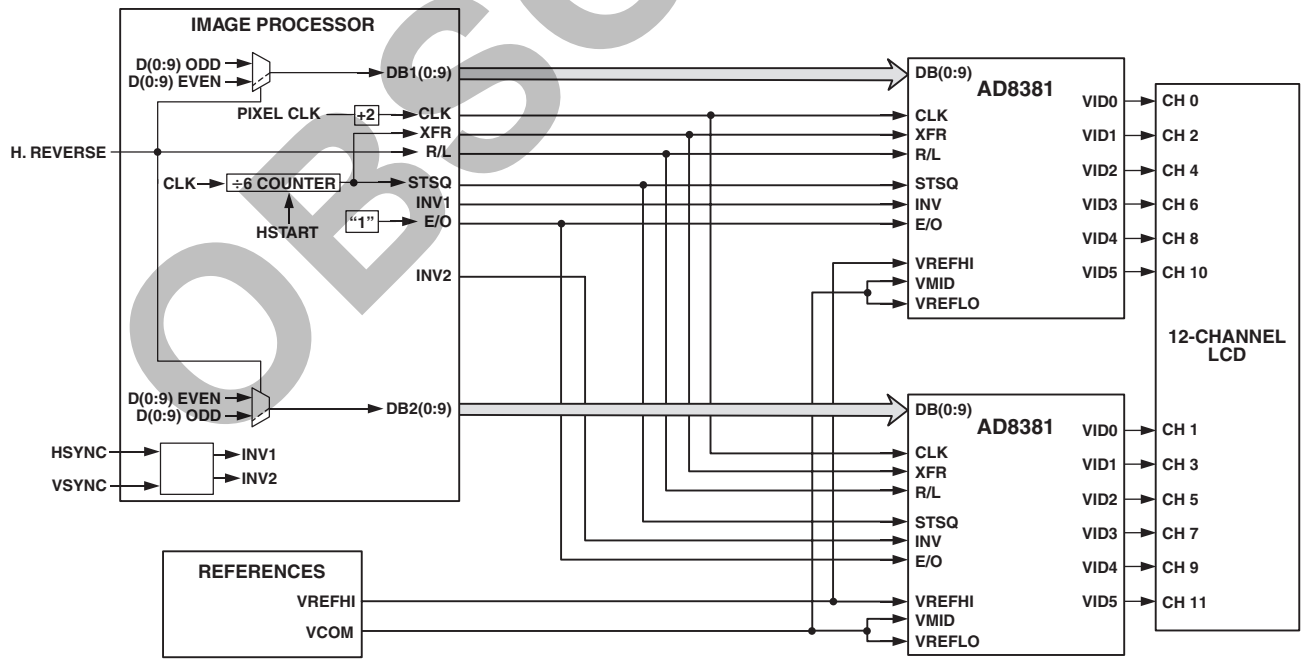


Figure 10. Dual Parallel Data Bus 12-Channel System Block Diagram

LAYOUT CONSIDERATIONS

The AD8381 is a mixed-signal, high speed, very accurate device. In order to realize its specifications, it is essential to use a properly designed printed circuit board.

Layout and Grounding

The analog outputs and the digital inputs of the AD8381 are pinned out on opposite sides of the package. When laying out the circuit board, keep these sections separate from each other to minimize crosstalk and noise and the coupling of the digital input signals into the analog outputs.

All signal trace lengths should be made as short and direct as possible to prevent signal degradation due to parasitic effects. Note that digital signals should not cross or be routed near analog signals.

It is imperative to provide a solid analog ground plane under and around the AD8381. All of the ground pins of the part should be connected directly to the ground plane with no extra signal path length. For conventional operation this includes the pins DGND, AGNDDAC, AGNDBIAS, AGND0, AGND1,2, AGND3,4, and AGND5. The return traces for any of the signals should be routed close to the ground pin for that section to prevent stray signals from coupling into other ground pins.

Power Supply Bypassing

All power supply and reference pins of the AD8381 must be properly bypassed to the analog ground plane for optimum performance.

All analog supply pins may be connected directly to an analog supply plane located as close to the part as possible. A 0.1 µF chip capacitor should be placed as close to each analog supply pin as possible and connected directly between each analog supply pin and the analog ground plane.

A minimum of 47 µF tantalum capacitor should be placed near the analog supply plane and connected directly between the supply and analog ground planes.

A minimum of 10 µF tantalum capacitor should be placed near the digital supply pin and connected directly to the analog ground plane. A 0.1 µF chip capacitor should be connected between the digital supply pin and the analog ground.

VREFHI, VMID, VREFLO Reference Distribution

To ensure well-matched video outputs, all AD8381s must operate from equal reference voltages.

Each reference voltage should be distributed to each AD8381 directly from the source of the reference voltage with approximately equal trace lengths.

A 0.1 µF chip capacitor should be placed as close to each reference input pin as possible and directly connected between the reference input pin and the analog ground plane.

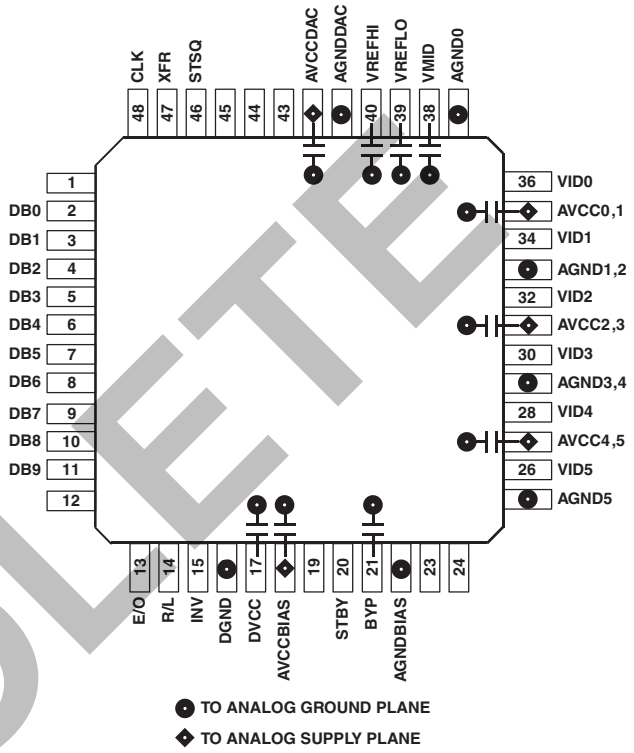
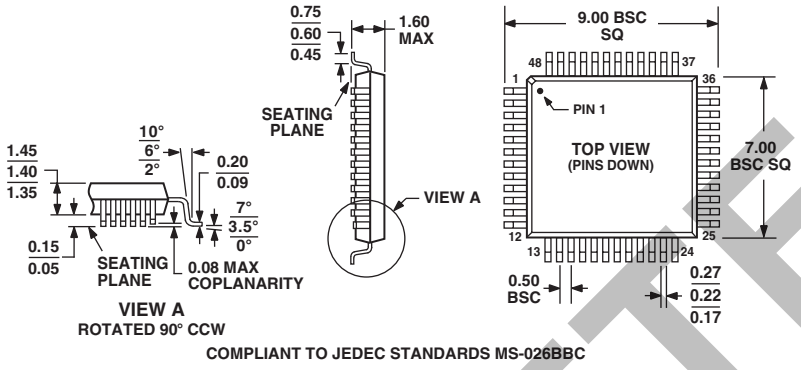


Figure 11.

OUTLINE DIMENSIONS

48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BBC

Revision History

Location	Page
10/03—Change from REV. A to REV. B.	
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9/03—Change from REV. 0 to REV. A.	
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