

### FEATURES

- Extreme high temperature operation**
  - 40°C to +210°C, flatpack package
  - 40°C to +175°C, SOIC package
- Rail-to-rail output**
- Low power: 1 mA maximum**
- Gain bandwidth product: 10 MHz at  $A_v = 100$  typical**
- Low offset voltage: 200  $\mu$ V maximum**
- Unity-gain stable**
- High slew rate: 2.5 V/ $\mu$ s typical**
- Low noise: 4 nV/ $\sqrt{\text{Hz}}$  typical at 1 kHz**

### APPLICATIONS

- Downhole drilling and instrumentation**
- Avionics**
- Heavy industrial**
- High temperature environments**

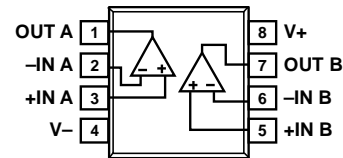
### GENERAL DESCRIPTION

The AD8634 is a single-supply, 10 MHz bandwidth, dual amplifier that features rail-to-rail outputs. The AD8634 is guaranteed to operate from 3 V to 30 V (or  $\pm 1.5$  V to  $\pm 15$  V) and at very high temperatures.

The AD8634 is well suited for single-supply applications that require both ac and precision dc performance. The combination of wide bandwidth, low noise, and precision makes the AD8634 useful in a wide variety of applications, including filters and interfacing with a variety of sensors.

This dual-channel op amp is offered in an 8-lead SOIC plastic package with an operating temperature range of  $-40^\circ\text{C}$  to  $+175^\circ\text{C}$ . It is also available in an 8-lead ceramic flat package (flatpack) with an operating temperature range of  $-40^\circ\text{C}$  to  $+210^\circ\text{C}$ . Both packages are designed for robustness at extreme temperatures and are qualified for 1000 hours of operation at the maximum temperature rating.

### PIN CONFIGURATION



**AD8634**  
TOP VIEW  
(Not to Scale)

Figure 1. SOIC and Flatpack Pinout

11524-001

The AD8634 is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection table of available high temperature products, see the high temperature product list and qualification data available at [www.analog.com/hightemp](http://www.analog.com/hightemp).

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## SPECIFICATIONS

ELECTRICAL CHARACTERISTICS,  $V_{SY} = \pm 15.0\text{ V}$ 

$V_{SY} = \pm 15.0\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $V_{OUT} = 0\text{ V}$ ,  $T_{MIN} \leq T_A \leq T_{MAX}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions	SOIC Package $-40^{\circ}\text{C} \leq T_A \leq +175^{\circ}\text{C}$			Flatpack Package $-40^{\circ}\text{C} \leq T_A \leq +210^{\circ}\text{C}$			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Offset Voltage	$V_{OS}$				200			200	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.6			0.8		$\mu\text{V}/^{\circ}\text{C}$
Offset Voltage Matching		$T_A = 175^{\circ}\text{C}$			150			150	$\mu\text{V}$
Input Bias Current	$I_B$		-200		+200	-200		+200	nA
Input Offset Current	$I_{OS}$				30			30	nA
Input Voltage Range			-14.7		+14.7	-14.5		+14.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -14.0\text{ V to }+14.0\text{ V}$	105	120		100	115		dB
Large Signal Voltage Gain	$A_{VO}$	$-13.5\text{ V} \leq V_O \leq +13.5\text{ V}$ , $R_L = 2\text{ k}\Omega$	104	112		100	108		dB
Input Impedance Differential				TBD			TBD		$\text{k}\Omega    \text{pF}$
Input Impedance Common-Mode				TBD			TBD		$\text{M}\Omega    \text{pF}$
OUTPUT CHARACTERISTICS									
Output Voltage High	$V_{OH}$	$R_L = 10\text{ k}\Omega$ to $V_{CM}$	14.8	14.90		14.8	14.90		V
		$R_L = 2\text{ k}\Omega$ to $V_{CM}$	14.0	14.5		14.0	14.5		V
		$R_L = 2\text{ k}\Omega$ to $V_{CM}$ , $T_A = T_{MAX}$	14.60	14.75		14.60	14.75		V
Output Voltage Low	$V_{OL}$	$R_L = 10\text{ k}\Omega$ to $V_{CM}$		-14.95	-14.8		-14.95	-14.8	V
		$R_L = 2\text{ k}\Omega$ to $V_{CM}$		-14.8	-14.70		-14.75	-14.65	V
Short-Circuit Current	$I_{SC}$			+100/-20			+105/-18		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 2\text{ V to } \pm 18\text{ V}$	105	115		103	113		dB
Supply Current per Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$ , $T_A = T_{MAX}$		1.0	1.2		1.1	1.3	mA
DYNAMIC PERFORMANCE									
Slew Rate	SR	$R_L = 2\text{ k}\Omega$	3.6			3.6			$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP	$V_{IN} = 5\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $A_V = 100$		9.7			9.7		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 5\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $A_V = 1$		2.5			2.5		MHz
-3 dB Closed-Loop Bandwidth	-3dB	$V_{IN} = 5\text{ mV p-p}$ , $A_V = 1$		4.9			4.9		MHz
Phase Margin	$\Phi_M$			84			82		Degrees
NOISE PERFORMANCE									
Voltage Noise	$e_n$ p-p	0.1 Hz to 10 Hz		0.13			0.13		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		4.0			4.0		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$			0.6			0.6		$\text{pA}/\sqrt{\text{Hz}}$

**ELECTRICAL CHARACTERISTICS,  $V_{SY} = +3.0\text{ V}$** 

$V_{SY} = \pm 3.0\text{ V}$ ,  $V_{CM} = +1.5\text{ V}$ ,  $V_{OUT} = -1.5\text{ V}$ ,  $T_{MIN} \leq T_A \leq T_{MAX}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions	SOIC Package $-40^\circ\text{C} \leq T_A \leq +175^\circ\text{C}$			Flatpack Package $-40^\circ\text{C} \leq T_A \leq +210^\circ\text{C}$			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Offset Voltage	$V_{OS}$				200			200	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.6			0.8		$\mu\text{V}/^\circ\text{C}$
Offset Voltage Matching		$T_A = 175^\circ\text{C}$			150			150	$\mu\text{V}$
Input Bias Current	$I_B$		-200		+200	-200		+200	nA
Input Offset Current	$I_{OS}$				30			30	nA
Input Voltage Range			0.3		2.7	0.5		2.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0.3\text{ V to } 2.7\text{ V}$	60	65		55	60		dB
Large Signal Voltage Gain	$A_{VO}$	$0.5\text{ V} \leq V_O \leq 2.5\text{ V}$ , $R_L = 2\text{ k}\Omega$	104	112		100	108		dB
Input Impedance									
Differential				TBD			TBD		$\text{k}\Omega    \text{pF}$
Common-Mode				TBD			TBD		$\text{M}\Omega    \text{pF}$
OUTPUT CHARACTERISTICS									
Output Voltage High	$V_{OH}$	$R_L = 10\text{ k}\Omega$ to $V_{CM}$	2.8	2.90		2.8	2.90		V
		$R_L = 2\text{ k}\Omega$ to $V_{CM}$	2.0	2.5		2.0	2.5		V
		$R_L = 2\text{ k}\Omega$ to $V_{CM}$ , $T_A = T_{MAX}$	2.60	2.75		2.60	2.75		V
Output Voltage Low	$V_{OL}$	$R_L = 10\text{ k}\Omega$ to $V_{CM}$		50	200		50	200	mV
		$R_L = 2\text{ k}\Omega$ to $V_{CM}$		200	300		250	350	mV
Short-Circuit Current	$I_{SC}$		—	15			15		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 1.25\text{ V to } \pm 1.75\text{ V}$	97	102		95	100		dB
Supply Current per Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$ , $T_A = T_{MAX}$		0.9	1.1		1.0	1.2	mA
DYNAMIC PERFORMANCE									
Slew Rate	SR	$R_L = 2\text{ k}\Omega$	3.5			3.5			$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP	$V_{IN} = 5\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $A_V = 100$		9.7			9.7		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 5\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $A_V = 1$		2.5			2.5		MHz
-3 dB Closed-Loop Bandwidth	-3dB	$V_{IN} = 5\text{ mV p-p}$ , $A_V = 1$		4.9			4.9		MHz
Phase Margin	$\Phi_M$			84			82		Degrees
NOISE PERFORMANCE									
Voltage Noise	$e_n$ p-p	0.1 Hz to 10 Hz		0.13			0.13		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		4.0			4.0		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$			0.6			0.6		$\text{pA}/\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$V- \leq V_{IN} \leq V+$
Differential Input Voltage <sup>1</sup>	±0.6 V
Output Short-Circuit Duration to GND	TBD
Storage Temperature Range	-65°C to +210°C
Operating Temperature Range	
SOIC Package	-40°C to +175°C
Flatpack Package	-40°C to +210°C
Junction Temperature	
SOIC Package	210°C
Flatpack Package	210°C
Lead Temperature (Soldering 60 sec)	300°C

<sup>1</sup> For input differential voltages greater than 0.6 V, the input current should be limited to less than 5 mA to prevent degradation or destruction of the input devices.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the device soldered on a 4-layer JEDEC standard printed circuit board (PCB) with zero airflow.

Table 4. Thermal Resistance

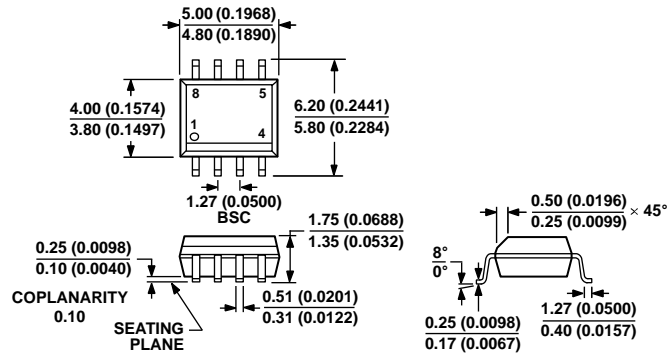
Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead SOIC_N	121	43	°C/W
8-Lead Flatpack	TBD	TBD	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 2. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)

Dimensions shown in millimeters and (inches)

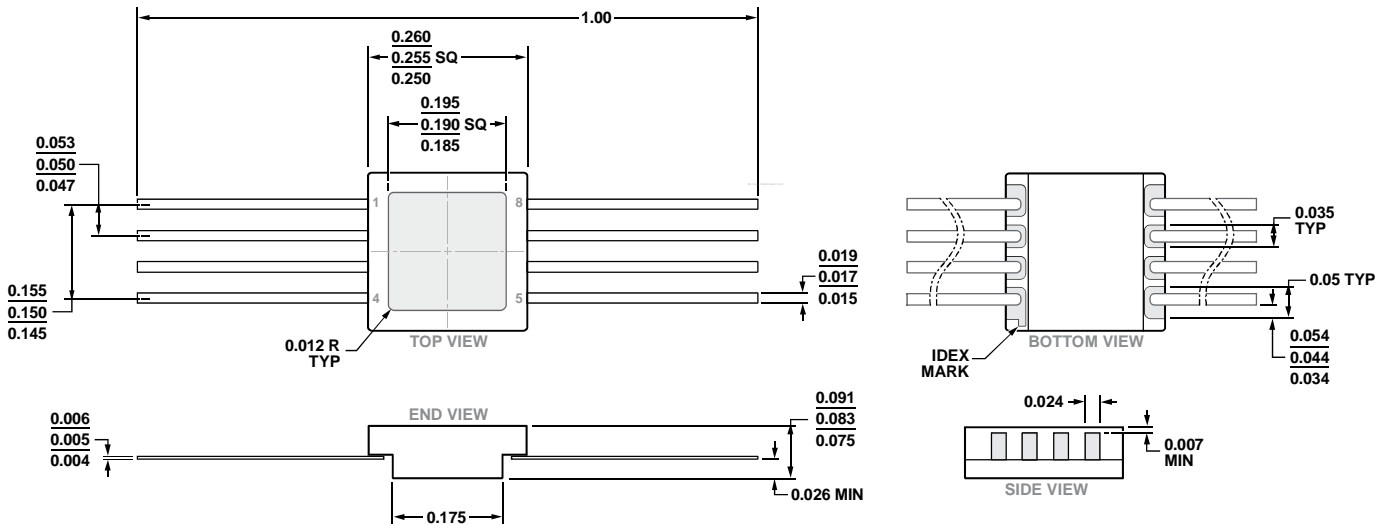


Figure 3. 8-Lead Ceramic Flat Package [FLATPACK]  
 (F-8-2)

Dimensions shown in inches

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
AD8634HRZN	-40°C to +175°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD8634HFZ	-40°C to +210°C	8-Lead Ceramic Flat Package [FLATPACK]	F-8-2

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**