
2x20W Stereo / 1x40W Mono Digital Audio Amplifier With 20 Bands EQ Functions + Capless Line Driver

Features

- 16/18/20/24-bits input with I²S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
Loudspeaker: 97dB (PSNR), 105dB (DR) @24V
- Multiple sampling frequencies (Fs)
32kHz / 44.1kHz / 48kHz and
64kHz / 88.2kHz / 96kHz and
128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
64x~512x Fs for 64kHz / 88.2kHz / 96kHz
64x~256x Fs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
3.3V for digital circuit
10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@24V
10W x 2ch into 8Ω @0.09% THD+N
15W x 2ch into 8Ω @0.13% THD+N
20W x 2ch into 8Ω @0.17% THD+N
- Loudspeaker output power for Mono@24V
20W x 1ch into 8Ω @0.06% THD+N
30W x 1ch into 8Ω @0.09% THD+N
40W x 1ch into 8Ω @0.12% THD+N
- Sound processing including :
20 bands parametric speaker EQ
Volume control (+24dB~-103dB, 0.125dB/step),
Dynamic range control (DRC)
Dual band dynamic range control
Power clipping
3D surround sound
Channel mixing
Noise gate with hysteresis window
Bass/Treble tone control
Bass management crossover filter
DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I²C control interface with selectable device address

- Support hardware and software reset
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode
- Support initial EEPROM setting

Applications

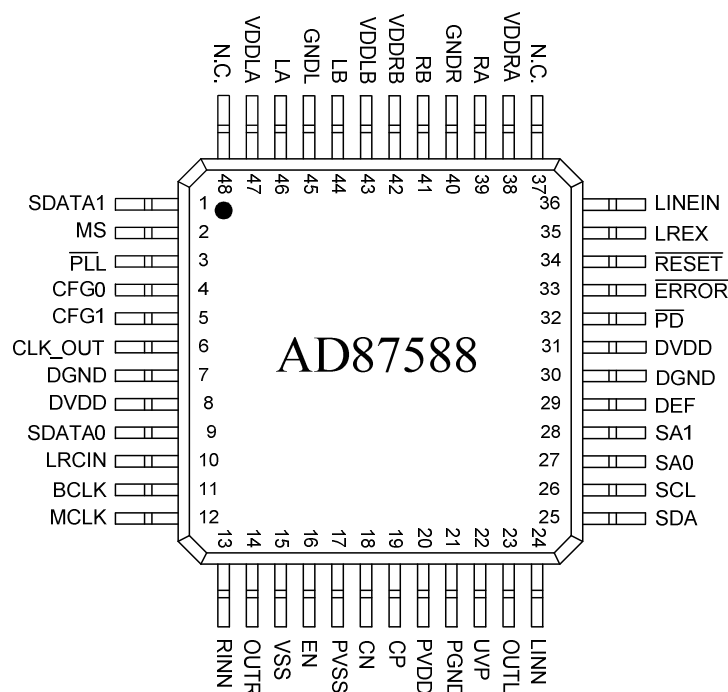
- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

The AD87588 is an integrated audio system solution, embedding digital audio process, power stage amplifier, and a stereo 3Vrms line driver. AD87588 is a digital audio amplifier capable of driving a pair of 8Ω, 20W or a single 4Ω, 40W operating at 24V supply. AD87588 is also capable of driving 4Ω, 10W (SE)x2 + 8Ω, 20W (BTL)x1 at 24V supply for 2.1CH application.

AD87588 can provide advanced audio processing capabilities, such as volume control, 20 bands speaker EQ, audio mixing, 3D surround and Dynamic Range Control (DRC). These functions are fully programmable via a simple I²C control interface. Robust protection circuits are provided to protect AD87588 from damage due to accidental erroneous operating condition. AD87588 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. AD87588 is pop free during instantaneous power switch because of its built-in, robust anti-pop circuit.

Pin Assignment

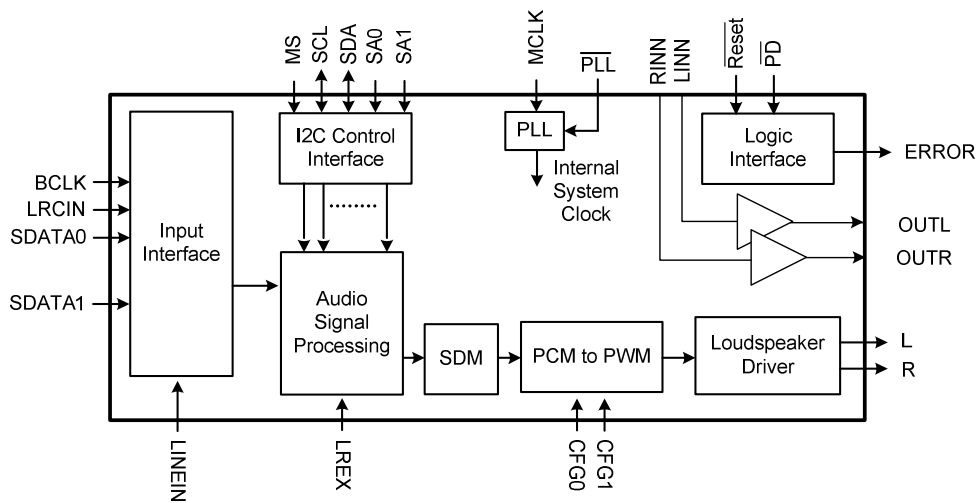


Pin Description

| PIN | NAME | TYPE | DESCRIPTION | CHARACTERISTICS |
|-----|-------------------------|------|--|----------------------------------|
| 1 | SDATA1 | I | Serial audio data input 1 | Schmitt trigger TTL input buffer |
| 2 | MS | I | EEPROM selection | Schmitt trigger TTL input buffer |
| 3 | $\overline{\text{PLL}}$ | I | PLL enable, low active | Schmitt trigger TTL input buffer |
| 4 | CFG0 | I | Stereo/Mono/2.1CH configuration pin | Schmitt trigger TTL input buffer |
| 5 | CFG1 | I | Stereo/Mono/2.1CH configuration pin | Schmitt trigger TTL input buffer |
| 6 | CLK_OUT | O | Clock output from PLL | TTL output buffer |
| 7 | DGND | P | Digital Ground (3.3V) | |
| 8 | DVDD | P | Digital Power (3.3V) | |
| 9 | SDATA0 | I | Serial audio data input 0 | Schmitt trigger TTL input buffer |
| 10 | LRCIN | I | Left/Right clock input (Fs) | Schmitt trigger TTL input buffer |
| 11 | BCLK | I | Bit clock input (64Fs) | Schmitt trigger TTL input buffer |
| 12 | MCLK | I | Master clock input | Schmitt trigger TTL input buffer |
| 13 | RINN | I | Right input for line driver | |
| 14 | ROUT | O | Right output for line driver | |
| 15 | SGND | P | Ground for line driver | |
| 16 | EN | I | Enable for line driver | |
| 17 | PVSS | P | Supply voltage for line driver | |
| 18 | CN | IO | Charge pump flying capacitor negative connection for line driver | |

| | | | | |
|----|--------------------|-----|--|----------------------------------|
| 19 | CP | IO | Charge pump flying capacitor positive connection for line driver | |
| 20 | PVDD | P | Supply voltage for line driver | |
| 21 | PGND | P | Ground for line driver | |
| 22 | UVP | I | Under voltage protection for line driver | |
| 23 | LOUT | O | Left output for Line driver | |
| 24 | LINN | I | Left input for Line driver | |
| 25 | SDA | I/O | I ² C bi-directional serial data | Schmitt trigger TTL input buffer |
| 26 | SCL | I/O | I ² C serial clock input | Schmitt trigger TTL input buffer |
| 27 | SA0 | I | I ² C select address 0 | Schmitt trigger TTL input buffer |
| 28 | SA1 | I | I ² C select address 1 | Schmitt trigger TTL input buffer |
| 29 | DEF | I | Initial default volume setting (1:Un-Mute ; 0:Mute) | Schmitt trigger TTL input buffer |
| 30 | DGND | P | Digital Ground (3.3V) | |
| 31 | DVDD | P | Digital Power (3.3V) | |
| 32 | \overline{PD} | I | Power down, low active | Schmitt trigger TTL input buffer |
| 33 | \overline{ERROR} | O | Error status, low active | Open-drain output |
| 34 | \overline{RESET} | I | Reset, low active | Schmitt trigger TTL input buffer |
| 35 | LREX | I | Left/Right channel exchange (0:Unchanged ; 1:Exchanged) | Schmitt trigger TTL input buffer |
| 36 | LINEIN | I | Select input data (0:SDATA0 ; 1:SDATA1) | Schmitt trigger TTL input buffer |
| 37 | N.C. | | | |
| 38 | VDDRA | P | Right channel supply A | |
| 39 | RA | O | Right channel output A | |
| 40 | GNDR | P | Right channel ground | |
| 41 | RB | O | Right channel output B | |
| 42 | VDDR B | P | Right channel supply B | |
| 43 | VDDL B | P | Left channel supply B | |
| 44 | LB | O | Left channel output B | |
| 45 | GNDL | P | Left channel ground | |
| 46 | LA | O | Left channel output A | |
| 47 | VDDL A | P | Left channel supply A | |
| 48 | N.C. | | | |

Functional Block Diagram



Ordering Information

| Product ID | Package | Packing / MPQ | Comments |
|-----------------|----------------------|--|----------|
| AD87588-LG48NAY | E-LQFP-48L 7x7 mm | 250 Units / Tray 2.5K Units / Box (10 Tray) | Green |
| AD87588-LG48NAR | | 2K Units Tape & Reel | Green |

Available Package

| Package Type | Device No. | $\theta_{ja} (^{\circ}C/W)$ | $\Psi_{jt} (^{\circ}C/W)$ | $\theta_{jc} (^{\circ}C/W)$ | Exposed Thermal Pad |
|--------------------|------------|-----------------------------|---------------------------|-----------------------------|---------------------|
| E-LQFP 48L (7x7mm) | AD87588 | 27 | 1.33 | 6.0 | Yes (Note1) |

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja} is measured on a room temperature ($T_A=25^{\circ}C$), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: Ψ_{jt} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtaining θ_{ja} , using a procedure described in JESD51-2.

Note 1.4: θ_{jc} represents the thermal resistance for the heat flow between the chip junction and the package's bottom surface. It's extracted from the simulation data with obtaining a cold plate on the package bottom.

Marking Information

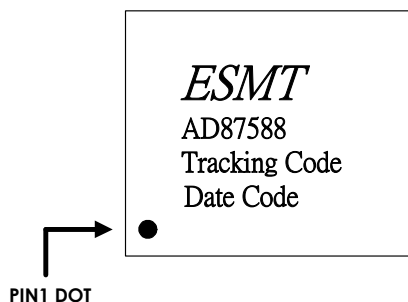
AD87588

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code

Line 4 : Date Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

| Symbol | Parameter | Min | Max | Units |
|------------------|--------------------------------|------|-----|-------|
| DVDD | Supply for Digital Circuit | -0.3 | 3.6 | V |
| VDDL/R | Supply for Driver Stage | -0.3 | 30 | V |
| PVDD | Supply for Line out | -0.3 | 6 | V |
| V _i | Input Voltage | -0.3 | 3.6 | V |
| T _{stg} | Storage Temperature | -65 | 150 | °C |
| T _J | Junction Operating Temperature | -10 | 150 | °C |

Recommended Operating Conditions

| Symbol | Parameter | Typ | Units |
|----------------|--------------------------------|-----------|-------|
| DVDD | Supply for Digital Circuit | 3.15~3.45 | V |
| VDDL/R | Supply for Driver Stage | 10~26 | V |
| PVDD | Supply for Line out | 3~5.5 | V |
| T _J | Junction Operating Temperature | -10~125 | °C |
| T _A | Ambient Operating Temperature | -10~70 | °C |

Digital Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------------|---------------------------|-----|-----|-----|-------|
| V _{IH} | High-Level Input Voltage | 2.0 | | | V |
| V _{IL} | Low-Level Input Voltage | | | 0.8 | V |
| V _{OH} | High-Level Output Voltage | 2.4 | | | V |
| V _{OL} | Low-Level Output Voltage | | | 0.4 | V |
| C _i | Input Capacitance | | 6.4 | | pF |

General Electrical Characteristics

● Audio Amplifier

Condition: $T_A=25\text{ }^\circ\text{C}$ (unless otherwise specified).

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------------|---|-------------------------|-----|-----|-----|------------------|
| $I_{PD(HV)}$ | VDDL/R Supply Current during Power Down | VDDL/R=24V | | 10 | 200 | μA |
| $I_{PD(LV)}$ | DVDD Supply Current during Power Down | DVDD=3.3V | | 4 | 20 | μA |
| T_{SENSOR} | Junction Temperature for Driver Shutdown | | | 150 | | $^\circ\text{C}$ |
| | Temperature Hysteresis for Recovery from Shutdown | | | 30 | | $^\circ\text{C}$ |
| UV_H | Under Voltage Disabled (For DVDD) | | | 2.8 | | V |
| UV_L | Under Voltage Enabled (For DVDD) | | | 2.7 | | V |
| Rds-on | Static Drain-to-Source On-state Resistor, PMOS | VDDL/R=24V, Id=500mA | | 270 | | $\text{m}\Omega$ |
| | Static Drain-to-Source On-state Resistor, NMOS | | | 230 | | $\text{m}\Omega$ |
| I_{SC} | L(R) Channel Over-Current Protection (Note 2) | VDDL/R=24V | | 5 | | A |
| | | VDDL/R=12V | | 2.7 | | |
| | Mono Channel Over-Circuit Protection (Note 2) | VDDL/R=24V | | 10 | | A |
| | | VDDL/R=12V | | 5.4 | | |

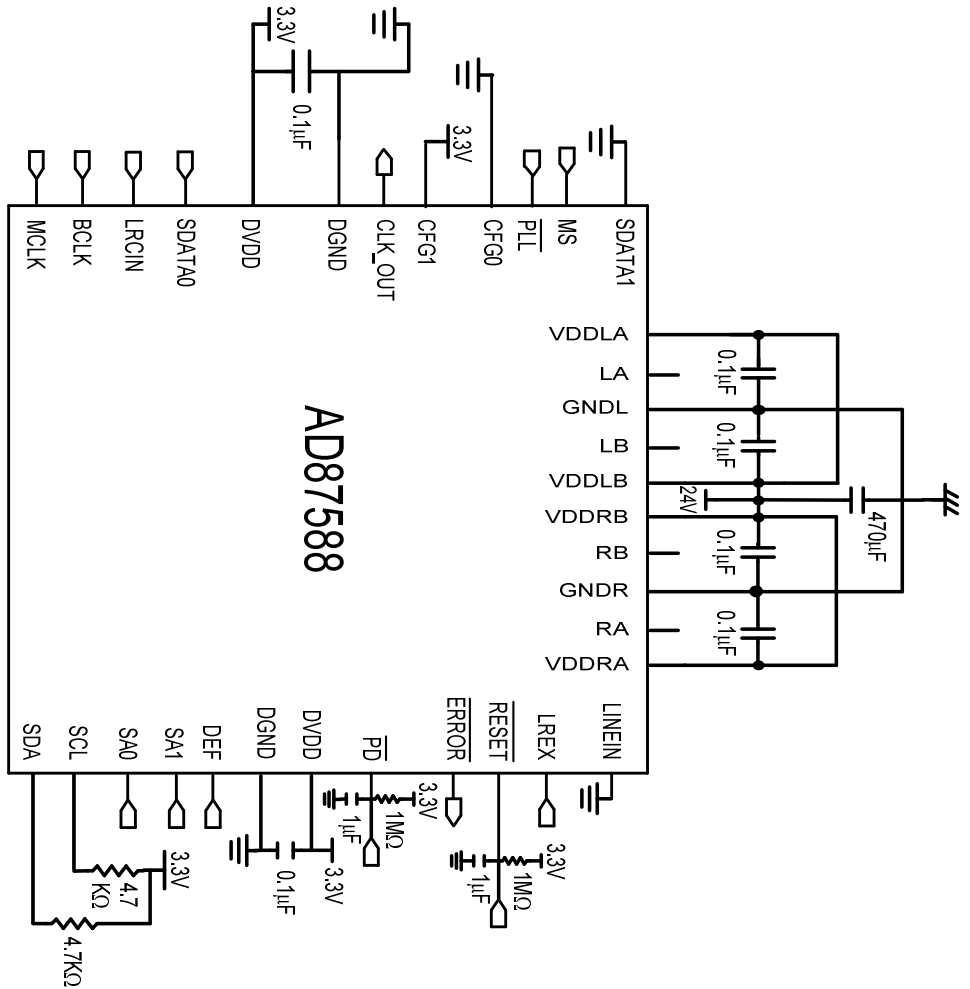
Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

● Capless Line Driver

Condition: $T_A=25\text{ }^\circ\text{C}$ (unless otherwise specified).

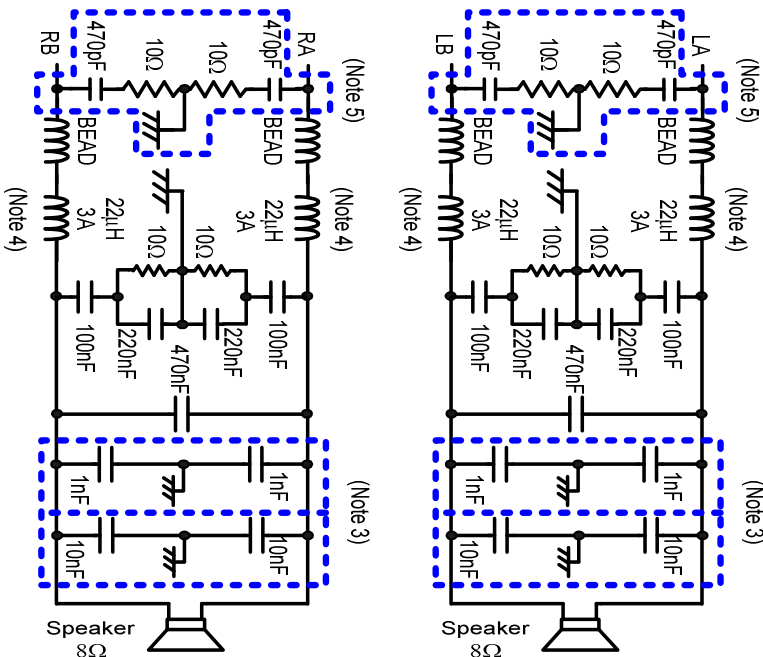
| SYMBOL | PARAMETER | TEST CONDITIONS | Min | NOM | Max | UNIT |
|----------|---------------------------|------------------|-----|-----|-----|---------------|
| I_{DD} | V_{DD} Supply Current | PVDD=EN=3.3V | | 7 | 15 | mA |
| I_{SD} | V_{DD} Shutdown Current | PVDD=3.3V; EN=0V | | | 100 | μA |
| II | Input Current | EN pin | | 0.1 | | μA |

Application Circuit Example for Stereo

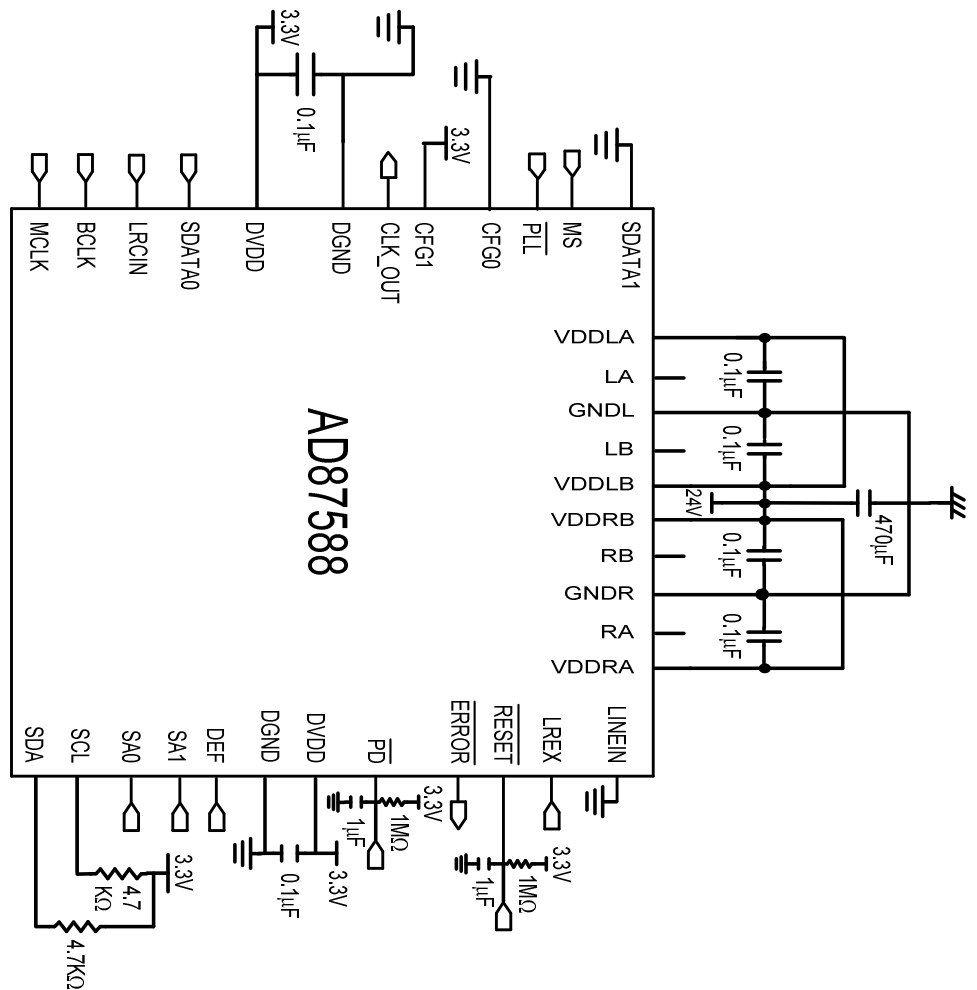


- Note 3: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.
- Note 4: When concerning about short-circuit protection, it is suggested using the choke with its I_{DC} larger than 5A.
- Note 5: The snubber circuit can be removed while the PVDD <= 20V.

| Pin | Logic | 0 | 1 |
|-------------------------|--------------|---|-----------------|
| $\overline{\text{PD}}$ | Power Down | | Normal |
| DEF | Default Mute | | Default Un-Mute |
| $\overline{\text{PLL}}$ | Enable | | External |

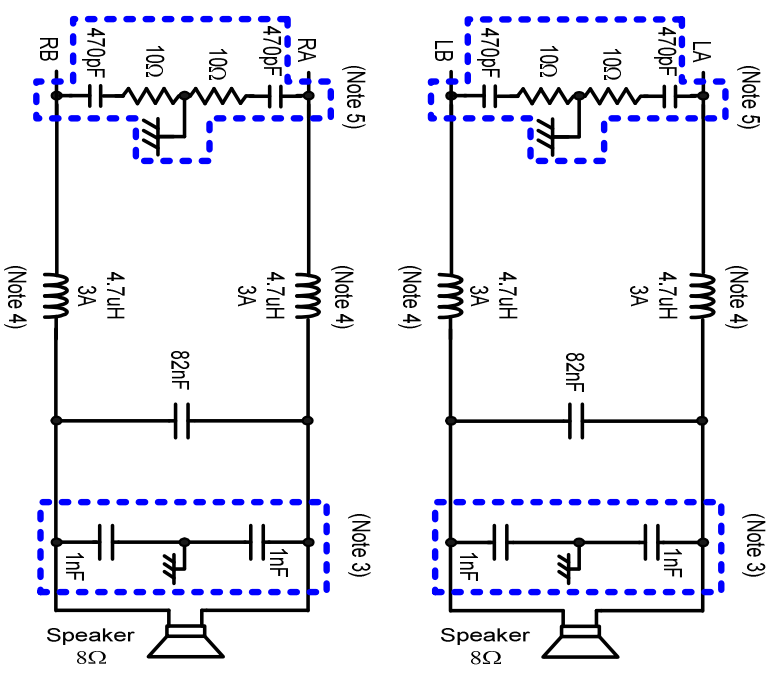


Application Circuit Example for Stereo (Economic type, moderate EMI suppression)

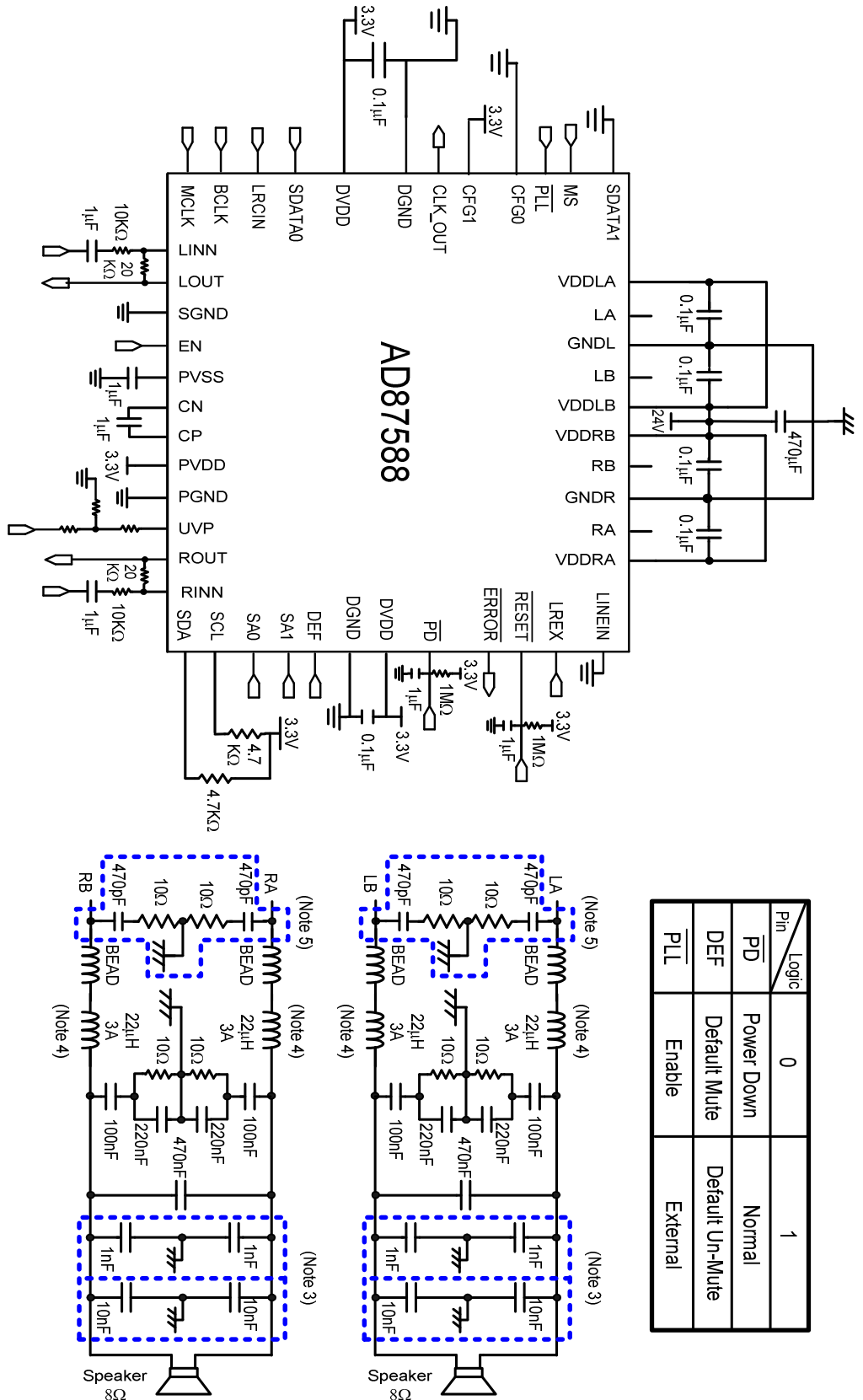


Note 3: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.
 Note 4: When concerning about short-circuit protection, it is suggested using the choke with its I_{pc} larger than 5A.
 Note 5: The snubber circuit can be removed while the $PVDD \leq 20V$.

| Pin | Logic | 0 | 1 |
|-----------------|--------------|---|-----------------|
| \overline{PD} | Power Down | | Normal |
| DEF | Default Mute | | Default Un-Mute |
| PLL | Enable | | External |

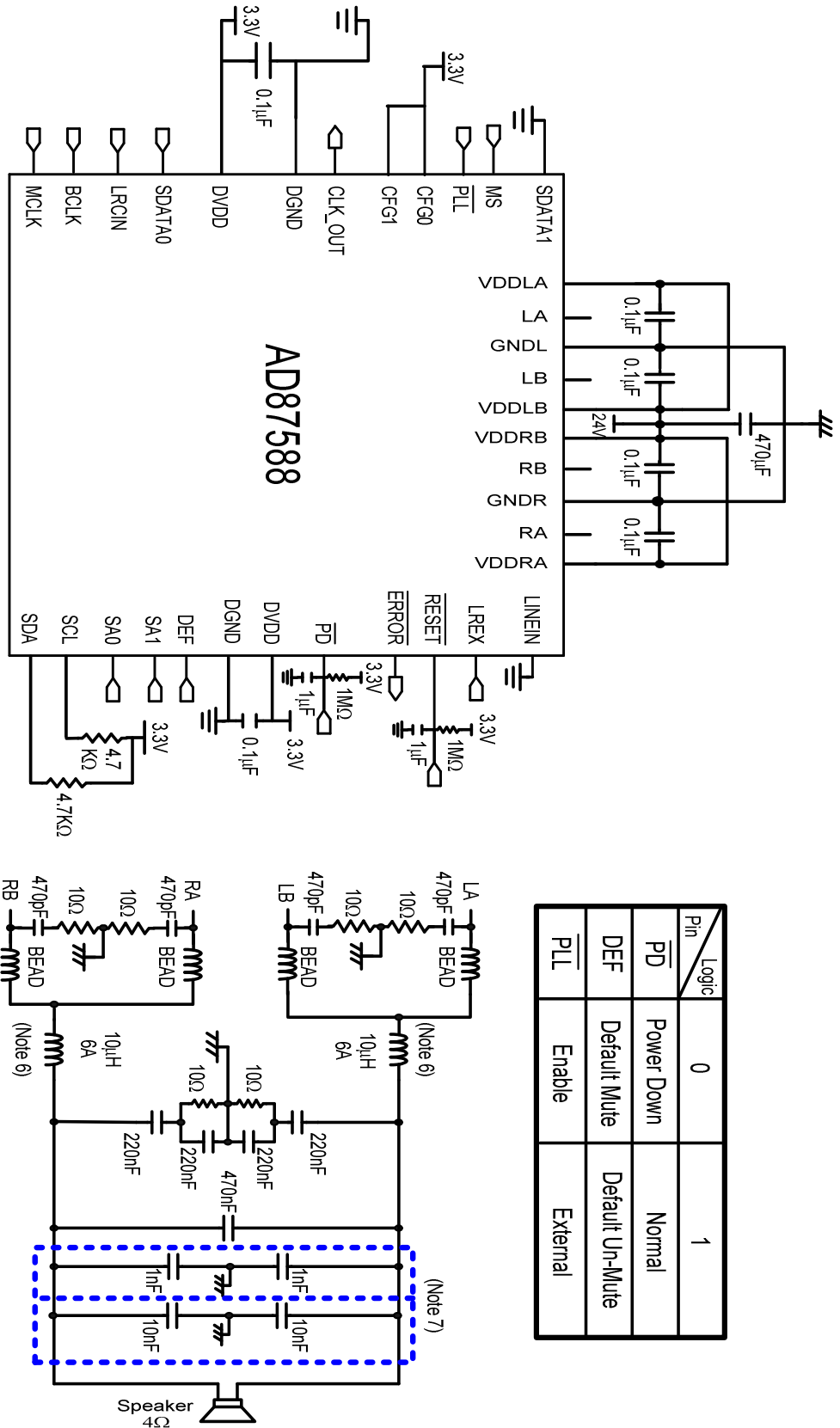


Application Circuit Example for Stereo with Line Driver



Note 3: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.
 Note 4: When concerning about short-circuit protection, it is suggested using the choke with its I_{DC} larger than 5A.
 Note 5: The snubber circuit can be removed while the PVDD <= 20V.

Application Circuit Example for Mono

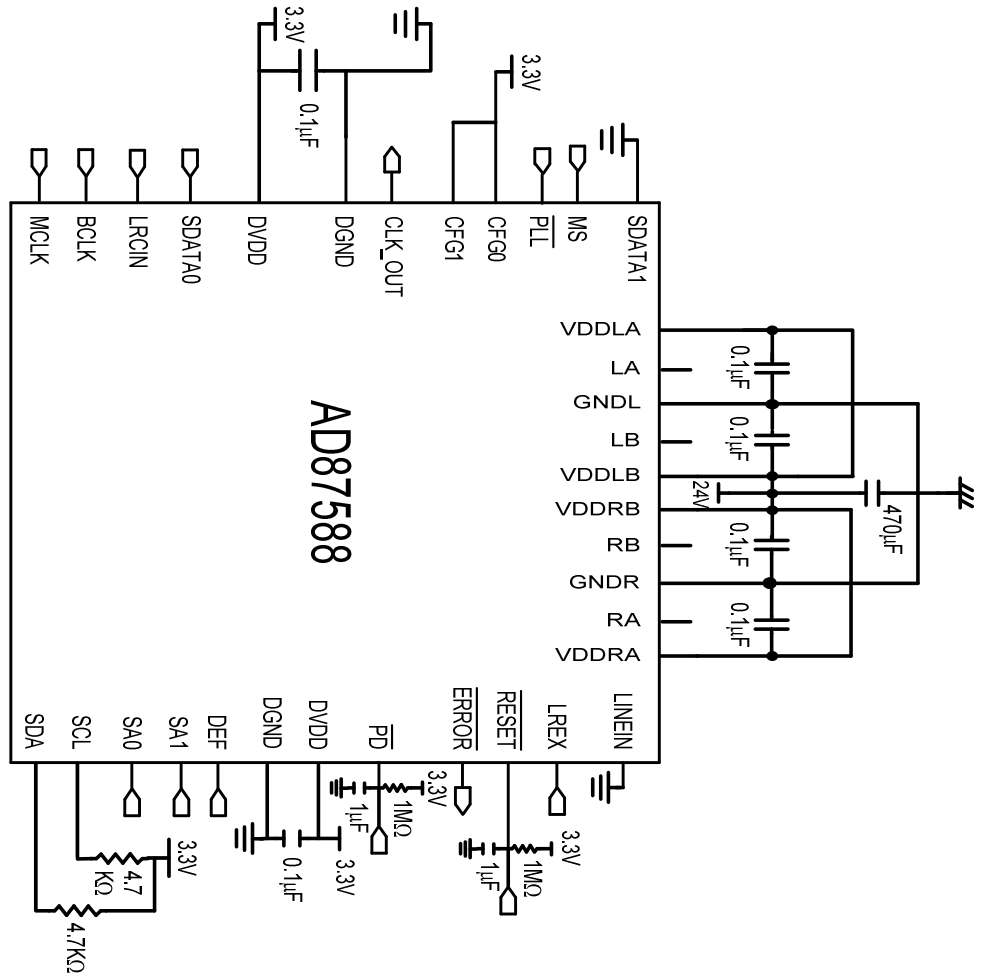


| Pin | Logic | 0 | 1 |
|-----|--------------|---|-----------------|
| PD | Power Down | | Normal |
| DEF | Default Mute | | Default Un-Mute |
| PLL | Enable | | External |

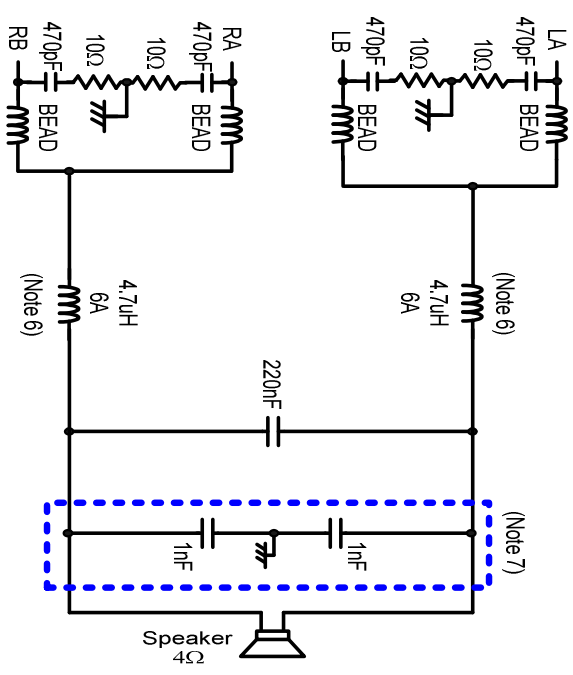
Note 6: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{pc} larger than 10A.

Note 7: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Application Circuit Example for Mono (Economic type, moderate EMI suppression)



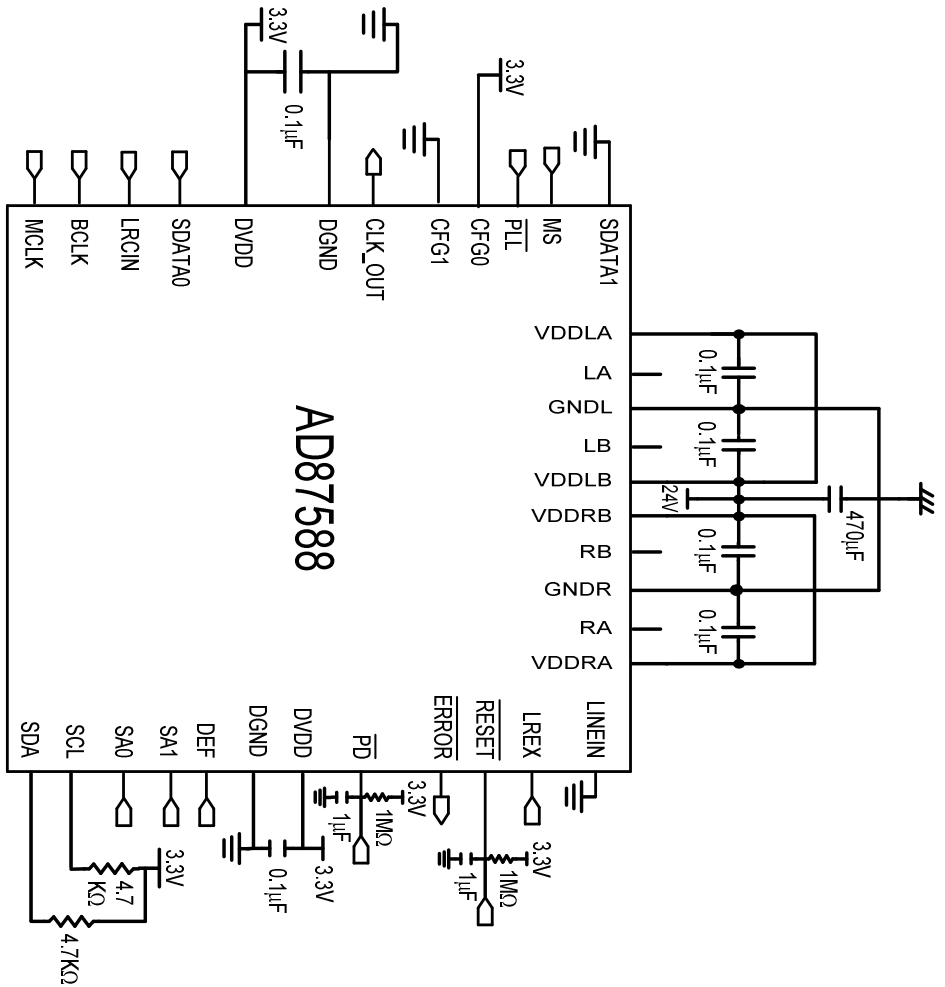
| Pin | Logic | 0 | 1 |
|-----|--------------|-----------------|---|
| PD | Power Down | Normal | |
| DEF | Default Mute | Default Un-Mute | |
| PLL | Enable | External | |



Note 6: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{pc} larger than 10A.

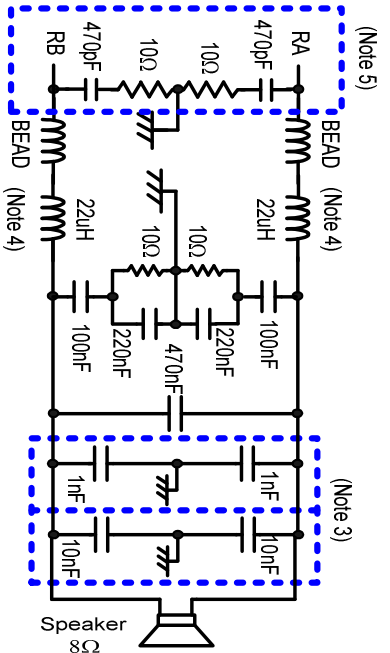
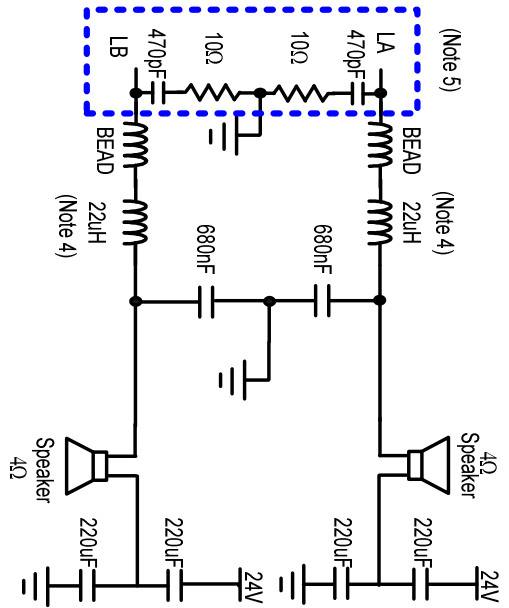
Note 7: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Application Circuit Example for 2.1CH



Note 3: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.
 Note 4: When concerning about short-circuit protection, it is suggested using the choke with its I_{bc} larger than 5A.
 Note 5: The snubber circuit can be removed while the PVDD <= 20V.

| Pin | Logic | 0 | 1 |
|-----|--------------|--------------|-----------------|
| PD | Power Down | 0 | Normal |
| DEF | Default Mute | Default Mute | Default Un-Mute |
| PLL | Enable | Enable | External |



Electrical Characteristics and Specifications for Loudspeaker

● **Stereo output (BTL output)**

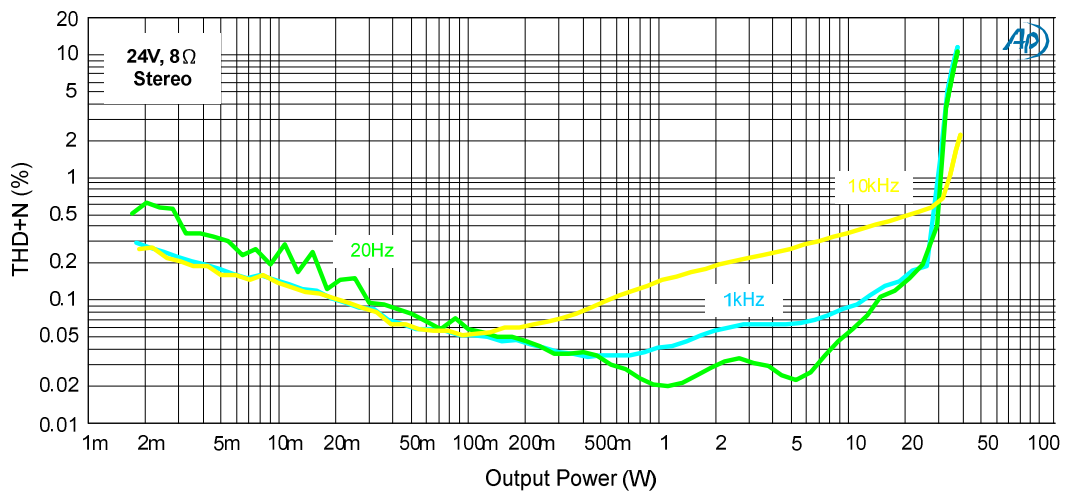
Condition: $T_A=25^\circ\text{C}$, $DVDD=3.3\text{V}$, $VDDL=VDDR=24\text{V}$, $F_S=48\text{kHz}$, Load= 8Ω with passive LC lowpass filter ($L=22\mu\text{H}$ with $R_{DC}=0.12\Omega$, $C=470\text{nF}$); Input is 1kHz sinewave.

| Symbol | Parameter | Condition | Input Level | Min | Typ | Max | Units |
|-------------------|-----------------------------------|--|-------------|-----|------|-----|---------------|
| P_O (Note 9) | RMS Output Power (THD+N=0.17%) | +8dB volume | | | 20 | | W |
| | RMS Output Power (THD+N=0.13%) | | | | 15 | | W |
| | RMS Output Power (THD+N=0.09%) | | | | 10 | | W |
| THD+N | Total Harmonic Distortion + Noise | $P_O=7.5\text{W}$ | | | 0.07 | | % |
| SNR | Signal to Noise Ratio (Note 8) | +8dB volume | -9dB | | 97 | | dB |
| DR | Dynamic Range (Note 8) | +8dB volume | -68dB | | 105 | | dB |
| V_n | Output Noise (Note 8) | 20Hz to 20kHz | | | 136 | | μV |
| PSRR | Power Supply Rejection Ratio | $V_{\text{RIPPLE}}=1V_{\text{RMS}}$ at 1kHz | | | -76 | | dB |
| | Channel Separation | 1W @1kHz | | | -66 | | dB |

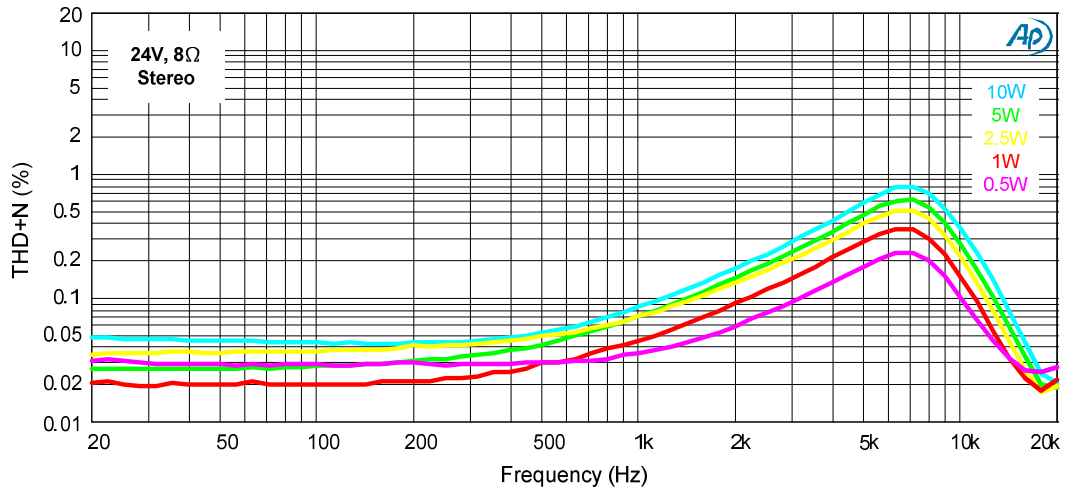
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

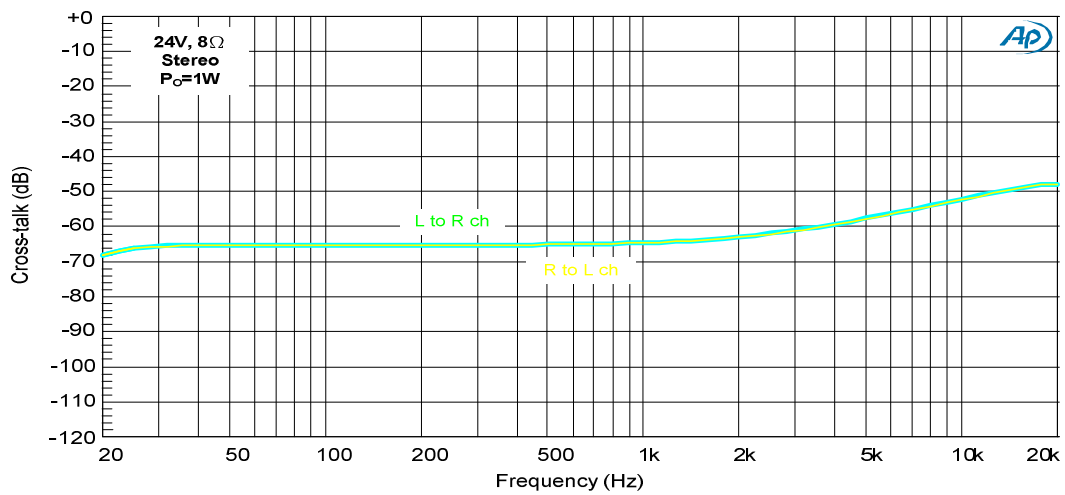
Total Harmonic Distortion + Noise vs. Output Power (Stereo)



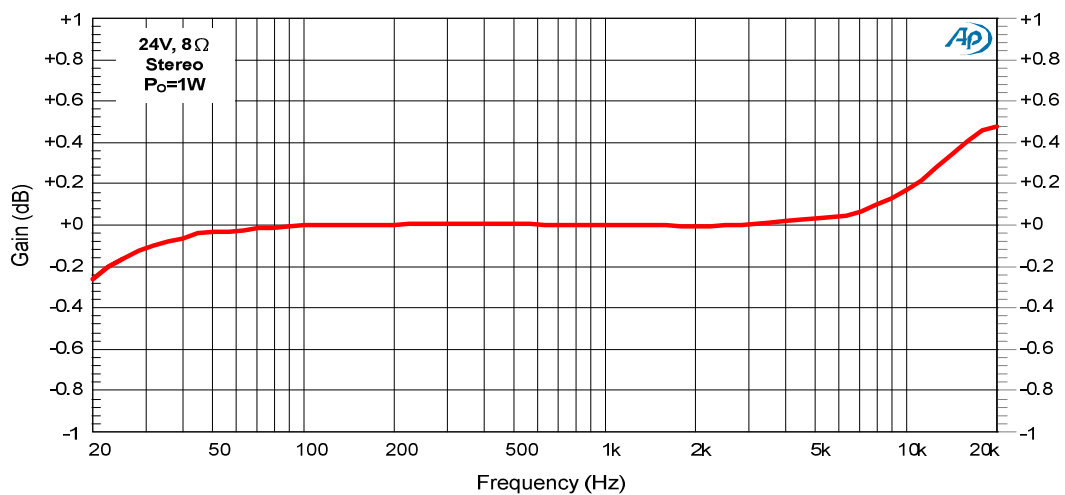
Total Harmonic Distortion + Noise vs. Frequency (Stereo)



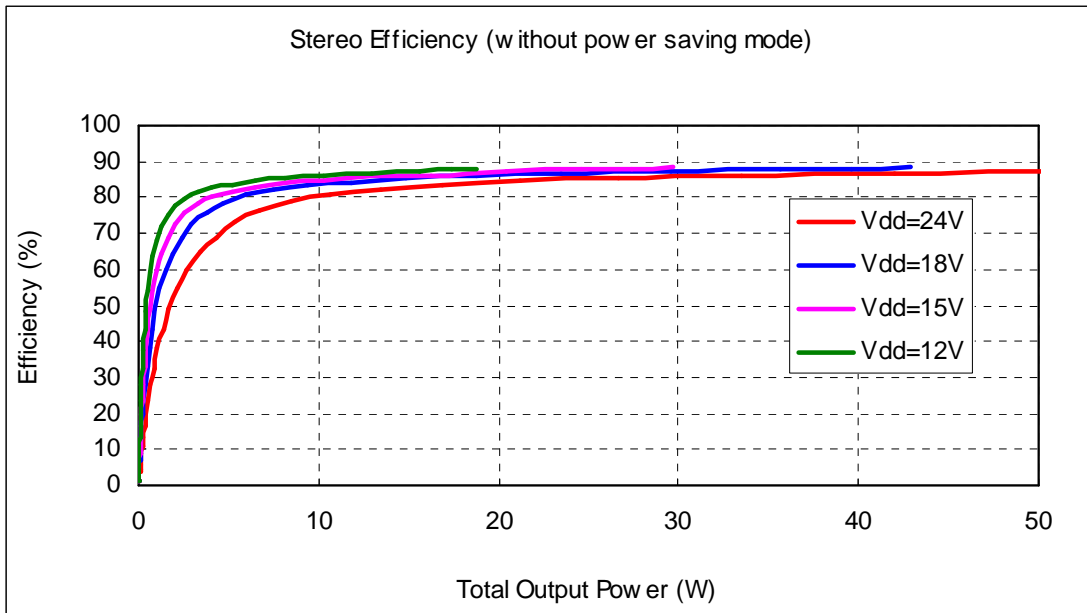
Cross-talk (Stereo)



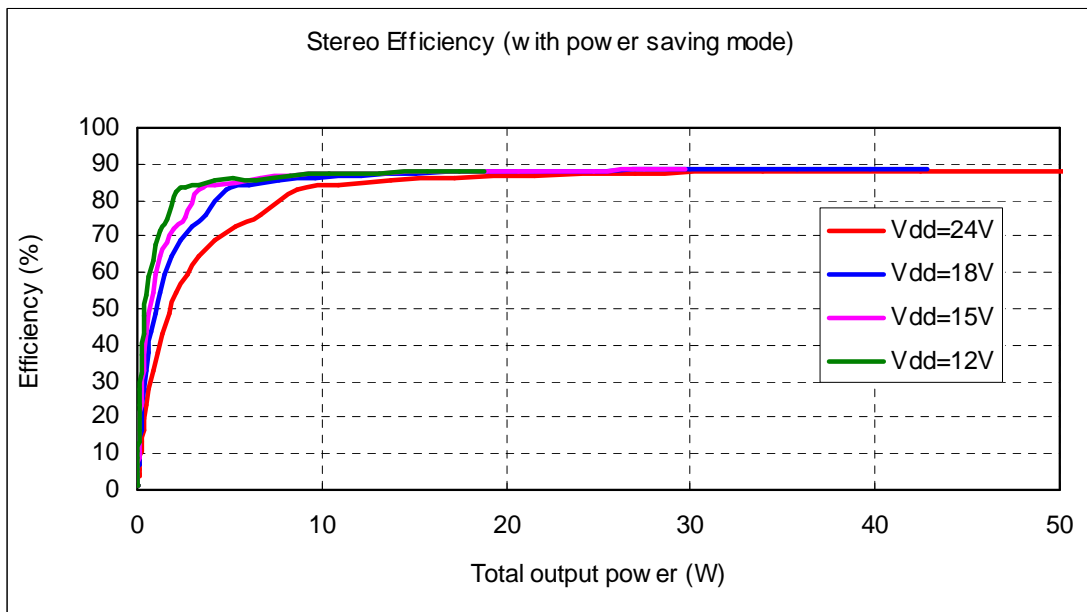
Frequency Response (Stereo)



Efficiency (Stereo)



Efficiency (Stereo) for Power Saving Mode



Electrical Characteristics and Specifications for Loudspeaker (cont.)

● **Mono output (PBTL output)**

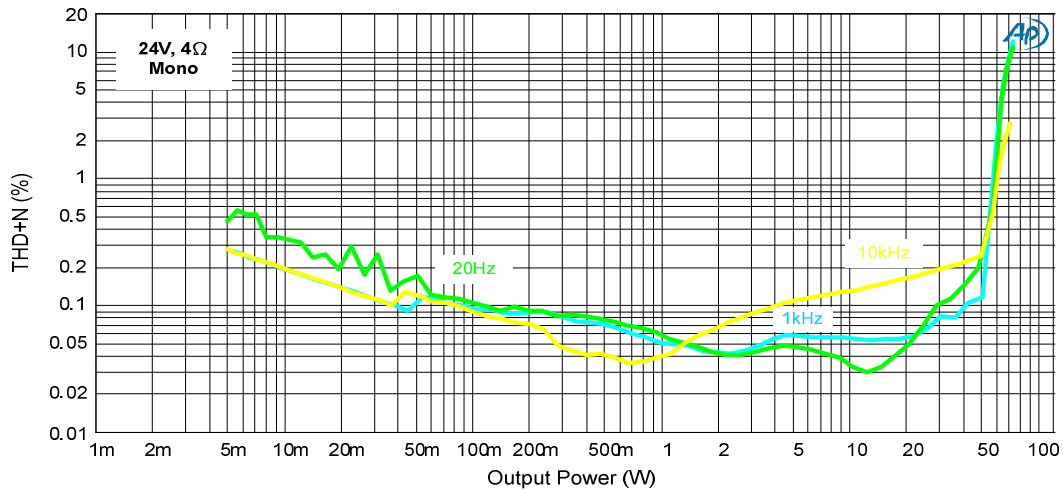
Condition: $T_A=25^\circ\text{C}$, DVDD= 3.3V, VDDL=VDDR=24V, $F_S=48\text{kHz}$, Load= 4Ω with passive LC lowpass filter ($L=10\ \mu\text{H}$ with $R_{DC}=0.12\Omega$, $C=470\text{nF}$); Input is 1kHz sinewave.

| Symbol | Parameter | Condition | Input Level | Min | Typ | Max | Units |
|-------------------|-----------------------------------|--|-------------|-----|------|-----|---------------|
| P_o (Note 9) | RMS Output Power (THD+N=0.12%) | +8dB volume | | | 40 | | W |
| | RMS Output Power (THD+N=0.09%) | | | | 30 | | W |
| | RMS Output Power (THD+N=0.06%) | | | | 20 | | W |
| THD+N | Total Harmonic Distortion + Noise | $P_o=15\text{W}$ | | | 0.06 | | % |
| SNR | Signal to Noise Ratio (Note 8) | +8dB volume | -9dB | | 97 | | dB |
| DR | Dynamic Range (Note 8) | +8dB volume | -68dB | | 106 | | dB |
| V_n | Output Noise (Note 8) | 20Hz to 20kHz | | | 125 | | μV |
| PSRR | Power Supply Rejection Ratio | $V_{\text{RIPPLE}}=1V_{\text{RMS}}$ at 1kHz | | | -76 | | dB |

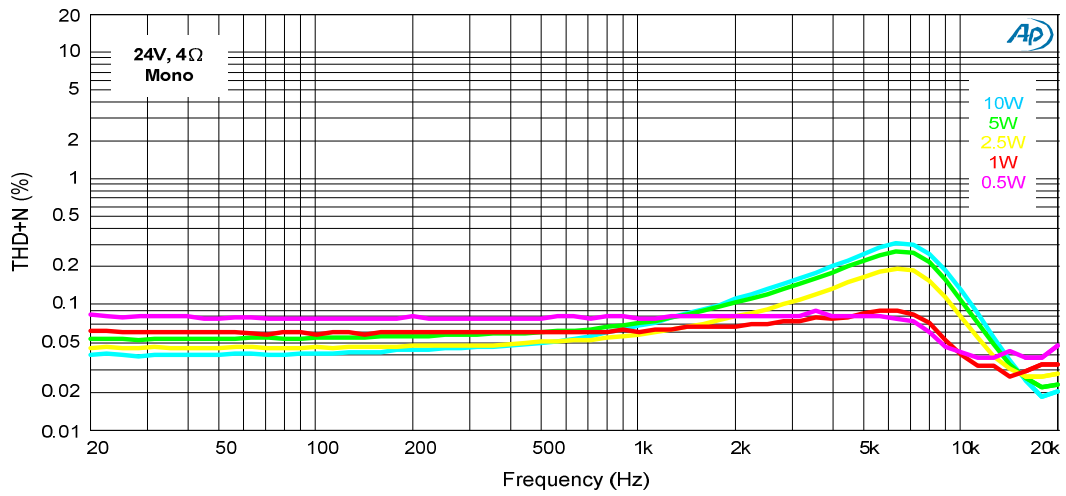
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

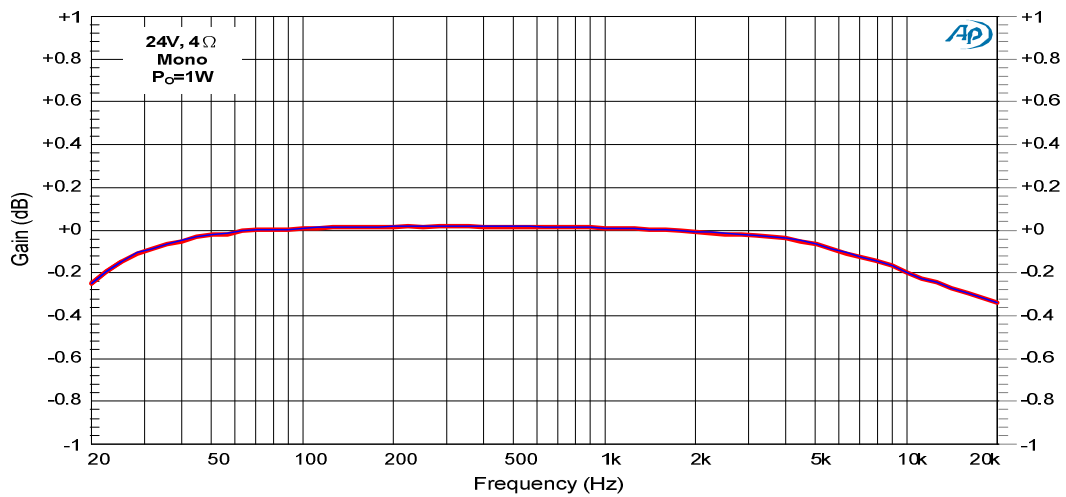
Total Harmonic Distortion + Noise vs. Output Power (Mono)



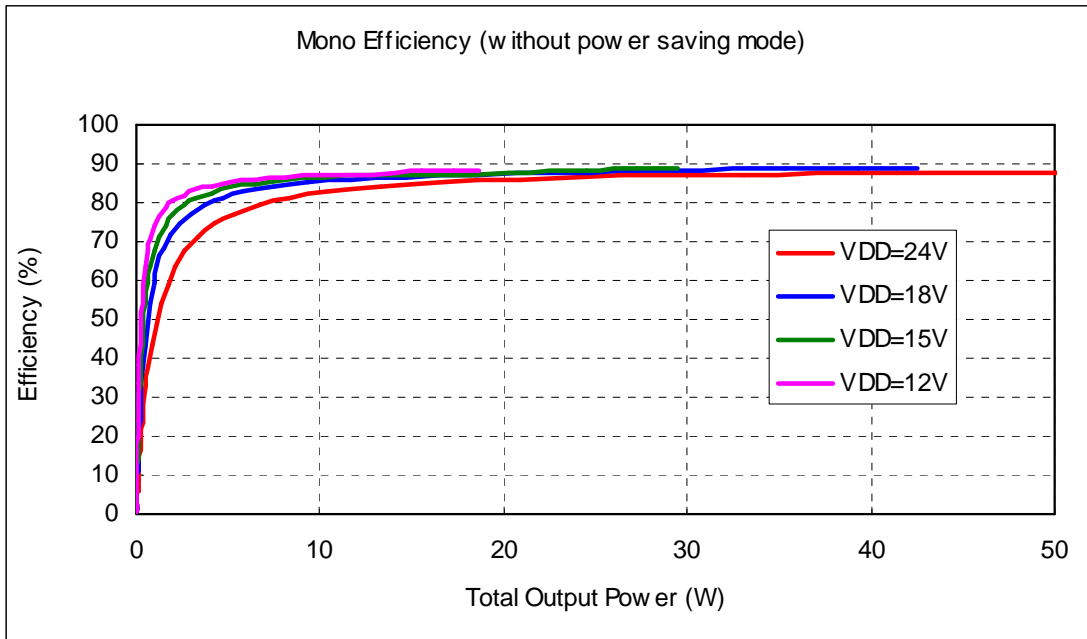
Total Harmonic Distortion + Noise vs. Frequency (Mono)



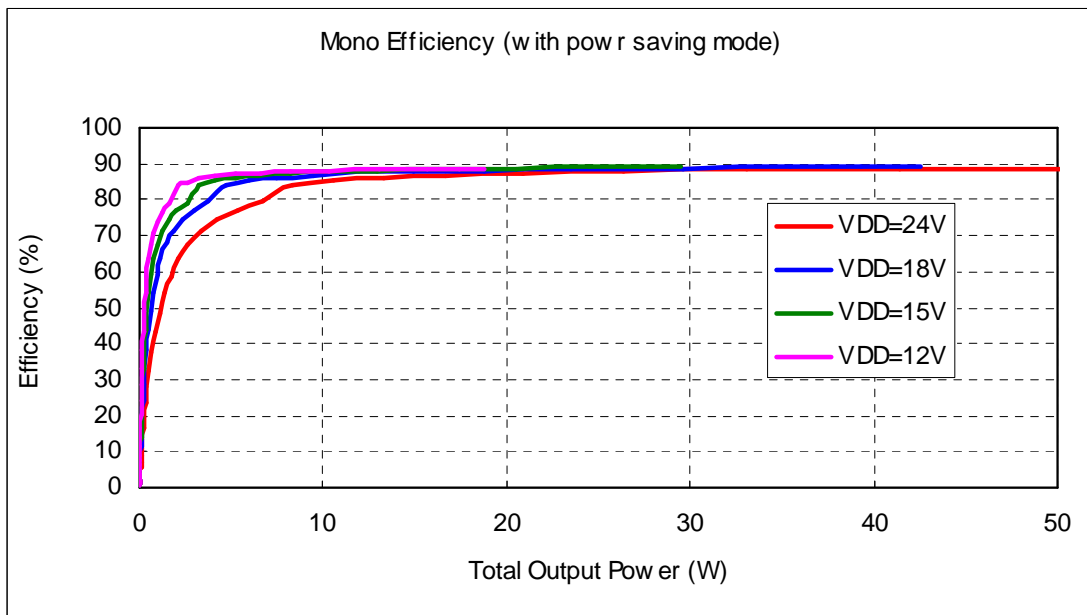
Frequency Response (Mono)



Efficiency (Mono)



Efficiency (Mono) for Power Saving Mode



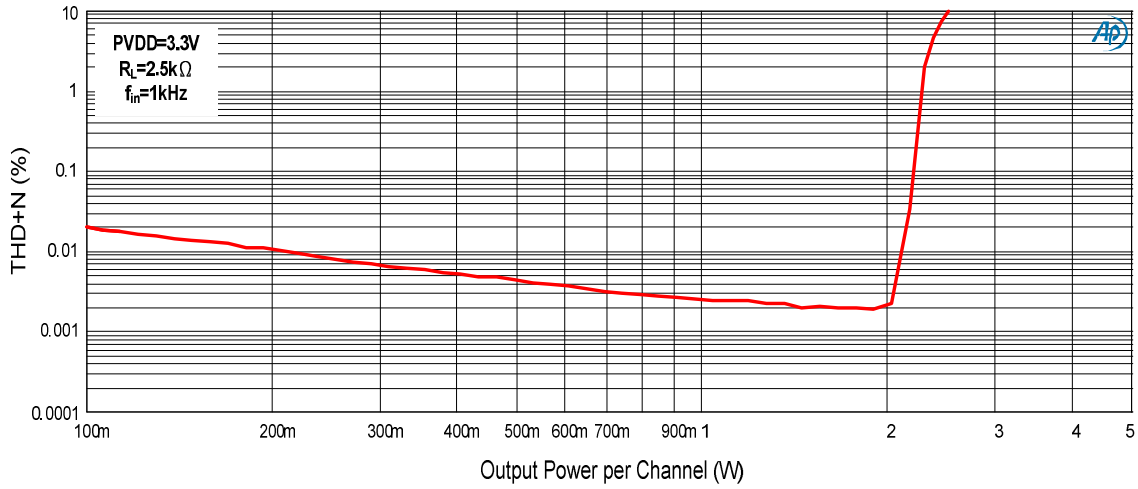
Electrical Characteristics and Specifications for Line Driver

● **Capless line driver**

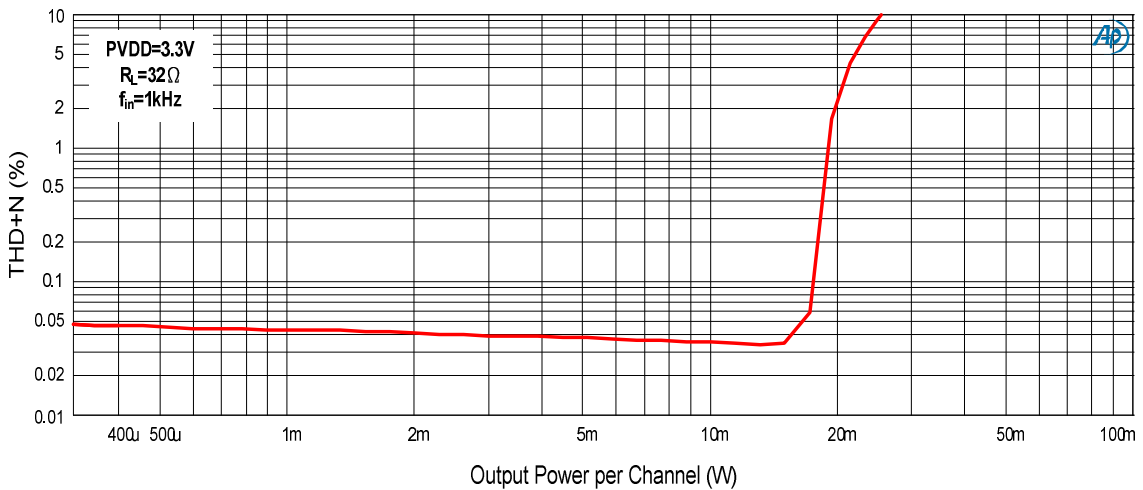
Condition: $T_A=25^\circ\text{C}$, $PVDD=3.3\text{V}$, $T_A=25^\circ\text{C}$, $R_L=2.5\text{k}\Omega$, $C_{FLY}=C_{PVSS}=1\mu\text{F}$, $C_{IN}=1\mu\text{F}$, $R_I=10\text{k}\Omega$, $R_F=20\text{k}\Omega$ (unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-----------------------|---|--|-----|-------|-----|------------------|
| V_O | Output Voltage (Outputs In Phase) | THD+N=1%, $V_{DD}=3.3\text{V}$, $f_{IN}=1\text{kHz}$ | | 2.2 | | Vrms |
| THD+N | Total Harmonic Distortion Plus Noise | $V_O=2\text{Vrms}$, $f_{IN}=1\text{kHz}$ | | 0.002 | | % |
| Crosstalk | Channel Separation | $V_O=2\text{Vrms}$, $f_{IN}=1\text{kHz}$ | | -106 | | dB |
| V_N | Output Noise | $R_I=10\text{k}$, $R_F=10\text{k}$ | | 11 | 15 | μVrms |
| V_{SR} | Slew Rate | | | 8 | | V/ μs |
| SNR | Signal to Noise Ratio | $V_O=2\text{Vrms}$, $R_I=10\text{k}$, $R_F=10\text{k}$, A-weighted | | 107 | | dB |
| G_{BW} | Unit-Gain Bandwidth | | | 8 | | MHz |
| A_{VO} | Open-Loop Gain | | 80 | | | dB |
| V_{OS} | Output Offset Voltage | $V_{DD}=3\text{V}$ to 5.5V , Input Grounded | -5 | | 5 | mV |
| PSRR | Power Supply Rejection Ratio | $V_{DD}=3\text{V}$ to 5.5V , $V_{rr}=200\text{mVrms}$, $f_{IN}=1\text{kHz}$ | | -80 | -60 | dB |
| R_I | Input Resistor Range | | 1 | 10 | 47 | $\text{k}\Omega$ |
| R_F | Feedback Resistor Range | | 4.7 | 20 | 100 | $\text{k}\Omega$ |
| f_{CP} | Charge-Pump Frequency | | 400 | 500 | 600 | kHz |
| | Maximum capacitive Load | | | 220 | | pF |
| V_{UVP} | External Under Voltage Detection | | | 1.25 | | V |
| I_{HYS} | External Under Voltage Detection Hysteresis Current | | | 5 | | μA |
| $T_{\text{start-up}}$ | Start-up Time | | | 2 | | ms |

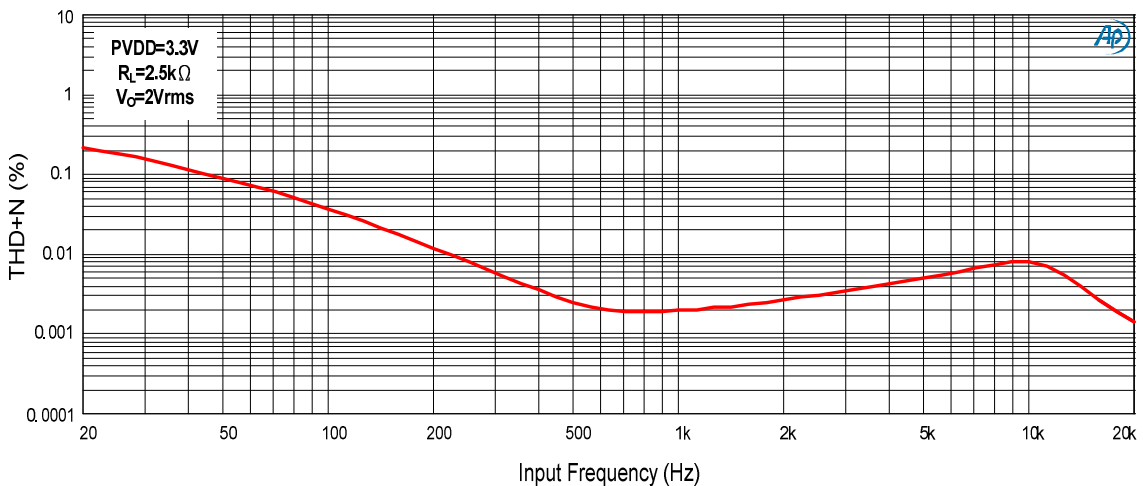
Total Harmonic Distortion + Noise (THD+N) vs. Output Power ($R_L=2.5k\Omega$)



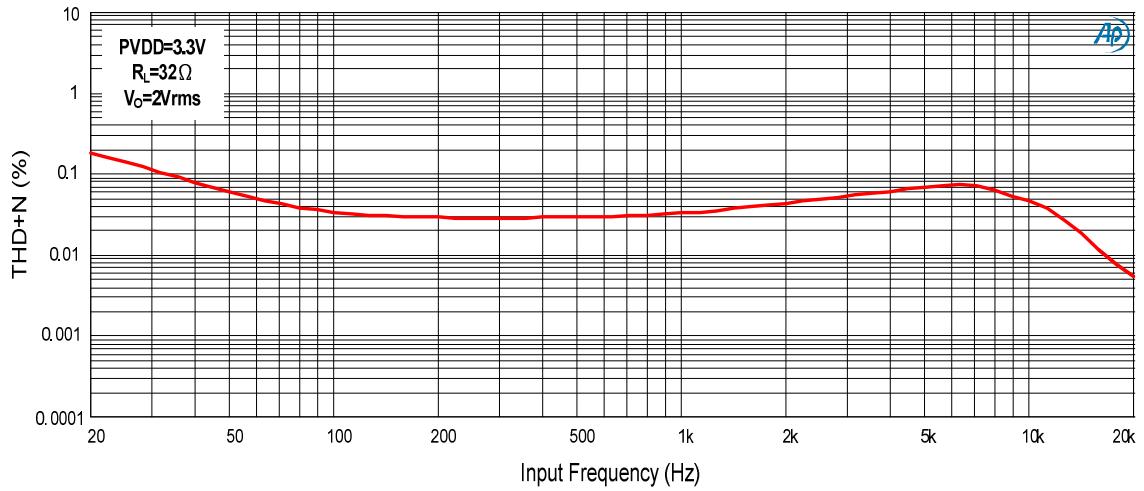
Total Harmonic Distortion + Noise (THD+N) vs. Output Power ($R_L=32\Omega$)



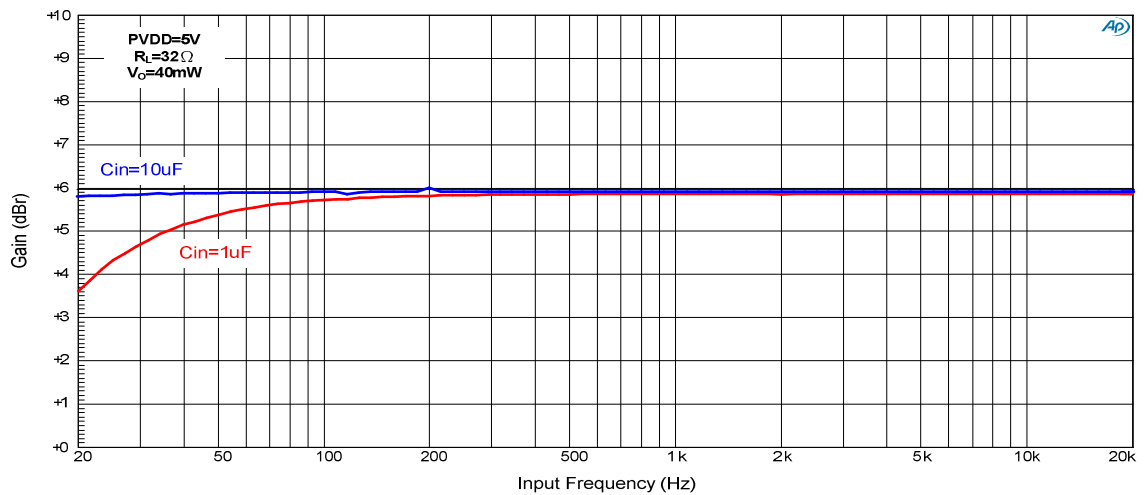
Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency ($R_L=2.5k\Omega$)



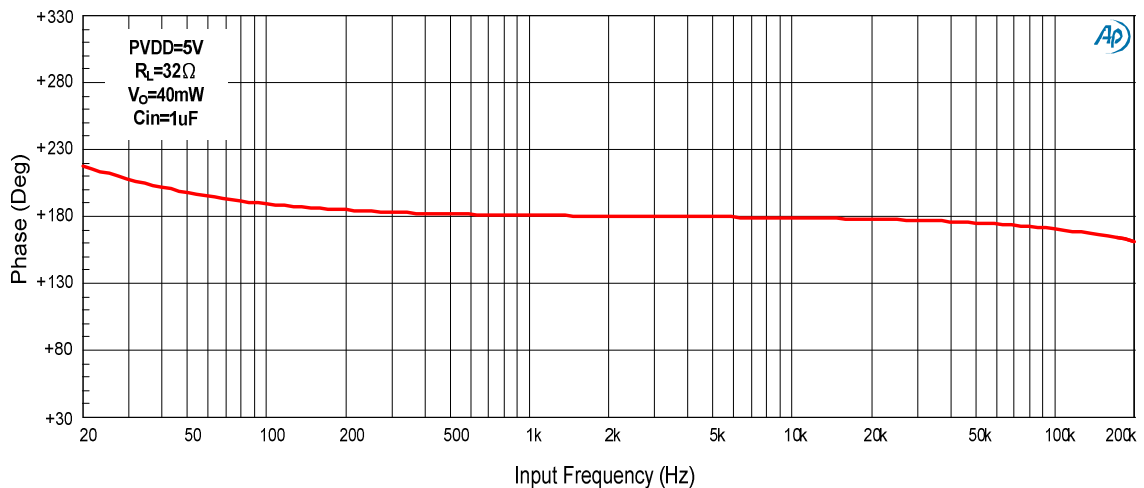
Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency ($R_L=32\ \Omega$)



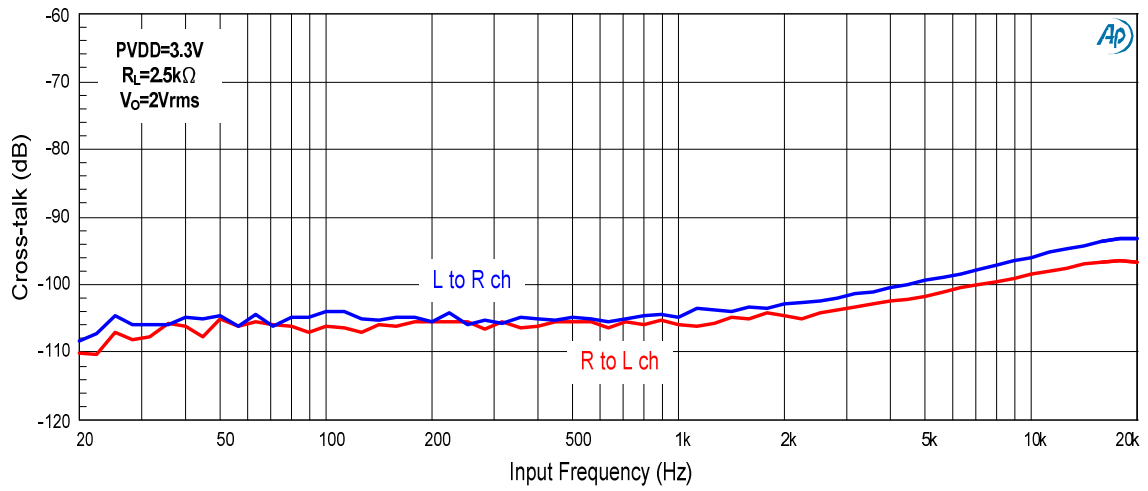
Gain vs. Signal Frequency



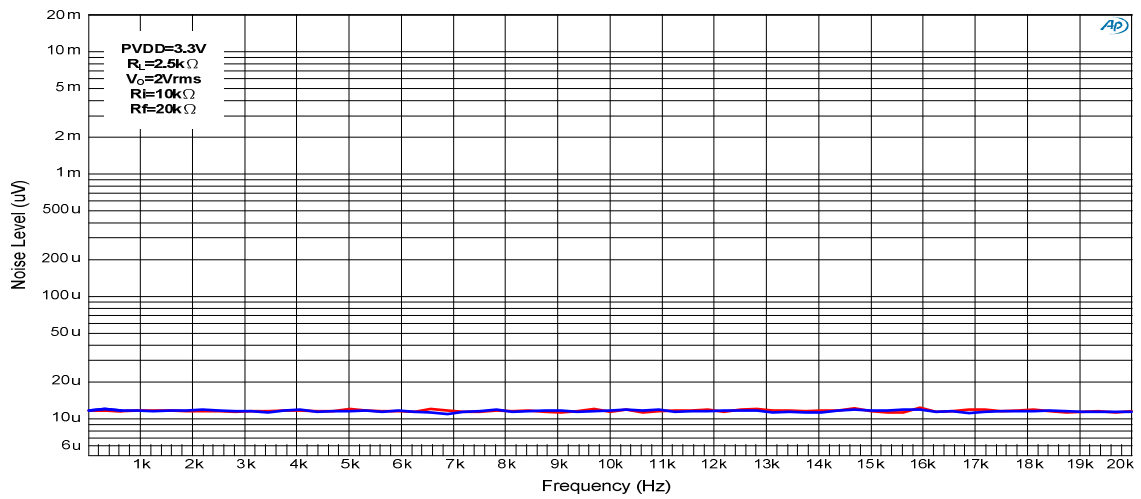
Phase vs. Signal Frequency



Cross-talk

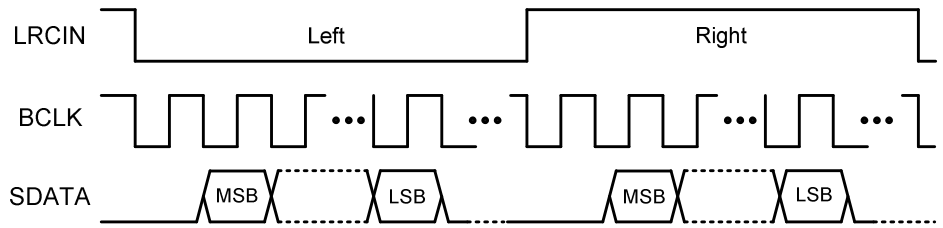


Noise Level

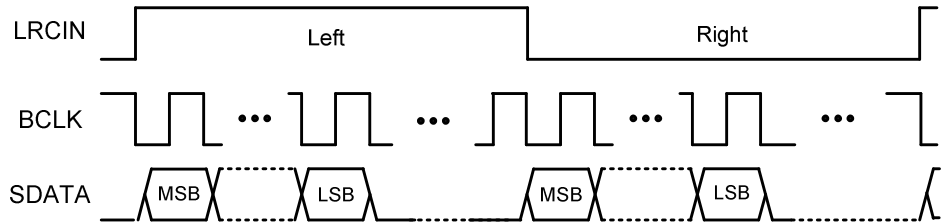


Interface configuration

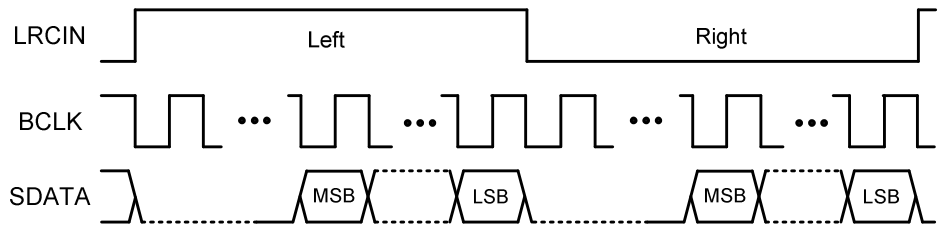
● I²S



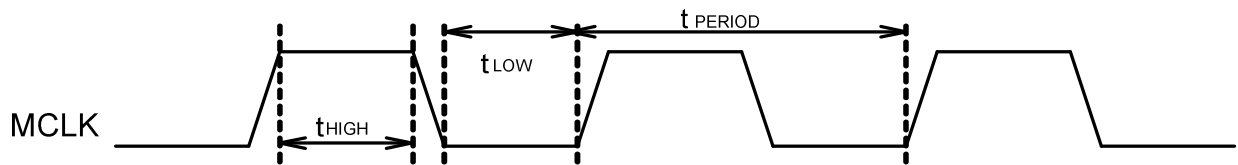
● Left-Alignment



● Right-Alignment

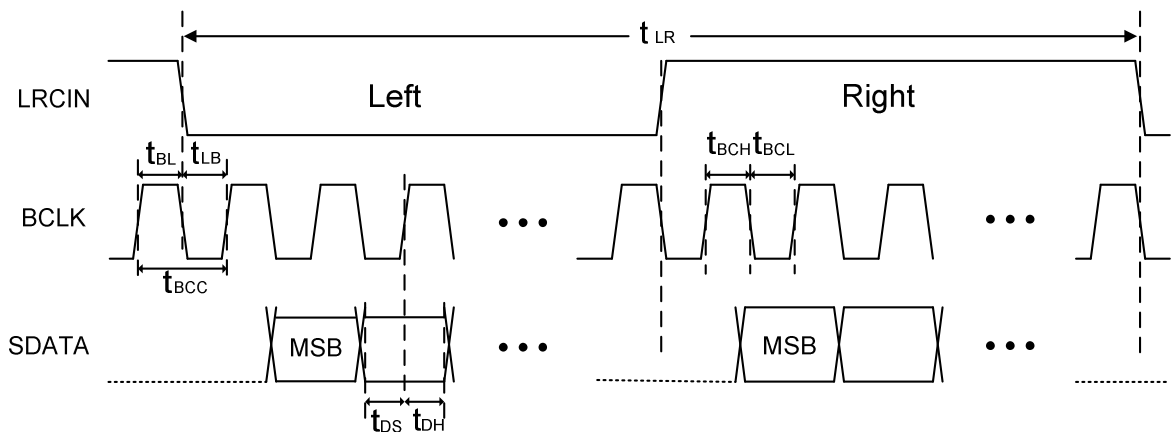


● System Clock Timing



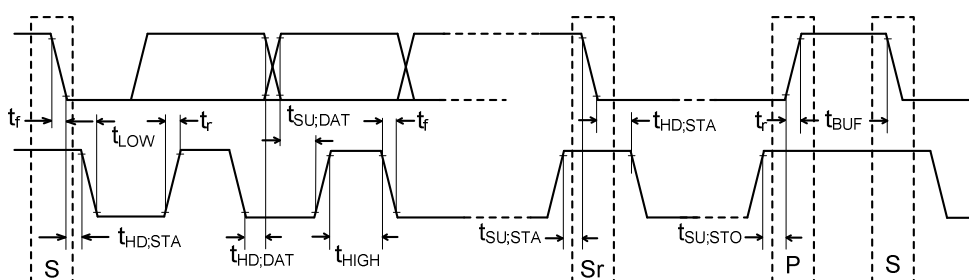
$t_{HIGH} \geq 40.4 \text{ ns}$, $t_{LOW} \geq 40.4 \text{ ns}$, $t_{PERIOD} \geq 80.8 \text{ ns}$ Default setting, when PLL is enable
 $t_{HIGH} \geq 10.1 \text{ ns}$, $t_{LOW} \geq 10.1 \text{ ns}$, $t_{PERIOD} \geq 20.2 \text{ ns}$ When PLL is disable

● Timing Relationship (Using I²S format as an example)



| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|--------------------------------|--------|-----|-------|---------|
| t_{LR} | LRCIN Period ($1/F_S$) | 10.41 | | 31.25 | μs |
| t_{BL} | BCLK Rising Edge to LRCIN Edge | 50 | | | ns |
| t_{LB} | LRCIN Edge to BCLK Rising Edge | 50 | | | ns |
| t_{BCC} | BCLK Period ($1/64F_S$) | 162.76 | | 488.3 | ns |
| t_{BCH} | BCLK Pulse Width High | 81.38 | | 244 | ns |
| t_{BCL} | BCLK Pulse Width Low | 81.38 | | 244 | ns |
| t_{DS} | SDATA Set-Up Time | 50 | | | ns |
| t_{DH} | SDATA Hold Time | 50 | | | ns |

● I²C Timing



| Parameter | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|--------------|---------------|------|-------------|------|---------|
| | | MIN. | MAX. | MIN. | MAX. | |
| SCL clock frequency | f_{SCL} | 0 | 100 | 0 | 400 | kHz |
| Hold time for repeated START condition | $t_{HD;STA}$ | 4.0 | --- | 0.6 | --- | μs |
| LOW period of the SCL clock | t_{LOW} | 4.7 | --- | 1.3 | --- | μs |
| HIGH period of the SCL clock | t_{HIGH} | 4.0 | --- | 0.6 | --- | μs |
| Setup time for repeated START condition | $t_{SU;STA}$ | 4.7 | --- | 0.6 | --- | μs |
| Hold time for I ² C bus data | $t_{HD;DAT}$ | 0 | 3.45 | 0 | 0.9 | μs |
| Setup time for I ² C bus data | $t_{SU;DAT}$ | 250 | --- | 100 | --- | Ns |
| Rise time of both SDA and SCL signals | t_r | --- | 1000 | $20+0.1C_b$ | 300 | Ns |
| Fall time of both SDA and SCL signals | t_f | --- | 300 | $20+0.1C_b$ | 300 | Ns |
| Setup time for STOP condition | $t_{SU;STO}$ | 4.0 | --- | 0.6 | --- | μs |
| Bus free time between STOP and the next START condition | t_{BUF} | 4.7 | --- | 1.3 | --- | μs |
| Capacitive load for each bus line | C_b | | 400 | | 400 | pF |
| Noise margin at the LOW level for each connected device (including hysteresis) | V_{nL} | $0.1V_{DD}$ | --- | $0.1V_{DD}$ | --- | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | V_{nH} | $0.2V_{DD}$ | --- | $0.2V_{DD}$ | --- | V |

Operation Description**● Operation modes****(i) Without I²C control**

The default settings, Bass, Treble, EQ, Volume, DRC, PLL, Subwoofer Bandwidth, ..., and Sub-woofer gain are applied to register table content when using AD87588 without I²C control. The more information about default settings, please refer to the highlighted column of register table section.

(ii) With I²C control

When using I²C control, user can program suitable parameters into AD87588 for their specific applications. Please refer to the register table section to get the more detail.

● Internal PLL (PLL)

AD87588 has a built-in PLL internally. When the external MCLK clock is high quality enough, you can bypass the PLL function by pulling the PLL pin is high. Otherwise, the internal PLL with an external reference MCLK is highly recommended.

● Default volume (DEF)

The default volume of AD87588 is +1.625dB while DEF pin setting at high, the default volume can be muted by selecting DEF pin low. When using AD87588 without I²C control interface, users should pull this pin high. The default value of register table setting will be changed for different applications. About the more detailed information, please refer to the register table section.

● LINEIN

When set LINEIN pin low, AD87588 will select I²S data from SDATA0. On the contrary, AD87588 will select I²S data from SDATA1 when set LINEIN pin high. Before changing LINEIN pin status, users need to send I²C signal to mute AD87588 to avoid pop sound.

● MS

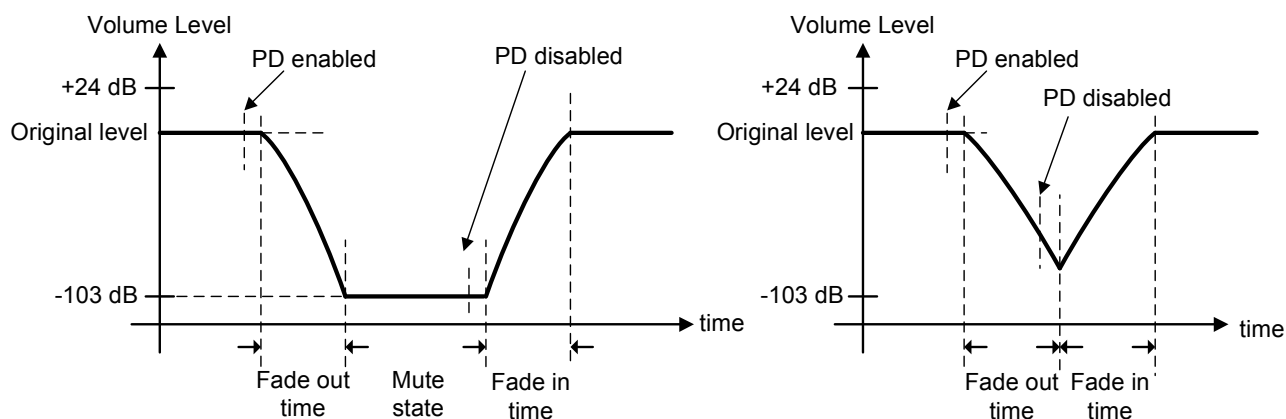
During system initialization, the content of this EEPROM can be loaded automatically into AD87588 registers and RAM when MS pin of AD87588 is set high. In other words, during initialization, for a short period of time, AD87588 will behave like an IC master to fetch data from EEPROM content into registers and RAM automatically. After this is finished, AD87588 will become an I²C slave, waiting the master to send commands. When MS pin is set low, AD87588 will always behave like an I²C slave. Note that the size of the EEPROM shall be larger than 4Kb, such as Microchips' 24LC04B, because in total, there are 371 bytes of data. The first 256 bytes of data is stored from address 1010000, and the last 115 bytes of data is stored from address 101001.

- **Reset**

When the $\overline{\text{RESET}}$ pin is lowered, AD87588 will clear the stored data and reset the register table to default values. AD87588 will exit reset state at the 256th MCLK cycle after the $\overline{\text{RESET}}$ pin is raised to high.

- **Power down control**

AD87588 has a built-in volume fade-in/fade-out design for PD/Mute function. The relative PD timing diagrams for loudspeakers are shown below.



The volume level will be decreased to $-\infty$ dB in several LRCIN cycles. Once the fade-out procedure is finished, AD87588 will turn off the power stages, stop clock signals (MCLK, BCLK) from feeding into digital circuit and turn off the current of the internal analog circuits. After PD pin is pulled low, AD87588 needs up to 256 LRCIN clocks to finish the above works before entering power down state. Users can't program AD87588 during power down state, but all the settings of register table will still be kept except that DVDD is removed.

If the PD function is disabled in the midway of the fade-out procedure, AD87588 will also execute the fade-in procedure. In addition, AD87588 will establish the analog circuits' bias current and feed the clock signals (MCLK, BCLK) into digital circuits. Then, AD87588 will return to its normal operation without power down.

- **Self-protection circuits**

AD87588 has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

- (i) When the internal junction temperature is higher than 150°C, power stages will be turned off and AD87588 will return to normal operation once the temperature drops to 120°C. The temperature values may vary around 10%.
- (ii) The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or GND/VDD. For normal 24V operations, the current flowing through the power stage will be less than 5A for stereo configuration or less than 10A for mono configuration. Otherwise, the short-circuit detectors may pull the $\overline{\text{ERROR}}$ pin to DGND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain $\overline{\text{ERROR}}$ pin will be pulled low and latched into ERROR state.

Once the over-temperature or short-circuit condition is removed, AD87588 will exit ERROR state when one of the following conditions is met: (1) $\overline{\text{RESET}}$ pin is pulled low, (2) $\overline{\text{PD}}$ pin is pulled low, (3) Master mute is enabled through the I²C interface.

- (iii) Once the DVDD voltage is lower than 2.7V, AD87588 will turn off its loudspeaker power stages and cease the operation of digital processing circuits. When DVDD becomes larger than 2.8V, AD87588 will return to normal operation.

- **Anti-pop design**

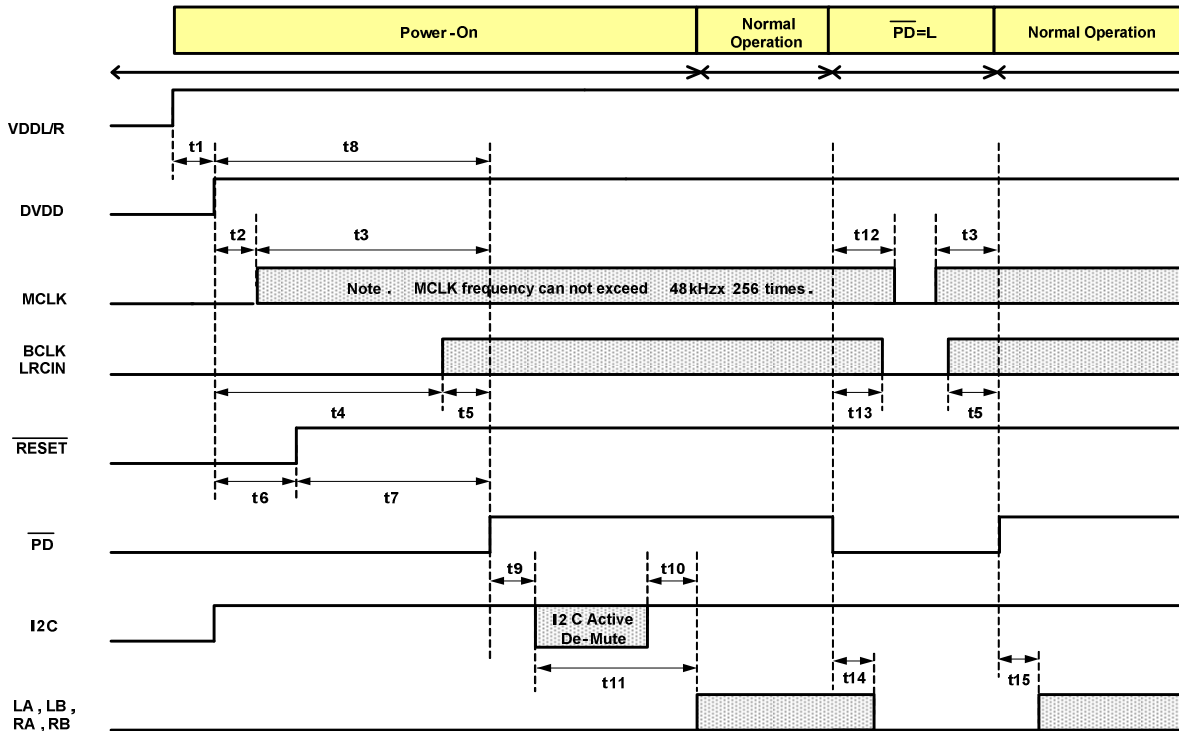
AD87588 will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- **3D surround sound**

AD87588 provides the virtual surround sound technology with greater separation and depth voice quality for stereo signals.

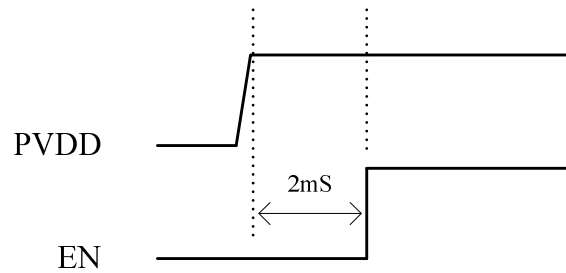
● Power on sequence

Hereunder is AD87588's power on sequence for Class-D amplifier. Please note that we suggested users set DEF pin at low state initially, and then give a de-mute command via I²C when the whole system is stable.



| Symbol | Condition | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| t1 | | 0 | - | msec |
| t2 | | 0 | - | msec |
| t3 | | 10 | - | msec |
| t4 | | 0 | - | msec |
| t5 | | 10 | - | msec |
| t6 | | 10 | - | msec |
| t7 | | 0 | - | msec |
| t8 | | 200 | - | msec |
| t9 | | 20 | - | msec |
| t10 | DEF=L | - | 0.1 | msec |
| t11 | DEF=H | - | 0.1 | msec |
| t12 | | 25 | - | msec |
| t13 | | 25 | - | msec |
| t14 | | - | 22 | msec |
| t15 | DEF= L or H | - | 0.1 | Msec |

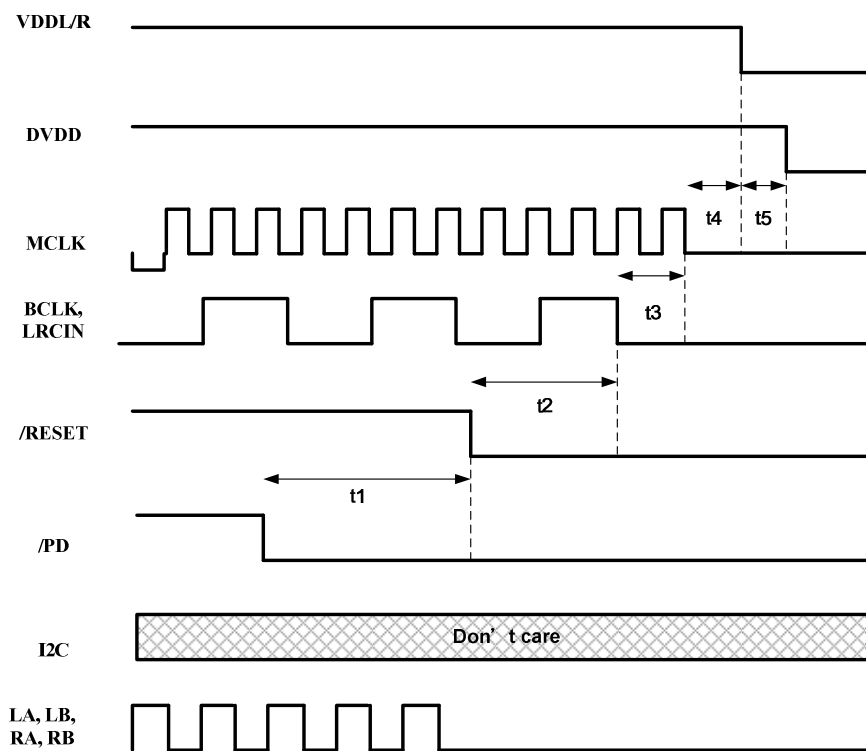
Hereunder is AD87588's Line Driver power on sequence. Please put 2mS timing delay to enable the Line Driver after PVDD power up ready.



Power on sequence for Line Driver

● Power off sequence

Hereunder is AD87588's power off sequence for Class-D amplifier.



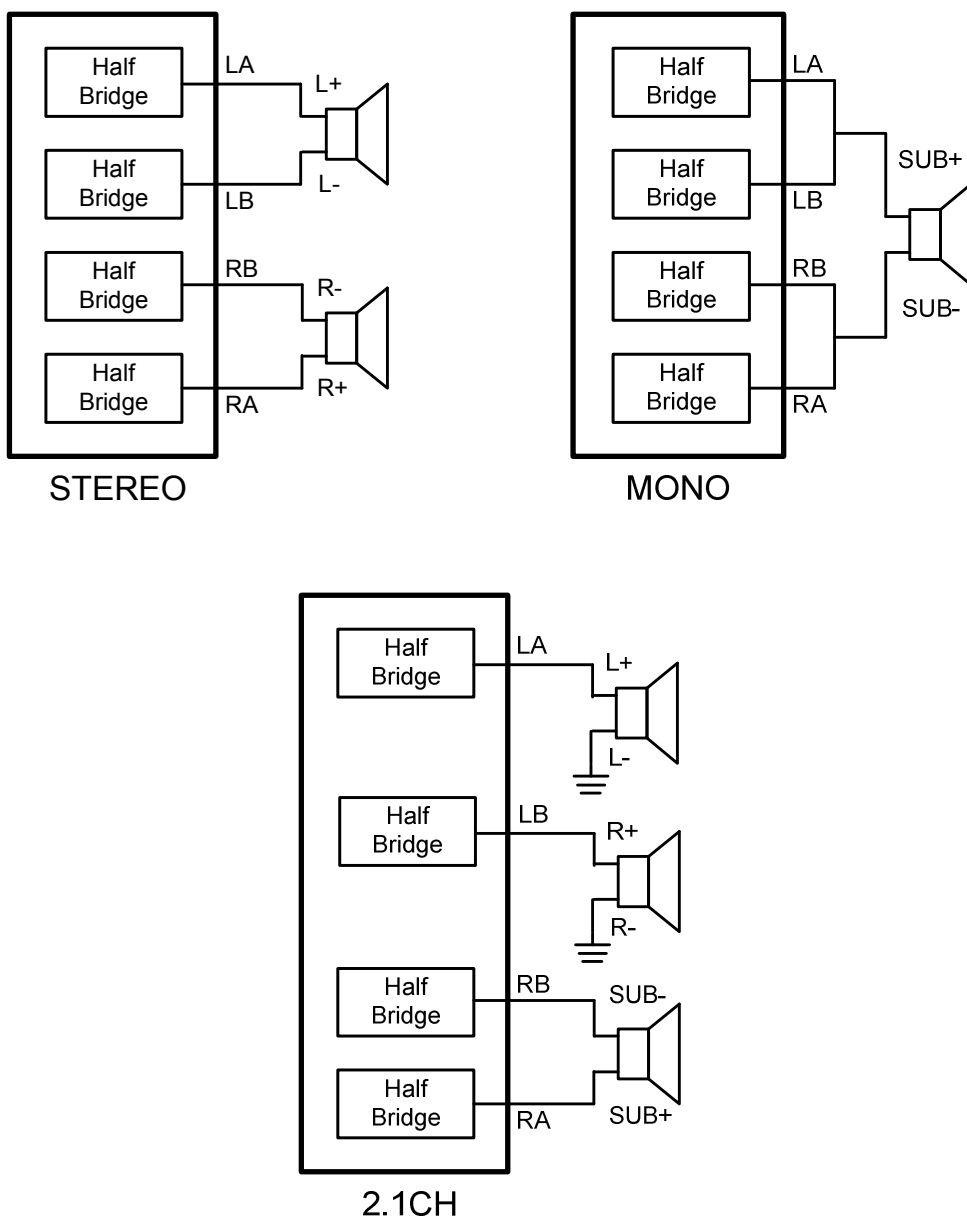
| Symbol | Condition | Min | Max | Units |
|--------|-----------|-----|-----|-------|
| t1 | | 35 | - | msec |
| t2 | | 0.1 | - | msec |
| t3 | | 0 | - | msec |
| t4 | | 1 | - | msec |
| t5 | | 1 | - | msec |

● Output configuration

AD87588 can be configured to Stereo, Mono or 2.1CH mode by the pin of CFG0 and CFG1 to enable it.

| CFG1 | CFG0 | Configuration Mode |
|------|------|--------------------|
| 0 | 0 | Reserved |
| 0 | 1 | 2.1CH |
| 1 | 0 | Stereo |
| 1 | 1 | Mono |

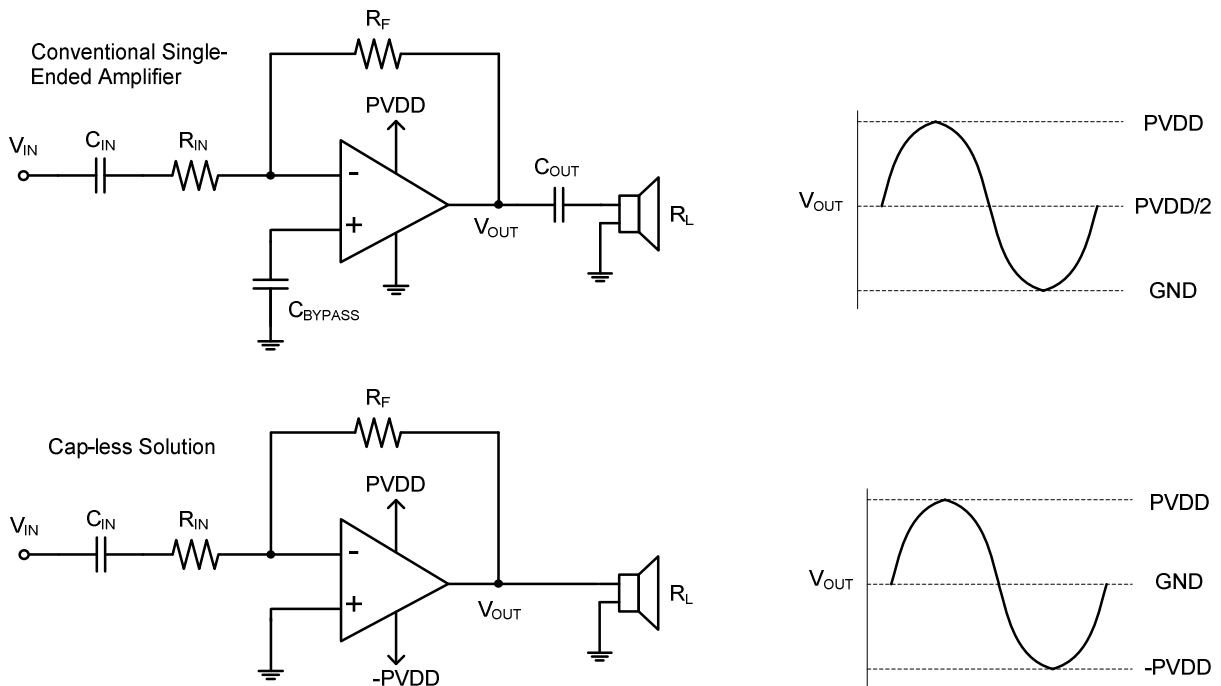
Configuration figures:



● **Line Driver Amplifiers Operation**

A conventional inverting line-driver amplifier always requires an output dc-blocking capacitor and a bypass capacitor. DC blocking capacitors are large in size and cost a lot. It also restricts the output low frequency response. POP will occur if the charge and discharge processes on output capacitors are not carefully take cared. Besides, it needs to wait for a long time to charge V_{OUT} from 0V to $PVDD/2$.

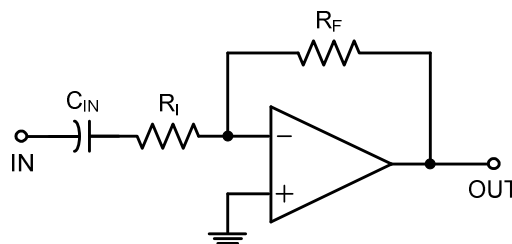
For a cap-less line driver, a negative supply voltage (-PVDD) is produced by the integrated charge-pump, and feeds to line driver's negative supply instead of ground. The positive input can directly connect to ground without a C_{BYPASS} , and V_{OUT} is biased at ground which can eliminate the output dc-blocking capacitors. The output voltage swing is doubled compared to conventional amplifiers.



● **Gain Setting Resistors (R_I and R_F) in Line Driver**

The line driver's gain is determined by R_I and R_F . The configuration of the amplifier is inverting type, The gain equation is listed as follows:

Inverting configuration:
$$A_v = -\frac{R_F}{R_I}$$



The values of R_I and R_F must be chosen with consideration of stability, frequency response and noise. The recommended value of R_I is in the range from $1k\Omega$ to $47k\Omega$, and R_F is from $4.7k\Omega$ to $100k\Omega$ for. The gain is in the range from $-1V/V$ to $-10V/V$ for inverting configuration. The following table show the recommended resistor values for different configurations.

| R_I (k Ω) | R_F (k Ω) | Inverting Input Gain (V/V) |
|---------------------|---------------------|----------------------------|
| 22 | 22 | -1 |
| 15 | 30 | -2 |
| 33 | 68 | -2.1 |
| 10 | 100 | -10 |

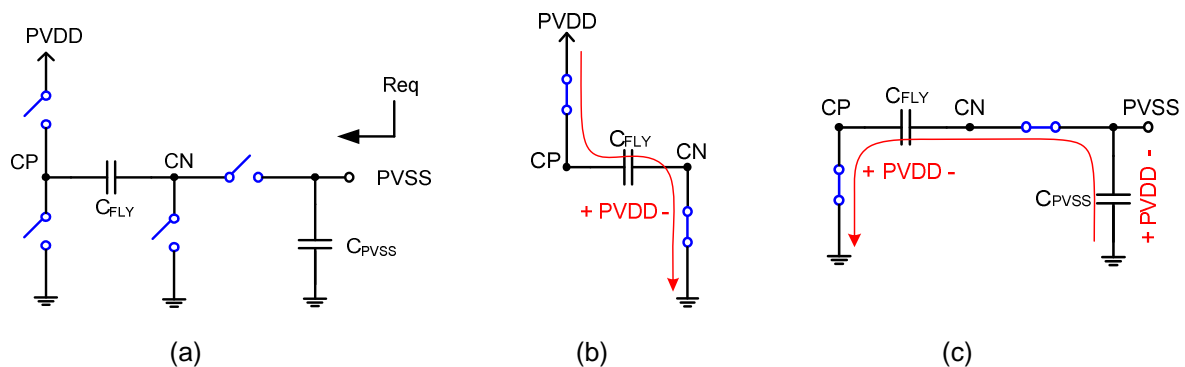
● **Input Blocking Capacitors (C_{IN}) for Line Driver**

An input blocking capacitor is required to block the dc voltage of the audio source and allows the input to bias at a proper dc level for optimum operation. The input capacitor and input resistor (R_I) form a high-pass filter with the corner frequency determined as following equation:

$$f_c = \frac{1}{2\pi R_I C_{IN}}$$

● **Charge-Pump Operation for Line Driver**

The charge-pump is used to generate a negative supply voltage to supply to line-driver. It needs two external capacitors, C_{FLY} and C_{PVSS} , for normal operation, see figure (a). The operation can be analyzed with two phase. In phase I, see figure (b), C_{FLY} is charged to PVDD, and in phase II, see figure (c), the charges on C_{FLY} are shared with C_{PVSS} , that makes PVSS a negative voltage. After an adequate clock cycles, PVSS will be equaled to $-PVDD$. Low ESR capacitors are recommended, and the typical value of C_{FLY} and C_{PVSS} is $1\mu F$. A smaller capacitance can be used, but the maximum output voltage may be reduced.



● Decoupling Capacitors in Line Driver

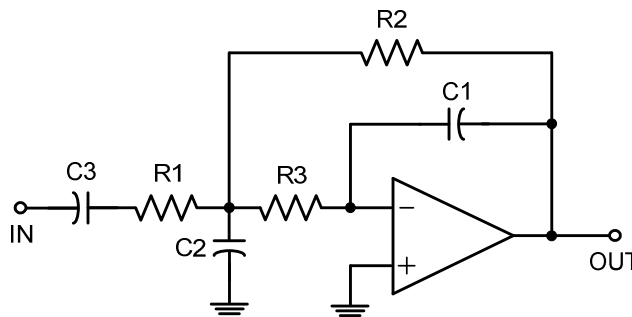
A low ESR power supply decoupling capacitor for PVDD is required for better performance. The capacitor should place as close to chip as possible, the value is typically 1μF. For filtering low frequency noise signals, a 10μF or greater capacitor placed near the chip is recommended.

● Second-Order Filter Configuration for Line Driver

Line Driver can be used like a standard OPAMP. Several filter topologies can be implemented by using line driver, both single-ended and differential input configuration. For inverting input configuration, the overall gain

is $-\frac{R2}{R1}$, the high-pass filter's cutoff frequency is $\frac{1}{2\pi R1 C3}$, the low-pass filter's cutoff frequency is

$\frac{1}{2\pi\sqrt{R2R3C1C2}}$, The following table show the detail component values.



| Gain (V/V) | High Pass (Hz) | Low Pass (kHz) | C1 (pF) | C2 (pF) | C3 (μF) | R1 (kΩ) | R2 (kΩ) | R3 (kΩ) |
|------------|----------------|----------------|---------|---------|---------|---------|---------|---------|
| -1 | 1.6 | 40 | 100 | 680 | 10 | 10 | 10 | 24 |
| -1.5 | 1.3 | 40 | 68 | 680 | 15 | 8.2 | 12 | 30 |
| -2 | 1.6 | 60 | 33 | 150 | 6.8 | 15 | 30 | 47 |
| -2 | 1.6 | 30 | 47 | 470 | 6.8 | 15 | 30 | 43 |
| -3.33 | 1.2 | 30 | 33 | 470 | 10 | 13 | 43 | 43 |
| -10 | 1.5 | 30 | 22 | 1000 | 22 | 4.7 | 47 | 27 |

● External Under-Voltage Protection for Line Driver

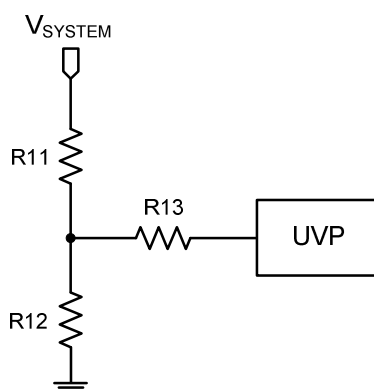
The external under-voltage protection is used to mute the line-driver before any input voltage change to generate a POP. The threshold of UVP pin is designed to 1.25V. By using a resistor divider, users can decide the UVP level and hysteresis level. The levels can be obtained by following equations:

$$V_{UVP} = (1.25V - 6\mu A \times R13) \times (R11 + R12) / R12$$

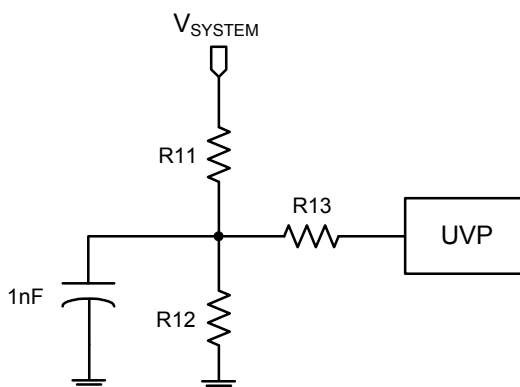
$$Hysteresis = 5\mu A \times R13 \times (R11 + R12) / R12$$

With the condition $R13 \gg (R11 // R12)$.

For example, to obtain $V_{UVP}=2.67V$, $Hysteresis=0.37V$, $R11=1.5k\Omega$, $R12=1k\Omega$, $R13=30k\Omega$.



The UVP pin voltage ripple needs to take care during power up state within 2mS. The UVP pin ripple lower 1.25V by 2~4 times will trigger test mode in Line Driver. To put a capacitor parallel with UVP pin can improve test mode mis-operating triggered while V_{SYSTEM} is not stable during power up initially. That's recommended 2mS timing delay to enable the Line Driver after PVDD power up ready.



UVP pin is pulled high internally, and therefore it can be floated to disable the external under-voltage protection feature.

I²C-Bus Transfer Protocol

● Introduction

AD87588 employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD87588 is always an I²C slave device.

● Protocol

■ START and STOP condition

START is identified by a high to low transition of the SDA signal.. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD87588 and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

■ Data validity

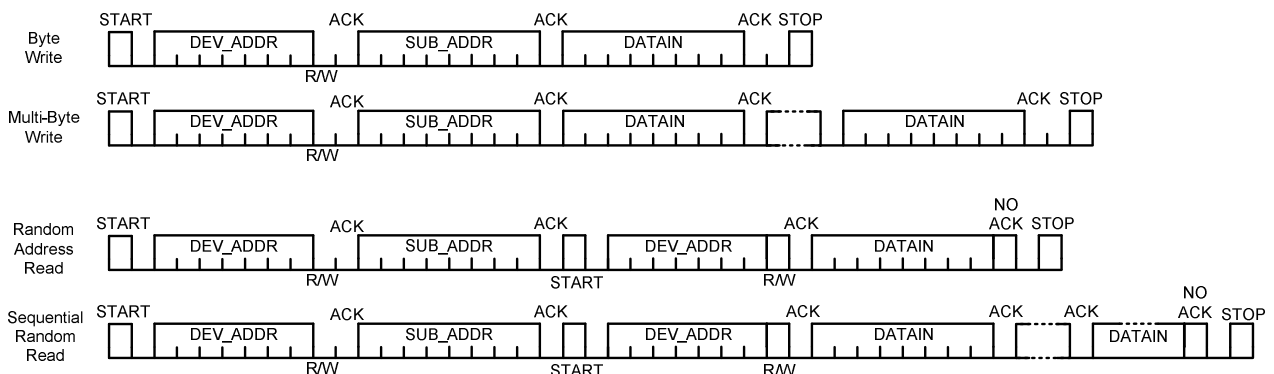
The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD87588 samples the SDA signal at the rising edge of SCL signal.

■ Device addressing

The master generates 7-bit address to recognize slave devices. When AD87588 receives 7-bit address matched with 0110x0y (where x and y can be selected by external SA0 and SA1 pins, respectively), AD87588 will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD87588 internal sub-addresses.

■ Data transferring

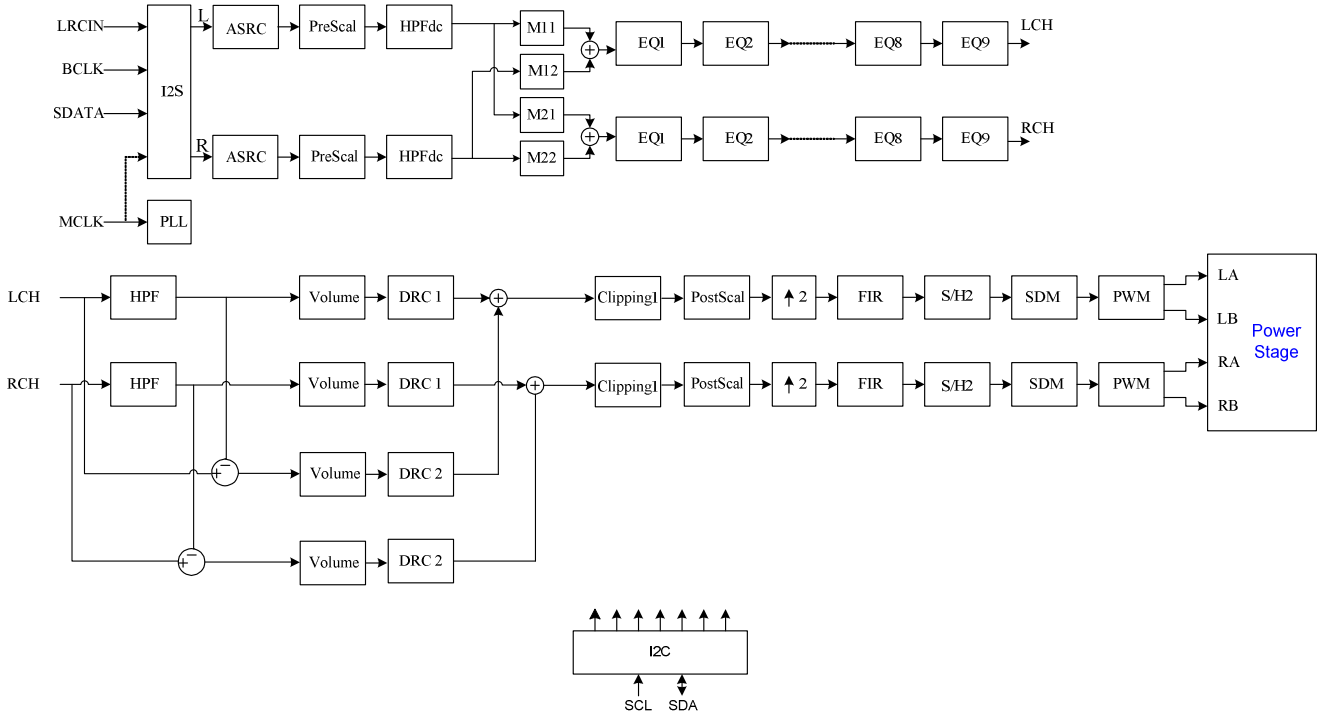
Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD87588 supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



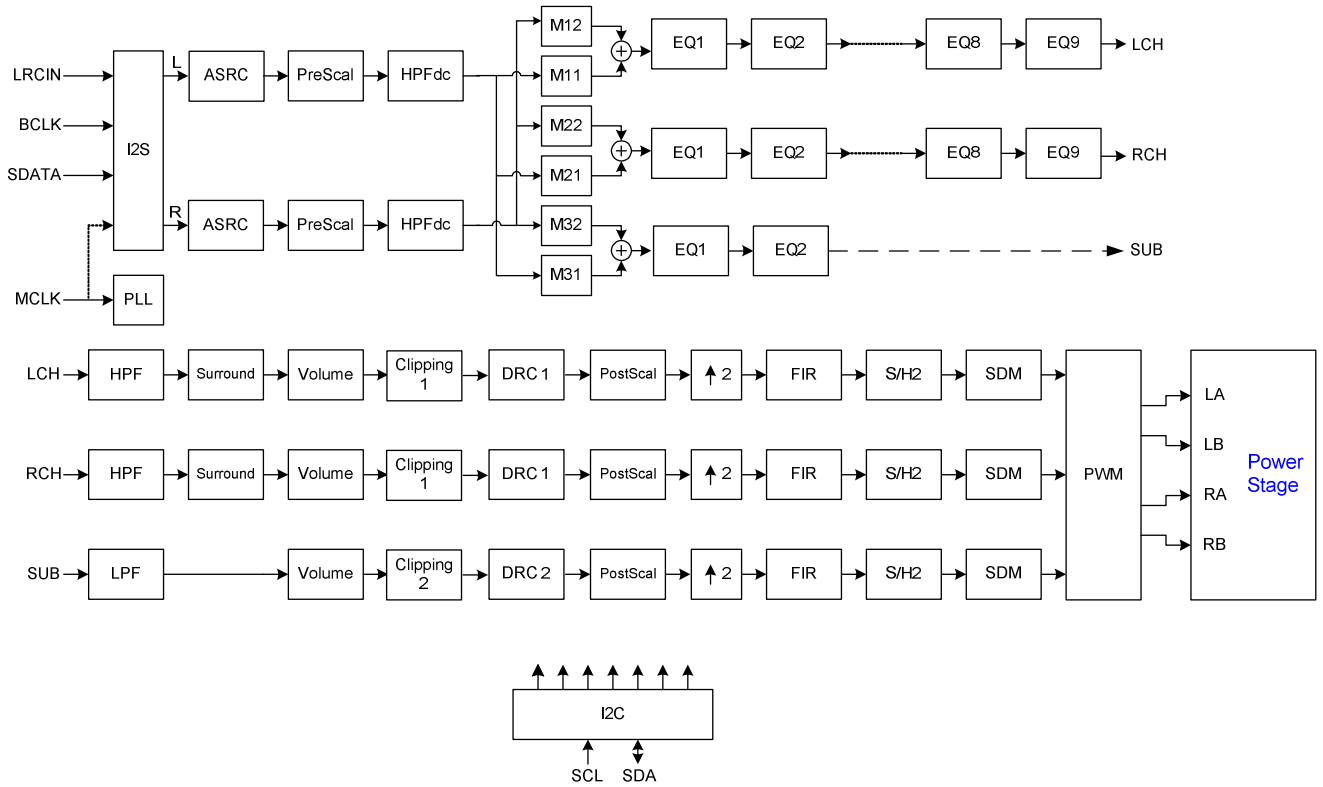
Register Table

The AD87588’s audio signal processing data flow is shown below. Users can control these functions by programming appropriate settings in the register table. In this section, the register table is summarized first. The definition of each register follows in the next section.

Dual bands DRC enable (only for stereo mode, CFG0=Low)



Dual bands DRC disable



| Address | Name | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] |
|---------|-------|----------|----------|--------|----------|--------|---------|----------|--------|
| 0X00 | SCTL1 | IF[2] | IF[1] | IF[0] | Reserved | PWML_X | PWML_X | LV_UVSEL | LRXC |
| 0X01 | SCTL2 | Reserved | | FS[1] | FS[0] | PMF[3] | PMF[2] | PMF[1] | PMF[0] |
| 0X02 | SCTL3 | EN_CLKO | Reserved | | | MUTE | CM1 | CM2 | CM3 |
| 0X03 | MVOL | MV[7] | MV[6] | MV[5] | MV[4] | MV[3] | MV[2] | MV[1] | MV[0] |
| 0X04 | C1VOL | C1V[7] | C1V[6] | C1V[5] | C1V[4] | C1V[3] | C1V[2] | C1V[1] | C1V[0] |
| 0X05 | C2VOL | C2V[7] | C2V[6] | C2V[5] | C2V[4] | C2V[3] | C2V[2] | C2V[1] | C2V[0] |
| 0X06 | C3VOL | C3V[7] | C3V[6] | C3V[5] | C3V[4] | C3V[3] | C3V[2] | C3V[1] | C3V[0] |
| 0X07 | BTONE | Reserved | | | BTC[4] | BTC[3] | BTC[2] | BTC[1] | BTC[0] |
| 0X08 | TTONE | Reserved | | | TTC[4] | TTC[3] | TTC[2] | TTC[1] | TTC[0] |
| 0X09 | XOF | Reserved | | | | XO[3] | XO[2] | XO[1] | XO[0] |
| 0X0A | SCTL4 | SRBP | BTE | TBDRCE | NGE | EQL | PSL | DSPB | HPB |
| 0X0B | C1CFG | Reserved | | | C1DRCM | C1PCBP | C1DRCBP | C1HPFBP | C1VBP |
| 0X0C | C2CFG | Reserved | | | C2DRCM | C2PCBP | C2DRCBP | C2HPFBP | C2VBP |
| 0X0D | C3CFG | Reserved | | | C3DRCM | C3PCBP | C3DRCBP | C3HPFBP | C3VBP |
| 0X0E | LAR | LA[3] | LA[2] | LA[1] | LA[0] | LR[3] | LR[2] | LR[1] | LR[0] |
| 0X0F | | Reserved | | | | | | | |
| 0X10 | ERDLY | Reserved | | | | | | | |

| | | | | | | | | | | |
|------|-----------------|----------|----------|-----------|--------------------|--------------------|--------------------|--------------------|--------------------|---------|
| 0X11 | SCTL5 | LOM | LOS | SW_RSTB | Reserved | | | DIS_MCLK_DET | QT_EN | PWM_SEL |
| 0X12 | HVUV | DIS_HVUV | Reserved | | | HV_UVSEL [3] | HV_UVSEL [2] | HV_UVSEL [1] | HV_UVSEL [0] | |
| 0X13 | NGCFG | Reserved | | | DIS_NG_FADE | Reserved | | NG_GAIN[1] | NG_GAIN[0] | |
| 0X14 | CFADDR | Reserved | CFA[6] | CFA[5] | CFA[4] | CFA[3] | CFA[2] | CFA[1] | CFA[0] | |
| 0X15 | A1CF1 | C1B[23] | C1B[22] | C1B[21] | C1B[20] | C1B[19] | C1B[18] | C1B[17] | C1B[16] | |
| 0X16 | A1CF2 | C1B[15] | C1B[14] | C1B[13] | C1B[12] | C1B[11] | C1B[10] | C1B[9] | C1B[8] | |
| 0X17 | A1CF3 | C1B[7] | C1B[6] | C1B[5] | C1B[4] | C1B[3] | C1B[2] | C1B[1] | C1B[0] | |
| 0X18 | A2CF1 | C2B[23] | C2B[22] | C2B[21] | C2B[20] | C2B[19] | C2B[18] | C2B[17] | C2B[16] | |
| 0X19 | A2CF2 | C2B[15] | C2B[14] | C2B[13] | C2B[12] | C2B[11] | C2B[10] | C2B[9] | C2B[8] | |
| 0X1A | A2CF3 | C2B[7] | C2B[6] | C2B[5] | C2B[4] | C2B[3] | C2B[2] | C2B[1] | C2B[0] | |
| 0X1B | B1CF1 | C3B[23] | C3B[22] | C3B[21] | C3B[20] | C3B[19] | C3B[18] | C3B[17] | C3B[16] | |
| 0X1C | B1CF2 | C3B[15] | C3B[14] | C3B[13] | C3B[12] | C3B[11] | C3B[10] | C3B[9] | C3B[8] | |
| 0X1D | B1CF3 | C3B[7] | C3B[6] | C3B[5] | C3B[4] | C3B[3] | C3B[2] | C3B[1] | C3B[0] | |
| 0X1E | B2CF1 | C4B[23] | C4B[22] | C4B[21] | C4B[20] | C4B[19] | C4B[18] | C4B[17] | C4B[16] | |
| 0X1F | B2CF2 | C4B[15] | C4B[14] | C4B[13] | C4B[12] | C4B[11] | C4B[10] | C4B[9] | C4B[8] | |
| 0X20 | B2CF3 | C4B[7] | C4B[6] | C4B[5] | C4B[4] | C4B[3] | C4B[2] | C4B[1] | C4B[0] | |
| 0X21 | A0CF1 | C5B[23] | C5B[22] | C5B[21] | C5B[20] | C5B[19] | C5B[18] | C5B[17] | C5B[16] | |
| 0X22 | A0CF2 | C5B[15] | C5B[14] | C5B[13] | C5B[12] | C5B[11] | C5B[10] | C5B[9] | C5B[8] | |
| 0X23 | A0CF3 | C5B[7] | C5B[6] | C5B[5] | C5B[4] | C5B[3] | C5B[2] | C5B[1] | C5B[0] | |
| 0X24 | CFRW | Reserved | | | | RA | R1 | WA | W1 | |
| 0X25 | FDCFG | Reserved | | | | | | | | |
| 0X26 | MBIST | Reserved | | | | | | | | |
| 0X27 | Status | Reserved | | | | | | | | |
| 0X28 | PWM_CTRL | Reserved | | | | | | | | |
| 0X29 | TM_CTRL | Reserved | | | | | | | | |
| 0X2A | QT_SW_LEV EL | Reserved | | | QT_SW_LEVEL [4] | QT_SW_LEVEL [3] | QT_SW_LEVEL [2] | QT_SW_LEVEL [1] | QT_SW_LEVEL [0] | |
| 0X2B | VFT | MV_FT[1] | MV_FT[0] | C1V_FT[1] | C1V_FT[0] | C2V_FT[1] | C2V_FT[0] | C3V_FT[1] | C3V_FT[0] | |
| 0X2C | OC | OCBIT[1] | OCBIT[0] | SCM[1] | SCM[0] | Reserved | | | | |

Detail Description for Register

Note that the highlighted columns are default values of these tables. If there is no highlighted value, the default setting of this bit is determined by the external pin.

● Address 0X00 : State control 1

AD87588 supports multiple serial data input formats including I²S, Left-alignment and Right-alignment.

These formats are selected by users via bit7~bit5 of address 0X00. The left/right channels can be exchanged to each other by programming to address 0X00/bit0, LREXC.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|----------|------------------------------------|-------|-----------------------------|
| B[7:5] | IF[2:0] | Input Format | 000 | I ² S 16-24 bits |
| | | | 001 | Left-alignment 16-24 bits |
| | | | 010 | Right-alignment 16 bits |
| | | | 011 | Right-alignment 18 bits |
| | | | 100 | Right-alignment 20 bits |
| | | | 101 | Right-alignment 24 bits |
| B[4] | | Reserved | | |
| B[3] | PWML_X | LA/LB exchange | 0 | No exchange |
| | | | 1 | Exchange |
| B[2] | PWMR_X | RA/RB exchange | 0 | No exchange |
| | | | 1 | Exchange |
| B[1] | LV_UVSEL | LV under voltage selection | 0 | 2.7v |
| | | | 1 | 3.0v |
| B[0] | LREXC | Left/Right (L/R) Channel exchanged | 0 | No exchanged |
| | | | 1 | L/R exchanged |

● Address 0X01 : State control 2

AD87588 has a built-in PLL which can be bypassed by pulling the PLL pin High. When PLL is bypassed, AD87588 only supports 1024x, 512x and 256x MCLK/Fs ratio for Fs is 32/44.1/48kHz, 64/88.2/96kHz, and 128/176.4/192kHz respectively. When PLL is enabled, multiple MCLK/Fs ratios are supported. Detail setting is shown in the following table.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|---------|--------------------|-------|------------------|
| B[7:6] | | Reserved | | |
| B[5:4] | FS[1:0] | Sampling Frequency | 00 | 32/44.1/48kHz |
| | | | 01 | 64/88.2/96kHz |
| | | | 1x | 128/176.4/192kHz |

Multiple MCLK/FS ratio setting table

| BIT | NAME | DESCRIPTION | VALUE | B[5:4]=00 | B[5:4]=01 | B[5:4]=1x |
|--------|----------|--|-------|----------------------|----------------------|----------------------|
| B[3:0] | PMF[3:0] | MCLK/FS setup when PLL is not bypassed | 0000 | 1024x | 512x | 256x |
| | | | 0001 | 64x | 64x | 64x |
| | | | 0010 | 128x | 128x | 128x |
| | | | 0011 | 192x | 192x | 192x |
| | | | 0100 | Reset Default (256x) | Reset Default (256x) | Reset Default (256x) |
| | | | 0101 | 384x | 384x | Reserved |
| | | | 0110 | 512x | 512x | |
| | | | 0111 | 576x | Reserved | |
| | | | 1000 | 768x | | |
| | | | 1001 | 1024x | | |

● Address 0X02 : State control 3

AD87588 has mute function including master mute and channel mute. When master mute is enabled, all 3 processing channels are muted. User can mute these 3 channels individually by channel mute. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|------|------------|------------------|-------|-----------------------|
| B[7] | EN_CLK_OUT | PLL Clock Output | 0 | Disabled |
| | | | 1 | Enabled |
| B[6] | | Reserved | | |
| B[5] | | Reserved | | |
| B[4] | | Reserved | | |
| B[3] | MUTE | Master Mute | 0 | All channel not muted |
| | | | 1 | All channel muted |
| B[2] | CM1 | Channel 1 Mute | 0 | Ch1 not muted |
| | | | 1 | Only Ch1 muted |
| B[1] | CM2 | Channel 2 Mute | 0 | Ch2 not muted |
| | | | 1 | Only Ch2 muted |
| B[0] | CM3 | Channel 3 Mute | 0 | Ch3 not muted |
| | | | 1 | Only Ch3 muted |

● Address 0X03 : Master volume control

AD87588 supports both master-volume (Address 0X03) and channel-volume control (Address 0x04, 0x05 and 0X06) modes. Both volume control settings range from +12dB ~ -103dB and 0.5dB per step. Note that the master volume control is added to the individual channel volume control as the total volume control. For example, if the master volume level is set at, Level A (in dB unit) and the channel volume level is set at Level B (in dB unit), the total volume control setting is equal to Level A plus with Level B.

$$-103\text{dB} \leq \text{Total volume (Level A + Level B)} \leq +24\text{dB}.$$

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|----------|---------|---------------|----------|--------------|
| BIT[7:0] | MV[7:0] | Master Volume | 00000000 | +12.0dB |
| | | | 00000001 | +11.5dB |
| | | | 00000010 | +11.0dB |
| | | | : | : |
| | | | 00010111 | +0.5dB |
| | | | 00011000 | 0.0dB |
| | | | 00011001 | -0.5dB |
| | | | : | : |
| | | | 11100110 | -103.0dB |
| | | | 11100111 | $-\infty$ dB |
| | | | : | : |
| | | | 11111111 | $-\infty$ dB |

● Address 0X04 : Channel 1 volume

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|----------|----------|-----------------|----------|--------------|
| BIT[7:0] | C1V[7:0] | Channel1 Volume | 00000000 | +12.0dB |
| | | | 00000001 | +11.5dB |
| | | | : | : |
| | | | 00010100 | +2dB |
| | | | : | : |
| | | | 00011000 | 0.0dB |
| | | | 00011001 | -0.5dB |
| | | | : | : |
| | | | 11100110 | -103.0dB |
| | | | 11100111 | $-\infty$ dB |
| | | | : | : |
| | | | 11111111 | $-\infty$ dB |

- Address 0X05 : Channel 2 volume

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|----------|----------|-----------------|----------|----------|
| BIT[7:0] | C2V[7:0] | Channel2 Volume | 00000000 | +12.0dB |
| | | | 00000001 | +11.5dB |
| | | | : | : |
| | | | 00010100 | +2dB |
| | | | : | : |
| | | | 00011000 | 0.0dB |
| | | | 00011001 | -0.5dB |
| | | | : | : |
| | | | 11100110 | -103.0dB |
| | | | 11100111 | -∞dB |
| | | | : | : |
| | | | 11111111 | -∞dB |

- Address 0X06 : Channel 3 volume

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|----------|----------|-----------------|----------|----------|
| BIT[7:0] | C3V[7:0] | Channel3 Volume | 00000000 | +12.0dB |
| | | | 00000001 | +11.5dB |
| | | | : | : |
| | | | 00010100 | +2dB |
| | | | : | : |
| | | | 00011000 | 0.0dB |
| | | | 00011001 | -0.5dB |
| | | | : | : |
| | | | 11100110 | -103.0dB |
| | | | 11100111 | -∞dB |
| | | | : | : |
| | | | 11111111 | -∞dB |

- Address 0X07/0X08 : Bass/Treble tone boost and cut

Last two sets of EQ can be programmed as bass/treble tone boost and cut. When, register with address-0X0A, bit-6, BTE is set to high, the EQ-8 and EQ-9 will perform as bass and treble respectively. The -3dB corner frequency of bass is 360Hz, and treble is 7kHz. The gain range for both filters is +12db ~ -12dB with 1dB per step.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|---------------------------|---|-------|----------|
| B[7:5] | | Reserved | | |
| B[4:0] | BTC[4:0] / TTC[4:0] | The gain setting of boost and cut | 00000 | +12dB |
| | | | ... | ... |
| | | | 00100 | +12dB |
| | | | 00101 | +11dB |
| | | | 00110 | +10dB |
| | | | ... | ... |
| | | | 01110 | +2dB |
| | | | 01111 | +1dB |
| | | | 10000 | 0dB |
| | | | 10001 | -1dB |
| | | | 10010 | -2dB |
| | | | ... | ... |
| | | | 11010 | -10dB |
| | | | 11011 | -11dB |
| | | | 11100 | -12dB |
| ... | ... | | | |
| 11111 | -12dB | | | |

- Address 0X09 : Bass management crossover frequency

The AD87588 provides bass management crossover frequency selection. A 1st order high-pass filter (channel 1 and 2) and a 2nd order low-pass filter (channel 3) at selected frequency are performed.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|---------|-------------------------------------|-------|----------|
| B[7:4] | | Reserved | | |
| B[3:0] | XO[3:0] | Bass management crossover frequency | 0000 | 80Hz |
| | | | 0001 | 100Hz |
| | | | 0010 | 120Hz |
| | | | 0011 | 140Hz |
| | | | 0100 | 160Hz |
| | | | 0101 | 180Hz |
| | | | 0110 | 200Hz |
| | | | 0111 | 300Hz |
| | | | 1000 | 400Hz |
| | | | 1001 | 500Hz |
| | | | 1010 | 600Hz |
| | | | 1011 | 700Hz |
| | | | 1100 | 800Hz |
| | | | 1101 | 900Hz |
| 1110 | 1000Hz | | | |
| 1111 | --- | | | |

- Address 0X0A : State control 4

The AD82586B provides several DSP setting as following.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|------|--------|---------------------------------|-------|--|
| B[7] | SRBP | Surround bypass | 0 | Surround enable |
| | | | 1 | Surround bypass |
| B[6] | BTE | Bass/Treble Selection bypass | 0 | Bass/Treble Disable |
| | | | 1 | Bass/Treble Enable |
| B[5] | TBDRCE | Two Band DRC Enable | 0 | Two Band DRC Disable |
| | | | 1 | Two Band DRC Enable |
| B[4] | NGE | Noise gate enable | 0 | Noise gate disable |
| | | | 1 | Noise gate enable |
| B[3] | EQL | EQ Link | 0 | Each channel uses individual EQ |
| | | | 1 | Channel-2 uses channel-1 EQ |
| B[2] | PSL | Post-scale link | 0 | Each channel uses individual post-scale |
| | | | 1 | Use channel-1 post-scale |
| B[1] | DSPB | EQ bypass | 0 | EQ enable |
| | | | 1 | EQ bypass |
| B[0] | HPB | DC blocking HPF bypass | 0 | HPF dc enable |
| | | | 1 | HPF dc bypass |

● Address 0X0B, 0X0C and 0X0D : Channel configuration registers

The AD87588 can configure each channel to enable or bypass DRC and channel volume and select the limiter set. AD87588 support two mode of DRC, RMS and PEAK detection which can be selected via bit 4.

Address 0X0B and 0X0C; where x=1 or 2

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|------|---------|--------------------------------------|-------|-------------------------------------|
| B[7] | | Reserved | | |
| B[6] | | Reserved | | |
| B[5] | | Reserved | | |
| B[4] | CxDRCM | Channel x DRC Mode | 0 | PEAK detection |
| | | | 1 | RMS detection |
| B[3] | CxPCBP | Channel x Power Clipping bypass | 0 | Channel x PC enable |
| | | | 1 | Channel x PC bypass |
| B[2] | CxDRCBP | Channel x DRC bypass | 0 | Channel x DRC enable |
| | | | 1 | Channel x DRC bypass |
| B[1] | CxHPFBP | Channel x bass management HPF bypass | 0 | Channel x HPF enable |
| | | | 1 | Channel x HPF bypass |
| B[0] | CxVBP | Channel x Volume bypass | 0 | Channel x's master volume operation |
| | | | 1 | Channel x's master volume bypass |

Address 0X0D

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|------|---------|--------------------------------------|-------|----------------------------|
| B[7] | | Reserved | | |
| B[6] | | Reserved | | |
| B[5] | | Reserved | | |
| B[4] | C3DRCM | Channel 3 DRC Mode | 0 | PEAK detection |
| | | | 1 | RMS detection |
| B[3] | C3PCBP | Channel 3 Power Clipping bypass | 0 | Channel 3 PC enable |
| | | | 1 | Channel 3 PC bypass |
| B[2] | C3DRCBP | Channel 3 DRC bypass | 0 | Channel 3 DRC enable |
| | | | 1 | Channel 3 DRC bypass |
| B[1] | C3HPFBP | Channel 3 bass management LPF bypass | 0 | Channel 3 LPF enable |
| | | | 1 | Channel 3 LPF bypass |
| B[0] | C3VBP | Channel 3 Volume bypass | 0 | Channel 3 volume operation |
| | | | 1 | Channel 3 volume bypass |

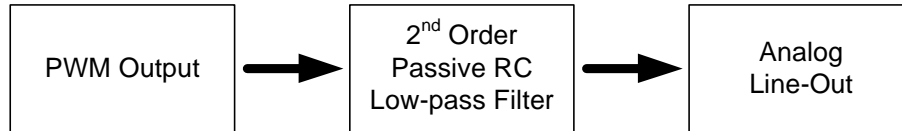
● Address 0X0E : DRC limiter attack/release rate

The AD87588 defines a set of limiter. The attack/release rates are defines as following table.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|---------|------------------|-------|--------------|
| B[7:5] | LA[3:0] | DRC attack rate | 0000 | 3 dB/ms |
| | | | 0001 | 2.667 dB/ms |
| | | | 0010 | 2.182 dB/ms |
| | | | 0011 | 1.846 dB/ms |
| | | | 0100 | 1.333 dB/ms |
| | | | 0101 | 0.889 dB/ms |
| | | | 0110 | 0.4528 dB/ms |
| | | | 0111 | 0.2264 dB/ms |
| | | | 1000 | 0.15 dB/ms |
| | | | 1001 | 0.1121 dB/ms |
| | | | 1010 | 0.0902 dB/ms |
| | | | 1011 | 0.0752 dB/ms |
| | | | 1100 | 0.0645 dB/ms |
| | | | 1101 | 0.0563 dB/ms |
| | | | 1110 | 0.0501 dB/ms |
| | | | 1111 | 0.0451 dB/ms |
| B[3:0] | LR[3:0] | DRC release rate | 0000 | 0.5106 dB/ms |
| | | | 0001 | 0.1371 dB/ms |
| | | | 0010 | 0.0743 dB/ms |
| | | | 0011 | 0.0499 dB/ms |
| | | | 0100 | 0.0360 dB/ms |
| | | | 0101 | 0.0299 dB/ms |
| | | | 0110 | 0.0264 dB/ms |
| | | | 0111 | 0.0208 dB/ms |
| | | | 1000 | 0.0198 dB/ms |
| | | | 1001 | 0.0172 dB/ms |
| | | | 1010 | 0.0147 dB/ms |
| | | | 1011 | 0.0137 dB/ms |
| | | | 1100 | 0.0134 dB/ms |
| | | | 1101 | 0.0117 dB/ms |
| | | | 1110 | 0.0112 dB/ms |
| | | | 1111 | 0.0104 dB/ms |

● Address 0X11 : State control 5

AD87588 can output PWM signal via the pins of SDATA1 and LINEIN by enabling LOM register. The Left / Right channel or subwoofer PWM output source can be selected via LOS register.



| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|------|--------------|-----------------------------|-------|---|
| B[7] | LOM | Line out mode | 0 | Disable |
| | | | 1 | Enable |
| B[6] | LOS | Line out source | 0 | Source from left and right channel LINEIN pin → Left channel SDATA1 pin → Right channel |
| | | | 1 | Source from subwoofer |
| B[5] | SW_RSTB | Software reset | 0 | Reset |
| | | | 1 | Normal operation |
| B[4] | | Reserved | | |
| B[3] | | Reserved | | |
| B[2] | DIS_MCLK_DET | Disable MCLK detect circuit | 0 | Enable MCLK detect circuit |
| | | | 1 | Disable MCLK detect circuit |
| B[1] | QT_EN | Power saving mode | 0 | Disable |
| | | | 1 | Enable |
| B[0] | PWM_SEL | PWM modulation | 0 | Qua-ternary |
| | | | 1 | Ternary |

- Address 0X12 : Class-D under voltage selection

AD87588 can disable HV under voltage detection via bit 7.

AD87588 support multi-level HV under voltage detection via bit3~ bit0, using this function, AD87588 will fade out signal to avoid pop sounds if high voltage supply disappear before low voltage supply.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|-----------|------------------------------------|--------|----------|
| B[7] | Dis_HVUV | Disable HV under voltage selection | 0 | Enable |
| | | | 1 | Disable |
| B[6:4] | | Reserved | | |
| B[3:0] | HV_UV SEL | UV detection level | 0000 | 8.2V |
| | | | 0001 | 9.7V |
| | | | 0011 | 13.2 V |
| | | | 0100 | 15.5 V |
| | | | 1100 | 19.5 V |
| | | | Others | 9.7V |

Note: Under voltage range has +/-10% max variation due to process window.

- Address 0X13 : Noise gate gain

AD87588 provide noise gate function if receiving 2048 signal sample points smaller than noise gate attack level. User can change noise gate gain via bit1~ bit0. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, x0). User can select fade out or not via bit 4.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|--------------|-------------------------|-------|----------|
| B[7:5] | | Reserved | | |
| B[4] | DIS_NG_FADE | Disable noise gate fade | 0 | Fade |
| | | | 1 | No fade |
| B[3:2] | | Reserved | | |
| B[1:0] | NG_GAIN[1:0] | Noise gate gain | 00 | x1/8 |
| | | | 01 | x1/4 |
| | | | 10 | x1/2 |
| | | | 11 | Mute |

- Address 0X14 ~0X24 : User-defined coefficients registers

An on-chip RAM in AD87588 stores user-defined EQ and mixing coefficients. The content of this coefficient RAM is indirectly accessed via coefficient registers, which consist of one base address register (address 0X14), five sets of registers (address 0X15 to 0X23) of three consecutive 8-bit entries for each 24-bit coefficient, and one control register (address 0X24) to control access of the coefficients in the RAM.

Address 0X14

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|----------|------------------------------|---------|----------|
| B[7] | | Reserved | | |
| B[6:0] | CFA[6:0] | Coefficient RAM base address | 0000000 | |

Address 0X15, A1cf1

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|------------|-------------------------------|-------|----------|
| B[7:0] | C1B[23:16] | Top 8-bits of coefficients A1 | | |

Address 0X16, A1cf2

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|-----------|----------------------------------|-------|----------|
| B[7:0] | C1B[15:8] | Middle 8-bits of coefficients A1 | | |

Address 0X17, A1cf3

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|----------|----------------------------------|-------|----------|
| B[7:0] | C1B[7:0] | Bottom 8-bits of coefficients A1 | | |

Address 0X18, A2cf1

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|------------|-------------------------------|-------|----------|
| B[7:0] | C2B[23:16] | Top 8-bits of coefficients A2 | | |

Address 0X19, A2cf2

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|-----------|----------------------------------|-------|----------|
| B[7:0] | C2B[15:8] | Middle 8-bits of coefficients A2 | | |

Address 0X1A, A2cf3

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|----------|----------------------------------|-------|----------|
| B[7:0] | C2B[7:0] | Bottom 8-bits of coefficients A2 | | |

Address 0X1B, B1cf1

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|------------|-------------------------------|-------|----------|
| B[7:0] | C3B[23:16] | Top 8-bits of coefficients B1 | | |

Address 0X1C, B1cf2

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|-----------|----------------------------------|-------|----------|
| B[7:0] | C3B[15:8] | Middle 8-bits of coefficients B1 | | |

Address 0X1D, B1cf3

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|----------|----------------------------------|-------|----------|
| B[7:0] | C3B[7:0] | Bottom 8-bits of coefficients B1 | | |

Address 0X1E, B2cf1

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|------------|-------------------------------|-------|----------|
| B[7:0] | C4B[23:16] | Top 8-bits of coefficients B2 | | |

Address 0X1F, B2cf2

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|-----------|----------------------------------|-------|----------|
| B[7:0] | C4B[15:8] | Middle 8-bits of coefficients B2 | | |

Address 0X20, B2cf3

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|----------|----------------------------------|-------|----------|
| B[7:0] | C4B[7:0] | Bottom 8-bits of coefficients B2 | | |

Address 0X21, A0cf1

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|------------|-------------------------------|-------|----------|
| B[7:0] | C5B[23:16] | Top 8-bits of coefficients A0 | | |

Address 0X22, A0cf2

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|-----------|----------------------------------|-------|----------|
| B[7:0] | C5B[15:8] | Middle 8-bits of coefficients A0 | | |

Address 0X23, A0cf3

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|----------|----------------------------------|-------|----------|
| B[7:0] | C5B[7:0] | Bottom 8-bits of coefficients A0 | | |

Address 0X24, CfRW

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|------|--|-------|----------------|
| B[7:4] | | Reserved | | |
| B[3] | RA | Enable of reading a set of coefficients from RAM | 0 | Read complete |
| | | | 1 | Read enable |
| B[2] | R1 | Enable of reading a single coefficient from RAM | 0 | Read complete |
| | | | 1 | Read enable |
| B[1] | WA | Enable of writing a set of coefficients to RAM | 0 | Write complete |
| | | | 1 | Write enable |
| B[0] | W1 | Enable of writing a single coefficient to RAM | 0 | Write complete |
| | | | 1 | Write enable |

- Address 0X2A : Power saving mode switching level

If the PWM exceeds the programmed switching power level (default 26*40ns), the modulation algorithm will change from quaternary into power saving mode. It results in higher power efficiency during larger power output operations. If the PWM drops below the programmed switching power level, the modulation algorithm will change back to quaternary modulation.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|-------------|-----------------|-------|----------|
| B[7] | | Reserved | | |
| B[6] | | Reserved | | |
| B[5] | | Reserved | | |
| B[4:0] | QT_SW_LEVEL | Switching level | 11111 | 62 |
| | | | 11110 | 60 |
| | | | : | : |
| | | | 10000 | 32 |
| | | | 01111 | 30 |
| | | | 01110 | 28 |
| | | | 01101 | 26 |
| | | | : | : |
| | | | 00001 | 4 |
| | | | 00000 | 4 |

- Address 0X2B : Volume fine tune

AD87588 supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|--------|----------------------------|-------|----------|
| B[7:6] | MV_FT | Master Volume Fine Tune | 00 | 0dB |
| | | | 01 | -0.125dB |
| | | | 10 | -0.25dB |
| | | | 11 | -0.375dB |
| B[5:4] | C1V_FT | Channel 1 Volume Fine Tune | 00 | 0dB |
| | | | 01 | -0.125dB |
| | | | 10 | -0.25dB |
| | | | 11 | -0.375dB |
| B[3:2] | C2V_FT | Channel 2 Volume Fine Tune | 00 | 0dB |
| | | | 01 | -0.125dB |
| | | | 10 | -0.25dB |
| | | | 11 | -0.375dB |
| B[1:0] | C3V_FT | Channel 3 Volume Fine Tune | 00 | 0dB |
| | | | 01 | -0.125dB |
| | | | 10 | -0.25dB |
| | | | 11 | -0.375dB |

- Address 0X2C : OC level

AD87588 supports OC level increasing adjustment for $VDDL/R \leq 18V$ application via bit5-bit4. The default OC step is at lowest OC level, 72k (I_{SC} level please refer to page 6, electrical characteristic table), user can program it to avoid abnormal OC trigger while the load smaller 8ohm is adopted. The OC level adjustment is prohibited for $VDDL/R > 18V$ application, the larger OC level may lead to short protection level weakness.

| BIT | NAME | DESCRIPTION | VALUE | FUNCTION |
|--------|--------|---------------------|-------|----------|
| B[7] | OCBIT2 | OC Delay bit2 | 1 | Turn On |
| | | | 0 | Turn off |
| B[6] | OCBIT1 | OC Delay bit1 | 1 | Turn On |
| | | | 0 | Turn off |
| B[5:4] | SCM | Short circuit level | 00 | 72k |
| | | | 01 | 66k |
| | | | 10 | 60k |
| | | | 11 | 54k |
| B[3:0] | | Reserved | | |

| $T_A=25^\circ C$ | B[5:4] | | OC level @12V |
|--------------------------------|--------|-----|---------------|
| Short circuit level adjustment | 00 | 72k | 2.7A |
| | 01 | 66k | 2.95A |
| | 10 | 60k | 3.25A |
| | 11 | 54k | 3.6A |

● RAM access

The procedure to read/write coefficient(s) from/to RAM is as followings:

Read a single coefficient from RAM:

1. Write 7-bis of address to I2C address-0X14
2. Write 1 to R1 bit in address-0X24
3. Read top 8-bits of coefficient in I2C address-0X15
4. Read middle 8-bits of coefficient in I2C address-0X16
5. Read bottom 8-bits of coefficient in I2C address-0X17

Read a set of coefficients from RAM:

1. Write 7-bits of address to I2C address-0X14
2. Write 1 to RA bit in address-0X24
3. Read top 8-bits of coefficient A1 in I2C address-0X15
4. Read middle 8-bits of coefficient A1 in I2C address-0X16
5. Read bottom 8-bits of coefficient A1 in I2C address-0X17
6. Read top 8-bits of coefficient A2 in I2C address-0X18
7. Read middle 8-bits of coefficient A2 in I2C address-0X19
8. Read bottom 8-bits of coefficient A2 in I2C address-0X1A
9. Read top 8-bits of coefficient B1 in I2C address-0X1B
10. Read middle 8-bits of coefficient B1 in I2C address-0X1C
11. Read bottom 8-bits of coefficient B1 in I2C address-0X1D
12. Read top 8-bits of coefficient B2 in I2C address-0X1E
13. Read middle 8-bits of coefficient B2 in I2C address-0X1F
14. Read bottom 8-bits of coefficient B2 in I2C address-0X20
15. Read top 8-bits of coefficient A0 in I2C address-0X21
16. Read middle 8-bits of coefficient A0 in I2C address-0X22
17. Read bottom 8-bits of coefficient A0 in I2C address-0X23

Write a single coefficient from RAM:

1. Write 7-bis of address to I2C address-0X14
2. Write top 8-bits of coefficient in I2C address-0X15
3. Write middle 8-bits of coefficient in I2C address-0X16
4. Write bottom 8-bits of coefficient in I2C address-0X17
5. Write 1 to W1 bit in address-0X24

Write a set of coefficients from RAM:

1. Write 7-bits of address to I2C address-0X14
2. Write top 8-bits of coefficient A1 in I2C address-0X15
3. Write middle 8-bits of coefficient A1 in I2C address-0X16
4. Write bottom 8-bits of coefficient A1 in I2C address-0X17
5. Write top 8-bits of coefficient A2 in I2C address-0X18
6. Write middle 8-bits of coefficient A2 in I2C address-0X19
7. Write bottom 8-bits of coefficient A2 in I2C address-0X1A
8. Write top 8-bits of coefficient B1 in I2C address-0X1B
9. Write middle 8-bits of coefficient B1 in I2C address-0X1C
10. Write bottom 8-bits of coefficient B1 in I2C address-0X1D
11. Write top 8-bits of coefficient B2 in I2C address-0X1E
12. Write middle 8-bits of coefficient B2 in I2C address-0X1F
13. Write bottom 8-bits of coefficient B2 in I2C address-0X20
14. Write top 8-bits of coefficient A0 in I2C address-0X21
15. Write middle 8-bits of coefficient A0 in I2C address-0X22
16. Write bottom 8-bits of coefficient A0 in I2C address-0X23
17. Write 1 to WA bit in address-0X24

Note that: the read and write operation on RAM coefficients works only if LRCIN (pin-15) switching on rising edge. And, before each writing operation, it is necessary to read the address-0X24 to confirm whether RAM is writable current in first. If the logic of W1 or WA is high, the coefficient writing is prohibited.

● User-defined equalizer

The AD87588 provides 18 parametric Equalizer (EQ). Users can program suitable coefficients via I²C control interface to program the required audio band frequency response for every EQ. The transfer function

$$H(z) = \frac{A_0 + A_1z^{-1} + A_2z^{-2}}{1 + B_1z^{-1} + B_2z^{-2}}$$

The data format of 2's complement binary code for EQ coefficient is 3.21. i.e., 3-bits for integer (MSB is the sign bit) and 21-bits for mantissa. Each coefficient range is from 0x800000 (-4) to 0x7FFFFFFF (+3.999999523). These coefficients are stored in User Defined RAM and are referenced in following manner:

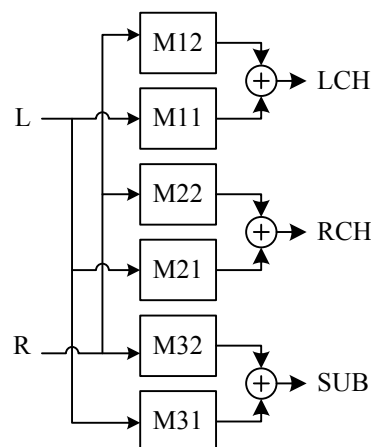
$$\begin{aligned} CHxEQyA0 &= A0 \\ CHxEQyA1 &= A1 \\ CHxEQyA2 &= A2 \\ CHxEQyB1 &= -B1 \\ CHxEQyB2 &= -B2 \end{aligned}$$

Where x and y represents the number of channel and the band number of EQ equalizer.

All user-defined filters are path-through, where all coefficients are defaulted to 0 after being powered up, except the A0 that is set to 0x200000 which represents 1.

● Mixer

The AD87588 provides mixers to generate the extra audio source from the input left and right channels. The coefficients of mixers are defined in range from 0x800000 (-1) to 0x7FFFFFFF (0.9999998808). The function block diagram is as following:



- **Pre-scale**

For each audio channel, AD87588 can scale input signal level prior to EQ processing which is realized by a 24-bit signed fractional multiplier. The pre-scale factor, ranging from -1 (0x800000) to 0.9999998808 (0x7FFFFFFF), for this multiplier, can be loaded into RAM. The default values of the pre-scaling factors are set to 0x7FFFFFFF. Programming of RAM is described in RAM access.

- **Post-scale**

The AD87588 provides an additional multiplication after equalizing and before interpolation stage, which is realized by a 24-bit signed fractional multiplier. The post-scaling factor, ranging from -1 (0x800000) to 0.9999998808 (0x7FFFFFFF), for this multiplier, can be loaded into RAM. The default values of the post-scaling factors are set to 0x7FFFFFFF. All channels can use the channel-1 post-scale factor by setting the post-scale link. Programming of RAM is described in RAM access.

- **Power Clipping**

The AD87588 provides power clipping function to avoid excessive signal that may destroy loud speaker. Two sets of power clipping are provided. One is used for both channel 1 and channel 2, while the other is used for channel 3. The power clipping level is defined by 24-bit representation and is stored in RAM address 0X6F and 0X70. The following table shows the power clipping level's numerical representation.

Sample calculation for power clipping

| Max amplitude | dB | Linear | Decimal | Hex (3.21 format) |
|----------------|----|-----------------|---------------|----------------------|
| VDDL/R | 0 | 1 | 2097152 | 200000 |
| VDDL/R * 0.707 | -3 | 0.707 | 1482686 | 169FBE |
| VDDL/R * 0.5 | -6 | 0.5 | 1048576 | 100000 |
| VDDL/R * L | x | $L=10^{(x/20)}$ | $D=2097152xL$ | $H=dec2hex(D)$ |

- **Attack threshold for Dynamic Range Control (DRC)**

The AD87588 provides dynamic range control (DRC) function. When the input RMS exceeds the programmable attack threshold value, the output power will be limited by this threshold power level via gradual gain reduction. Two sets of dynamic range control are provided. One is used of channel 1 and channel 2, while the other is used for channel3. Attack threshold is defined by 24-bit representation and is stored in RAM address 0X71 and 0X72.

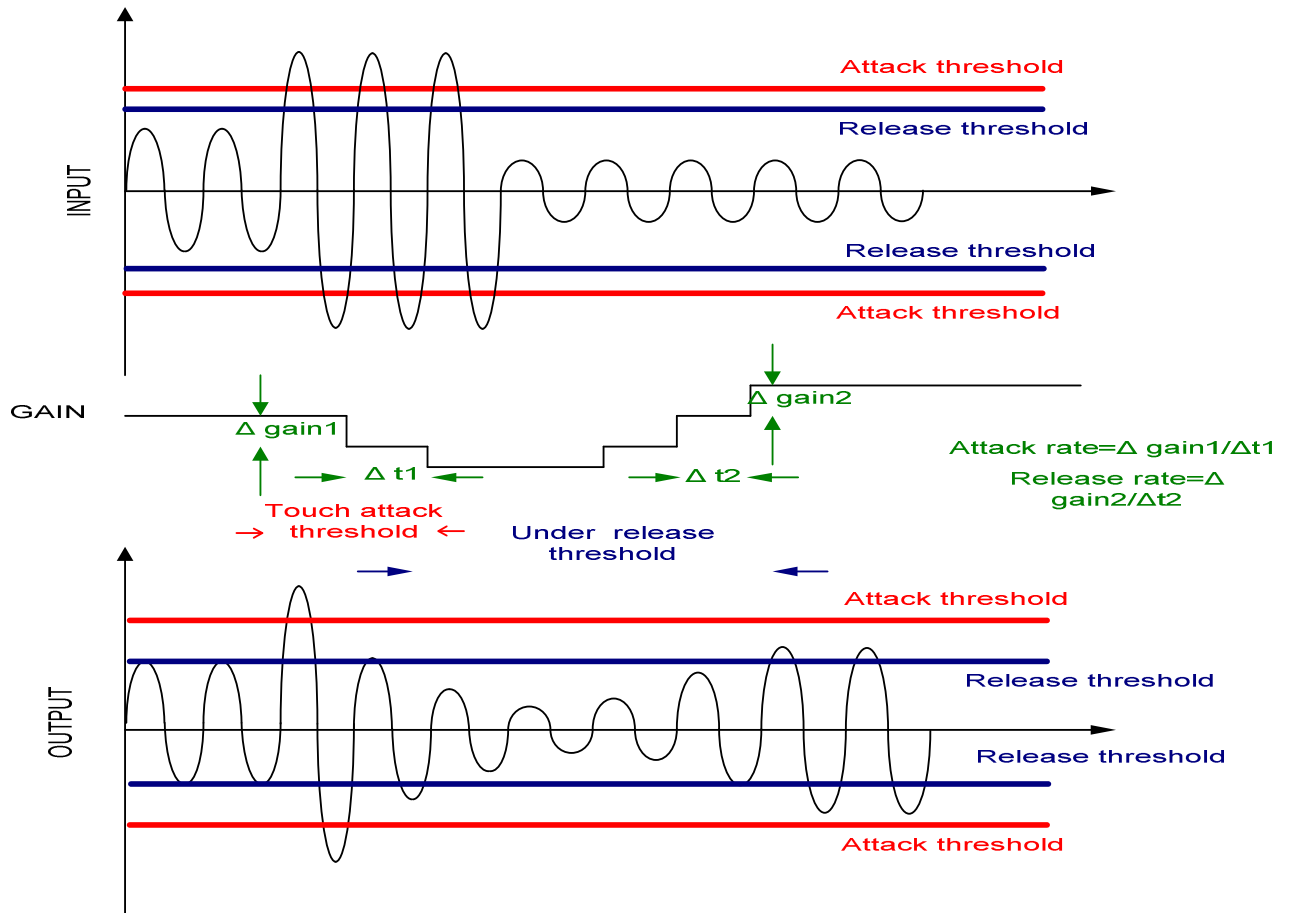
- **Release threshold for Dynamic Range Control (DRC)**

After AD87588 has reached the attack threshold, its output power will be limited to that level. The output power level will be gradually adjusted to the programmable release threshold level. Two sets of dynamic range control are provided. One is used of channel 1 and channel 2, while the other is used for channel3. Release threshold is defined by 24-bit representation and is stored in RAM address 0X73 and 0X74. The following table shows the attack and release threshold's numerical representation.

Sample calculation for attack and release threshold

| Power | dB | Linear | Decimal | Hex (3.21 format) |
|----------------------|----|-----------------|---------------|----------------------|
| $(VDDL/R^2)/R_L$ | 0 | 1 | 2097152 | 200000 |
| $(VDDL/R^2)/2R_L$ | -3 | 0.5 | 1048576 | 100000 |
| $(VDDL/R^2)/4R_L$ | -6 | 0.25 | 524288 | 80000 |
| $((VDDL/R^2)/R_L)*L$ | x | $L=10^{(x/10)}$ | $D=2097152xL$ | $H=dec2hex(D)$ |

To best illustrate the dynamic range control, please refer to the following figure.



- **Noise Gate Attack Level**

When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or zero if the noise gate function is enabled. Noise gate attack level is defined by 24-bit representation and is stored in RAM address 0X75.

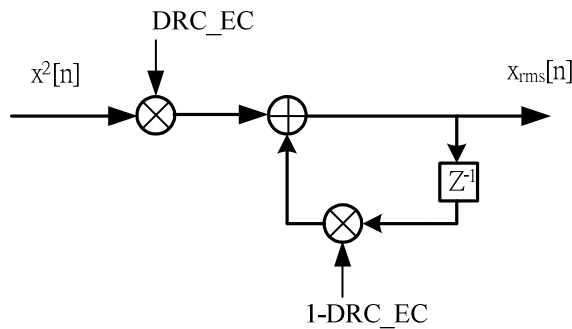
- **Noise Gate Release Level**

After entering the noise gating status, the noise gain will be removed whenever AD82586B receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 24-bit representation and is stored in RAM address 0X76. The following table shows the noise gate attack and release threshold level's numerical representation.

Sample calculation for noise gate attack and release level

| Input amplitude (dB) | Linear | Decimal | Hex (1.23 format) |
|----------------------|-----------------|----------------------|-----------------------|
| 0 | 1 | 8388607 | 7FFFFFF |
| -100 | 10^{-5} | 83 | 53 |
| -110 | $10^{-5.5}$ | 26 | 1A |
| x | $L=10^{(x/20)}$ | $D=8388607 \times L$ | $H=\text{dec2hex}(D)$ |

● DRC Energy Coefficient



The above figure illustrates the digital processing of calculating RMS signal power. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Two sets of energy coefficients are provided. One is used of channel 1 and channel 2, while the other is used for channel3. Energy coefficient is defined by 24-bit representation and is stored in RAM address 0X77 and 0X78. The following table shows the DRC energy coefficient numerical representation.

Sample calculation for DRC energy coefficient

| DRC energy coefficient | dB | Linear | Decimal | Hex (1.23 format) |
|------------------------|-------|-----------------|----------------------|-------------------|
| 1 | 0 | 1 | 8388607 | 7FFFFFF |
| 1/256 | -48.2 | 1/256 | 32768 | 8000 |
| 1/1024 | -60.2 | 1/1024 | 8192 | 2000 |
| L | x | $L=10^{(x/20)}$ | $D=8388607 \times L$ | $H=dec2hex(D)$ |

The user defined RAM

The contents of user defined RAM is represented in following table.

| Address | NAME | Coefficient | Default |
|---------|---------------|-------------|----------|
| 0x00 | Channel-1 EQ1 | CH1EQ1A1 | 0x000000 |
| 0x01 | | CH1EQ1A2 | 0x000000 |
| 0x02 | | CH1EQ1B1 | 0x000000 |
| 0x03 | | CH1EQ1B2 | 0x000000 |
| 0x04 | | CH1EQ1A0 | 0x200000 |
| 0x05 | Channel-1 EQ2 | CH1EQ2A1 | 0x000000 |
| 0x06 | | CH1EQ2A2 | 0x000000 |
| 0x07 | | CH1EQ2B1 | 0x000000 |
| 0x08 | | CH1EQ2B2 | 0x000000 |
| 0x09 | | CH1EQ2A0 | 0x200000 |
| 0x0A | Channel-1 EQ3 | CH1EQ3A1 | 0x000000 |
| 0x0B | | CH1EQ3A2 | 0x000000 |
| 0x0C | | CH1EQ3B1 | 0x000000 |
| 0x0D | | CH1EQ3B2 | 0x000000 |
| 0x0E | | CH1EQ3A0 | 0x200000 |
| 0x0F | Channel-1 EQ4 | CH1EQ4A1 | 0x000000 |
| 0x10 | | CH1EQ4A2 | 0x000000 |
| 0x11 | | CH1EQ4B1 | 0x000000 |
| 0x12 | | CH1EQ4B2 | 0x000000 |
| 0x13 | | CH1EQ4A0 | 0x200000 |
| 0x14 | Channel-1 EQ5 | CH1EQ5A1 | 0x000000 |
| 0x15 | | CH1EQ5A2 | 0x000000 |
| 0x16 | | CH1EQ5B1 | 0x000000 |
| 0x17 | | CH1EQ5B2 | 0x000000 |
| 0x18 | | CH1EQ5A0 | 0x200000 |
| 0x19 | Channel-1 EQ6 | CH1EQ6A1 | 0x000000 |
| 0x1A | | CH1EQ6A2 | 0x000000 |
| 0x1B | | CH1EQ6B1 | 0x000000 |
| 0x1C | | CH1EQ6B2 | 0x000000 |
| 0x1D | | CH1EQ6A0 | 0x200000 |
| 0x1E | Channel-1 EQ7 | CH1EQ7A1 | 0x000000 |
| 0x1F | | CH1EQ7A2 | 0x000000 |
| 0x20 | | CH1EQ7B1 | 0x000000 |

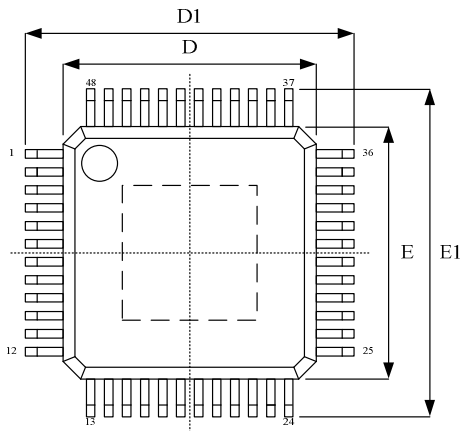
| | | | |
|------|---------------|---------------|----------|
| 0x21 | | CH1EQ7B2 | 0x000000 |
| 0x22 | | CH1EQ7A0 | 0x200000 |
| 0x23 | Channel-1 EQ8 | CH1EQ8A1 | 0x000000 |
| 0x24 | | CH1EQ8A2 | 0x000000 |
| 0x25 | | CH1EQ8B1 | 0x000000 |
| 0x26 | | CH1EQ8B2 | 0x000000 |
| 0x27 | | CH1EQ8A0 | 0x200000 |
| 0x28 | | Channel-1 EQ9 | CH1EQ9A1 |
| 0x29 | CH1EQ9A2 | | 0x000000 |
| 0x2A | CH1EQ9B1 | | 0x000000 |
| 0x2B | CH1EQ9B2 | | 0x000000 |
| 0x2C | CH1EQ9A0 | | 0x200000 |
| 0x2D | Channel-3 EQ1 | | CH3EQ1A1 |
| 0x2E | | CH3EQ1A2 | 0x000000 |
| 0x2F | | CH3EQ1B1 | 0x000000 |
| 0x30 | | CH3EQ1B2 | 0x000000 |
| 0x31 | | CH3EQ1A0 | 0x200000 |
| 0x32 | | Channel-2 EQ1 | CH2EQ1A1 |
| 0x33 | CH2EQ1A2 | | 0x000000 |
| 0x34 | CH2EQ1B1 | | 0x000000 |
| 0x35 | CH2EQ1B2 | | 0x000000 |
| 0x36 | CH2EQ1A0 | | 0x200000 |
| 0x37 | Channel-2 EQ2 | | CH2EQ2A1 |
| 0x38 | | CH2EQ2A2 | 0x000000 |
| 0x39 | | CH2EQ2B1 | 0x000000 |
| 0x3A | | CH2EQ2B2 | 0x000000 |
| 0x3B | | CH2EQ2A0 | 0x200000 |
| 0x3C | | Channel-2 EQ3 | CH2EQ3A1 |
| 0x3D | CH2EQ3A2 | | 0x000000 |
| 0x3E | CH2EQ3B1 | | 0x000000 |
| 0x3F | CH2EQ3B2 | | 0x000000 |
| 0x40 | CH2EQ3A0 | | 0x200000 |
| 0x41 | Channel-2 EQ4 | | CH2EQ4A1 |
| 0x42 | | CH2EQ4A2 | 0x000000 |
| 0x43 | | CH2EQ4B1 | 0x000000 |
| 0x44 | | CH2EQ4B2 | 0x000000 |
| 0x45 | | CH2EQ4A0 | 0x200000 |

| | | | |
|------|--------------------|----------|------------|
| 0x46 | Channel-2 EQ5 | CH2EQ5A1 | 0x000000 |
| 0x47 | | CH2EQ5A2 | 0x000000 |
| 0x48 | | CH2EQ5B1 | 0x000000 |
| 0x49 | | CH2EQ5B2 | 0x000000 |
| 0x4A | | CH2EQ5A0 | 0x200000 |
| 0x4B | Channel-2 EQ6 | CH2EQ6A1 | 0x000000 |
| 0x4C | | CH2EQ6A2 | 0x000000 |
| 0x4D | | CH2EQ6B1 | 0x000000 |
| 0x4E | | CH2EQ6B2 | 0x000000 |
| 0x4F | | CH2EQ6A0 | 0x200000 |
| 0x50 | Channel-2 EQ7 | CH2EQ7A1 | 0x000000 |
| 0x51 | | CH2EQ7A2 | 0x000000 |
| 0x52 | | CH2EQ7B1 | 0x000000 |
| 0x53 | | CH2EQ7B2 | 0x000000 |
| 0x54 | | CH2EQ7A0 | 0x200000 |
| 0x55 | Channel-2 EQ8 | CH2EQ8A1 | 0x000000 |
| 0x56 | | CH2EQ8A2 | 0x000000 |
| 0x57 | | CH2EQ8B1 | 0x000000 |
| 0x58 | | CH2EQ8B2 | 0x000000 |
| 0x59 | | CH2EQ8A0 | 0x200000 |
| 0x5A | Channel-2 EQ9 | CH2EQ9A1 | 0x000000 |
| 0x5B | | CH2EQ9A2 | 0x000000 |
| 0x5C | | CH2EQ9B1 | 0x000000 |
| 0x5D | | CH2EQ9B2 | 0x000000 |
| 0x5E | | CH2EQ9A0 | 0x200000 |
| 0x5F | Channel-3 EQ2 | CH3EQ2A1 | 0x000000 |
| 0x60 | | CH3EQ2A2 | 0x000000 |
| 0x61 | | CH3EQ2B1 | 0x000000 |
| 0x62 | | CH3EQ2B2 | 0x000000 |
| 0x63 | | CH3EQ2A0 | 0x200000 |
| 0x64 | Channel-1 Mixer1 | M11 | 0x7FFFFFFF |
| 0x65 | Channel-1 Mixer2 | M12 | 0x000000 |
| 0x66 | Channel-2 Mixer1 | M21 | 0x000000 |
| 0x67 | Channel-2 Mixer2 | M22 | 0x7FFFFFFF |
| 0x68 | Channel-3 Mixer1 | M31 | 0x400000 |
| 0x69 | Channel-3 Mixer2 | M32 | 0x400000 |
| 0x6A | Channel-1 Prescale | C1PRS | 0x7FFFFFFF |

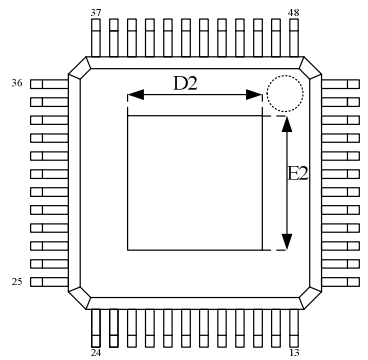
| | | | |
|------|-----------------------------|----------|-----------|
| 0x6B | Channel-2 Prescale | C2PRS | 0x7FFFFFF |
| 0x6C | Channel-1 Postscale | C1POS | 0x7FFFFFF |
| 0x6D | Channel-2 Postscale | C2POS | 0x7FFFFFF |
| 0x6E | Channel-3 Postscale | C3POS | 0x7FFFFFF |
| 0x6F | CH1.2 Power Clipping | PC1 | 0x200000 |
| 0x70 | CH3 Power Clipping | PC2 | 0x200000 |
| 0x71 | CH1.2 DRC Attack threshold | DRC1_ATH | 0x200000 |
| 0x72 | CH1.2 DRC Release threshold | DRC1_RTH | 0x80000 |
| 0x73 | CH3 DRC Attack threshold | DRC2_ATH | 0x200000 |
| 0x74 | CH3 DRC Release threshold | DRC2_RTH | 0x80000 |
| 0x75 | Noise Gate Attack Level | NGAL | 0x00001A |
| 0x76 | Noise Gate Release Level | NGRL | 0x000053 |
| 0x77 | DRC1 Energy Coefficient | DRC1_EC | 0x80000 |
| 0x78 | DRC2 Energy Coefficient | DRC2_EC | 0x20000 |

Package Dimensions

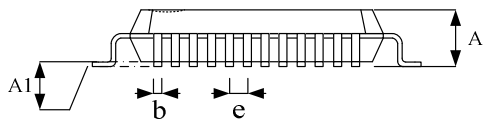
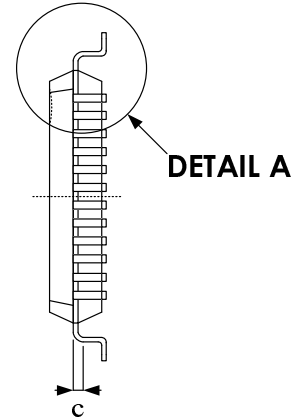
- E-LQFP 48L (7x7mm)



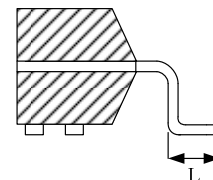
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL A

| Symbol | Dimension in mm | |
|--------|-----------------|------|
| | Min | Max |
| A | -- | 1.60 |
| A1 | 0.05 | 0.15 |
| b | 0.17 | 0.27 |
| c | 0.09 | 0.20 |
| D | 6.90 | 7.10 |
| D1 | 8.90 | 9.10 |
| E | 6.90 | 7.10 |
| E1 | 8.90 | 9.10 |
| e | 0.50 BSC | |
| L | 0.45 | 0.75 |

Exposed pad

| | Dimension in mm | |
|----|-----------------|------|
| | Min | Max |
| D2 | 4.31 | 5.21 |
| E2 | 4.31 | 5.21 |

Revision History

| Revision | Date | Description |
|-----------------|-------------|---|
| 0.1 | 2014.10.02 | Initial version. |
| 0.2 | 2015.02.03 | 1) Added 12V OC data into this datasheet. 2) Operating temperature supports from 0°C~70°C changed to -10°C~70°C. |
| 1.0 | 2015.02.10 | Remove preliminary word and modify version to 1.0 |
| 1.1 | 2015.10.19 | Modified line-driver start-up time. |
| 1.2 | 2016.02.24 | 1) Updated line-driver UVP operating information. 2) Updated line-driver power on sequence. 3) Added Class-D HVUV range information into. |
| 1.3 | 2016.06.29 | Add packing code in ordering information table. |
| 1.4 | 2016.11.22 | Add tape reel packing |
| 1.5 | 2017.10.06 | Add description of LOS and LOS in address 0X11 |

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