| Parameter | Conditions | AD892EJ/AD892TJ Min | Typ | Max | Units |
|---|---|---|---|---|---|
| COMPARATORS | | | | | |
| Input Offset Voltage | | | 0.25 | **2.0** | mV |
| Input Offset Current | | | 100 | | nA |
| Input Bias Current | | | 0.68 | | μA |
| Open Loop Gain | f = 10 MHz | | 66 | | dB |
| Input Resistance | Differential | | 500 | | kΩ |
| Input Capacitance | Differential | | 1 | 5 | pF |
| Input Common Mode Range | Referred to Digital Ground | 2.8 | | + 5 | V |
| OUTPUT/FILTER ONE-SHOT | AD892T | | | | |
| Resistor Scaling[5] | One-Shot Pulse ≈ $10+3.0\times R_{SET}$ | | | | ns |
| Pulse Duration | $R_{SET} = R_{min}$ to $R_{max}$ | 9 | | 180 | ns |
| | $R_{SET}$ = 10 kΩ | **31** | 38 | **45** | ns |
| Resistor Range | $R_{SET} = R_{min}$ to $R_{max}$ | 0.75 | | 56 | kΩ |
| OUTPUT/FILTER ONE-SHOT | AD892E | | | | |
| Resistor Scaling[5] | One-Shot Pulse ≈ $3.5+3.5\times R_{SET}$ | | | | ns |
| Pulse Duration | $R_{SET} = R_{min}$ to $R_{max}$ | 7 | | 52 | ns |
| | $R_{SET}$ = 3 kΩ | **9** | 14 | **19** | ns |
| Resistor Range | $R_{SET} = R_{min}$ to $R_{max}$ | 1 | | 14 | kΩ |
| EXTERNAL LOGIC | | | | | |
| Data Output Level (AD892T) | 400 Ω Pull-Up to +5 V | | | | |
| Output Logic "1" | User Defined (Open Collector Output) | | | | |
| Output Logic "0" | | | 0.25 | 0.5 | V |
| Data Output Level (AD892E) | 1 kΩ Pull-Down to Ground | | | | |
| Output Logic "1" | | 4.02 | 4.15 | 4.19 | V |
| Output Logic "0" | | 3.05 | 3.15 | 3.37 | V |
| DATA THROUGHPUT | | | | | |
| Propagation Delay[6] | Differentiator Input to Data Output | | 12.3 | | ns |
| Additional Pulse Pairing[7] | | | | 1000 | ps |
| Max Transfer Rate (AD892T) | | 25 | | | Mb/s |
| Max Transfer Rate (AD892E) | | 30 | | | Mb/s |
| POWER SUPPLY REQUIREMENTS | | | | | |
| Supply Voltage $V_{12}$ | | 10.8 | 12 | 13.2 | V |
| Supply Voltage $V_5$ | | 4.5 | 5 | 5.5 | V |
| Quiescent Current $I_{12}$ | $T_{min}$ to $T_{max}$ | 40 | 49 | 61 | mA |
| Quiescent Current $I_5$ | $T_{min}$ to $T_{max}$ | 10 | 16 | 24 | mA |
| ABSOLUTE MAXIMUM RATINGS[8] | | | | | |
| Supply Voltage $V_{12}$ | | | | 14.5 | V |
| Supply Voltage $V_5$ | | | | 7.5 | V |
| RF Input Stage Differential Input Voltage | | −0.8 | | 5.6 | V |
| Comparator Differential Input Voltage | | −0.8 | | 5.6 | V |
| Storage Temperature Range | | −65 | | 130 | °C |
| Operating Temperature Range[9] | | 0 | | 70 | °C |
| Lead Temperature Range | Soldering 60 Sec | | | 300 | °C |

NOTES

[1]Gain calibrated in gain set mode with 0 volts applied to the gain set pin.

[2]Clamp operation is specified with a source impedance of 200 Ω in series with 0.1 μF.

[3]Over the full 50 MHz bandwidth of the AD892E/AD892T, the worst-case rms signal-to-noise ratio is 40 dB or better with a 40 dB AGC range.

[4]Measured using a 4 kΩ resistor connected between qualifier threshold pin and ground; also between the differentiator pin and ground.

[5]$R_{SET}$ specified in kΩ.

[6]Propagation delay is measured from the zero crossing comparator input to the "Data Output" with 200 mV overdrive.

[7]Measurements were performed using a ±100 mV square wave having a rise time under 5 ns; this was applied to the input of the zero crossing comparator. The resultant pulse pairing is the difference in delay times for two consecutive output pulses.

[8]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.

[9]44-pin PLCC package: $\theta_{JA}$ = +65°C/watt.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

# Typical Characteristics (@ +25°C with +5 V, +12 V Supplies)

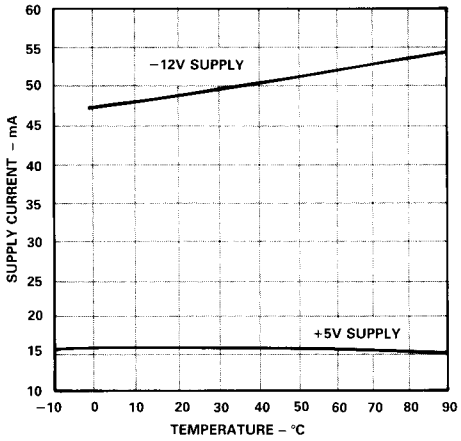



*Figure 1. Supply Current vs. Temperature*

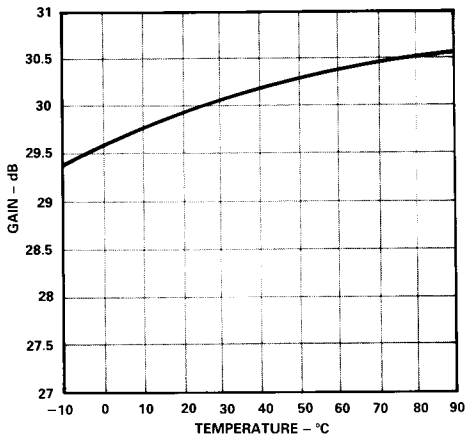



*Figure 2. VGA Gain vs. Temperature*

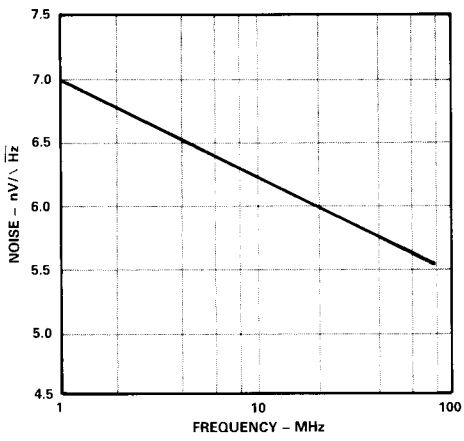



*Figure 3. VGA Input Voltage Noise vs. Frequency*

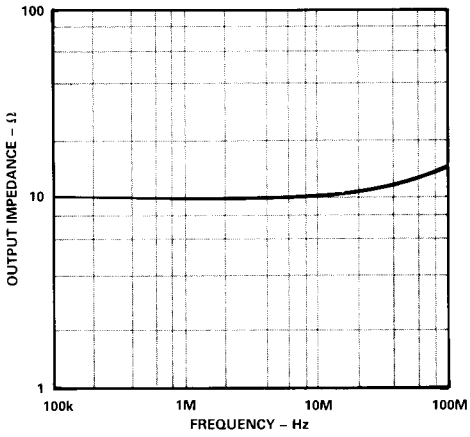



*Figure 4. VGA Output Impedance vs. Frequency*

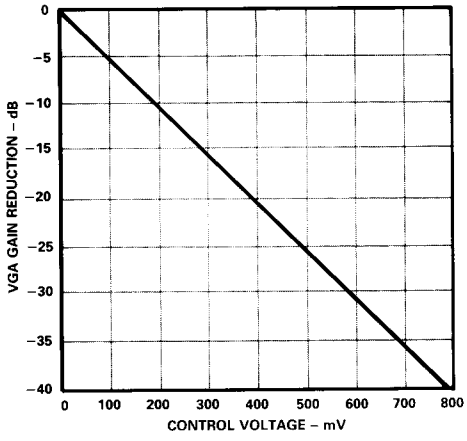



*Figure 5. VGA Gain Reduction vs. Control Voltage*

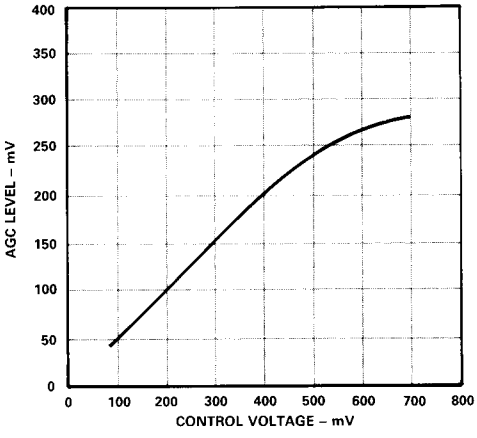



*Figure 6. AGC Level vs. Control Voltage*

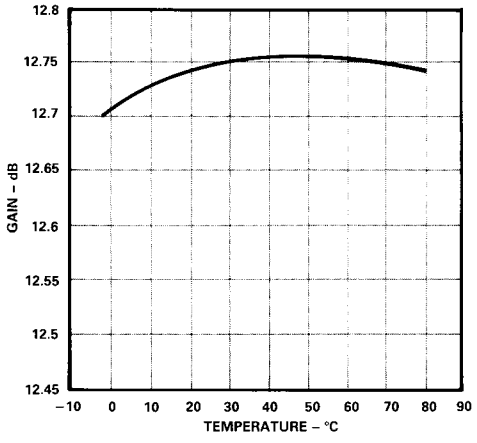



*Figure 7. ×4 Buffer Gain vs. Temperature*

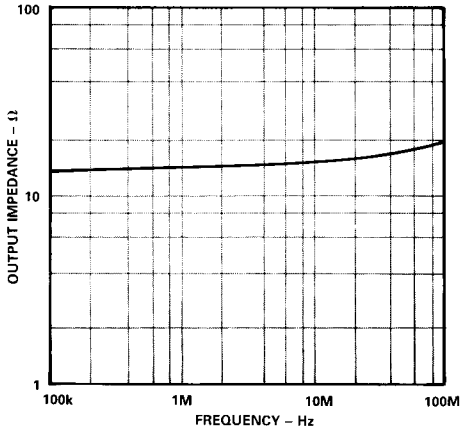



*Figure 8. ×4 Buffer Output Impedance vs. Frequency*

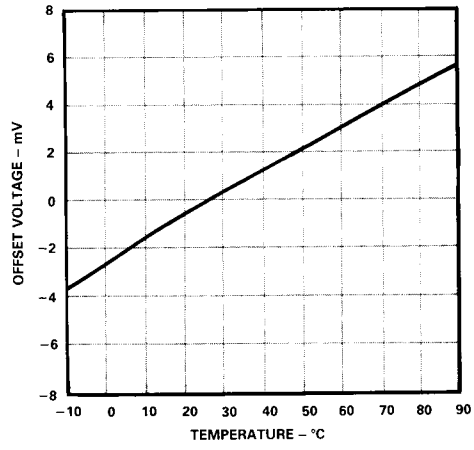



*Figure 9. Rectifier Offset vs. Temperature*

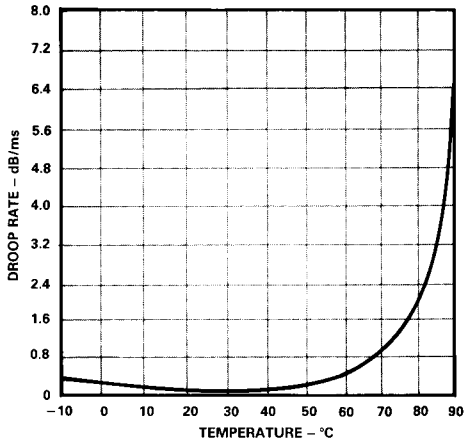



*Figure 10. Hold Mode Droop Rate vs. Temperature ($C_{HOLD}$ = 1000pF)*

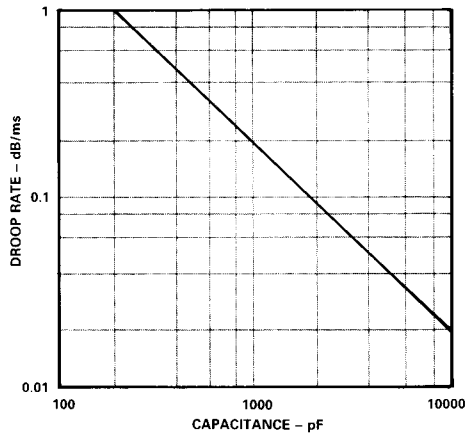



*Figure 11. Hold Mode Droop Rate vs. Capacitance*

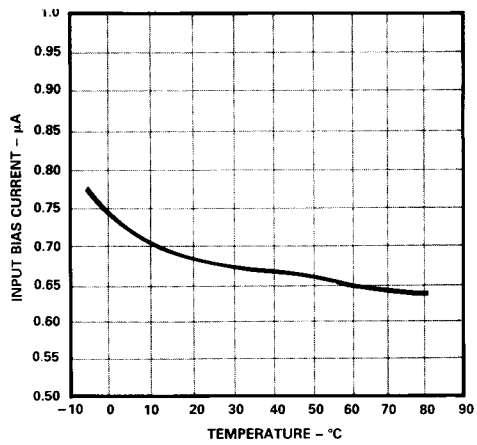



*Figure 12. Comparator Input Bias Current vs. Temperature*

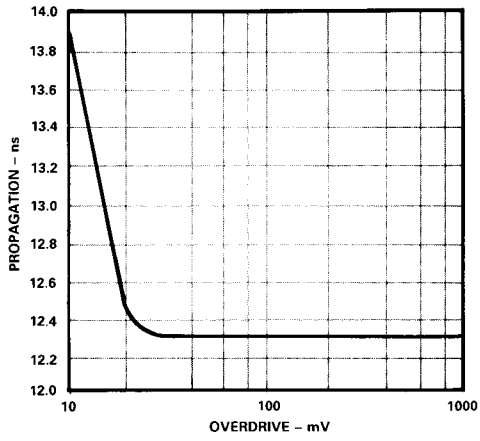



*Figure 13. Propagation Delay (Comparator to Data Out) vs. Input Overdrive*

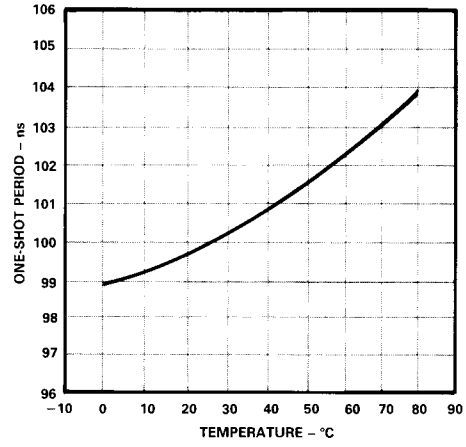



*Figure 14. One-Shot Period vs. Temperature ($R_{SET}$ = 30 kΩ)*

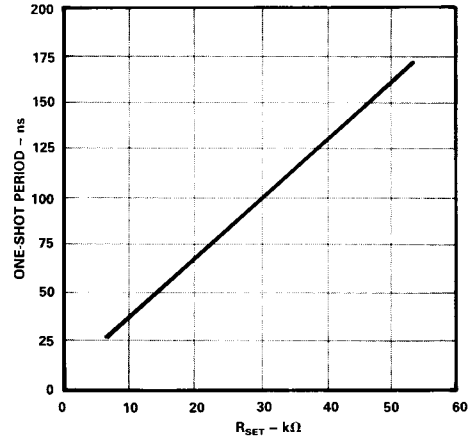



*Figure 15. One-Shot Period vs. $R_{SET}$*

## CHANNEL PROCESSING STAGES

### The VGA Stage

The 30 dB variable gain stage input is biased at a potential of 5.0 V above analog ground. No additional dc bias is required, but ac coupling is necessary. The bias voltage is maintained during normal operation and during operation of the read-after-write recovery clamp.

The VGA differential output stage is an emitter follower with nominal dc biasing of 6.7 V. An internal 1.4 mA current source provides bias current to the output emitter followers. Output drive can be increased by an additional 1.4 mA by paralleling external resistors to the analog ground. However, caution should be exercised in order to avoid causing excess power dissipation for the package. The recommended output level for the VGA is 300 mV p-p differential into 200 Ω loads.

When the AD892E/AD892T is used in the "VGA Set Gain" mode, Control Bit A = 0 (Pin 5) and Bit B = 1 (Pin 4), the VGA gain is programmable through the "VGA Level Set" pin (Pin 11). The VGA gain and exponentiator scale factor are trimmed with respect to the dc control potential applied to the "VGA Level Set" pin. A 0 V potential applied to the "VGA Level Set" pin will produce a nominal VGA gain of 30 dB. Each 20 mV increment of voltage applied will produce a 1 dB reduction in VGA gain. Therefore, a simple equation can be used to calculate the nominal gain of the VGA in this mode:

$$VGA\ Gain\ (dB) = 30 - (50 \times V_{SET\ LEVEL})$$

The AD892E/AD892T offers a read-after-write overdrive protection clamp. The clamp mode, Control Bit A = 0 (Pin 5), Bit B = 0 (Pin 4), lowers the input impedance of the VGA from nominally 24 kΩ to 28 Ω. In order for the clamp to operate correctly with an emitter driven input, a 50 Ω minimum resistor should be placed in series with the input coupling capacitors. The input resistor can be used in conjunction with a shunt capacitor to limit the input bandwidth. For example, a 100 Ω series resistor with a 10 pF shunt capacitor will limit the input bandwidth to 75 MHz. When the VGA input is being driven by an open collector driver with resistive termination, no additional series resistors are required.

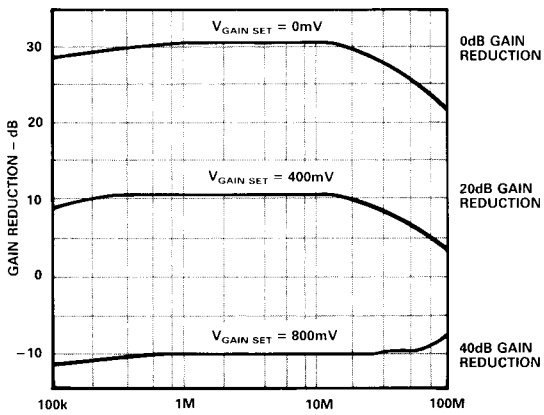



*Figure 16. VGA Gain Reduction vs. Frequency*

### The ×4 Buffers

The inputs of these stages have on chip dc biasing of 4.2 V (the internal reference voltage, $V_{REF}$); therefore, no input bias current path needs to be provided. The inputs to the buffers should then be ac coupled. When not used, the inputs should be shorted together in order to avoid noise pickup and instability.

The nominal dc output level is 5.75 V with an internal 2.9 mA pull down current source. Output drive can be increased in a similar manner to that described for the VGA stage. Therefore, output current can be increased by up to an additional 2.9 mA by paralleling external resistors to analog ground. As before, precautions to limit excessive overall power dissipation apply when steps are taken to increase the output drive capability.

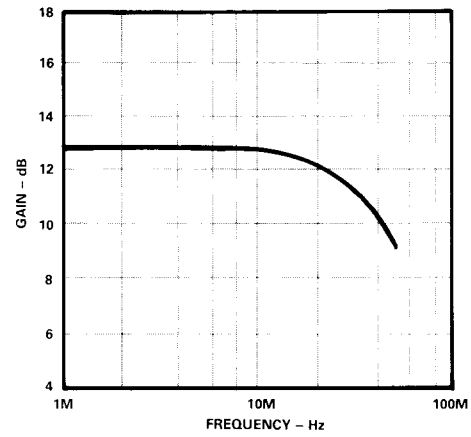



*Figure 17. ×4 Buffer Gain vs. Frequency (200 Ω in Series with 1 μF Load)*

### The Full Wave Rectifiers

The inputs to the three full wave rectifiers are biased at an internal voltage of 5 V; therefore, only ac coupling is recommended. The full wave rectifier outputs consist of three nearly identical stages. All three employ emitter follower outputs. The nominal output voltage with zero input voltage is close to the reference voltage of 4.2 V (Pin 39).

The rectified output to the sample-and-hold amplifier (Pin 34) has an internal 2.15 kΩ resistor in series with one diode tied to ground. This allows for accurate AGC operation in sinusoidal fields; however, if your application requires a peak-hold mode AGC operation, the AD892E/AD892T can be ordered with the resistor removed.

The other two full wave rectifier outputs – one rectified signal to drive the differentiator network and another to derive the threshold for the peak detector – are connected directly to their respective emitter follower output stages. Neither output has a built in pull-down resistor. Therefore, to obtain a zero nominal offset, their quiescent currents must be matched. A 1 mA quiescent current is recommended to ensure accurate operation.

**The AGC Sample and Hold**

When the AD892E/AD892T is used in the "AGC Acquire" mode, Control Bit A = 1 (Pin 5) and Bit B = 1 (Pin 4), the AGC level is programmable through the "AGC Level Set" pin (Pin 8). The AGC Level is defined as the AVERAGE of the full wave rectifier output voltage (Pin 34). A 400 mV dc potential applied to the "AGC Level Set" pin will produce a nominal average AGC level of 200 mV. Each 10 mV increment/decrement of the applied "AGC level set" voltage will produce a 5 mV increase/decrease in the average AGC level. Therefore, a simple equation can be used to calculate the nominal AGC level in this mode:

$$AGC\ Level = 0.5 \times V_{AGC\ LEVEL\ SET}$$

Without a peak hold capacitor at the full wave rectifier output for the sample-and-hold amplifier (Pin 34), accurate AGC operation only occurs with sinusoidal input signals. If your application requires the AGC operation to use a peak hold scheme, the AD892E/AD892T can be ordered with the pull down resistor removed on the rectified signal output to the sample-and-hold amplifier (Pin 34). The removal of this resistor now allows the user to program the degree of peak hold, by applying a RC combination to the rectified signal output for the sample-and-hold amplifier. The addition of the capacitor alters the symmetry of the attack and decay rates of the rectifier, which is otherwise symmetric in operation. In order to ensure that the overall AGC response is the same for both high to low and low to high input level steps, it is necessary to make the rectifier attack and decay times at least a factor of two less than the AGC response time.

The AGC acquire time is approximately 1 μs per 1000 pF of hold capacitor applied at Pin 22. A low leakage variety of hold capacitor, such as a silver mica, is necessary to ensure a low droop rate. The "VGA Level Set" pin should be tied to analog ground if not used.

The AGC control potential is present at the "sample-and-hold capacitor" pin. If control over open loop gain is desired, based on AGC control potentials measured during trial AGC operations, a FET input op amp should be used to buffer this node in order to avoid disturbing the hold operation.

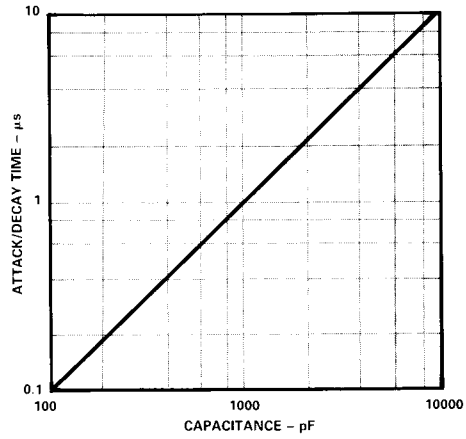



*Figure 18. AGC Attack/Decay vs. Capacitance*

## DATA QUALIFIER STAGES

The data qualifier section of the AD892E/AD892T consists of two comparators, one D-type flip-flop, an internal bandgap reference and a pair of externally adjustable one-shots. One comparator is used to provide data amplitude qualification, while the other acts as a zero-crossing detector when used with an external passive differentiator circuit.

Figure 19 illustrates the operation of the data qualifier using the recommended passive delay line differentiator described in the Application section. Sequence "A" represents the pattern written on the disk where a Logic "1" is a change in magnetic state. Each change in magnetic state results in an output pulse. The analog input to the data qualifier consists of a sequence of rectified pulses "B." The data pattern shown is worst case for a RLL 1, 7 code input. "C" represents the output waveform from the external differentiator, such that the points at which zero-crossings occur correspond to the peaks of the analog input "B." Sequence "D" shows the output from the zero-crossing comparator. Changes in state of this output are used to clock the internal D-type flip-flop. The flip-flop is enabled using the output "E" from the amplitude-threshold comparator. The amplitude-comparator output changes state only when the analog input exceeds the programmed threshold level. When the threshold level is exceeded and a zero-crossing event occurs, the flip-flop changes state, producing an output pulse "F." The duration of this pulse, seen at the "Data Output" pin (Pin 43), is set using an external resistor (applied between Pin 42 and $V_S$), as is the internal time-out (a resistor applied between Pin 41 and $V_S$) which is used to prevent noise induced retriggering. The final output data sequence is shown in "G". As can be seen, despite inflections in the analog input, the data is correctly detected and the output is a time-shifted version of the write data.

Since the RLL 1, 7 code input is the most demanding of the popular encoding schemes to qualify, the AD892E/AD892T easily handles such other codes as MFM and RLL 2, 7.

## GENERAL LAYOUT REQUIREMENTS

The channel processing section of the AD892E/AD892T has almost 60 dB of total gain available at 50 MHz. Good RF layout must be used in the circuit board to avoid oscillations in the 150 MHz to 350 MHz region. A single pole RC filter applied at the input of each stage, with a cut-off in the region of 75 MHz to 125 MHz, will help avoid oscillation problems. As a general rule, keep the connections to interstage components as short as possible; it is also recommended that any low pass filtering that may be required by the system be performed between the VGA stage and the first ×4 buffer amplifier. A ground plane should be used to surround any interstage components wherever possible. If these simple rules are followed, stable operation should be assured.

A parallel combination of 0.1 μF and 0.01 μF ceramic capacitors should be used as close to the supply pins as possible, for both the +12 V analog (Pin 18), +12 V digital (Pin 40) and +5 V (Pin 1) supplies. It is also recommended that the $V_{REFERENCE}$ (Pin 39) is decoupled with a 0.1 μF ceramic capacitor.

Extensive use of a ground plane is recommended. An analog ground (Pin 28) is supplied for the AGC section, while two digital grounds are supplied: one for the data qualifier section (Pin 6), and one for the emitter of the open collector output transistor (Pin 44 for the AD892T only). The digital ground should be connected to the analog ground as near to the power supply common as possible to minimize noise injection to the analog ground.

The filter and output pulse setting resistors should be tied, as directly possible, to the +5 V supply. To prevent the data output pulse from coupling into the output pulse setting circuit, a 1000 pF capacitor can be used in parallel with the output pulse setting resistor.

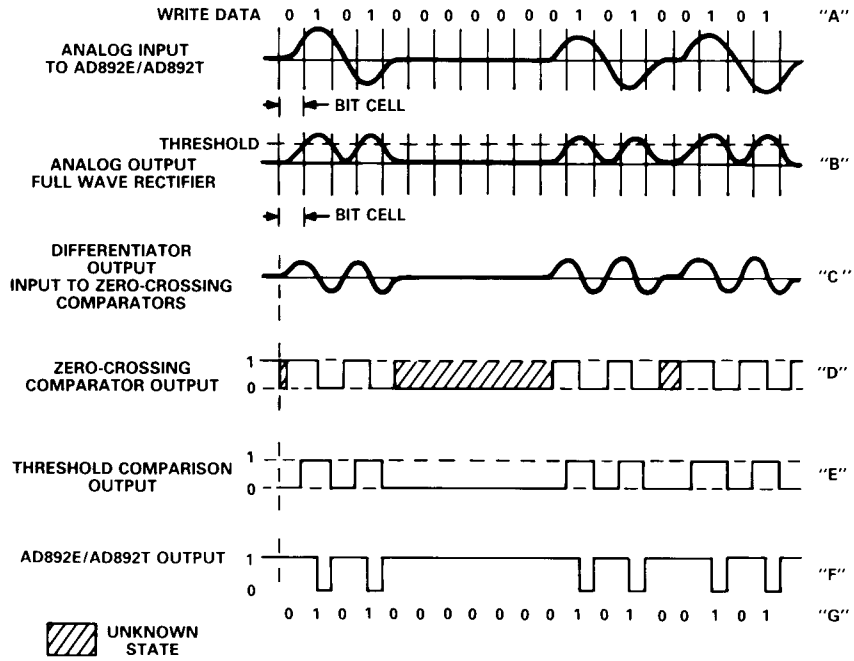



*Figure 19. AD892E/AD892T Operation for Worst Case 1–7 RLL*

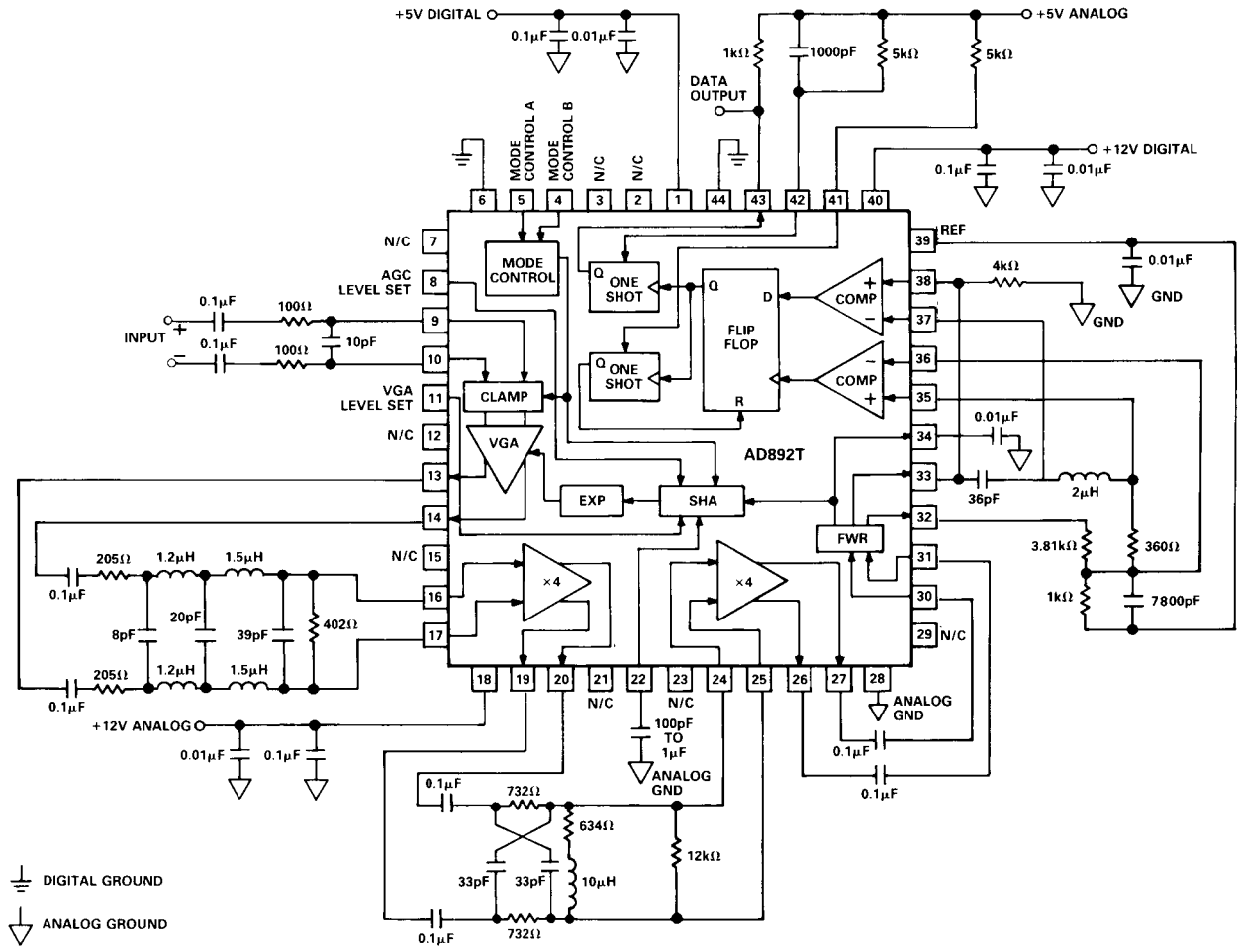



*Figure 20. Typical AD892T Connection for a 15 MHz Channel*

## A 15 MHz APPLICATION

Figure 20 shows a typical application using the AD892T in a 15 MHz channel. This circuit includes a 5-pole 15 MHz Gaussian-to-6 dB transitional filter plus a second-order RLC time domain equalizer. A single ended passive delay-line differentiator is also included.

### Using Equalizers with the AD892E/AD892T

The AD892E/AD892T is ideal for applications where equalization is employed. The ×4 buffer output drivers are designed to operate into 200 Ω loads, making tapped delay-line designs easy. Sum and differencing of different tap weights can be achieved by simple resistive dividers.

### The RLC Equalizer

As an alternative, a simple RLC network can be implemented to provide a low cost, fully differential alternative to the three tap, tapped delay-line equalizer which often is used for pulse slimming. The equalizer shown in Figure 21 approximates a function in the form of $F(\omega\tau) = 1 - k \cos(\omega\tau)$. The approximation

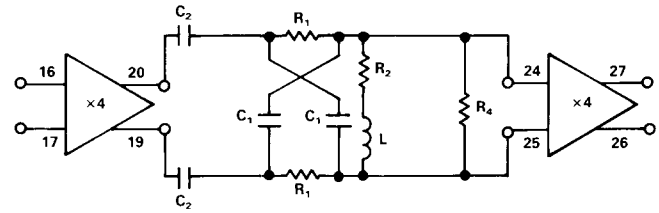



*Figure 21. RLC Equalizer*

is achieved by first creating a magnitude function and then adding phase compensation to provide a flat group delay characteristic over the frequency range of interest. Our 15 MHz application example employs the cosine equalizer; where K = 0.6 and $\tau$ = 24 ns. The magnitude and group delay characteristics of the equalizer employed in the 15 MHz application are shown in Figures 22 and 23, respectively.

### Magnitude Approximation

The magnitude approximation is achieved by an RC lattice (Figure 24).

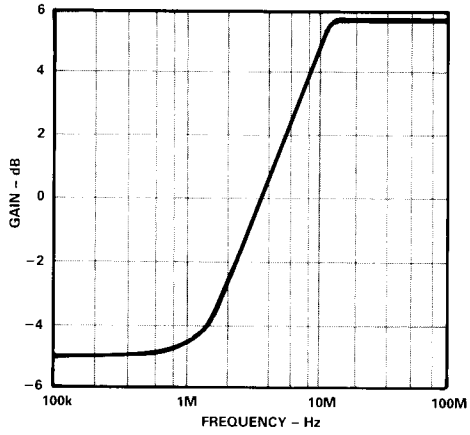



*Figure 22. RLC Equalizer Magnitude Response*

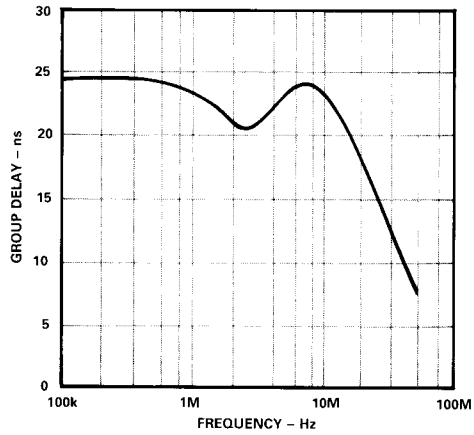



*Figure 23. RLC Equalizer Group Delay Response*

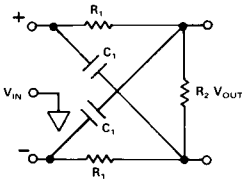



*Figure 24. RC Lattice*

The transfer function is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2(1-CR_1S)}{CR_1R_2S+R_2+2R_1}$$

at dc

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2}{2R_1+R_2}$$

and at high frequency

$$\frac{V_{OUT}}{V_{IN}} = -1$$

In the above case we can see that K in the $1-K\cos(\omega\tau)$ expression is given by:

$$K = \frac{R_1}{R_1+R_2}$$

and the average gain is then equal to:

$$\frac{R_1+R_2}{2R_1+R_2}$$

From these results we can see that K can be changed by altering either $R_1$ or $R_2$. However, doing so will change the frequency response of the network. Normal rules of impedance scaling should be followed when changing the value of either $R_1$ or $R_2$.

**Group Delay Approximation**

An inductor can now be added to give a suitable group delay response. We now have the RLC lattice depicted in Figure 25.

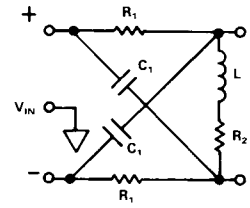



*Figure 25. RLC Lattice*

The complete derivation for the response of this equalizer is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\left[\frac{R_2}{2}+\frac{SL}{2}\right]\cdot\frac{1}{SC}}{\frac{R_2}{2}+\frac{SL}{2}+\frac{1}{SC}} - \frac{\left[\frac{R_2}{2}+\frac{SL}{2}\right]\cdot R_1}{\frac{R_2}{2}+\frac{SL}{2}+R_1}$$

$$R_1+\frac{\left[\frac{R_2}{2}+\frac{SL}{2}\right]\cdot\frac{1}{SC}}{\frac{R_2}{2}+\frac{SL}{2}+\frac{1}{SC}} \qquad \frac{1}{SC}+\frac{\left[\frac{R_2}{2}+\frac{SL}{2}\right]\cdot R_1}{\frac{R_2}{2}+\frac{SL}{2}+R_1}$$

$$= \frac{\left[\frac{R_2}{2}+\frac{SL}{2}\right]\cdot\left[\frac{1}{SC}-R_1\right]}{\frac{R_1R_2}{2}+\frac{SLR_1}{2}+\frac{R_1}{SC}+\frac{R_2}{2SC}+\frac{SL}{2SC}}$$

$$= -\left[\frac{S^2R_1LC-S[L-CR_1R_2]-R_2}{S^2R_1LC+S[L+CR_1R_2]+2R_1+R_2}\right]$$

ALL PASS NETWORK

$$= -\left[\frac{S^2R_1LC-S[L+CR_1R_2]+2R_1+R_2}{S^2R_1LC+S[L+CR_1R_2]+2R_1+R_2}\right] +$$

MAGNITUDE TERM

$$\left[\frac{2[R_1+R_2+SCR_1R_2]}{S^2R_1LC+S[L+CR_1R_2]+2R_1+R_2}\right]$$

There is no "best" solution to the group delay question. The choice of inductor value in the 15 MHz application example was based on SPICE simulation of the transfer function. However, if K remains the same as in the example, then altering $\tau$ becomes a simple frequency scaling of the network.

If $R_1$ and $R_2$ remain unchanged

*and if* $\tau \rightarrow \tau'$

$$\textit{then } C \rightarrow \frac{\tau' C}{\tau} \textit{ and } L \rightarrow \frac{\tau L}{\tau'}$$

Any deviation from the K value given in the example will require the value of L to be recalculated.

## CHOICE OF LOW PASS FILTER WITH THE RECOMMENDED EQUALIZER

A fifth order, Gaussian-to −6 dB transitional filter is recommended for use with the equalizer. This type of low pass filter, shown in Figure 26, is also used in the 15 MHz application example. Low group delay ripple and high out-of-band rejection make this design work well with the recommended equalizer and differentiator networks. The recommended location for the low pass filter is between the VGA and the first ×4 buffer. The equalizer is then placed between the first and second ×4 buffers. This minimizes the potential for oscillations induced by interstage feedback.

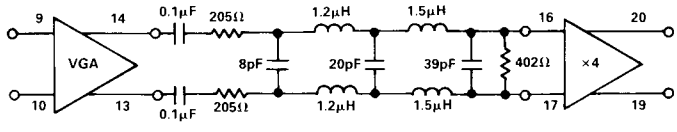



*Figure 26. 5th Order Guassian to 6 dB Transitional Filter*

The magnitude and group delay characteristics of this filter are shown in Figures 27 and 28, respectively.

## THE SINGLE ENDED PASSIVE DELAY-LINE DIFFERENTIATOR

The recommended configuration of the passive delay-line differentiator is shown in Figure 29. Again, this configuration is employed in the 15 MHz application example.

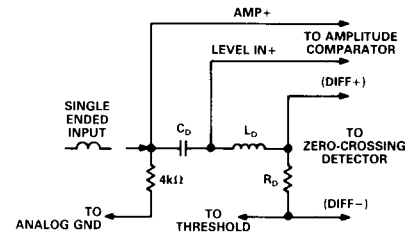



*Figure 29. Single Ended Configuration of Passive Delay Line Differentiator*

## RECOMMENDED COMPONENTS

$$f_D = \frac{1}{2\pi\sqrt{L_D C_D}}$$

$f_D$ = 1.5 Times the Maximum Desired Differentiated Frequency

$$R_D = K\left[\sqrt{\frac{L_D}{C_D}}\right]$$

$R_D$ Minimum Value: 120 Ω
150 Ω or Greater is Recommended

$1.3 \leq K \leq 1.7$

(Best Magnitude Response) (Best Group Delay Response)

Figures 30 through 33 show the typical performance to be expected from the recommended passive delay-line differentiator. The choice of components used to obtain these characteristics are the ones used in the 15 MHz application example.

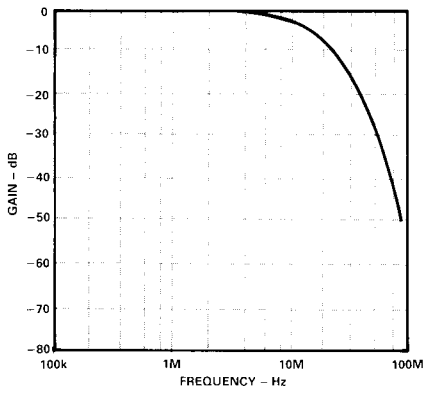



*Figure 27. Gaussian Low Pass Filter Magnitude Response*

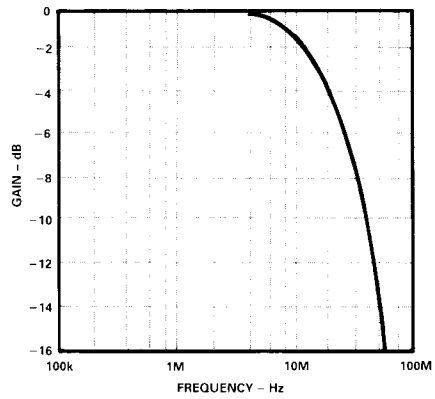



*Figure 30. Magnitude Response of Undifferentiated Output*

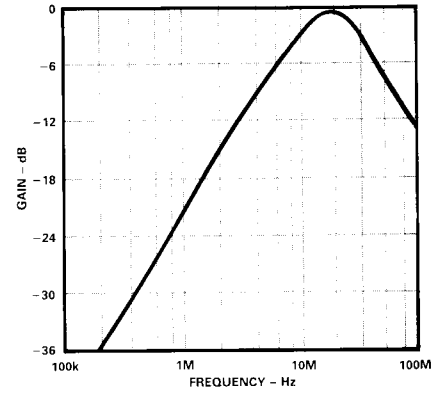



*Figure 32. Magnitude Response of Differentiated Output*

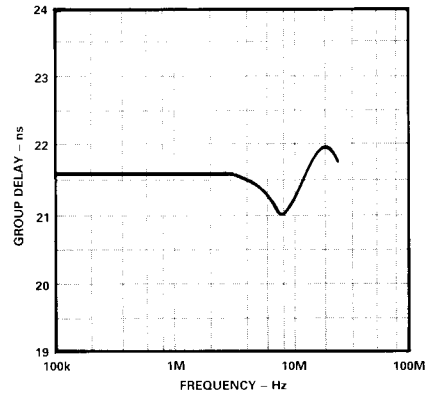



*Figure 28. Gaussian Low Pass Filter Group Delay Response*

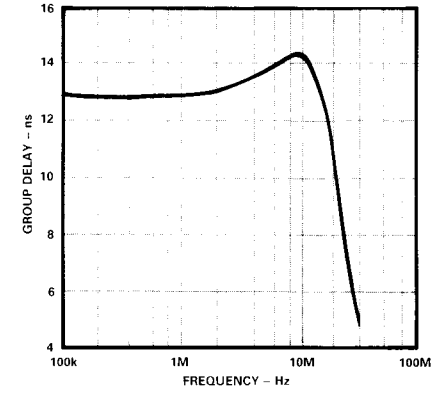



*Figure 31. Group Delay Characteristics of Undifferentiated Output*

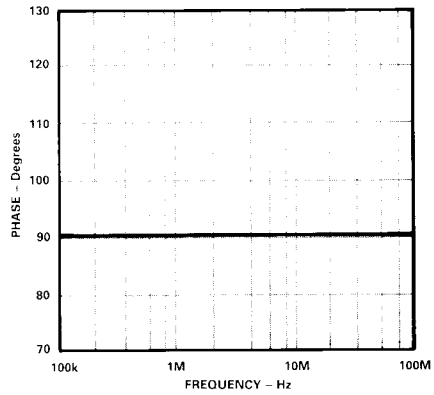
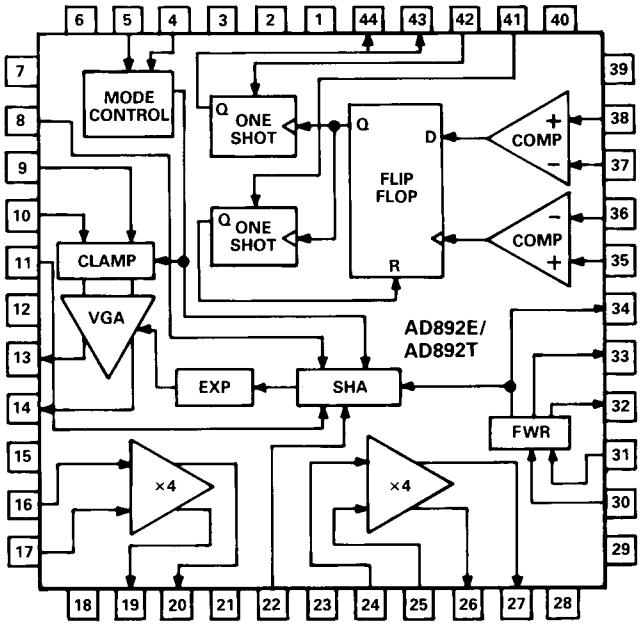



*Figure 33. Relative Phase Between Differentiated and Undifferentiated Output*

## PIN ASSIGNMENTS

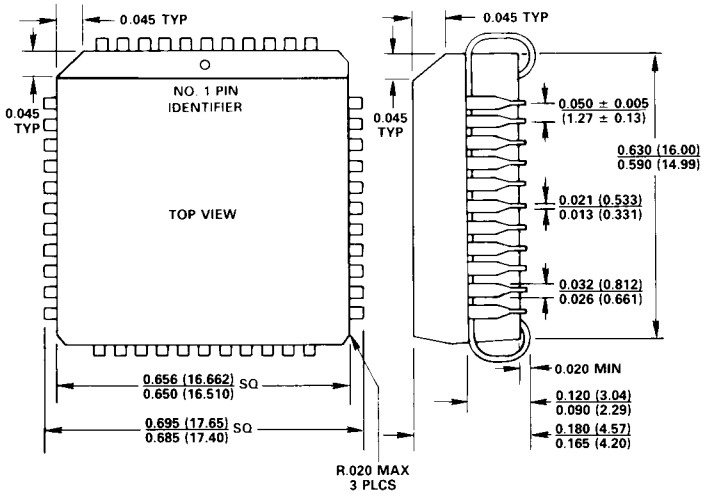
| Pin | Description |
|---|---|
| 1 | +5 V Supply |
| 2 | No Connection (Can Be Left Floating) |
| 3 | No Connection (Can Be Left Floating) |
| 4 | Mode Control Bit B (TTL Compatible) |
| 5 | Mode Control Bit A (TTL Compatible) |
| 6 | Digital Ground |
| 7 | No Connection (Can Be Left Floating) |
| 8 | "AGC Level Set" Input Voltage |
| 9 | Variable Gain Amplifier Input (+) |
| 10 | Variable Gain Amplifier Input (− ) |
| 11 | "VGA Level Set" Input Voltage |
| 12 | No Connection (Can Be Left Floating) |
| 13 | Variable Gain Amplifier Output (−) |
| 14 | Variable Gain Amplifier Output (+) |
| 15 | No Connection (Can Be Left Floating) |
| 16 | #1 12.75 dB Buffer Input (− ) |
| 17 | #1 12.75 dB Buffer Input (+) |
| 18 | +12 V Supply (Analog) |
| 19 | #1 12.75 dB Buffer Output (+) |
| 20 | #1 12.75 dB Buffer Output (− ) |
| 21 | No Connection (Can Be Left Floating) |
| 22 | Sample-and-Hold Capacitor |
| 23 | No Connection (Can Be Left Floating) |
| 24 | #2 12.75 dB Buffer Input (− ) |
| 25 | #2 12.75 dB Buffer Input (+) |
| 26 | #2 12.75 dB Buffer Output (+) |
| 27 | #2 12.75 dB Buffer Output (− ) |
| 28 | Analog Ground |
| 29 | No Connection (Can Be Left Floating) |
| 30 | Full Wave Rectifier Input (+) |
| 31 | Full Wave Rectifier Input (− ) |
| 32 | Rectified Signal to Derive Threshold |
| 33 | Rectified Signal for Differentiator |
| 34 | Rectified Signal to S/H; AGC Attack and Decay Is Programmed at This Point |
| 35 | Zero Crossing Comparator Input (+) |
| 36 | Zero Crossing Comparator Input (− ) |
| 37 | Minimum Threshold Level Input |
| 38 | Signal Amplitude Comparator Input |
| 39 | Internal Voltage Reference |
| 40 | +12 V Supply (Digital) |
| 41 | Apply Resistor to Program Time Domain Filter Pulse Width |
| 42 | Apply Resistor to Program Output Pulse Width |
| 43 | Data Output (Open Collector AD892T)<br>Data Output (+ ECL AD892E) |
| 44 | Data Output Ground (Emitter of Output Device AD892T)<br>Data Output (− ECL AD892E) |




## PACKAGE OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 44-Pin PLCC (P) Package




## ORDERING GUIDE

| Model No. | Package |
|---|---|
| AD892EJP | 44-Pin PLCC |
| AD892TJP | 44-Pin PLCC |

**CAUTION**

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PLESSEY
SEMICONDUCTORS

MAY 1990
PRELIMINARY INFORMATION

# SP5510

## 1.3 GHz BI-DIRECTIONAL $I^2C$ BUS CONTROLLED SYNTHESISER

*(Supersedes October 1989 Edition)*

The SP5510 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device also contains 4 addressable current limited outputs and 4 addressable Bi-Directional open collector ports one of which is a 3 Bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

### FEATURES

- Complete 1.3GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 43mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi-Directional (DP18/MP20)
- 5 Controllable Outputs, 4 Bi-Directional (MP16)
- 5 Level ADC
- Variable I²C BUS Address For Picture in Picture TV
- Full ESD Protection

### APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz Prescaler
- Cable Tuning Systems
- VCRs

### PACKAGE DETAILS

- SP5510 - DP18
- SP5510S - MP16
- SP5510T - MP20 Wide Body

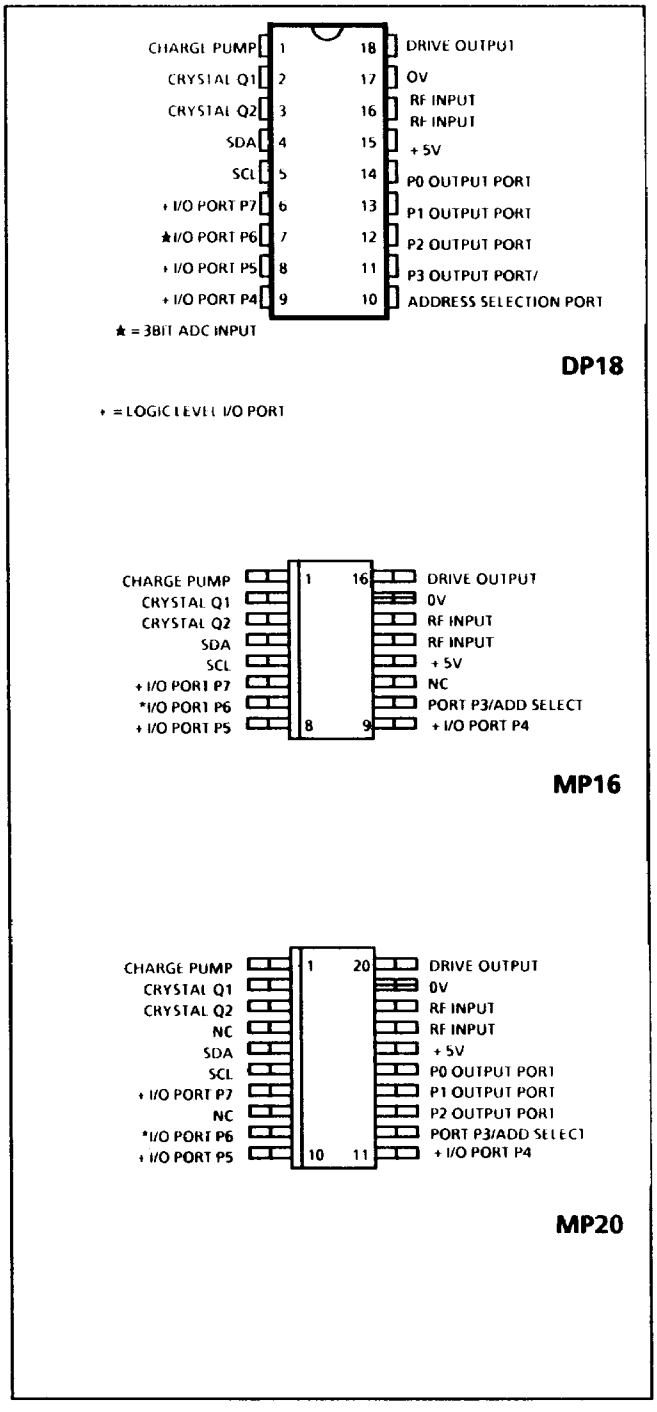



*Fig.1 Pin Connections*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**
$T_{amb}$ = -10°C to 80°C, $V_{CC}$ = +4.5V TO 5.5V
(All pin connections refer to DP package )

| Characteristic | Pin | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Supply current | 14 | | 43 | 50 | mA | $V_{CC}$ = 5V |
| Prescaler Input Voltage | 15,16 | 12.5 | | 300 | $mV_{RMS}$ | 50MHz to 1GHz |
| Prescaler Input Voltage | 15,16 | 30 | | 300 | $mV_{RMS}$ | 1.3GHz |
| Prescaler Input Impedance<br>Input Capacitance | 15,16 | | 50<br>2 | | Ω<br>pF | |
| **SDA,SCL** Input High Voltage<br>Input Low Voltage<br>Input High Current<br>Input Low Current<br>Leakage Current | 4,5<br>4,5<br>4,5<br>4,5<br>4,5 | 3<br>0 | | 5.5<br>1.5<br>10<br>-10<br>10 | V<br>V<br>µA<br>µA<br>µA | <br><br>Input Voltage = $V_{CC}$<br>Input Voltage = 0V<br>When $V_{CC}$ = 0V |
| **SDA** Output Voltage | 4 | | | 0.4 | V | $I_{sink}$ = 3mA |
| Charge Pump Current Low | 1 | | ±50 | | µA | Byte 4 Bit 2 = 0 Pin 1 = 2V |
| Charge Pump Current High | 1 | | ±200 | | µA | Byte 4 Bit 2 = 1 Pin 1 = 2V |
| Charge Pump Output Leakage Current | 1 | | | ±5 | nA | Byte 4 Bit 4 = 1 Pin 1 = 2V |
| Charge Pump Drive Output Current | 18 | 500 | | | µA | V pin 18 = 0.7V |
| Charge Pump Amplifier Gain | | 2500 | 6400 | 22500 | | |
| Recommended Crystal Series Resistance | | 10 | | 200 | Ω | |
| Crystal Oscillator Drive Level | | 30 | | 50 | mVp-p | |
| Crystal Oscillator Source Impedance | 2 | | -400 | | Ω | Nominal Spread ± 15% |
| **Output Ports** | | | | | | |
| P0-P3 Sink Current* | 10-13 | 0.7 | 1 | 1.5 | mA | $V_{OUT}$ = 12V |
| P0-P3 Leakage Current* | 10-13 | | | 10 | µA | $V_{OUT}$ = 13.2V |
| P4-P7 Sink Current | 6-9 | 10 | | | mA | $V_{OUT}$ = 0.7V |
| P4-P7 Leakage Current | 6-9 | | | 10 | µA | $V_{OUT}$ = 13.2V |
| **Input Ports** | | | | | | |
| P3 Input Current High | 10 | | | +10 | µA | V pin10 = 13.2V |
| P3 Input Current Low | 10 | | | -10 | µA | V pin10 = 0V |
| P4,P5,P7 Input Voltage Low | 6,7,9 | | | 0.8 | V | |
| P4,P5,P7 Input Voltage High | 6,7,9 | 2.7 | | | V | |
| P6 Input Current High | 7 | | | +10 | µA | See Table 3 for ADC Levels |
| P6 Input Current Low | 7 | | | -10 | µA | |

* Ports P0-P2 not available in MP16 Package