Quad, Low Power, 12-Bit, 180 MSPS, Digital-to-Analog Converter and Waveform Generator

FEATURES

▸ Highly integrated quad DAC
▸ On-chip 4096 × 12-bit pattern memory
▸ On-chip DDS
▸ Power dissipation @ 3.3 V, 4 mA output typical
  ▸ 315.25 mW at 180 MSPS
▸ Power-down mode: <5 mW at 3.3 V
▸ Supply voltage: 1.8 V to 3.3 V
▸ SFDR to Nyquist
  ▸ 86 dBc at 10 MHz output
▸ Phase noise at 1 kHz offset, 180 MSPS, 4 mA: −140 dBc/Hz
▸ Differential full-scale current outputs: 8 mA max at 3.3 V
▸ Small footprint, 5 mm × 5 mm with 3.5 mm × 3.6 mm exposed paddle, 32-lead LFCSP
▸ RoHS compliant package

APPLICATIONS

▸ Medical instrumentation
  ▸ Ultrasound transducer excitation
▸ Portable instrumentation
  ▸ Signal generators, arbitrary waveform generators

GENERAL DESCRIPTION

The AD9106 TxDAC® and waveform generator is a high performance, quad digital-to-analog converter (DAC) integrating on-chip pattern memory for complex waveform generation with a direct digital synthesizer (DDS).

The DDS is a 12-bit output, up to 180 MHz main clock sinewave generator with a 24-bit tuning word allowing 10.8 Hz/LSB frequency resolution. The DDS has a single frequency output for all four DACs and independent programmable phase shift outputs for each of the four DACs.

SRAM data can include directly generated stored waveforms, amplitude modulation patterns applied to DDS outputs, or DDS frequency tuning words.

An internal pattern control state machine allows the user to program the pattern period for all four DACs as well as the start delay within the pattern period for the signal output on each DAC channel.

Registers accessed using the serial peripheral interface (SPI) configure the digital waveform generator and load patterns into the SRAM.

There are gain adjustment factors and offset adjustments applied to the digital signals on their way into the four DACs.

The AD9106 offers exceptional ac and dc performance and supports DAC sampling rates up to 180 MSPS. The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9106 make it well suited for portable and low power applications.

PRODUCT HIGHLIGHTS

1. High Integration: On-chip DDS and 4096 x 12 pattern memory
2. Low Power: Power-down mode provides for low power idle periods
3. Flexible Operation: 3- or 4-wire SPI interface; 1.8 V or 3.3 V supply

Rev. C

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FUNCTIONAL BLOCK DIAGRAM

Figure 1.

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DC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDDx = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		12		Bits
ACCURACY AT 3.3 V				
Differential Nonlinearity (DNL)		±0.4		LSB
Integral Nonlinearity (INL)		±0.5		LSB
DAC OUTPUTS				
Offset Error		±0.00025		% of FSR
Gain Error Internal Reference—No Automatic I_{OUTFS} Calibration	−1.0		+1.0	% of FSR
Full-Scale Output Current[1] at 3.3 V	2	4	8	mA
Output Resistance		200		MΩ
Output Compliance Voltage	−0.5		+1.0	V
Crosstalk, DAC to DAC				
f_{OUT} = 10 MHz		96		dBc
f_{OUT} = 60 MHz		82		dBc
DAC TEMPERATURE DRIFT				
Gain with Internal Reference		±251		ppm/°C
Internal Reference Voltage		±119		ppm/°C
REFERENCE OUTPUT				
Internal Reference Voltage with AVDDx = 3.3 V		1.0		V
Output Resistance		10		kΩ
REFERENCE INPUT				
Voltage Compliance	0.1		1.25	V
Input Resistance External, Reference Mode		1		MΩ
DAC MATCHING				
Gain Matching—No Automatic I_{OUTFS} Calibration		±0.75		% of FSR

[1] Based on use of 8 kΩ external R_{SETx} resistors.

DC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDDx = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V, I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
RESOLUTION		12		Bits
ACCURACY AT 1.8 V				
Differential Nonlinearity (DNL)		±0.4		LSB
Integral Nonlinearity (INL)		±0.4		LSB
DAC OUTPUTS				
Offset Error		±0.00025		% of FSR
Gain Error Internal Reference—No Automatic I_{OUTFS} Calibration	−1.0		+1.0	% of FSR
Full-Scale Output Current[1] at 1.8 V	2	4	4	mA
Output Resistance		200		MΩ
Output Compliance Voltage	−0.5		+1.0	V

SPECIFICATIONS

Table 2. (Continued)

Parameter	Min	Typ	Max	Unit
Crosstalk, DAC to DAC				
f_{OUT} = 30 MHz		94		dB
f_{OUT} = 60 MHz		78		dB
DAC TEMPERATURE DRIFT				
Gain		±228		ppm/°C
Reference Voltage		±131		ppm/°C
REFERENCE OUTPUT				
Internal Reference Voltage with AVDDx = 1.8 V		1.0		V
Output Resistance		10		kΩ
REFERENCE INPUT				
Voltage Compliance	0.1		1.25	V
Input Resistance External, Reference Mode		1		MΩ
DAC MATCHING				
Gain Matching—No Automatic I_{OUTFS} Calibration		±0.75		% of FSR

[1] Based on use of 8 kΩ external R_{SETx} resistors.

DIGITAL TIMING SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDDx = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKx)				
Maximum Clock Rate	180			MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)	80			MHz
Minimum Pulse Width High		6.25		ns
Minimum Pulse Width Low		6.25		ns
Setup Time, SDIO to SCLK	3.5			ns
Hold Time, SDIO to SCLK	1.5			ns
Output Data Valid, SCLK to SDO[1] or SDIO		6.2		ns
Setup Time, $\overline{CS}$ to SCLK	4.0			ns
$\overline{TRIGGER}$ TIMING RELATIVE TO CLKP/CLKN RISING EDGE				
Setup Time (t_{SU}), $\overline{TRIGGER}$ Edge to CLKP/CLKN	1.5			ns
Hold Time, CLKP/CLKN to $\overline{TRIGGER}$ Edge	2.0			ns

[1] Note that throughout this data sheet, multifunction pins, such as SDO/SDI2/DOUT, are referred to either by the entire pin name or by a single function of the pin, for example, SDO, when only that function is relevant.

DIGITAL TIMING SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDDx = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V, I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKx)				
Maximum Clock Rate	180			MSPS

SPECIFICATIONS

Table 4. (Continued)

Parameter	Min	Typ	Max	Unit
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)	80			MHz
Minimum Pulse Width High		6.25		ns
Minimum Pulse Width Low		6.25		ns
Setup Time, SDIO to SCLK	3.5			ns
Hold Time, SDIO to SCLK	1.5			ns
Output Data Valid, SCLK to SDO or SDIO		8.8		ns
Setup Time, $\overline{CS}$ to SCLK	4.0			ns
$\overline{TRIGGER}$ TIMING RELATIVE TO CLKP/CLKN RISING EDGE				
Setup Time, $\overline{TRIGGER}$ Edge to CLKP/CLKN	1.5			ns
Hold Time, CLKP/CLKN to $\overline{TRIGGER}$ Edge	2.0			ns

INPUT/OUTPUT SIGNAL SPECIFICATIONS

Table 5.

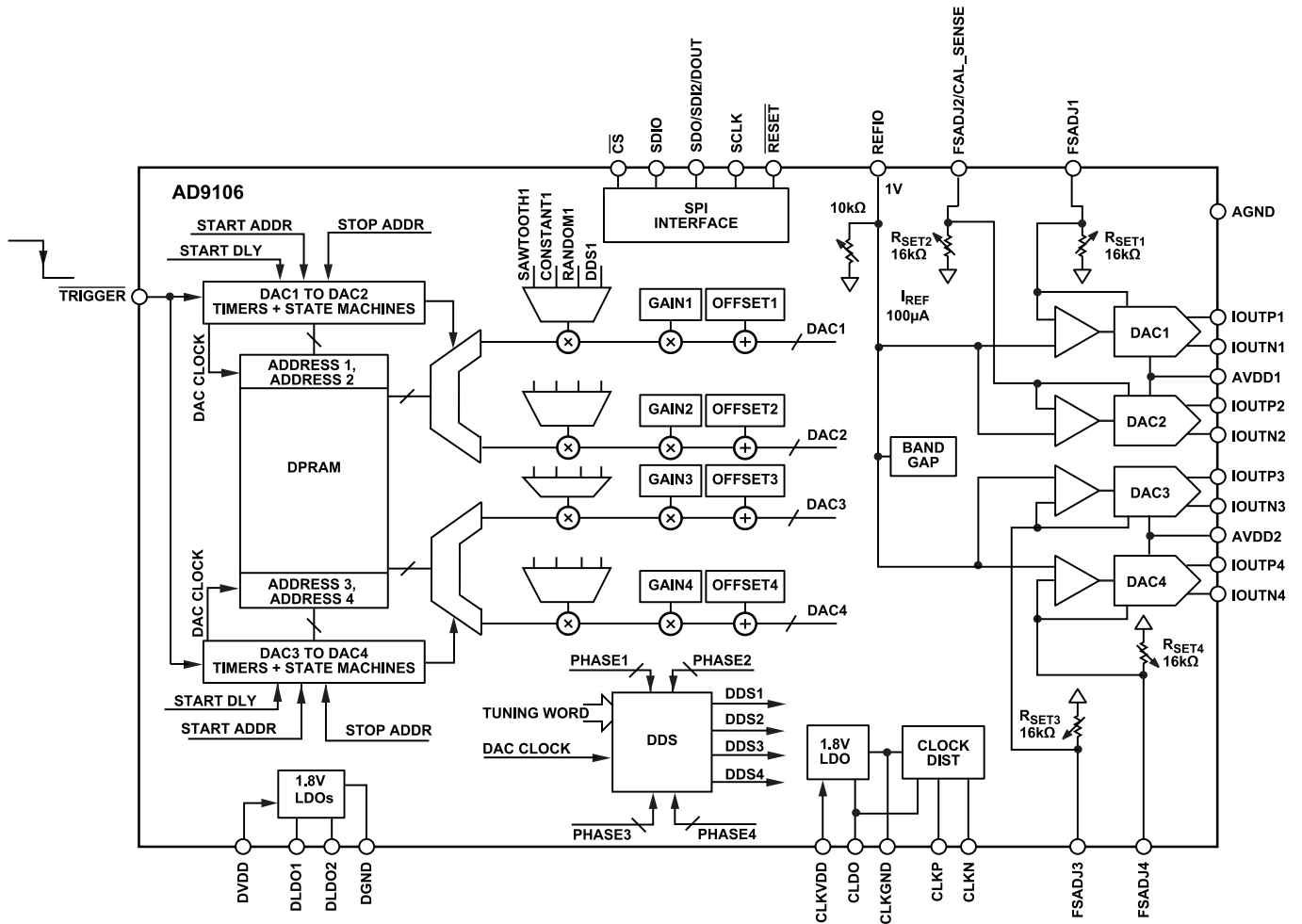| Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL (SCLK, $\overline{CS}$, SDIO, SDO/SDI2/DOUT, $\overline{RESET}$, $\overline{TRIGGER}$)					
Input Voltage, V_{IN}					
Logic High	DVDD = 1.8 V	1.53			V
	DVDD = 3.3 V	2.475			V
Logic Low	DVDD = 1.8 V			0.27	V
	DVDD = 3.3 V			0.825	V
CMOS OUTPUT LOGIC LEVEL (SDIO, SDO/SDI2/DOUT)					
Output Voltage, V_{OUT}					
Logic High	DVDD = 1.8 V	1.79			V
	DVDD = 3.3 V	3.28			V
Logic Low	DVDD = 1.8 V			0.25	V
	DVDD = 3.3 V			0.625	V
DAC CLOCK INPUT (CLKP, CLKN)					
Minimum Peak-to-Peak Differential Input Voltage, V_{CLKP}/V_{CLKN}			150		mV
Maximum Voltage at V_{CLKP} or V_{CLKN}			V_{DVDD}		V
Minimum Voltage at V_{CLKP} or V_{CLKN}			V_{DGND}		V
Common-Mode Voltage Generated on Chip			0.9		V

AC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDDx = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
DAC Sample Rate (f_{DAC}) = 180 MSPS, DAC Output Frequency (f_{OUT}) = 10 MHz		86		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		73		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		92		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		77		dBc
NOISE SPECTRAL DENSITY (NSD)				
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		−167		dBm/Hz

SPECIFICATIONS

Table 6. (Continued)

Parameter	Min	Typ	Max	Unit
PHASE NOISE AT 1 kHz FROM CARRIER				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		−140		dBc/Hz
DYNAMIC PERFORMANCE				
Output Settling Time, Full-Scale Output Step (to 0.1%)[1]		31.2		ns
Trigger to Output Delay, f_{DAC} = 180 MSPS[2]		96		ns
Rise Time, Full-Scale Swing[1]		3.25		ns
Fall Time, Full-Scale Swing[1]		3.26		ns

[1] Based on the 85 Ω resistors from DAC output terminals to ground.

[2] Start delay = 0 f_{DAC} clock cycles.

AC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDDx = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V, I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 7.

Parameter	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		83		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		74		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		91		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		83		dBc
NSD				
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		−163		dBm/Hz
PHASE NOISE AT 1 kHz FROM CARRIER				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		−140		dBc/Hz
DYNAMIC PERFORMANCE				
Output Settling Time (to 0.1%)[1]		31.2		ns
Trigger to Output Delay, f_{DAC} = 180 MSPS[2]		96		ns
Rise Time[1]		3.25		ns
Fall Time[1]		3.26		ns

[1] Based on the 85 Ω resistors from DAC output terminals to ground.

[2] Start delay = 0 f_{DAC} clock cycles.

POWER SUPPLY VOLTAGE INPUTS AND POWER DISSIPATION

Table 8.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG SUPPLY VOLTAGES					
AVDD1, AVDD2		1.7		3.6	V
CLKVDD		1.7		3.6	V
CLDO	On-chip low dropout (LDO) regulator not in use	1.7		1.9	V
DIGITAL SUPPLY VOLTAGES					
DVDD		1.7		3.6	V
DLDO1, DLDO2	On-chip LDO not in use	1.7		1.9	V
POWER CONSUMPTION, 3.3 V	AVDDx = 3.3 V; DVDD = 3.3 V; CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2				

SPECIFICATIONS

Table 8. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f_{DAC} = 180 MSPS, Pure Continuous Waveform (CW) Sine Wave	12.5 MHz (DDS only), all four DACs		315.25		mW
I_{AVDDx}			28.51		mA
I_{DVDD}					
DDS Only	CW sine wave output		60.3		mA
RAM Only	50% duty cycle full-scale (FS) pulse output		27.1		mA
DDS and RAM Only	50% duty cycle sine wave output		39.75		mA
I_{CLKVDD}			6.72		mA
Power-Down Mode	REF_PDN = 0, DACs sleep, clock power down, external clock, and supplies on		4.73		mW
POWER CONSUMPTION, 1.8 V	AVDDx = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V				
f_{DAC} = 180 MSPS, Pure CW Sine Wave	12.5 MHz (DDS only)		167		mW
I_{AVDDx}			28.14		mA
I_{DVDD}			0.151		mA
I_{DLDO2}					
DDS Only	CW sine wave output		53.75		mA
RAM Only	50% duty cycle FS pulse output		17.78		mA
DDS and RAM Only—50% Duty Cycle Sine Wave Output			35.4		mA
I_{DLDO1}			4.0		mA
I_{CLKVDD}			0.0096		mA
I_{CLDO}			6.6		mA
Power-Down Mode	REF_PDN = 0, DACs sleep, clock power down, external clock, and supplies on		1.49		mW

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ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
AVDD1, AVDD2, DVDD to AGND, DGND, CLKGND	−0.3 V to +3.9 V
CLKVDD to AGND, DGND, CLKGND	−0.3 V to +3.9 V
CLDO, DLDO1, DLDO2 to AGND, DGND, CLKGND	−0.3 V to +2.2 V
AGND to DGND, CLKGND	−0.3 V to +0.3 V
DGND to AGND, CLKGND	−0.3 V to +0.3 V
CLKGND to AGND, DGND	−0.3 V to +0.3 V
$\overline{CS}$, SDIO, SCLK, SDO/SDI2/DOUT, $\overline{RESET}$, $\overline{TRIGGER}$ to DGND	−0.3 V to DVDD + 0.3 V
CLKP, CLKN to CLKGND	−0.3 V to CLKVDD + 0.3 V
REFIO to AGND	−1.0 V to AVDDx + 0.3 V
IOUTP1, IOUTN1, IOUTP2, IOUTN2, IOUTP3, IOUTN3, IOUTP4, IOUTN4 to AGND	−0.3 V to DVDD + 0.3 V
FSADJ1, FSADJ2/CAL_SENSE, FS4DJ3, FSADJ4 to AGND	−0.3 V to AVDDx + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JB} is the junction to board thermal resistance. θ_{JC} is the junction to case thermal resistance.

Table 10. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
CP-32-12[1]	30.18	6.59	3.84	°C/W

[1] Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a JEDEC 4-layer 2S2P board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA} and θ_{JB}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS
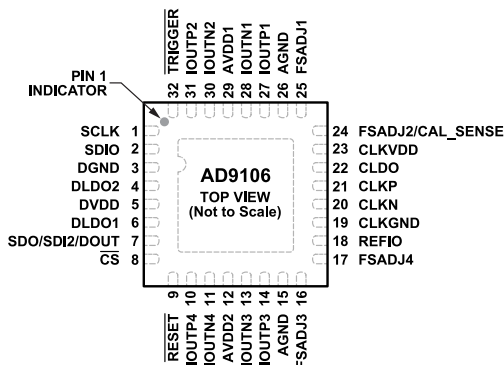
Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	SPI Clock Input.
2	SDIO	SPI Data Input/Output. Primary bidirectional data line for the SPI port.
3	DGND	Digital Ground.
4	DLDO2	1.8 V Internal Digital LDO2 Output. When the internal digital LDO2 is enabled, bypass this pin with a 0.1 µF capacitor.
5	DVDD	3.3 V External Digital Power Supply. DVDD defines the level of the digital interface of the AD9106 (SPI interface).
6	DLDO1	1.8 V Internal Digital LDO1 Output. When the internal digital LDO1 is enabled, bypass this pin with a 0.1 µF capacitor.
7	SDO/SDI2/DOUT	Serial Data Output (SDO). In 4-wire SPI mode, this pin outputs the data from the SPI.
		Second Data Input Line (SDI2). In double-SPI mode, this pin is a second data input line, SDI2, for the SPI port used to write to the SRAM.
		Pulse Output (DOUT). In data output mode, this terminal is a programmable pulse output.
8	$\overline{CS}$	SPI Port Chip Select, Active Low.
9	$\overline{RESET}$	Active Low Reset Pin. Resets registers to their default values.
10	IOUTP4	DAC4 Current Output, Positive Side.
11	IOUTN4	DAC4 Current Output, Negative Side.
12	AVDD2	1.8 V to 3.3 V Power Supply Input for DAC3 and DAC4.
13	IOUTN3	DAC3 Current Output, Negative Side.
14	IOUTP3	DAC3 Current Output, Positive Side.
15	AGND	Analog Ground.
16	FSADJ3	External Full-Scale Current Output Adjust for DAC3.
17	FSADJ4	External Full-Scale Current Output Adjust for DAC4.
18	REFIO	DAC Voltage Reference Input/Output.
19	CLKGND	Clock Ground.
20	CLKN	Clock Input, Negative Side.
21	CLKP	Clock Input, Positive Side.
22	CLDO	1.8 V Clock Power Supply Output (Internal Regulator in Use), Clock Power Supply Input (Internal Regulator Bypassed). When the internal clock LDO is enabled, bypass this pin with a 0.1 µF capacitor.
23	CLKVDD	1.8 to 3.3 V Clock Power Supply Input.
24	FSADJ2/CAL_SENSE	External Full-Scale Current Output Adjust for DAC2 (FSADJ2).
		Sense Input for Automatic I_{OUTFS} Calibration (CAL_SENSE).
25	FSADJ1	External Full-Scale Current Output Adjust for DAC1 or Full-Scale Current Output Adjust Reference for Automatic I_{OUTFS} Calibration.
26	AGND	Analog Ground.
27	IOUTP1	DAC1 Current Output, Positive Side.
28	IOUTN1	DAC1 Current Output, Negative Side.
29	AVDD1	1.8 V to 3.3 V Power Supply Input for DAC1 and DAC2.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 11. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
30	IOUTN2	DAC2 Current Output, Negative Side.
31	IOUTP2	DAC2 Current Output, Positive Side.
32	$\overline{\text{TRIGGER}}$	Pattern Trigger Input, Active Low.
	EPAD	Exposed Pad. The exposed pad must be connected to DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDDx = 3.3 V; DVDD = 3.3 V; CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2.
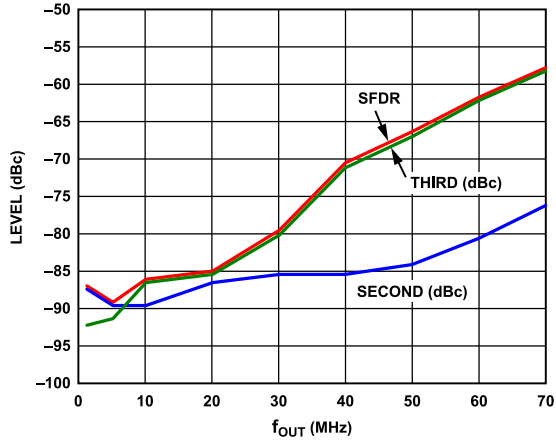
Figure 3. SFDR, Second and Third Harmonics vs. f_{OUT}, I_{OUTFS} = 8 mA
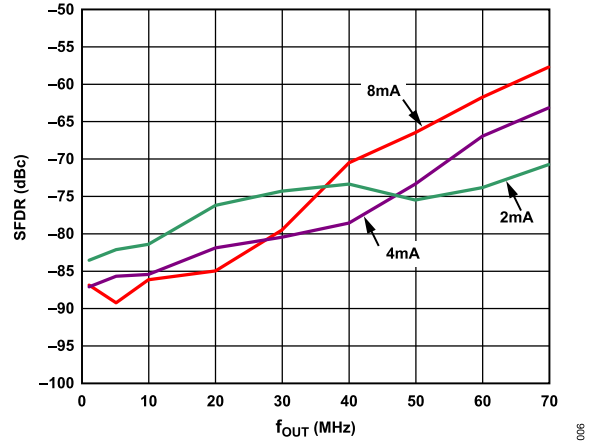
Figure 6. SFDR vs. f_{OUT}, at Three I_{OUTFS} Values
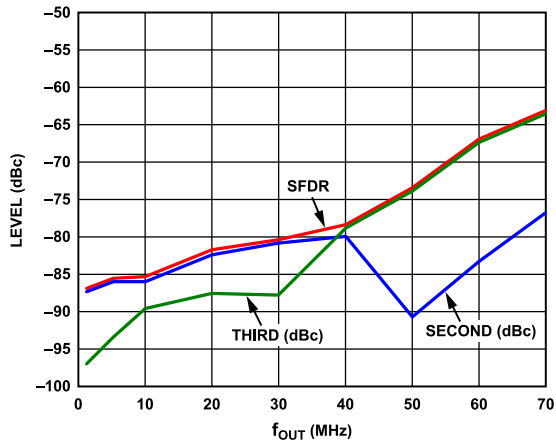
Figure 4. SFDR, Second and Third Harmonics vs. f_{OUT}, I_{OUTFS} = 4 mA
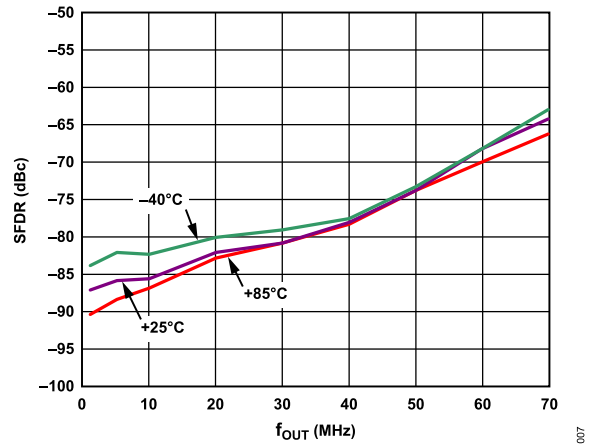
Figure 7. SFDR vs. f_{OUT}, at Three Temperatures
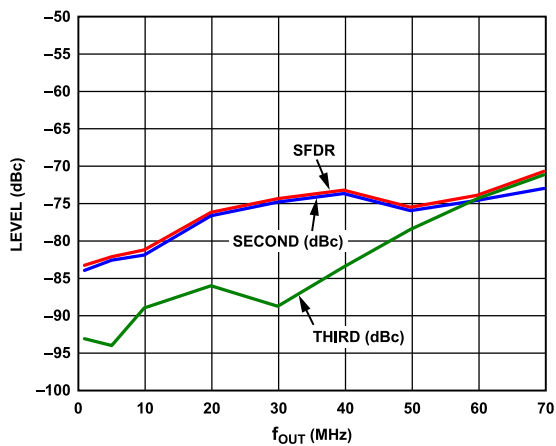
Figure 5. SFDR, Second and Third Harmonics vs. f_{OUT}, I_{OUTFS} = 2 mA
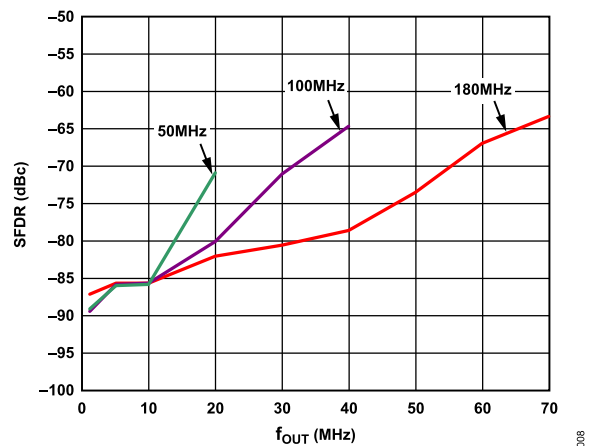
Figure 8. SFDR vs. f_{OUT}, at Three f_{DAC} Values

TYPICAL PERFORMANCE CHARACTERISTICS
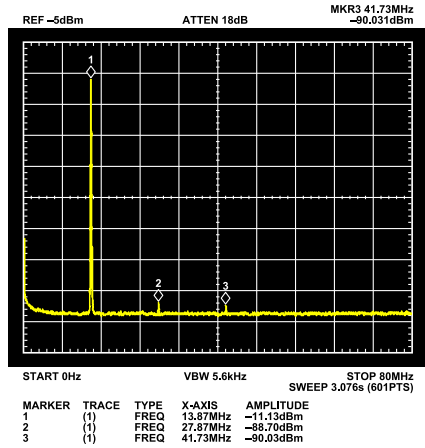
Figure 9. Output Spectrum, f_{OUT} = 13.87 MHz

Figure 10. IMD vs. f_{OUT}, at Three f_{DAC} Values

Figure 11. IMD vs. f_{OUT}, at Three I_{OUTFS} Values

Figure 12. IMD vs. f_{OUT}, All Four DACs

Figure 13. NSD vs. f_{OUT}, at Three I_{OUTFS} Values
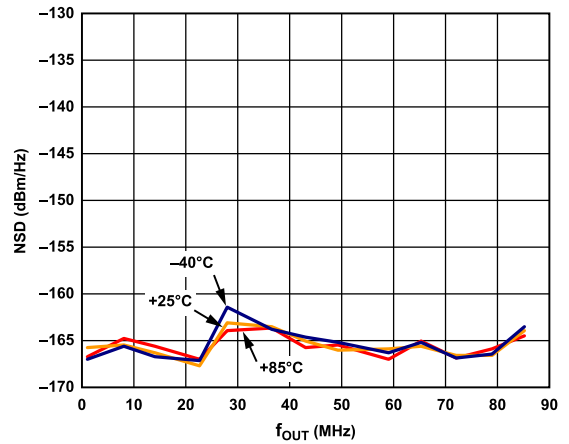
Figure 14. NSD vs. f_{OUT}, at Three Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS
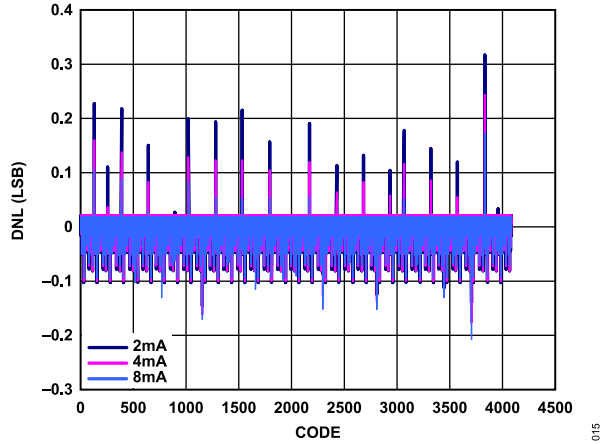
Figure 15. DNL, at Three I_{OUTFS} Values
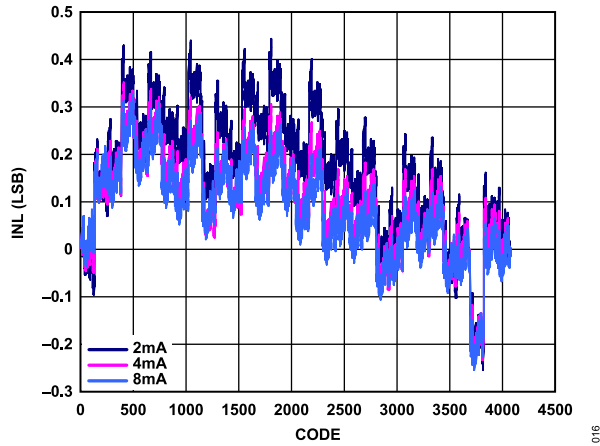
Figure 16. INL, at Three I_{OUTFS} Values
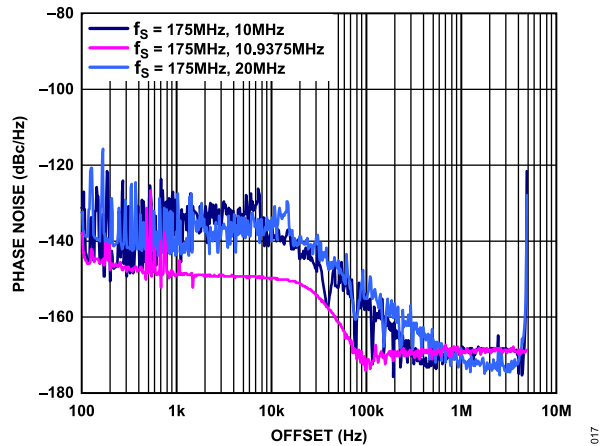
Figure 17. Phase Noise

TYPICAL PERFORMANCE CHARACTERISTICS

AVDDx = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V.
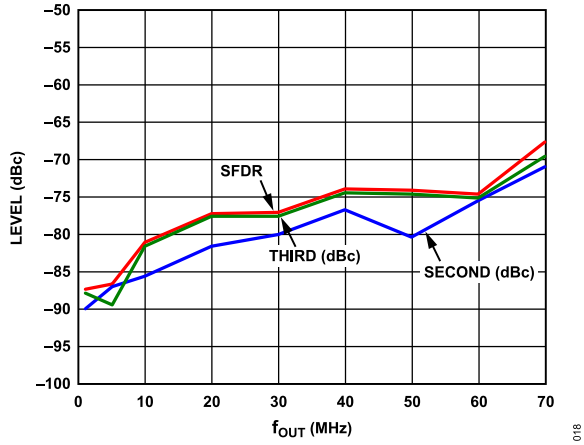
Figure 18. SFDR, Second and Third Harmonics vs. f_{OUT}, I_{OUTFS} = 4 mA
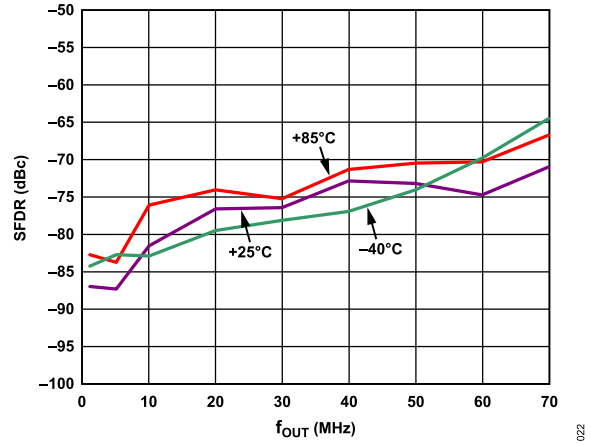
Figure 21. SFDR vs. f_{OUT}, at Three Temperatures
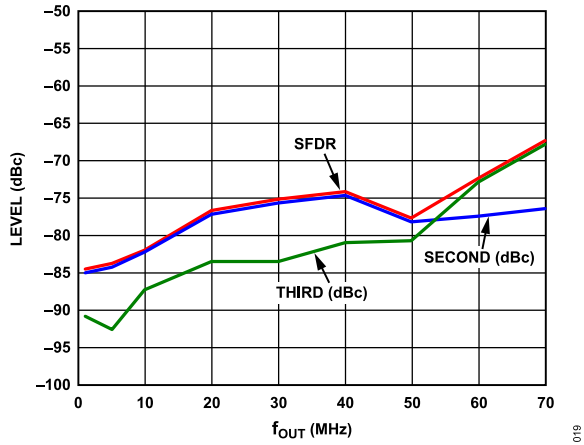
Figure 19. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 2 mA vs. f_{OUT}
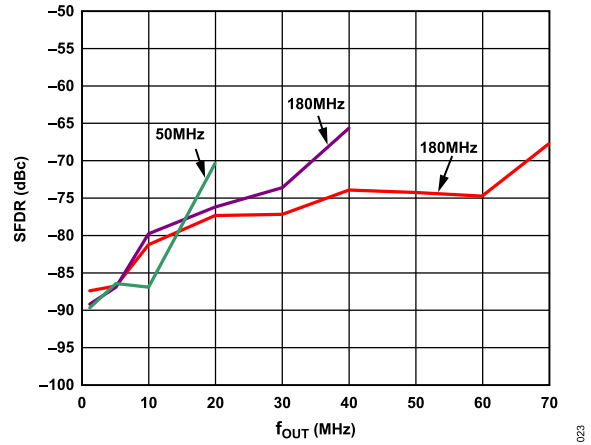
Figure 22. SFDR vs. f_{OUT}, at Three f_{DAC} Values
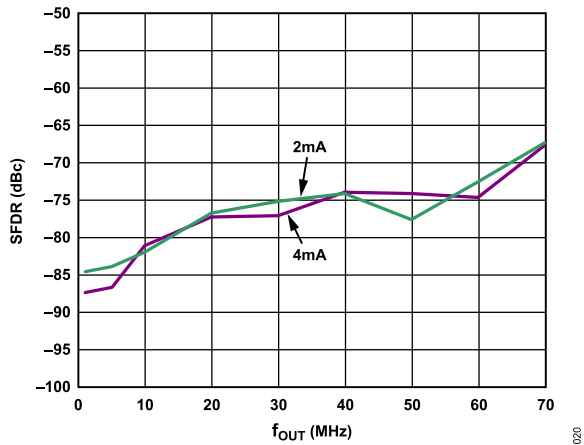
Figure 20. SFDR vs. f_{OUT}, at Two I_{OUTFS} Values
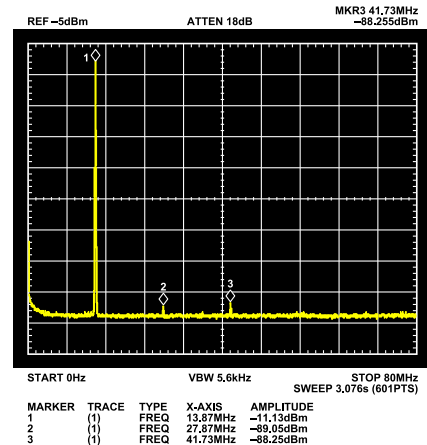
Figure 23. Output Spectrum, f_{OUT} = 13.87 MHz

TYPICAL PERFORMANCE CHARACTERISTICS
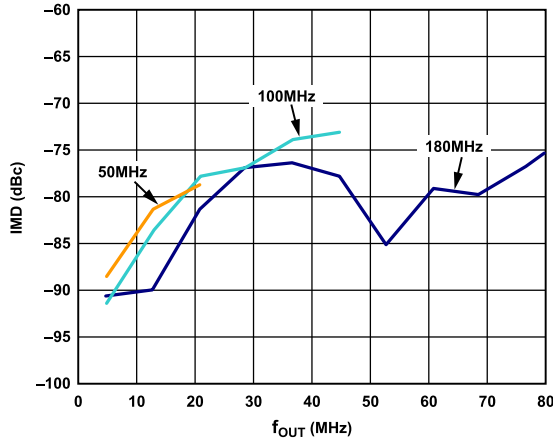
Figure 24. IMD vs. f_{OUT}, at Three f_{DAC} Values
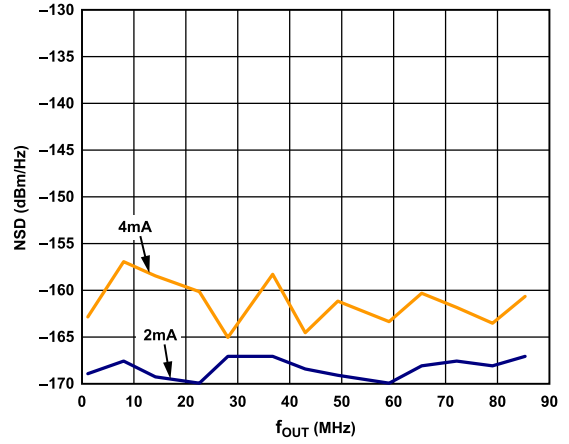
Figure 27. NSD vs. f_{OUT}, at Two I_{OUTFS} Values
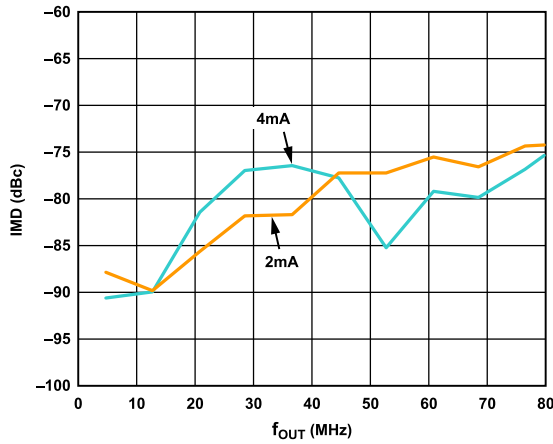
Figure 25. IMD vs. f_{OUT}, at Two I_{OUTFS} Values
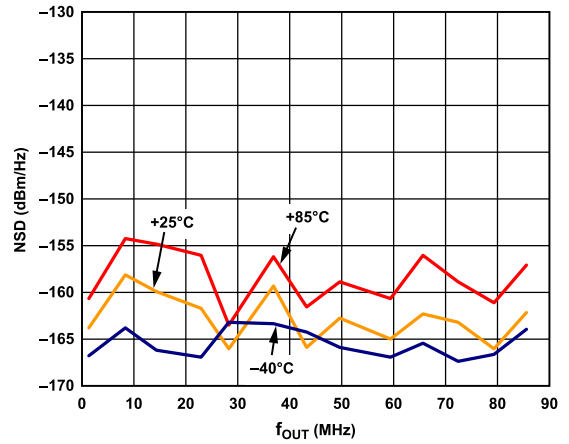
Figure 28. NSD vs. f_{OUT}, at Three Temperatures
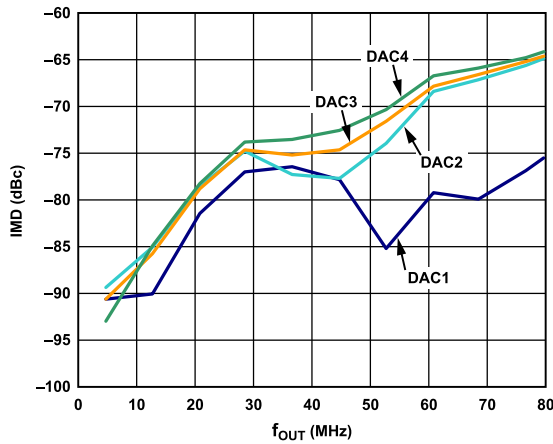
Figure 26. IMD vs. f_{OUT}, at All Four DACs
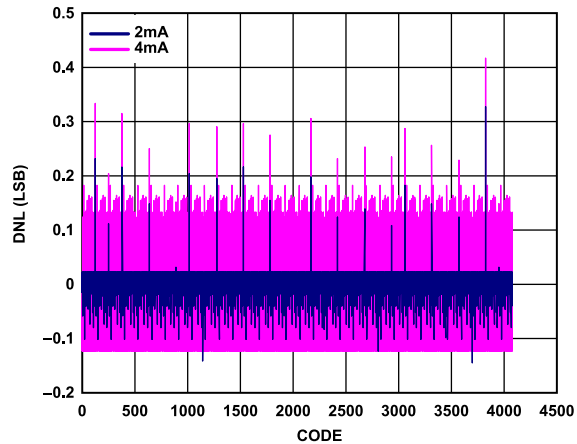
Figure 29. DNL, at Three I_{OUTFS} Values

TYPICAL PERFORMANCE CHARACTERISTICS
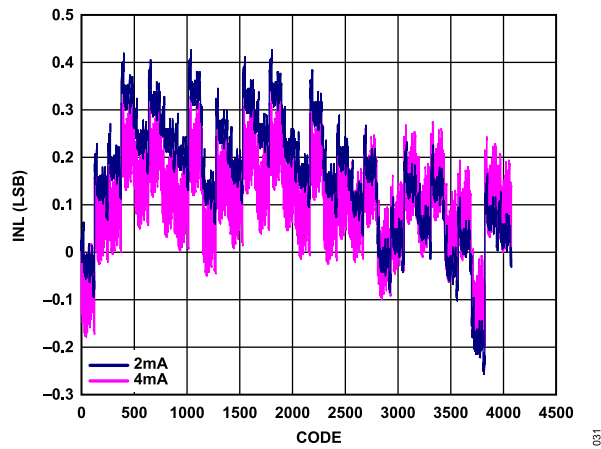
Figure 30. INL, at Two I_{OUTFS} Values

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)

INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity DNL

DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity

A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error

Offset error is the deviation of the output current from the ideal of zero. For IOUTPx, 0 mA output is expected when the inputs are all 0s. For IOUTNx, 0 mA output is expected when all inputs are set to 1.

Gain Error

Gain error is the difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1, minus the output when all inputs are set to 0. The ideal gain is calculated using the measured V_{REFIO}. Therefore, the gain error does not include effects of the reference.

Output Compliance Voltage

Output compliance voltage is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or break-down, resulting in nonlinear performance.

Temperature Drift

Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection

Power supply rejection is the maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time

Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse

Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in picovolt-seconds (pV-sec).

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Noise Spectral Density (NSD)

Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

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Figure 1 is a block diagram of the AD9106. The AD9106 has four 12-bit current output DACs.

The DACs use a single common voltage reference. An on-chip band gap reference is provided. Optionally, an off-chip voltage reference can be used. Full-scale DAC output current, also known as gain, is governed by the current, I_{REFx}. I_{REFx} is the current that flows through each I_{REFx} resistor. Each DAC has its own I_{REFx} set resistor. These resistors can be on or off chip at the discretion of the user. When on-chip R_{SETx} resistors are in use, DAC gain accuracy can be improved by employing the AD9106 built in automatic gain calibration capability. Automatic calibration can be used with the on-chip reference or an external REFIO voltage. See the Automatic IOUTFSx Calibration section for a procedure for automatic gain calibration.

The power supply rails for the AD9106 are AVDDx for the analog circuits, CLKVDD/CLDO for the clock input receiver, and DVDD/DLDO1/DLDO2 for the digital I/O and for the on-chip digital data path. AVDDx, DVDD, and CLKVDD can range from 1.8 V to 3.3 V nominal. DLDO1, DLDO2, and CLDO operate at 1.8 V. If DVDD = 1.8 V, DLDO1 and DLDO2 must both be connected to DVDD, with the on-chip LDOs disabled. All three supplies are provided externally in this case. Likewise, if CLKVDD = 1.8 V, CLDO must be connected to CLKVDD, with the on-chip LDO disabled.

Digital signals input to the four DACs are generated by on-chip digital waveform generation resources. From a dedicated digital data path, 12-bit samples are input to each DAC at the CLKP/CLKN sample rate. The data path of each DAC includes gain and offset corrections and a digital waveform source selection multiplexer. Waveform sources are SRAM, direct digital synthesizer (DDS), DDS output amplitude modulated by SRAM data, a sawtooth generator, DC constant, and a pseudorandom sequence generator.

The waveforms output by the source selection multiplexer have programmable pattern characteristics. The waveforms can be set up to be continuous pulsed (fixed pattern period and start delay within each pattern period), or finite pulsed (a set number of pattern periods are output, then the pattern stops). Pulsed waveforms (finite or continuous) have a programmed pattern period and start delay. The waveform is present in each pulse period following the global (applies to all four DACs) programmed pattern period start and the start delay of each DAC.

An SPI port enables loading of data into SRAM and programming of all the control registers inside the device.

SPI PORT

The AD9106 provides a flexible, synchronous serial communications (SPI) port that allows easy interfacing to application specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and industry-standard microcontrollers. The interface allows read/write access to all registers that configure the AD9106 and to the on-chip SRAM. Its data rate can be up to the SCLK clock speed shown in Table 3 and Table 4.

The SPI interface operates as a standard synchronous serial communication port. Chip Select ($\overline{CS}$) is an active low chip select pin. When $\overline{CS}$ is active low, SPI address and data transfer begins on the SCLK rising edge. The first bit coming on SDIO is a read/write indicator (high for read, low for write). The next 15 bits are the initial register address.

For multiple consecutive register write/read operations in the 0x00 to 0x60 address space, the SPI port automatically decrements the register address if $\overline{CS}$ stays low beyond the first data-word, allowing writes to or reads from a set of contiguous addresses. Note that 0x60 must be used as the starting address for this to work. In this mode, there is no provision to choose the beginning and ending addresses to write. Refer to the SRAM section on how to access the SRAM.

Table 12. Command Word

MSB							LSB
DB15	DB14	DB13	DB12	...	DB2	DB1	DB0
R/$\overline{W}$	A14	A13	A12	...	A2	A1	A0

When the first bit of the command byte is a logic low (R/$\overline{W}$ bit = 0), the SPI command is a write operation. In this case, SDIO remains an input (see Figure 31 and Figure 33). When the first bit of the command byte is a logic high (R/$\overline{W}$ bit = 1), the SPI command is a read operation. In this case, data is driven out of the SDIO (see Figure 32).

The SPI interface has a provision for 4-wire (default) or 3-wire interface set in Bit 14 (SPI3WIRE) and Bit 1 (SPI3WIREM) in SPICONFIG (Register 0x00). In 4-wire SPI interface mode (see Figure 33), the AD9106 acts as the responder, whereas the FPGA (such as the SDP-K1) acts as the controller. Data is read from SDO (Pin 7), and data is written by the controller through SDIO (Pin 2). The SPI communication finishes after $\overline{CS}$ goes high.
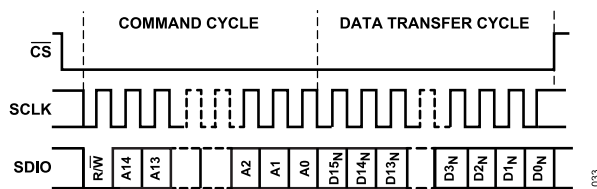
Figure 31. Serial Register Interface Timing, MSB First Write, 3-Wire SPI
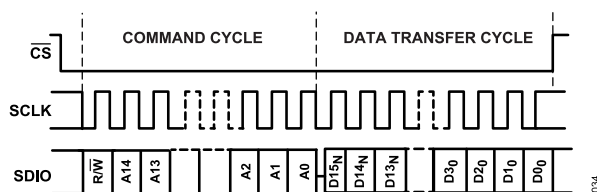
Figure 32. Serial Register Interface Timing, MSB First Read, 3-Wire SPI

THEORY OF OPERATION
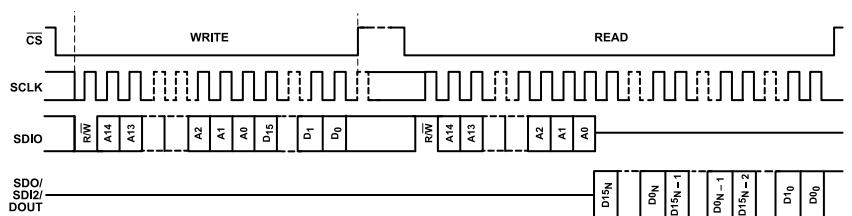
Figure 33. Serial Register Interface Timing, MSB First Write, 4-Wire SPI

Configuration Register Update Procedure

Most SPI accessible registers are double buffered. An active register set controls the operation of the AD9106 during pattern generation, while a set of shadow registers stores updated register values. Register configuration updates can be written at any time on the shadow registers. After SPI configuration update is complete, Bit 0 in RAMUPDATE (Register 0x1D) must be set to 1 to arm the register set for transfer from shadow registers to active registers. This is required regardless of the state of the pattern generator in PAT_STATUS (Register 0x1E, Bit 1).

The RAMUPDATE applies to all SPI settings but does not apply to the 4096 × 12-bit SRAM registers. Refer to the SRAM section for the SRAM update procedure. Because of the double buffer configuration, performing an SPI read operation returns the values in the shadow registers, not the active registers.

DAC TRANSFER FUNCTION

The AD9106 DACs provides four differential current outputs: IOUTP1/IOUTN1 to IOUTP4/IOUTN4. Digital waveforms, generated on-chip for input to the four DACs, use a two's complement number system. The sign bit of each digital waveform word is inverted immediately prior to input to each DAC core. The DACx Input Code variable in Equation 1 and Equation 2 uses an offset binary number system (two's complement with the sign bit inverted).

The DAC output current equations are as follows:

$$IOUTPx = I_{OUTFSx} \times DACx \text{ } Input \text{ } Code/2^{12} \quad (1)$$

$$IOUTNx = I_{OUTFSx} \times ((2^{12} - 1) - DACx \text{ } Input \text{ } Code)/2^{12} \quad (2)$$

where:

DACx Input Code = 0 to $2^{12} - 1$

$$I_{OUTFSx} = 32 \times I_{REFx} \quad (3)$$

$$I_{REFx} = V_{REFIO}/R_{SETx} \quad (4)$$

When using on-chip R_{SETx} resistors, DAC gain accuracy can be improved by employing the built-in automatic gain calibration feature of the device (see Automatic IOUTFSx Calibration section).

Analog Current Outputs

Optimum linearity and noise performance of DAC outputs can be achieved when they are connected differentially to an amplifier or a transformer. In these configurations, common-mode signals at the DAC outputs are rejected.

The output compliance voltage specifications listed in Table 1 and Table 2 must be adhered to for the performance specifications in those tables to be met.

SETTING DAC GAIN (I$_{OUTFSX}$)

I_{OUTFSx} is the full-scale current or DAC gain set independently for each DAC. I_{REFx} is the current that flows through the I_{REFx} resistor. I_{REFx} resistors can be on or off chip at the discretion of the user.

As expressed in Equation 3 and Equation 4, DAC gain (I_{OUTFSx}) is a function of the reference voltage at the REFIO terminal and the R_{SETx} for each DAC.

Voltage Reference

The AD9106 contains an internal 1.0 V nominal band gap reference, V_{BG}. By default, the on-chip reference is powered up and ready to be used. When using the on-chip reference, the REFIO terminal needs to be decoupled to AGND using a 0.1 µF compensation capacitor as shown in Figure 34.

Alternatively, the on-chip reference can be replaced by a more accurate off-chip reference. To apply external reference, set REF_EXT in POWERCONFIG (Register 0x01, Bit 4) to Logic 1 then apply the external reference to the REFIO pin. In this case, the 0.1 µF capacitor is not required. The internal reference can be directly overridden by the external reference.

When using an external reference, it is recommended to power down the internal reference to lessen power consumption. To do so, set the REF_PDN field in POWERCONFIG (Register 0x01, Bit 5) to Logic 1. An external reference can provide tighter reference voltage tolerances and/or lower temperature drift than the on-chip band gap. Table 13 summarizes reference connections and programming.

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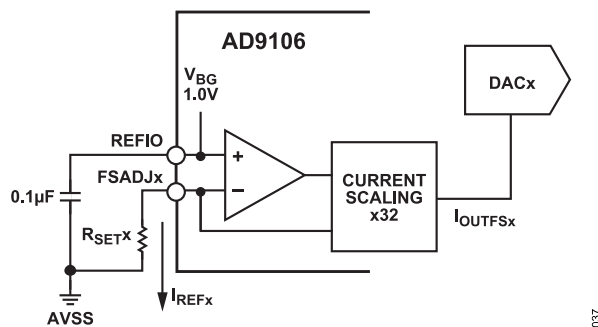
Figure 34. On-Chip Reference with External R_{SETx} Resistor

Table 13. Reference Operation

Reference Mode	REFIO Pin	Register Setting
Internal	Connect 0.1 µF capacitor	Register 0x01, Bit 4 = 0 (default)
External	Connect off-chip reference	Register 0x01, Bit 4 = 1

Programming Internal V_{REFIO}

When the internal voltage reference is in use, the BGDR field in REFADJ (Register 0x03, Bits[5:0]) adjusts the V_{REFIO} level. This adjustment adds or subtracts up to 20% from the nominal band gap voltage on REFIO. The voltage across the FSADJx resistor tracks this change. As a result, I_{REFx} varies by the same amount.

Figure 35 shows V_{REFIO} vs. BGDR code for an on-chip reference with a voltage (BGDR = 0x00) of 1.04 V. The V_{REFIO} voltage at BGDR = 0x00 can vary over the internal reference voltage range shown in Table 1 and Table 2 from chip to chip. The BGDR scaling is 6.25 mV per LSB, and the BGDR code is in two's complement format.
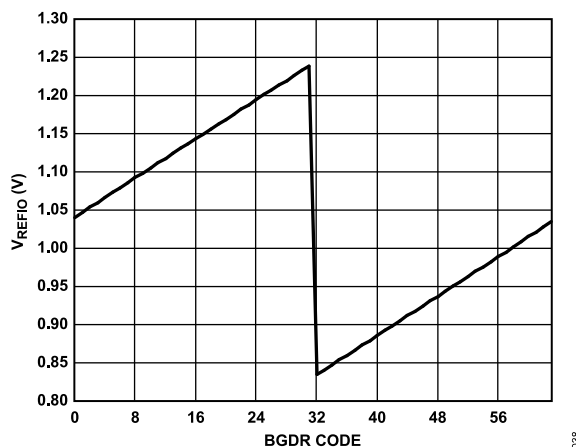
Figure 35. Typical V_{REF} Voltage vs. BGDR Code

R_{SETx} Resistors

R_{SETx} in Equation 4 for each DAC can be an internal resistor or a board level resistor of the user choosing connected to the appropriate FSADJx terminal.

To make use of the on-chip R_{SETx} resistors, set DACx_RSET_EN to Logic 1 in Bit 15 of Register 0x0C (DAC1), Register 0x0B (DAC2), Register 0x0A (DAC3), and Register 0x09 (DAC4). Use Bits[4:0] of those registers to manually program values for the on-chip R_{SETx} associated with each DAC. Bitfield [4:0] is set to 0x0A by default which programs R_{SETx} value to 8 kΩ. It can be adjusted from 4 kΩ to 16 kΩ with a resolution of 800 Ω.

Automatic I_{OUTFSx} Calibration

Many applications require tight DAC gain control. The AD9106 provides an automatic I_{OUTFSx} calibration procedure used with on-chip R_{SETx} resistors only. The voltage reference, V_{REFIO}, can be an on-chip reference or an off-chip reference. The automatic calibration procedure performs a fine adjustment of each internal R_{SETx} value and each current I_{REFx}.

When using automatic calibration, the following board level connections are required:

1. Connect FSADJ1 (Pin 25) and FSADJ2/CAL_SENSE (Pin 24) together.
2. Install a resistor between FSADJ2/CAL_SENSE (Pin 24) and GND. The value of this resistor must be R_{CAL_SENSE} = 32 × V_{REFIO}/I_{OUTFS}, where I_{OUTFS} is the target full-scale current for all four DACs.

Automatic calibration uses an internal clock. This calibration clock, described in Equation 5, is equal to the DAC clock divided by the division factor chosen in CAL_CLK_DIV (Register 0x0D, Bits[2:0]). Each calibration cycle is between 4 and 512 DAC clock cycles, depending on the value of CAL_CLK_DIV. The frequency of the calibration clock should be less than 500 kHz.

$$Calibration\ Clock = f_{CLKP/CLKN}/2^{(2+CAL\_CLK\_DIV)} \qquad (5)$$

To perform an automatic calibration, follow these steps:

1. Set the calibration ranges in DACxRANGE (Register 0x08, Bits[7:0]) and COMP_CAL_RNG (Register 0x0D, Bits[5:4]) to their minimum values to allow best calibration.
2. Enable the calibration clock bit, CAL_CLK_EN (Register 0x0D, Bit 3).
3. Set the divider ratio for the calibration clock by setting CAL_CLK_DIV (Register 0x0D, Bits[2:0]). See Table 29 for the clock divider values. The default is 512.
4. Set CAL_MODE_EN (Register 0x0D, Bit 6) to Logic 1.
5. Set START_CAL (Register 0x0E, Bit 0) to Logic 1 to begin the calibration of the comparator, R_{SETx}, and gain.
6. The CAL_MODE flag (Register 0x0D, Bit 7) goes to Logic 1 while the device is calibrating. The CAL_FIN flag (Register 0x0E, Bit 1) goes to Logic 1 when the calibration is complete.
7. Set START_CAL (Register 0x0E, Bit 0) to Logic 0.
8. After calibration, verify that the overflow and underflow flags (Register 0x0D, Bits[14:9]) are not set. If they are, change the

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corresponding calibration range to the next larger range and begin again at Step 5.

9. If no flag is set, read the values of DACx_RSET_CAL (Bits[12:8]) in DACxRSET (Registers 0x09 to 0x0C) and DACx_GAIN_CAL (Bits[14:8]) in DACxAGAIN (Registers 0x04 to 0x07), then write them into their corresponding DACxRSET (Bits[4:0]) and DACxAGAIN (Bits[6:0]) register fields.

10. Reset CAL_MODE_EN (Register 0x0D, Bit 6) and the calibration clock bit, CAL_CLK_EN (Register 0x0D, Bit 3) to Logic 0 to disable the calibration clock.

11. Set CAL_MODE_EN (Register 0x0D, Bit 6) to Logic 0 to set the R_{SETx} and gain control muxes to normal operation mode.

12. Disable the calibration clock bit, CAL_CLK_EN.

To reset the calibration, either pulse CAL_RESET (Register 0x0D, Bit 8) to Logic 1 then Logic 0, pulse $\overline{RESET}$ (Pin 9), or pulse the RESET bits in SPICONFIG (Register 0x00, Bit 13 and Bit 2).

CLOCK INPUT

For optimum DAC performance, the AD9106 clock input signal pair (CLKP/CLKN) must be a very low jitter, fast rise time differential signal. The clock receiver generates its own common-mode voltage, requiring these two inputs to be ac-coupled.

Figure 36 to Figure 39 are the preferred methods for clocking the AD9106. Figure 36 shows the recommended interface to a number of Analog Devices, Inc., low voltage differential signaling (LVDS) clock drivers that work well with the AD9106, where a 100 Ω termination resistor and two 0.1 μF coupling capacitors are used. Figure 37 shows an interface to an Analog Devices differential positive emitter coupled logic (PECL) driver, while Figure 38 shows a single-ended-to-differential converter using a balun driving CLKP/CLKN.

In applications where the analog output signals are at low frequencies, the AD9106 clock input can be driven with a single-ended complementary metal oxide semiconductor (CMOS) signal. Figure 39 shows such an interface. CLKP is driven directly from a CMOS gate, and CLKN is bypassed to ground with a 0.1 μF capacitor in parallel with a 39 kΩ resistor. The optional resistor is a series termination.
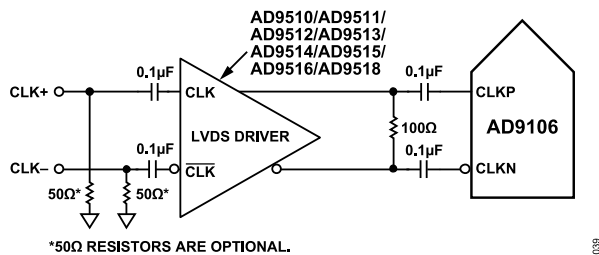
Figure 36. Differential LVDS Clock Input
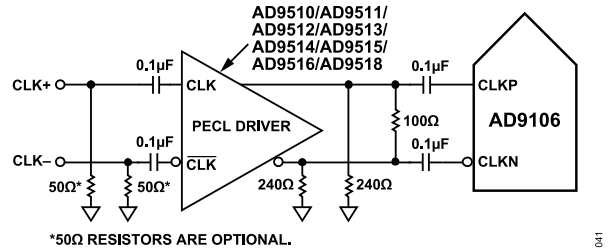
Figure 37. Differential PECL Sample Clock
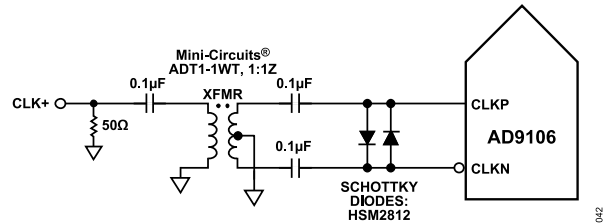
Figure 38. Transformer Coupled Clock
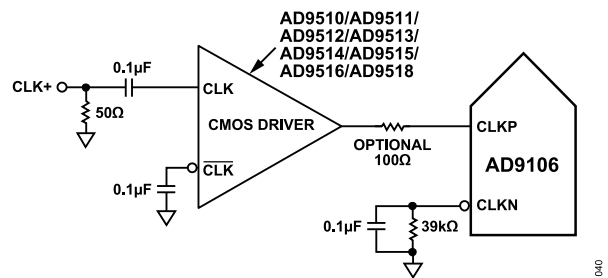
Figure 39. Single-Ended 1.8 V CMOS Sample Clock

DAC Output Clock Edge

Each of the four DACs can be configured independently to output samples on the rising or falling edge of the CLKP/CLKN clock input by configuring DACx_INV_CLK in CLOCKCONFIG (Register 0x02, Bits[3:0]). This functionality sets the DAC output timing resolution at $1/(2 \times f_{CLKP/CLKN})$.

GENERATING SIGNAL PATTERNS

The AD9106 can generate two types of signal patterns under the control of its programmable pattern generator.

▶ Periodic pulse train waveforms that repeat indefinitely, which are waveforms that are output once during each pattern period. Pattern periods occur one after the other so long as the pattern generator is in the pattern ON state.

▶ Periodic pulse train waveforms that repeat a finite number of times, which are similar to those that repeat indefinitely except that the waveforms are output during a finite number of consecutive pattern periods.

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Pattern Generator Programming

Figure 40 shows periodic pulse train waveforms as seen at the output of each DAC. The four DACs generate the same digital signal stored in SRAM multiplied by the DACx Digital Gain factor (see the DACx Digital Gain Multiplier section). The SRAM data is read using each DACx address counter simultaneously (see SRAM section). The waveforms are generated at every pattern period. Note that the pattern period is common among all DACs. See the Setting Pattern Period section on how to set the pattern period.
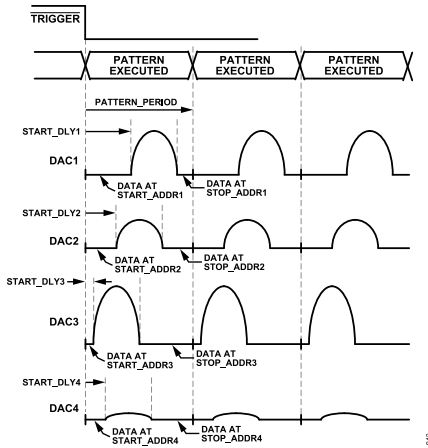
Figure 40. Periodic Pulse Trains Output on All DACx
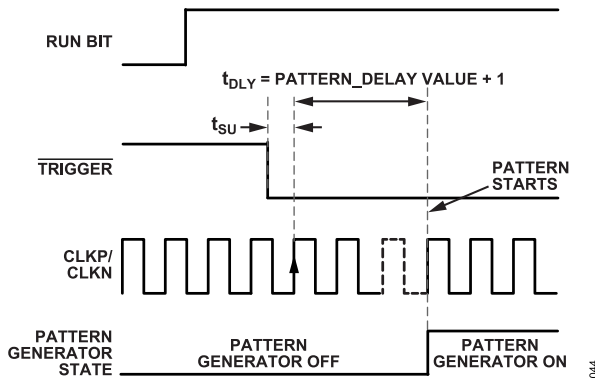
Figure 41. Trigger Initiated Pattern Start with Pattern Delay

Setting Waveform Start Delay

Each DAC channel has its own start delay which is the delay between the start of the pattern period and the start of the wave-form. This delay is set in START_DLYx in Register 0x5C (DAC1), Register 0x58 (DAC2), Register 0x54 (DAC3), and Register 0x50 (DAC4). To define the START_DELAYx registers as a repetitive delay for each pattern, PATTERN_RPT (Register 0x1F, Bit 0) and TRIG_DELAY_EN (Register 0x44, Bit 1) must be set to Logic 0.

The waveform start delay base is programmed in the START_DE-LAY_BASE field in PAT_TIMEBASE (Register 0x28, Bits[3:0]). START_DELAY_BASE determines how many CLKP/CLKN cycles there are per START_DELAYx LSB.
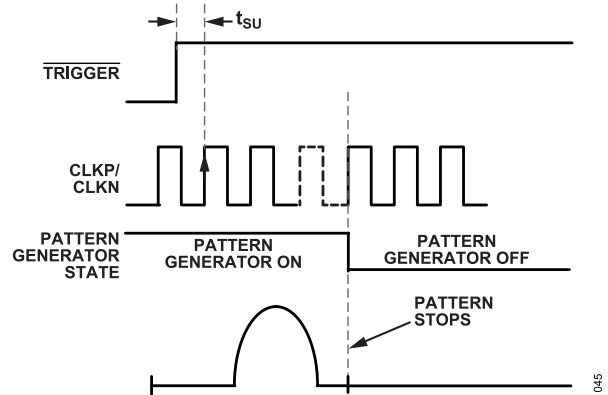
Figure 42. Trigger Rising Edge Initiated Pattern Stop
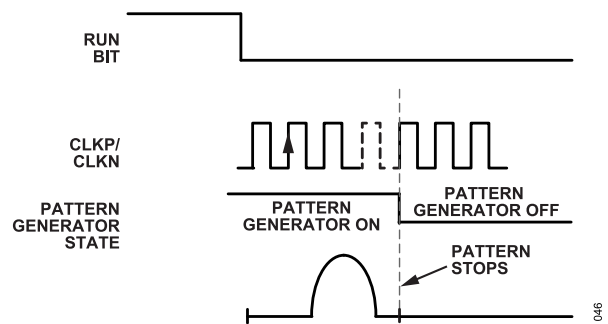
Figure 43. RUN Bit Driven Pattern Stop

Setting Pattern Period

Two register bit fields set the length of the pattern period. First is PAT_PERIOD (Register 0x29). The second is the PAT_PERIOD_BASE field in PAT_TIMEBASE (Register 0x28, Bits[7:4]) which sets the number of CLKP/CLKN cycles per PATTERN_PERIOD LSB. The longest pattern period available is $65535 \times 16/f_{CLKP/CLKN}$. The pattern period length can be determined through Equation 6 and Equation 7.

$$Pattern\ period = PAT\_PERIOD \times PATTERN\_PERIOD\ LSB \qquad (6)$$

where

$$PATTERN\_PERIOD\ LSB = PAT\_PERIOD\_BASE / f_{CLKP/CLKN} \qquad (7)$$

Note that the pattern period must be at least equal to the sum of START_DELAYx and the waveform length to generate the complete waveform for that DAC channel. If the pattern period set is less than this, the generated waveform appears trimmed and the error flag PERIOD_SHORT_ERR (Register 0x60, Bit 2) toggles high.

RUN Bit, Trigger Terminal, and Pattern Bit (Read Only)

Both the RUN bit in PAT_STATUS (Register 0x1E, Bit 0) and the Trigger terminal (Pin 32) are required to generate a pattern out of the AD9106. The RUN bit activates the pattern generator, whereas the falling edge on the Trigger terminal starts the generation of a pattern.

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Setting the RUN bit activates the AD9106 for pattern generation, whereas clearing it shuts down the pattern generator (see Figure 43). If the RUN bit is set, the falling edge on the Trigger terminal starts pattern generation after a short delay. As shown in Figure 41, the pattern generator state turns ON after a number of CLKP/CLKN cycles following the falling edge of Trigger. This delay is programmed in PATTERN_DLY (Register 0x20). Consequently, a rising edge on the Trigger terminal terminates pattern generation after a short delay (see Figure 42).

So long as the RUN bit is enabled last after writing to all other SPI registers, then pattern generation is successful when a falling edge is provided to the Trigger terminal.

The read-only Pattern bit (Register 0x1E, Bit 1) indicates whether the pattern generator is ON or OFF. A reading of 1 indicates that the pattern generator is ON, whereas a reading of 0 indicates the pattern generator is OFF.

DACX INPUT DATA PATH

Each of the four DACs has its own digital data path. Timing in the DACx data paths is governed by the pattern generator. Each DACx data path includes a waveform selector, a waveform repeat controller, RAM output and DDS output multiplier (RAM output can amplitude modulate DDS output), DDSx cycle counter, DACx digital gain multiplier, and a DACx digital offset summer. DACx input data path use a two's complement number system.

DACx Digital Gain Multiplier

On its way into each DACx, the digital waveform samples are multiplied by a 12-bit gain factor programmed in the DAC Digital Gain Registers (DACxDGAIN) in Register 0x32 to Register 0x35. The format of the register is in two's complement with a range of ±2.0 (unitless). The scaling of digital gain is $4/2^{12}$.

Although the digital data can be multiplied up to a magnitude of 2, the DAC output current is limited to the range 0 to I_{OUTFSx}. If the resulting DAC input code (DACx digital data times digital gain plus DAC offset) exceeds full-scale, the output is clipped at I_{OUTFSx}. If the resulting DAC input code is lower than negative full-scale, the output is clipped at 0 A.

DACx Digital Offset Summer

DACx input samples are summed with a 12-bit DC offset value programmed in the DAC Digital Offset registers (DACxDOF) in Registers 0x22 to Register 0x25. The format of the register is in two's complement with a range of ±50% of the DAC output current. The scaling of digital offset is $1/2^{12}$.

Like in DACx Digital Gain, if the resulting DAC input code with the digital offset exceeds full-scale, the output is clipped at I_{OUTFSx}. If the resulting DAC input code is lower than negative full-scale, the output is clipped at 0 A.

DACx Pattern Repeat Controller

The PATTERN_RPT bit in PAT_TYPE (Register 0x1F, bit 0) controls whether the pattern output repeats for infinite number of times (periodic pulse train repeats indefinitely) or repeats a number of consecutive times defined by the DACx_REPEAT_CYCLE fields in Register 0x2A and Register 0x2B. The latter are periodic pulse trains that repeat a finite number of times.

DACx Waveform Selectors

Waveform selector inputs are:

► Prestored waveform
  ► Pulsed, phase shifted DDS sine wave output
  ► Sawtooth generator output
  ► Pseudorandom sequence generator output.
  ► DC constant generator output.
► RAM loaded vectors (SRAM)
► Prestored waveform amplitude modulated by RAM output

Waveform selection for each DACx is made by programming WAVx_yCONFIG (Register 0x26 and Register 0x27).

DOUT FUNCTION

In applications where AD9106 DACs drives high voltage amplifiers, such as in ultrasound transducer array element driver signal chains, it can be useful to turn on and off each amplifier at precise times relative to the waveform generated by each AD9106 DAC. The SDO/SDI2/DOUT terminal can be configured to provide this function. One amplifier on/off strobe can be provided for all four DACs.

The SPI interface needs to be configured in 3-wire mode (see Figure 31 and Figure 32) by setting Bit 14 (SPI3WIRE) and Bit 3 (SPI3WIREM) in SPICONFIG (Register 0x00). When Bit 11 (SPI_DRV) and Bit 4 (SPI_DRVM) in SPICONFIG are set to Logic 1, the SDO/SDI2/DOUT terminal provides the DOUT function.

Pattern Generator Controlled DOUT

Figure 44 depicts the rising edge of a pattern generator controlled DOUT pulse, whereas Figure 45 shows the falling edge. The pattern generator controlled DOUT pulse is set up by setting DOUT_MODE bit in DOUT_CONFIG (Register 0x2D, Bit 4) to Logic 1. Then, the start delay is programmed in DOUT_START (Register 0x2C) and the stop delay is programmed in DOUT_STOP in DOUT_CONFIG (Register 0x2D, Bits[3:0]).

DOUT goes high after CLKP/CLKN cycles stated in DOUT_START after the falling edge of the signal input to the Trigger terminal (Pin 32). DOUT stays high as long as a pattern is being generated. DOUT goes low after CLKP/CLKN cycles stated in DOUT_STOP after the clock edge that causes pattern generation to stop.

THEORY OF OPERATION
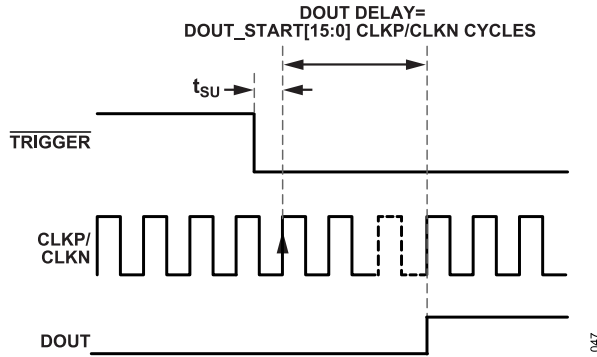
Figure 44. DOUT Start Sequence
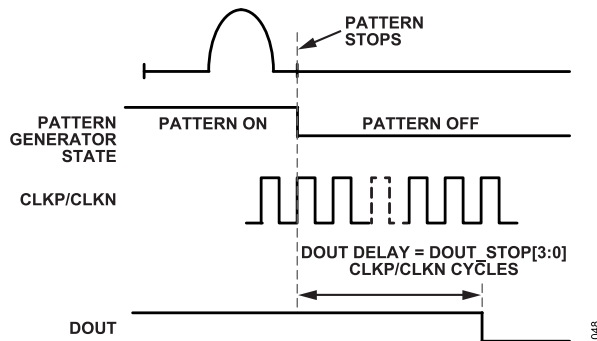
Figure 45. DOUT Stop Sequence

Manually Controlled DOUT

If DOUT_MODE is set to Logic 0, DOUT can be turned on or off using DOUT_VAL (Register 0x2D, Bit 5).

DIRECT DIGITAL SYNTHESIZER (DDS)

The DDS generates a single frequency sine wave that can be output on any of the four DACx. The DDS is a global shared signal resource. It can generate one sinusoid at a frequency determined by its tuning word input. The tuning word is 24 bits wide, and the resolution of DDS is $f_{CLKP/CLKN}/2^{24}$. Equation 8 describes the DDS output frequency as follows:

$$f_{OUT,DDS} = DDS\_TW \times f_{CLKP/CLKN}/2^{24} \qquad (8)$$

The DDS tuning word can be programmed in one of two ways. First, for a fixed frequency, DDSTW_MSB (Register 0x3E, Bits[15:0]) and DDSTW_LSB (Register 0x3F, Bits[15:8]) are programmed with a constant and the output follows Equation 8.

Second, when the frequency of the DDS needs to change within each pattern period, a sequence of values stored in SRAM is combined with a selection of DDSTW_MSB bits to form the tuning word (see the Clock Selection for Incrementing Pattern Generation Mode—SRAM Address Counters).

DACx, Number of DDS Cycles

Each DACx input data path establishes the pulse width of the sine wave output from the single common DDS in a finite number of sine wave cycles. The cycle counts are programmed in DDS_CYCx in Register 0x5F (DAC1), Register 0x5B (DAC2), Register 0x57 (DAC3), and Register 0x53 (DAC4).

For the values in those registers to take effect, the programmable pattern generator must generate waveforms that repeat a finite number of times. This is done by setting the WAVE_SELx field in WAVx_yCONFIG (Register 0x26 and Register 0x27) to 0x2.

DDS Phase Offset for Each DACx

The single shared DDS has an output for each DACx data path that includes a programmable phase shifter. The format of the register for the DDS phase offset Register is in two's complement with a range of 360°.

The phase shift is programmed in one of two ways. The first way is using DDSx_PW (Register 0x40 to Register 0x43). The DDSx_PW registers can be used to adjust the phase offset of a DDS-generated waveform only. It does not affect other prestored waveforms and SRAM-generated waveforms. The scaling or resolution of DDSx_PW is $360°/2^{16}$-1. Equation 9 describes the phase offset from DDSx_PW.

$$DDSx_{Phase\ offset} = DDSx\_PW \times 360°/(2^{16} - 1) \qquad (9)$$

The second way to program the DDS phase offset is by using PHASE_MEM_ENx (Register 0x45, Bit 9) which modifies the DDS phase offset based on the value stored in SRAM.

SRAM

The AD9106 contains an internal memory for storing data vectors which can be used for arbitrary waveform generation. The 4096 × 12-bit SRAM (SPI port address space located in 0x6000 to 0x6FFF) can contain any signal samples, such as amplitude modulation patterns, lists of DDS tuning words, or lists of DDS output phase offset words. The SRAM data follows a two's complement format, and SRAM data word is left justified. To output from SRAM, set the WAVE_SELx fields in WAVx_yCONFIG (Register 0x26 and Register 0x27) to 0.

SRAM can be accessed using any of the SPI operating modes shown in Figure 31 through Figure 33. Using the SPI modes of operation shown in Figure 31 and Figure 32 the entire SRAM can be written in (2 + 2 × 4096) × 8/f_{SCLK} seconds.

The SRAM is a shared signal generation resource. Data from the 4096 × 12-bit SRAM can be used to generate signals for all four DACs. Each DACx data path has its own SRAM address counter, and each address counter has its own START_ADDRx and STOP_ADDRx (can be anywhere from 0x000 to 0xFFF). During each pattern period, data is read from SRAM after the START_DE-LAYx period and while each address counter is incrementing. Refer

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to Waveform Generation Setups and Sample Sequence for sample register configurations of generating output from SRAM.

The SRAM length being written must be an even number if TRIG_DELAY_EN (Register 0x44, Bit 1) = 1. This requirement implies that the START_ADDRx and STOP_ADDRx cannot both be even or both be odd. Only one of the addresses can be even, while the other address must be odd.

Reading and Writing to On-Chip SRAM

Reading and writing is done directly in SRAM as opposed to SPI registers which implement a double buffer configuration (see the Configuration Register Update Procedure). Data is written to and read from the memory via the SPI port as long as the SRAM is not actively engaged in pattern generation (RUN bit in Register 0x1E = 0). Set up PAT_STATUS (Register 0x1E) to read and write from SRAM.

To write to any SRAM address, set PAT_STATUS to 0x04 as follows:

▶ BUF_READ (Bit 3) = 0
▶ MEM_ACCESS (Bit 2) = 1
▶ RUN (Bit 0) = 0

To read data from any SRAM address, set PAT_STATUS to 0x0C as follows:

▶ BUF_READ (Bit 3) = 1
▶ MEM_ACCESS (Bit 2) = 1
▶ RUN (Bit 0) = 0

For multiple consecutive write operations in the SRAM address space, the SPI port automatically decrements the register address (0x6FFF down to 0x6000) if $\overline{CS}$ stays low beyond the first data-word. The autodecrement feature does not apply to consecutive read operations from the SRAM.

Double SPI for Write for SRAM
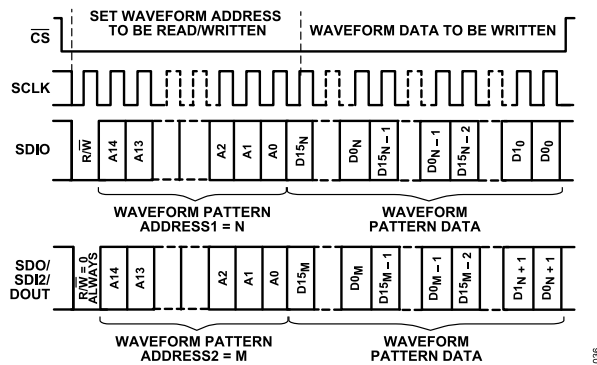
Figure 46. Double SPI Write of SRAM Data

The time to write data to an SRAM segment can be reduced by half using the SPI access mode shown in Figure 46. The SDO/

SDI2/DOUT line becomes a second serial data input line, doubling the achievable update rate of the on-chip SRAM. SDO/SDI2/DOUT is write only in this mode. The entire SRAM can be written in $(2 + 2 \times 4096) \times 8/(2 \times f_{SCLK})$ seconds.

Clock Selection for Incrementing Pattern Generation Mode—SRAM Address Counters

The SRAM address counters can be programmed to be incremented by either CLKP/CLKN (default) or by the rising edge of the DDSx output MSB. The DDS_MSB_ENx bit in DDSx_CONFIG (Registers 0x45) makes this selection.

For example, when generating SRAM waveform samples or DDS amplitude modulation samples, the SRAM address counters must be incremented by CLKP/CLKN (default). On the other hand, when generating a a list of DDS tuning words (such as a chirp waveform), the SRAM address counters can be incremented by either CLKP/CLKN (default) or by the rising edge of the DDSx output MSB. In this case, each frequency setting dwells for one DDS output sine wave cycle.

SAWTOOTH GENERATOR

Each DACx data path has separate sawtooth signal generators. When sawtooth is selected in any of the PRESTORE_SELx fields in WAVx_yCONFIG (Register 0x26 and Register 0x27), the appropriate sawtooth generator is connected to the desired DACx digital data path.

Sawtooth types, as shown in Figure 47, are selected using the SAW_TYPEx fields in SAWx_yCONFIG (Register 0x36 and Register 0x37). A positive sawtooth waveform ramps up from negative full-scale to positive full-scale in 1 LSB steps, while a negative sawtooth ramps down in the same manner.

The number of samples per sawtooth waveform step is programmed in each SAW_STEPx field in SAWx_yCONFIG. Each sawtooth waveform step can have up to 63 samples, and the total number of steps of the sawtooth waveform for AD9106 is 2^{14} or 16384. For a triangular waveform, the total number of steps is twice as many.

The sawtooth frequency is determined based on two parameters: the DAC clock input ($f_{CLKP/CLKN}$) and the SAW_STEPx field in SAWx_yCONFIG (Register 0x36 and Register 0x37). Equation 10 to Equation 13 describe the sawtooth frequency equation.
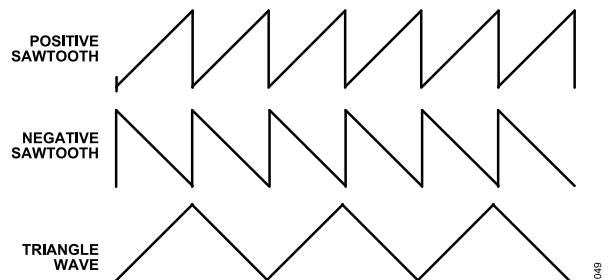
Figure 47. Sawtooth Patterns

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Sawtooth frequency = 1/*Sawtooth Ramp time* (10)

Sawtooth ramp time = $N \times 2^{14} \times$ *Step time* (11)

where:
N = 1 for positive/negative sawtooth.
N = 2 for triangular sawtooth

Step time = *DAC clock period* × *SAW_STEPx* (12)

DAC clock period = $1/f_{CLKP/CLKN}$ (13)

Note that the Sawtooth pattern period is not the same as the Sawtooth Ramp time. The Sawtooth pattern period is calculated based on the Sawtooth Ramp time and the PAT_PERIOD_BASE field in PAT_TIMEBASE (Register 0x28, Bits[7:4]). Refer to Setting Pattern Period section for the pattern period for all other waveforms. Equation 14 describes the Sawtooth pattern period:

$$Sawtooth\ \ Pattern\ \ Period = \frac{Sawtooth\ \ Ramp\ \ time}{PAT\_PERIOD\_BASE} \quad (14)$$

Table 14. Sample Sawtooth Waveforms Configurations

SAW_TYPEx	PAT_PERIOD_BASE	SAW_STEP	Sawtooth Frequency
Ramp-up	1	1	10.986 kHz
Triangular	2	2	2.746 kHz
Ramp-down	2	3	3.662 kHz
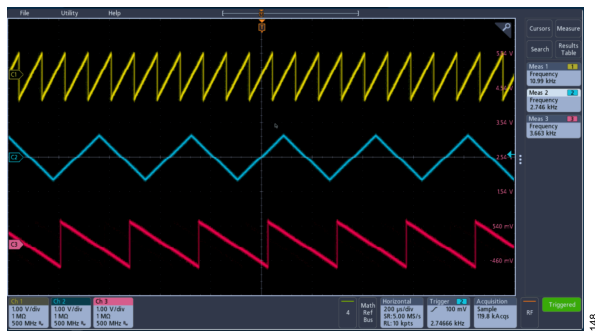
Figure 48. Sample Sawtooth Waveforms

Alternatively, sawtooth waveforms can be generated from SRAM. See the Reading and Writing to On-Chip SRAM section on how to access SRAM. Table 14 provides sample sawtooth configurations for a DAC clock input of 180 MHz (DAC clock period = 5.56 ns), and the sawtooth waveforms are illustrated in Figure 48. The sawtooth frequency is calculated based on Equation 10 to Equation 13.

PSEUDORANDOM SIGNAL GENERATOR

The pseudorandom noise generator generates a noise signal on each DACx output if pseudorandom sequence is selected in any of the PRESTORE_SELx fields in WAVx_yCONFIG (Register 0x26 and Register 0x27). The pseudorandom noise signals are generated as continuous waveforms only.

DC CONSTANT

A programmable DC current between 0.0 and I_{OUTFSx} can be generated on each DACx if constant value is selected in any of the PRESTORE_SELx fields in WAVx_yCONFIG (Register 0x26 and Register 0x27).

DC constant currents are generated as continuous waveform only. The DC current level is programmed by writing to the 12-bit DACx_CONST field in the appropriate DACx_CST (Register 0x2E to Register 0x31).

POWER SUPPLY NOTES

The AD9106 supply rails (AVDD1, AVDD2, DVDD, CLKVDD) are specified in Table 9. The AD9106 includes three on-chip linear regulators (CLDO, DLDO1, DLDO2). The supply rails driven by these regulators operate at 1.8 V. There are two usage rules for these regulators:

▸ When CLKVDD ≥ 2.5 V, the 1.8 V on-chip CLDO regulator can be used. If CLKVDD = 1.8 V, CLDO must be disabled by setting PDN_LDO_CLK in POWERCONFIG (Register 0x01, Bit 8). CLKVDD and CLDO must be strapped together.
▸ When DVDD ≥ 2.5 V, the 1.8 V on-chip DLDO1 and DLDO2 regulators can be used. If DVDD = 1.8 V, DLDO1 and DLDO2 must be disabled by setting PDN_LDO_DIG1 (Register 0x01, Bit 7) and PDN_LDO_DIG2 (Register 0x01, Bit 6) bits in the POWERCONFIG register. DVDD, DLDO1, and DLDO2 must be strapped together.

Power-Down Capabilities

By default, the DAC outputs (IOUTxP and IOUTxN) are at midrange or I_{OUTFSx}/2 during power up. This is also the case when the DACx are idle—before and after pattern generation. POWERCONFIG (Register 0x01) allows the user to place the AD9106 in a reduced power dissipation configuration while the CLKP/CLKN input is running and the power supplies are on. To save power, the DACx can all be put to sleep by setting the DACx_SLEEP bits in POWERCONFIG (Register 0x01, Bits[3:0]).

Clocking of the waveform generator and the DACs can be turned on or off by setting CLK_PDN in CLOCKCONFIG (Register 0x02, Bit 5). Taking these actions places the AD9106 in the power-down mode specified in Table 8.

APPLICATIONS INFORMATION

SIGNAL GENERATION EXAMPLES

Figure 49 shows different waveforms being generated by each DACx. The waveforms are all stored in the 4096 x 12-bit SRAM in different segments. Each waveform is repeated once during each pattern period. In each pattern period, a start delay is executed, then the pattern is read from SRAM.
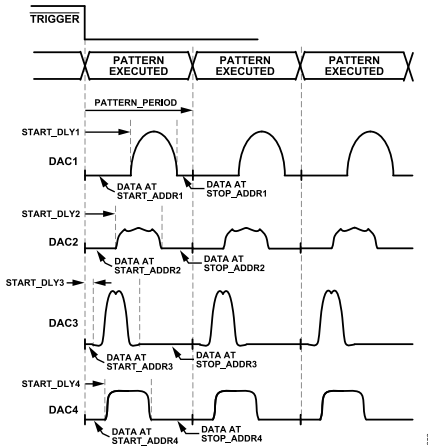
Figure 49. Pattern Using Different Waveforms Stored in SRAM

Figure 50 shows pulsed sine waves generated by each DACx. The DDS generates a sine wave at a programmed frequency based on Equation 8. Each DACx channel is programmed with a start delay and a number of sine wave cycles to output. Figure 51 shows a pulsed sine wave generated by DAC1 and each of the three available sawtooth wave types generated by DAC2 to DAC4 in successive pattern periods with start delay.
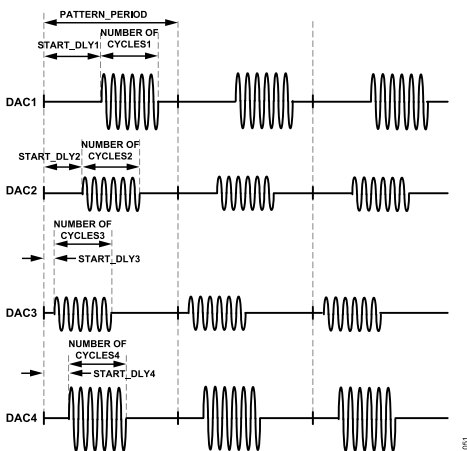
Figure 50. Pulsed Sine Waves in Pattern Periods

Figure 52 shows all DACx outputting sine waves modulated by an amplitude envelope. The sine wave is generated by the DDS, and the amplitude envelope is stored in SRAM. Different start delays and digital gain multipliers are applied by each DACx input data path.

Figure 53 and Figure 54 show the four DACs generating continuous waveforms, one with start delays, and one without.
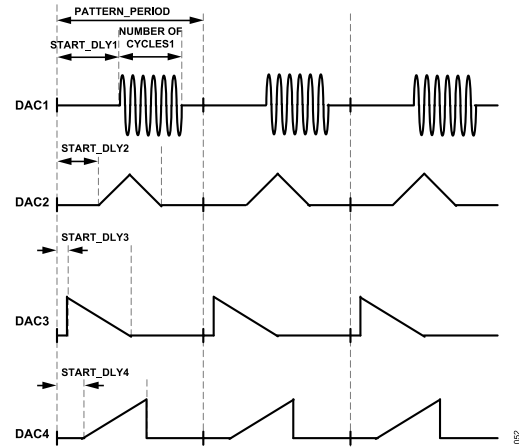
Figure 51. Pulsed Sine Waves and Sawtooth Waveforms in Pattern Periods
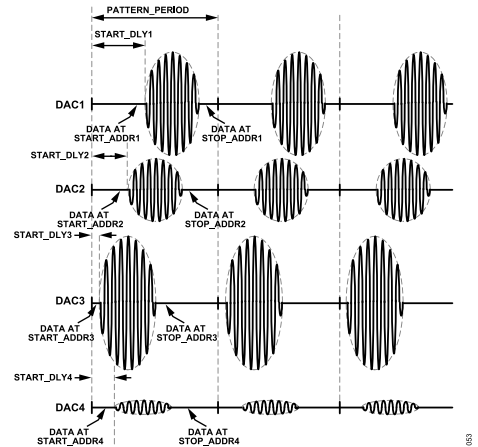
Figure 52. DDS Output Amplitude Modulated by RAM Envelope
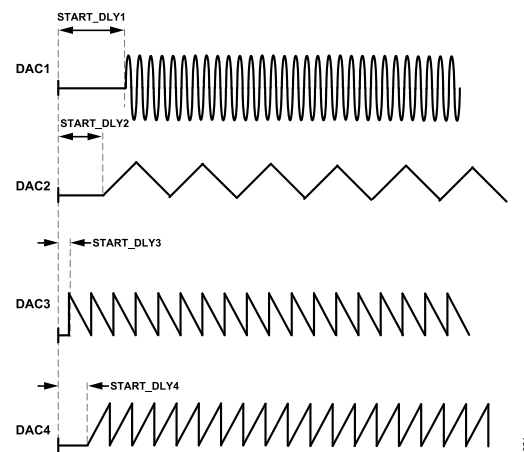
Figure 53. Waveforms with Start Delays

APPLICATIONS INFORMATION
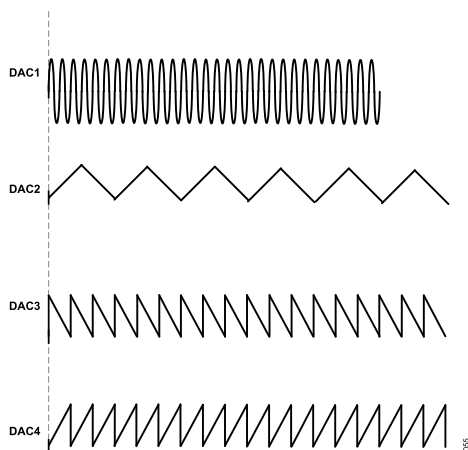
Figure 54. Waveforms Without Start Delays

WAVEFORM GENERATION SETUPS AND SAMPLE SEQUENCE

A sample sequence for generating DDS waveforms is as follows:

1. Set initial values of I/O pins ($\overline{RESET}$, $\overline{TRIGGER}$, and $\overline{CS}$ to Logic 1 (high).
2. Set SPI frequency and mode as preferred.
3. Assert $\overline{RESET}$ (Pin 9) by pulsing from Logic 0 (low) then Logic 1 (high) to reset register values. Deassert $\overline{RESET}$ afterward.
4. Proceed with register read and write for DDS:

   a. Set DDS output frequency in DDSTW_MSB (Register 0x3E, Bits[15:0]) and DDSTW_LSB (Register 0x3F, Bits[15:8]).
   b. (Optional) Set number of DDS cycles in DDS_CYCx. For this, WAVE_SELx in WAVx_yCONFIG must be set to 0x2.
   c. (Optional) Set phase offset for DDS output in DDS_PWx (Register 0x40 to Register 0x43).

5. Write to or read from SPI registers. Update RUN bit and RAMUPDATE bit and the end of the write sequence as follows:

   a. Set waveform select to DDS in WAVx_yCONFIG (Register 0x26 and Register 0x27).
   b. Set DACx digital gain in DACxDGAIN (Register 0x32 to Register 0x35).
   c. (Optional) Set DAC Digital Offset in DACxDOF (Register 0x22 to Register 0x25).
   d. Update RUN bit (Register 0x1E).
   e. Update RAMUPDATE bit (Register 0x1D).

6. Set Trigger terminal (Pin 32) to Logic 0 (low) to start pattern generation.

A sample sequence for generating SRAM waveforms is as follows:

1. Set initial values of I/O pins ($\overline{RESET}$, $\overline{TRIGGER}$, and $\overline{CS}$ to Logic 1 (high).
2. Set SPI frequency and mode as preferred.
3. Assert $\overline{RESET}$ (Pin 9) by pulsing from Logic 0 (low) then Logic 1 (high) to reset register values. Deassert $\overline{RESET}$ afterward.
4. Write data to SRAM. Set PAT_STATUS (Register 0x1E) = 0x04 as follows:

   a. BUF_READ (Bit 3) = 0
   b. MEM_ACCESS (Bit 2) = 1
   c. RUN (Bit 0) = 0
   d. Write left-justified data to SRAM registers (0x6000 to 0x6FFF address space). After writing, disable MEM_ACCESS bit.

5. Read data from SRAM. Set PAT_STATUS (Register 0x1E) = 0x0C as follows:

   a. BUF_READ (Bit 3) = 1
   b. MEM_ACCESS (Bit 2) = 1
   c. RUN (Bit 0) = 0
   d. After reading data from SRAM registers, disable BUF_READ and MEM_ACCESS bits.

6. Write to or read from SPI registers. Update RUN bit and RAMUPDATE bit and the end of the write sequence as follows:

   a. Set waveform select to SRAM in WAVx_yCONFIG (Register 0x26 and Register 0x27).
   b. Set SRAM start and stop addresses (can be anywhere from 0x000 to 0xFFF).
   c. Set DACx digital gain in DACxDGAIN (Register 0x32 to Register 0x35).
   d. (Optional) Set DAC digital offset in DACxDOF (Register 0x22 to Register 0x25).
   e. Update the RUN bit (Register 0x1E).
   f. Update the RAMUPDATE bit (Register 0x1D).

7. Set Trigger terminal (Pin 32) to Logic 0 (low) to start pattern generation.

APPLICATIONS INFORMATION

Programming Examples

For the programming examples (Figure 55 to Figure 60), the register value files and SRAM vectors can be obtained by downloading **EVAL-AD910x Program Files** under the **Code Examples** section from EVAL-AD9106 Software.
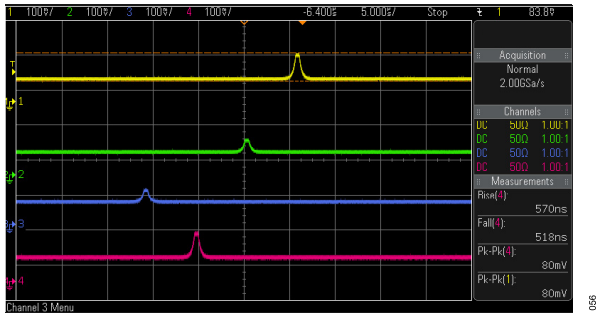
Figure 55. Programming Example 1: Four Gaussian Pulses from an SRAM Vector with Different Start Delay and Varied Digital Gain Settings
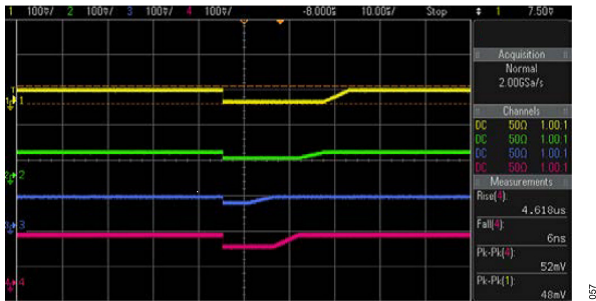
Figure 56. Programming Example 2: Four Pulses generated from an SRAM Vector
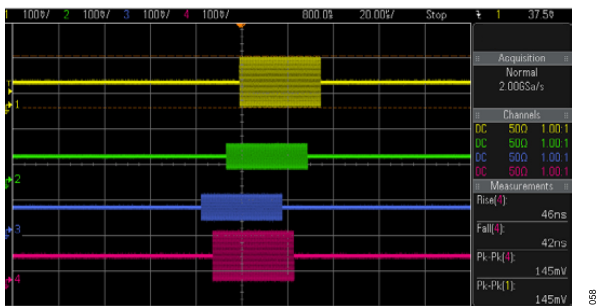
Figure 57. Programming Example 3: Four Pulsed DDS-Generated Sine Waves from a Prestored waveform with Different Start Delay and Digital Gain Settings
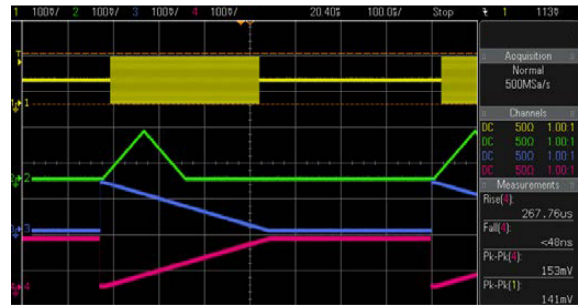
Figure 58. Programming Example 4: Pulsed DDS-Generated Sine Wave and 3 Sawtooth waveforms

Figure 59. Programming Example 5: Four Pulsed DDS-Generated Sine Waves Amplitude modulated by an SRAM Vector with Different Start Delay
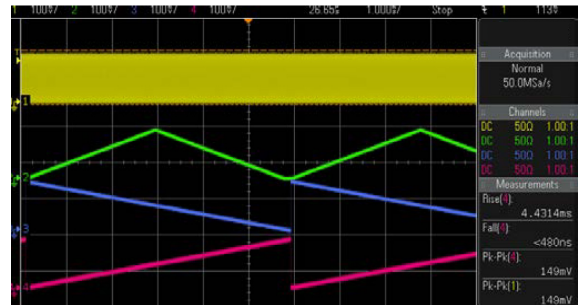
Figure 60. Programming Example 6: DDS-Generated Sine wave and 3 Sawtooth waveforms

REGISTER MAP

Table 15. Register Summary

Addr	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	SPICONFIG	[15:8]	LSBFIRST	SPI3WIRE	RESET	DOUBLESPI	SPI_DRV	DOUT_EN	RESERVED		0x00	RW
		[7:0]	RESERVED		DOUT_ENM	SPI_DRVM	DOUBLESPIM	RESETM	SPI3WIREM	LSBFIRSTM		
0x01	POWERCONFIG	[15:8]	RESERVED				CLK_LDO_STAT	DIG1_LDO_STAT	DIG2_LDO_STAT	PDN_LDO_CLK	0x00	RW
		[7:0]	PDN_LDO_DIG1	PDN_LDO_DIG2	REF_PDN	REF_EXT	DAC1_SLEEP	DAC2_SLEEP	DAC3_SLEEP	DAC4_SLEEP		
0x02	CLOCKCONFIG	[15:8]	RESERVED				DIS_CLK1	DIS_CLK2	DIS_CLK3	DIS_CLK4	0x00	RW
		[7:0]	DIS_DCLK	CLK_SLEEP	CLK_PDN	EPS	DAC1_INV_CLK	DAC2_INV_CLK	DAC3_INV_CLK	DAC4_INV_CLK		
0x03	REFADJ	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED			BGDR						
0x04	DAC4AGAIN	[15:8]	RESERVED	DAC4_GAIN_CAL							0x00	RW
		[7:0]	RESERVED	DAC4_GAIN								
0x05	DAC3AGAIN	[15:8]	RESERVED	DAC3_GAIN_CAL							0x00	RW
		[7:0]	RESERVED	DAC3_GAIN								
0x06	DAC2AGAIN	[15:8]	RESERVED	DAC2_GAIN_CAL							0x00	RW
		[7:0]	RESERVED	DAC2_GAIN								
0x07	DAC1AGAIN	[15:8]	RESERVED	DAC1_GAIN_CAL							0x00	RW
		[7:0]	RESERVED	DAC1_GAIN								
0x08	DACxRANGE	[15:8]	RESERVED								0x00	RW
		[7:0]	DAC4_GAIN_RNG		DAC3_GAIN_RNG		DAC2_GAIN_RNG		DAC1_GAIN_RNG			
0x09	DAC4RSET	[15:8]	DAC4_RSET_EN	RESERVED		DAC4_RSET_CAL					0x0A	RW
		[7:0]	RESERVED			DAC4_RSET						
0x0A	DAC3RSET	[15:8]	DAC3_RSET_EN	RESERVED		DAC3_RSET_CAL					0x0A	RW
		[7:0]	RESERVED			DAC3_RSET						
0x0B	DAC2RSET	[15:8]	DAC2_RSET_EN	RESERVED		DAC2_RSET_CAL					0x0A	RW
		[7:0]	RESERVED			DAC2_RSET						
0x0C	DAC1RSET	[15:8]	DAC1_RSET_EN	RESERVED		DAC1_RSET_CAL					0x0A	RW
		[7:0]	RESERVED			DAC1_RSET						
0x0D	CALCONFIG	[15:8]	REVEDSER	COMP_OFFSET_OF	COMP_OFFSET_UF	RSET_CAL_OF	RSET_CAL_UF	GAIN_CAL_OF	GAIN_CAL_UF	CAL_RESET	0x00	RW
		[7:0]	CAL_MODE	CAL_MODE_EN	COMP_CAL_RNG		CAL_CLK_EN	CAL_CLK_DIV				
0x0E	COMPOFFSET	[15:8]	RESERVED	COMP_OFFSET_CAL							0x00	RW
		[7:0]	RESERVED						CAL_FIN	START_CAL		
0x1D	RAMUPDATE	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED							RAMUPDATE		
0x1E	PAT_STATUS	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED				BUF_READ	MEM_ACCESS	PATTERN	RUN		
0x1F	PAT_TYPE	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED							PATTERN_RPT		

REGISTER MAP

Table 15. Register Summary (Continued)

Addr	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x20	PATTERN_DLY	[15:8]				PATTERN_DELAY[15:8]					0x0E	RW̄
		[7:0]				PATTERN_DELAY[7:0]						
0x22	DAC4DOF	[15:8]				DAC4_DIG_OFFSET[11:4]					0x00	RW̄
		[7:0]		DAC4_DIG_OFFSET[3:0]				RESERVED				
0x23	DAC3DOF	[15:8]				DAC3_DIG_OFFSET[11:4]					0x00	RW̄
		[7:0]		DAC3_DIG_OFFSET[3:0]				RESERVED				
0x24	DAC2DOF	[15:8]				DAC2_DIG_OFFSET[11:4]					0x00	RW̄
		[7:0]		DAC2_DIG_OFFSET[3:0]				RESERVED				
0x25	DAC1DOF	[15:8]				DAC1_DIG_OFFSET[11:4]					0x00	RW̄
		[7:0]		DAC1_DIG_OFFSET[3:0]				RESERVED				
0x26	WAV4_3CONFIG	[15:8]	RESERVED		PRESTORE_SEL4		RESERVED		WAVE_SEL4		0000	RW̄
		[7:0]	RESERVED		PRESTORE_SEL3		RESERVED		WAVE_SEL3			
0x27	WAV2_1CONFIG	[15:8]	RESERVED		PRESTORE_SEL2		MASK_DAC 4	CH2_ADD	WAVE_SEL2		0x00	RW̄
		[7:0]	RESERVED		PRESTORE_SEL1		MASK_DAC 3	CH1_ADD	WAVE_SEL1			
0x28	PAT_TIMEBASE	[15:8]	RESERVED				HOLD				0x011 1	RW̄
		[7:0]	PAT_PERIOD_BASE				START_DELAY_BASE					
0x29	PAT_PERIOD	[15:8]				PATTERN_PERIOD[15:8]					0x800 0	RW̄
		[7:0]				PATTERN_PERIOD[7:0]						
0x2A	DAC4_3PATx	[15:8]				DAC4_REPEAT_CYCLE					0x010 1	RW̄
		[7:0]				DAC3_REPEAT_CYCLE						
0x2B	DAC2_1PATx	[15:8]				DAC2_REPEAT_CYCLE					0x010 1	RW̄
		[7:0]				DAC1_REPEAT_CYCLE						
0x2C	DOUT_START _DLY	[15:8]				DOUT_START[15:8]					0x03	RW̄
		[7:0]				DOUT_START[7:0]						
0x2D	DOUT_CONFIG	[15:8]				RESERVED					0x00	RW̄
		[7:0]	RESERVED		DOUT_VAL	DOUT_MOD E	DOUT_STOP					
0x2E	DAC4_CST	[15:8]				DAC4_CONST[11:4]					0x00	RW̄
		[7:0]		DAC4_CONST[3:0]				RESERVED				
0x2F	DAC3_CST	[15:8]				DAC3_CONST[11:4]					0x00	RW̄
		[7:0]		DAC3_CONST[3:0]				RESERVED				
0x30	DAC2_CST	[15:8]				DAC2_CONST[11:4]					0x00	RW̄
		[7:0]		DAC2_CONST[3:0]				RESERVED				
0x31	DAC1_CST	[15:8]				DAC1_CONST[11:4]					0x00	RW̄
		[7:0]		DAC1_CONST[3:0]				RESERVED				
0x32	DAC4_DGAIN	[15:8]				DAC4_DIG_GAIN[11:4]					0x00	RW̄
		[7:0]		DAC4_DIG_GAIN[3:0]				RESERVED				
0x33	DAC3_DGAIN	[15:8]				DAC3_DIG_GAIN[11:4]					0x00	RW̄
		[7:0]		DAC3_DIG_GAIN[3:0]				RESERVED				
0x34	DAC2_DGAIN	[15:8]				DAC2_DIG_GAIN[11:4]					0x00	RW̄
		[7:0]		DAC2_DIG_GAIN[3:0]				RESERVED				
0x35	DAC1_DGAIN	[15:8]				DAC1_DIG_GAIN[11:4]					0x00	RW̄

REGISTER MAP

Table 15. Register Summary (Continued)

Addr	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	DAC1_DIG_GAIN[3:0]				RESERVED					
0x36	SAW4_3CONFIG	[15:8]	SAW_STEP4						SAW_TYPE4		0x00	RW̅
		[7:0]	SAW_STEP3						SAW_TYPE3			
0x37	SAW2_1CONFIG	[15:8]	SAW_STEP2						SAW_TYPE2		0x00	RW̅
		[7:0]	SAW_STEP1						SAW_TYPE1			
0x38 to 0x3D	RESERVED		RESERVED									
0x3E	DDS_TW32	[15:8]	DDSTW_MSB[15:8]								0x00	RW̅
		[7:0]	DDSTW_MSB[7:0]									
0x3F	DDS_TW1	[15:8]	DDSTW_LSB								0x00	RW̅
		[7:0]	RESERVED									
0x40	DDS4_PW	[15:8]	DDS4_PHASE[15:8]								0x00	RW̅
		[7:0]	DDS4_PHASE[7:0]									
0x41	DDS3_PW	[15:8]	DDS3_PHASE[15:8]								0x00	RW̅
		[7:0]	DDS3_PHASE[7:0]									
0x42	DDS2_PW	[15:8]	DDS2_PHASE[15:8]								0x00	RW̅
		[7:0]	DDS2_PHASE[7:0]									
0x43	DDS1_PW	[15:8]	DDS1_PHASE[15:8]								0x00	RW̅
		[7:0]	DDS1_PHASE[7:0]									
0x44	TRIG_TW_SEL	[15:8]	RESERVED								0x00	RW̅
		[7:0]	RESERVED						TRIG_DELAY_EN	RESERVED		
0x45	DDSx_CONFIG	[15:8]	DDS_COS_EN4	DDS_MSB_EN4	RESERVED		DDS_COS_EN3	DDS_MSB_EN3	PHASE_MEM_EN3	RESERVED	0x00	RW̅
		[7:0]	DDS_COS_EN2	DDS_MSB_EN2	RESERVED		DDS_COS_EN1	DDS_MSB_EN1	RESERVED	TW_MEM_EN		
0x47	TW_RAM_CONFIG	[15:8]	RESERVED								0x00	RW̅
		[7:0]	RESERVED				TW_MEM_SHIFT					
0x50	START_DLY4	[15:8]	START_DELAY4[15:8]								0x00	RW̅
		[7:0]	START_DELAY4[7:0]									
0x51	START_ADDR4	[15:8]	START_ADDR4[11:4]								0x00	RW̅
		[7:0]	START_ADDR4[3:0]				RESERVED					
0x52	STOP_ADDR4	[15:8]	STOP_ADDR4[11:4]								0x00	RW̅
		[7:0]	STOP_ADDR4[3:0]				RESERVED					
0x53	DDS_CYC4	[15:8]	DDS_CYC4[15:8]								0x01	RW̅
		[7:0]	DDS_CYC4[7:0]									
0x54	START_DLY3	[15:8]	START_DELAY3[15:8]								0x00	RW̅
		[7:0]	START_DELAY3[7:0]									
0x55	START_ADDR3	[15:8]	START_ADDR3[11:4]								0x00	RW̅
		[7:0]	START_ADDR3[3:0]				RESERVED					
0x56	STOP_ADDR3	[15:8]	STOP_ADDR3[11:4]								0x00	RW̅
		[7:0]	STOP_ADDR3[3:0]				RESERVED					
0x57	DDS_CYC3	[15:8]	DDS_CYC3[15:8]								0x01	RW̅
		[7:0]	DDS_CYC3[7:0]									
0x58	START_DLY2	[15:8]	START_DELAY2[15:8]								0x00	RW̅
		[7:0]	START_DELAY2[7:0]									
0x59	START_ADDR2	[15:8]	START_ADDR2[11:4]								0x00	RW̅

REGISTER MAP

Table 15. Register Summary (Continued)

Addr	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]		START_ADDR2[3:0]				RESERVED				
0x5A	STOP_ADDR2	[15:8]				STOP_ADDR2[11:4]					0x00	RW̄
		[7:0]		STOP_ADDR2[3:0]				RESERVED				
0x5B	DDS_CYC2	[15:8]				DDS_CYC2[15:8]					0x01	RW̄
		[7:0]				DDS_CYC2[7:0]						
0x5C	START_DLY1	[15:8]				START_DELAY1[15:8]					0x00	RW̄
		[7:0]				START_DELAY1[7:0]						
0x5D	START_ADDR1	[15:8]				START_ADDR1[11:4]					0x00	RW̄
		[7:0]		START_ADDR1[3:0]				RESERVED				
0x5E	STOP_ADDR1	[15:8]				STOP_ADDR1[11:4]					0x00	RW̄
		[7:0]		STOP_ADDR1[3:0]				RESERVED				
00x5F	DDS_CYC1	[15:8]				DDS_CYC1[15:8]					0x01	RW̄
		[7:0]				DDS_CYC1[7:0]						
00x60	CFG_ERROR	[15:8]	ERROR_CLEAR				RESERVED				0x00	R
		[7:0]	RESERVED		DOUT_START_LG_ERR	PAT_DLY_SHORT_ERR	DOUT_START_SHORT_ERR	PERIOD_SHORT_ERR	ODD_ADDR_ERR	MEM_READ_ERR		
0x6000 to 0x6FFF	SRAM_DATA	[15:8]				SRAM_DATA[11:4]					0x00	RW̄
		[7:0]		SRAM_DATA[3:0]				RESERVED				

REGISTER DESCRIPTIONS

SPI Control Register (SPICONFIG, Address 0x00)

Table 16. Bit Descriptions for SPICONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
15	LSBFIRST		LSB first selection.	0	RW̄
		0	MSB first per SPI standard (default).		
		1	LSB first per SPI standard.		
14	SPI3WIRE		Selects if SPI is using 3-wire or 4-wire interface.	0	RW̄
		0	4-wire SPI.		
		1	3-wire SPI.		
13	RESET		Executes software reset of SPI and controllers, reloads default register values, except for Register 0x00.	0	RW̄
		0	Normal status.		
		1	Resets whole register map, except for Register 0x00.		
12	DOUBLESPI		Double SPI data line.	0	RW̄
		0	The SPI port has only one data line and can be used as a 3-wire or 4-wire interface.		
		1	The SPI port has two data lines: both bidirectional defining a pseudo dual 3-wire interface where $\overline{CS}$ and SCLK are shared between the two ports. This mode is only available for SRAM data read or write.		
11	SPI_DRV		Double drive ability for SPI output.	0	RW̄
		0	Single SPI output drive ability.		
		1	Two-time drive ability on SPI output.		
10	DOUT_EN		Enable DOUT signal on SDO/SDI2/DOUT pin.	0	RW̄
		0	SDO/SDI2 function input/output.		
		1	DOUT function output.		
[9:6]	RESERVED			0x0	RW̄
5	DOUT_ENM		Enable DOUT signal on SDO/SDI2/DOUT pin.	0	RW̄
4	SPI_DRVM[1]		Double drive ability for SPI output.	0	RW̄
3	DOUBLESPIM[1]		Double SPI data line.	0	RW̄
2	RESETM[1]		Executes software reset of SPI and controllers, reloads default register values, except for Register 0x00.	0	RW̄
1	SPI3WIREM[1]		Selects if SPI is using 3-wire or 4-wire interface.	0	RW̄
0	LSBFIRSTM[1]		LSB first selection.	0	RW̄

[1] SPICONFIG, Bits[15:10] must always be set to the mirror of SPICONFIG, Bits[5:0] to allow simple recovery of the SPI operation when the LSBFIRST bit is set improperly. Bit 15 = Bit 0, Bit 14 = Bit 1, Bit 13 = Bit 2, Bit 12 = Bit 3, Bit 11 = Bit 4, and Bit 10 = Bit 5.

Power Status Register (POWERCONFIG, Address 0x01)

Table 17. Bit Descriptions for POWERCONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:12]	RESERVED			0x0	RW̄
11	CLK_LDO_STAT		Read only flag indicating the 1.8 V CLDO is on.	0	R
10	DIG1_LDO_STAT		Read only flag indicating the 1.8 V DVDD1 LDO is on.	0	R
9	DIG2_LDO_STAT		Read only flag indicating the 1.8 V DVDD2 LDO is on.	0	R
8	PDN_LDO_CLK		Disables the 1.8 V CLDO . An external supply is required.	0	RW̄
7	PDN_LDO_DIG1		Disables the DVDD1 LDO. An external supply is required.	0	RW̄
6	PDN_LDO_DIG2		Disables the DVDD2 LDO. An external supply is required.	0	RW̄

REGISTER MAP

Table 17. Bit Descriptions for POWERCONFIG (Continued)

Bits	Bit Field Name	Settings	Description	Reset	Access
5	REF_PDN		Disables 10 kΩ resistor that creates REFIO voltage. User can drive with external voltage or provide external bandgap (BG) resistor.	0	R$\overline{W}$
4	REF_EXT		Power down main BG reference including DAC bias.	0	R$\overline{W}$
3	DAC1_SLEEP		Disables DAC1 output current.	0	R$\overline{W}$
2	DAC2_SLEEP		Disables DAC2 output current.	0	R$\overline{W}$
1	DAC3_SLEEP		Disables DAC3 output current.	0	R$\overline{W}$
0	DAC4_SLEEP		Disables DAC4 output current.	0	R$\overline{W}$

Clock Control Register (CLOCKCONFIG, Address 0x02)

Table 18. Bit Descriptions for CLOCKCONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:12]	RESERVED			0x0	R$\overline{W}$
11	DIS_CLK1		Disables the analog clock to DAC1 out of the clock distribution block.	0	R$\overline{W}$
10	DIS_CLK2		Disables the analog clock to DAC2 out of the clock distribution block.	0	R$\overline{W}$
9	DIS_CLK3		Disables the analog clock to DAC3 out of the clock distribution block.	0	R$\overline{W}$
8	DIS_CLK4		Disables the analog clock to DAC4 out of the clock distribution block.	0	R$\overline{W}$
7	DIS_DCLK		Disables the clock to core digital block.	0	R$\overline{W}$
6	CLK_SLEEP		Enables a very low power clock mode.	0	R$\overline{W}$
5	CLK_PDN		Disables and powers down main clock receiver. No clocks are active in the device.	0	R$\overline{W}$
4	EPS		Enables Power Save (EPS). This enables a low power option for the clock receiver, but maintains low jitter performance on DAC clock rising edge. The DAC clock falling edge is substantially degraded.	0	R$\overline{W}$
3	DAC1_INV_CLK		Cannot use EPS while using this bit. Inverts the clock inside DAC Core 1 allowing 180° phase shift in DAC1 update timing.	0	R$\overline{W}$
2	DAC2_INV_CLK		Cannot use EPS while using this bit. Inverts the clock inside DAC Core 2 allowing 180° phase shift in DAC2 update timing.	0	R$\overline{W}$
1	DAC3_INV_CLK		Cannot use EPS while using this bit. Inverts the clock inside DAC Core 3 allowing 180° phase shift in DAC3 update timing.	0	R$\overline{W}$
0	DAC4_INV_CLK		Cannot use EPS while using this bit. Inverts the clock inside DAC Core 4 allowing 180° phase shift in DAC4 update timing.	0	R$\overline{W}$

Reference Resistor Register (REFADJ, Address 0x03)

Table 19. Bit Descriptions for REFADJ

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:6]	RESERVED			0x000	R$\overline{W}$
[5:0]	BGDR		Adjusts the BG 10 kΩ resistor (nominal) to 8 kΩ to 12 kΩ, which changes the BG voltage from 840 mV to 1.24 V, respectively (see Figure 35). Scaling is 6.25 mV per LSB.	0x00	R$\overline{W}$
		0x20	On-chip reference voltage of 1.24 V		
		0x00	On-chip reference voltage of 1.04 V (default)		
		0x1F	On-chip reference voltage of 800 mV		

DAC4 Analog Gain Register (DAC4AGAIN, Address 0x04)

Table 20. Bit Descriptions for DAC4AGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	R$\overline{W}$
[14:8]	DAC4_GAIN_CAL		DAC4 analog gain calibration output—read only.	0x00	R
7	RESERVED			0	R$\overline{W}$
[6:0]	DAC4_GAIN		DAC4 analog gain control while not in calibration mode — two's complement format. This allows to have fine gain control/adjustments in the DAC output current. The range of the fine gain adjustment and resolution of DAC4AGAIN depends on DAC4_GAIN_RNG (0x08, Bits[7:6]). For wider range and better accuracy, use digital gain registers.	0x00	R$\overline{W}$

DAC3 Analog Gain Register (DAC3AGAIN, Address 0x05)

Table 21. Bit Descriptions for DAC3AGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	R$\overline{W}$
[14:8]	DAC3_GAIN_CAL		DAC3 analog gain calibration output—read only.	0x00	R
7	RESERVED			0	R$\overline{W}$
[6:0]	DAC3_GAIN		DAC3 analog gain control while not in calibration mode — two's complement format. This allows to have fine gain control/adjustments in the DAC output current. The range of the fine gain adjustment and resolution of DAC3AGAIN depends on DAC3_GAIN_RNG (0x08, Bits[5:4]). For wider range and better accuracy, use digital gain registers.	0x00	R$\overline{W}$

DAC2 Analog Gain Register (DAC2AGAIN, Address 0x06)

Table 22. Bit Descriptions for DAC2AGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	R$\overline{W}$
[14:8]	DAC2_GAIN_CAL		DAC2 analog gain calibration output—read only.	0x00	R
7	RESERVED			0	R$\overline{W}$
[6:0]	DAC2_GAIN		DAC2 analog gain control while not in calibration mode — two's complement format. This allows to have fine gain control/adjustments in the DAC output current. The range of the fine gain adjustment and resolution of DAC2AGAIN depends on DAC2_GAIN_RNG (0x08, Bits[3:2]). For wider range and better accuracy, use digital gain registers.	0x00	R$\overline{W}$

DAC1 Analog Gain Register (DAC1AGAIN, Address 0x07)

Table 23. Bit Descriptions for DAC1AGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	R$\overline{W}$
[14:8]	DAC1_GAIN_CAL		DAC1 analog gain calibration output—read only.	0x00	R
7	RESERVED			0	R$\overline{W}$
[6:0]	DAC1_GAIN		DAC1 analog gain control while not in calibration mode — two's complement format. This allows to have fine gain control/adjustments in the DAC output current. The range of the fine gain adjustment and resolution of DAC1AGAIN depends on DAC1_GAIN_RNG (0x08, Bits[1:0]). For wider range and better accuracy, use digital gain registers.	0x00	R$\overline{W}$

REGISTER MAP

DAC Analog Gain Range Register (DACxRANGE, Address 0x08)

Table 24. Bit Descriptions for DACxRANGE

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x00	R$\overline{W}$
[7:6]	DAC4_GAIN_RNG		DAC4 gain range control, two's complement format.	0x0	R$\overline{W}$
[5:4]	DAC3_GAIN_RNG		DAC3 gain range control, two's complement format.	0x0	R$\overline{W}$
[3:2]	DAC2_GAIN_RNG		DAC2 gain range control, two's complement format.	0x0	R$\overline{W}$
[1:0]	DAC1_GAIN_RNG		DAC1 gain range control, two's complement format.	0x0	R$\overline{W}$
		0x0	±33% * 0.25		
		0x1	±33% * 0.50		
		0x2	±33% * 0.75		
		0x3	±33% * 1.00		

FSADJ4 Register (DAC4RSET, Address 0x09)

Table 25. Bit Descriptions for DAC4RSET

Bits	Bit Field Name	Settings	Description	Reset	Access
15	DAC4_RSET_EN		For write, enable the internal R_{SET4} resistor for DAC4; for read, R_{SET4} for DAC4 is enabled during calibration mode.	0	R$\overline{W}$
[14:13]	RESERVED			0x0	R$\overline{W}$
[12:8]	DAC4_RSET_CAL		Digital control value of R_{SET4} resistor for DAC4 after calibration—read only.	0x00	R
[7:5]	RESERVED			0x0	R$\overline{W}$
[4:0]	DAC4_RSET		Digital control to set the value of R_{SET4} resistor in DAC4. The scaling/resolution of DAC_RSET is 800 Ω per LSB.	0x0A	R$\overline{W}$
		0x05	R_{SETx} is set to 4 kΩ (minimum).		
		0x0A	R_{SETx} is set to 8 kΩ (default).		
		0x14	R_{SETx} is set to 16 kΩ (minimum).		

FSADJ3 Register (DAC3RSET, Address 0x0A)

Table 26. Bit Descriptions for DAC3RSET

Bits	Bit Field Name	Settings	Description	Reset	Access
15	DAC3_RSET_EN		For write, enable the internal R_{SET3} resistor for DAC3; for read, R_{SET3} for DAC3 is enabled during calibration mode.	0	R$\overline{W}$
[14:13]	RESERVED			0x0	R$\overline{W}$
[12:8]	DAC3_RSET_CAL		Digital control value of R_{SET3} resistor for DAC3 after calibration—read only.	0x00	R
[7:5]	RESERVED			0x0	R$\overline{W}$
[4:0]	DAC3_RSET		Digital control to set the value of R_{SET3} resistor in DAC3. The scaling/resolution of DAC_RSET is 800 Ω per LSB.	0x0A	R$\overline{W}$
		0x05	R_{SETx} is set to 4 kΩ (minimum).		
		0x0A	R_{SETx} is set to 8 kΩ (default).		
		0x14	R_{SETx} is set to 16 kΩ (minimum).		

FSADJ2 Register (DAC2RSET, Address 0x0B)

Table 27. Bit Descriptions for DAC2RSET

Bits	Bit Field Name	Settings	Description	Reset	Access
15	DAC2_RSET_EN		For write, enable the internal R_{SET2} resistor for DAC2; for read, R_{SET2} for DAC2 is enabled during calibration mode.	0	R$\overline{W}$

REGISTER MAP

Table 27. Bit Descriptions for DAC2RSET (Continued)

Bits	Bit Field Name	Settings	Description	Reset	Access
[14:13]	RESERVED			0x0	R$\overline{W}$
[12:8]	DAC2_RSET_CAL		Digital control value of R_{SET2} resistor for DAC2 after calibration—read only.	0x00	R
[7:5]	RESERVED			0x0	R$\overline{W}$
[4:0]	DAC2_RSET		Digital control to set the value of R_{SET2} resistor in DAC2. The scaling/resolution of DAC_RSET is 800 Ω per LSB.	0x0A	R$\overline{W}$
		0x05	R_{SETx} is set to 4 kΩ (minimum).		
		0x0A	R_{SETx} is set to 8 kΩ (default).		
		0x14	R_{SETx} is set to 16 kΩ (minimum).		

FSADJ1 Register (DAC1RSET, Address 0x0C)

Table 28. Bit Descriptions for DAC1RSET

Bits	Bit Field Name	Settings	Description	Reset	Access
15	DAC1_RSET_EN		For write, enable the internal R_{SET1} resistor for DAC1; for read, R_{SET1} for DAC1 is enabled during calibration mode.	0	R$\overline{W}$
[14:13]	RESERVED			0x0	R$\overline{W}$
[12:8]	DAC1_RSET_CAL		Digital control value of R_{SET1} resistor for DAC1 after calibration—read only.	0x00	R
[7:5]	RESERVED			0x0	R$\overline{W}$
[4:0]	DAC1_RSET		Digital control to set the value of R_{SET1} resistor in DAC1. The scaling/resolution of DAC_RSET is 800 Ω per LSB.	0x0A	R$\overline{W}$
		0x05	R_{SETx} is set to 4 kΩ (minimum).		
		0x0A	R_{SETx} is set to 8 kΩ (default).		
		0x14	R_{SETx} is set to 16 kΩ (minimum).		

Calibration Register (CALCONFIG, Address 0x0D)

Table 29. Bit Descriptions for CALCONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	R$\overline{W}$
14	COMP_OFFSET_OF		Compensation offset calibration value overflow.	0	R
13	COMP_OFFSET_UF		Compensation offset calibration value underflow.	0	R
12	RSET_CAL_OF		R_{SETx} calibration value overflow.	0	R
11	RSET_CAL_UF		R_{SETx} calibration value underflow.	0	R
10	GAIN_CAL_OF		Gain calibration value overflow.	0	R
9	GAIN_CAL_UF		Gain calibration value underflow.	0	R
8	CAL_RESET		Pulse this bit high and low to reset the calibration results.	0	R$\overline{W}$
7	CAL_MODE		Read only flag indicating calibration is being used.	0	R
6	CAL_MODE_EN		Enables the gain calibration circuitry.	0	R$\overline{W}$
[5:4]	COMP_CAL_RNG		Offset calibration range.	0x0	R$\overline{W}$
3	CAL_CLK_EN		Enables the calibration clock to calibration circuitry.	0	R$\overline{W}$
[2:0]	CAL_CLK_DIV		Sets divider from DAC clock to calibration clock. Clock dividers are powers of 2 (that is 2^{2+N}). Note that the calibration clock must be less than 500 kHz.	0x0	R$\overline{W}$
		0x0	CLK Divider = 4		
		0x1	CLK Divider = 8		
		0x2	CLK Divider = 16		
		0x3	CLK Divider = 32		
		0x4	CLK Divider = 64		
		0x5	CLK Divider = 128		

REGISTER MAP

Table 29. Bit Descriptions for CALCONFIG (Continued)

Bits	Bit Field Name	Settings	Description	Reset	Access
		0x6	CLK Divider = 256		
		0x7	CLK Divider = 512 (default)		

Comp Offset Register (COMPOFFSET, Address 0x0E)

Table 30. Bit Descriptions for COMPOFFSET

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	RW̄
[14:8]	COMP_OFFSET_CAL		The result of the offset calibration for the comparator.	0x00	R
[7:2]	RESERVED			0x00	RW̄
1	CAL_FIN		Read only flag indicating calibration is completed.	0	R
0	START_CAL		Start a calibration cycle.	0	RW̄

Update Pattern Register (RAMUPDATE, Address 0x1D)

Table 31. Bit Descriptions for RAMUPDATE

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x000	RW̄
0	RAMUPDATE		Update all SPI settings with a new configuration (self-clearing).	0	RW̄

Command/Status Register (PAT_STATUS, Address 0x1E)

Table 32. Bit Descriptions for PAT_STATUS

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	RESERVED			0x000	RW̄
3	BUF_READ		Read back from updated buffer.	0	RW̄
2	MEM_ACCESS		Memory (SRAM) SPI access enable.	0	RW̄
1	PATTERN		Status of pattern being played (Read only).	0	R
0	RUN		Allows the pattern generation and stop pattern after trigger.	0	RW̄

Command/Status Register (PAT_TYPE, Address 0x1F)

Table 33. Bit Descriptions for PAT_TYPE

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0000	RW̄
0	PATTERN_RPT		Setting this bit allows the pattern to repeat the number of times defined in DAC4_3PATx (Register 0x2A) and DAC2_1PATx (Register 0x2B).	0	RW̄
		0	Pattern continuously runs.		
		1	Pattern repeats the number of times defined in DAC4_3PATx (Register 0x2A) and DAC2_1PATx (Register 0x2B).		

Trigger Start to Real Pattern Delay Register (PATTERN_DLY, Address 0x20)

Table 34. Bit Descriptions for PATTERN_DLY

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	PATTERN_DELAY		Number of DAC clock cycles + 1 that it takes between Trigger low and pattern start. Increment = 1.	0x000E	RW̄
		0x000E	Sets Pattern Delay to minimum — 14 (default).		

REGISTER MAP

Table 34. Bit Descriptions for PATTERN_DLY (Continued)

Bits	Bit Field Name	Settings	Description	Reset	Access
		0xFFFF	Sets Pattern Delay to maximum — 65535.		

DAC4 Digital Offset Register (DAC4DOF, Address 0x22)

Table 35. Bit Descriptions for DAC4DOF

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC4_DIG_OFFSET		DAC4 digital offset.	0x000	R$\overline{W}$
		0x800	Digital offset = -0.500		
		0xC00	Digital offset = −0.250		
		0x000	Digital offset = 0		
		0x400	Digital offset = 0.250		
		0x7FF	Digital offset = 0.500 $\cong$ $2047/4096$		
[3:0]	RESERVED			0x0	R$\overline{W}$

DAC3 Digital Offset Register (DAC3DOF, Address 0x23)

Table 36. Bit Descriptions for DAC3DOF

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC3_DIG_OFFSET		DAC3 digital offset.	0x000	R$\overline{W}$
		0x800	Digital offset = -0.500		
		0xC00	Digital offset = −0.250		
		0x000	Digital offset = 0		
		0x400	Digital offset = 0.250		
		0x7FF	Digital offset = 0.500 $\cong$ $2047/4096$		
[3:0]	RESERVED			0x0	R$\overline{W}$

DAC2 Digital Offset Register (DAC2DOF, Address 0x24)

Table 37. Bit Descriptions for DAC2DOF

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC2_DIG_OFFSET		DAC2 digital offset.	0x000	R$\overline{W}$
		0x800	Digital offset = -0.500		
		0xC00	Digital offset = −0.250		
		0x000	Digital offset = 0		
		0x400	Digital offset = 0.250		
		0x7FF	Digital offset = 0.500 $\cong$ $2047/4096$		
[3:0]	RESERVED			0x0	R$\overline{W}$

DAC1 Digital Offset Register (DAC1DOF, Address 0x25)

Table 38. Bit Descriptions for DAC1DOF

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC1_DIG_OFFSET		DAC1 digital offset.	0x000	R$\overline{W}$
		0x800	Digital offset = -0.500		
		0xC00	Digital offset = −0.250		
		0x000	Digital offset = 0		
		0x400	Digital offset = 0.250		

REGISTER MAP

Table 38. Bit Descriptions for DAC1DOF (Continued)

Bits	Bit Field Name	Settings	Description	Reset	Access
		0x7FF	Digital offset $= 0.500 \cong {}^{2047}/_{4096}$		
[3:0]	RESERVED			0x0	R$\overline{W}$

Wave3/Wave4 Select Register (WAV4_3CONFIG, Address 0x26)

Table 39. Bit Descriptions for WAV4_3CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:14]	RESERVED			0x0	R$\overline{W}$
[13:12]	PRESTORE_SEL4		DAC4 prestored waveform selection.	0x0	R$\overline{W}$
		0x0	Constant value held into DAC4 constant value MSB/LSB register.		
		0x1	Sawtooth defined in DAC4 sawtooth configuration register (SAW4_3CONFIG).		
		0x2	Pseudorandom sequence.		
		0x3	DDS4 output.		
[11:10]	RESERVED			0x0	R$\overline{W}$
[9:8]	WAVE_SEL4		Selects source of generated waveform for DAC4.	0x1	R$\overline{W}$
		0x0	Waveform read from RAM between START_ADDR4 and STOP_ADDR4.		
		0x1	Prestored waveform.		
		0x2	Prestored waveform using START_DELAY4 and PATTERN_PERIOD.		
		0x3	Prestored waveform modulated by waveform from RAM.		
[7:6]	RESERVED			0x0	R$\overline{W}$
[5:4]	PRESTORE_SEL3		DAC3 prestored waveform selection.	0x0	R$\overline{W}$
		0x0	Constant value held into DAC3 constant value MSB/LSB register.		
		0x1	Sawtooth defined in DAC3 sawtooth configuration register (SAW4_3CONFIG).		
		0x2	Pseudorandom sequence.		
		0x3	DDS3 output.		
[3:2]	RESERVED			0x0	R$\overline{W}$
[1:0]	WAVE_SEL3		Selects source of generated waveform for DAC3.	0x1	R$\overline{W}$
		0x0	Waveform read from RAM between START_ADDR3 and STOP_ADDR3.		
		0x1	Prestored waveform.		
		0x2	Prestored waveform using START_DELAY3 and PATTERN_PERIOD.		
		0x3	Prestored waveform modulated by waveform from RAM.		

Wave1/Wave2 Select Register (WAV2_1CONFIG, Address 0x27)

Table 40. Bit Descriptions for WAV2_1CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:14]	RESERVED			0x0	R$\overline{W}$
[13:12]	PRESTORE_SEL2		DAC2 prestored waveform selection.	0x0	R$\overline{W}$
		0x0	Constant value held into DAC2 constant value MSB/LSB register.		
		0x1	Sawtooth defined in DAC2 sawtooth configuration register (SAW2_1CONFIG).		
		0x2	Pseudorandom sequence.		
		0x3	DDS2 output.		
11	MASK_DAC4		Mask DAC4 to DAC4_CONST value.	0	R$\overline{W}$
10	CH2_ADD		Add DAC2 and DAC4, output at DAC2.	0	R$\overline{W}$
		0	Normal operation for DAC2/DAC4.		
		1	Add DAC2 and DAC4, output from DAC2. In this START_DELAYx case, DAC4 output remains unchanged.		
[9:8]	WAVE_SEL2		Selects source of waveform output for DAC2.	0x1	R$\overline{W}$

REGISTER MAP

Table 40. Bit Descriptions for WAV2_1CONFIG (Continued)

Bits	Bit Field Name	Settings	Description	Reset	Access
		0x0	Waveform read from RAM between START_ADDR2 and STOP_ADDR2.		
		0x1	Prestored waveform.		
		0x2	Prestored waveform using START_DELAY2 and PATTERN_PERIOD.		
		0x3	Prestored waveform modulated by waveform from RAM.		
[7:6]	RESERVED			0x0	R$\overline{W}$
[5:4]	PRESTORE_SEL1		DAC1 prestored waveform selection.	0x0	R$\overline{W}$
		0x0	Constant value held into DAC1 constant value MSB/LSB register.		
		0x1	Sawtooth defined in DAC1 sawtooth configuration register (SAW2_1CONFIG).		
		0x2	Pseudorandom sequence.		
		0x3	DDS1 output.		
3	MASK_DAC3		Mask DAC3 to DAC3_CONST value.	0	R$\overline{W}$
2	CH1_ADD		Add DAC1 and DAC3, output at DAC1.	0	R$\overline{W}$
		0	Normal operation for DAC1/DAC3.		
		1	Add DAC1 and DAC3, and output from DAC1. In this START_DELAYx case, DAC3 output remains unchanged.		
[1:0]	WAVE_SEL1		Selects source of waveform output for DAC1.	0x1	R$\overline{W}$
		0x0	Waveform read from RAM between START_ADDR1 and STOP_ADDR1.		
		0x1	Prestored waveform.		
		0x2	Prestored waveform using START_DELAY1 and PATTERN_PERIOD.		
		0x3	Prestored waveform modulated by waveform from RAM.		

DAC Time Control Register (PAT_TIMEBASE, Address 0x28)

Table 41. Bit Descriptions for PAT_TIMEBASE

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:12]	RESERVED			0x0	R$\overline{W}$
[11:8]	HOLD		Specifies how long the DAC holds the SRAM sample in terms of DAC clock periods. This can be used for coarse adjustment of the SRAM increment clock.	0x1	R$\overline{W}$
		0x0	DAC holds each sample for 16 DAC clock periods.		
		0x1	DAC holds each sample for 1 DAC clock period (default).		
		0xF	DAC holds each sample for 15 DAC clock periods.		
[7:4]	PAT_PERIOD_BASE		Number of DAC clock periods per PATTERN_PERIOD LSB .	0x1	R$\overline{W}$
		0x0	PATTERN_PERIOD LSB = 16 DAC clock periods		
		0x1	PATTERN_PERIOD LSB = 1 DAC clock period (default)		
		0xF	PATTERN_PERIOD LSB = 15 DAC clock periods		
[3:0]	START_DELAY_BASE		Number of DAC clock period per START_DELAYx LSB.	0x1	R$\overline{W}$
		0x0	START_DELAYx LSB = 16 DAC clock periods		
		0x1	START_DELAYx LSB = 1 DAC clock period (default)		
		0xF	START_DELAYx LSB = 15 DAC clock periods		

Pattern Period Register (PAT_PERIOD, Address 0x029)

Table 42. Bit Descriptions for PAT_PERIOD

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	PATTERN_PERIOD		Pattern period register.	0x8000	R$\overline{W}$

REGISTER MAP

DAC3/DAC4 Pattern Repeat Cycles Register (DAC4_3PATx, Address 0x2A)

Table 43. Bit Descriptions for DAC4_3PATx

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	DAC4_REPEAT_CYCLE		Number of DAC4 pattern repeat cycles + 1, (0 → repeat 1 pattern).	0x01	R$\overline{W}$
[7:0]	DAC3_REPEAT_CYCLE		Number of DAC3 pattern repeat cycles + 1, (0 → repeat 1 pattern).	0x01	R$\overline{W}$

DAC1/DAC2 Pattern Repeat Cycles Register (DAC2_1PATx, Address 0x2B)

Table 44. Bit Descriptions for DAC2_1PATx

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	DAC2_REPEAT_CYCLE		Number of DAC2 pattern repeat cycles + 1, (0 → repeat 1 pattern).	0x01	R$\overline{W}$
[7:0]	DAC1_REPEAT_CYCLE		Number of DAC1 pattern repeat cycles + 1, (0 → repeat 1 pattern).	0x01	R$\overline{W}$

Trigger Start to DOUT Signal Register (DOUT_START, Address 0x2C)

Table 45. Bit Descriptions for DOUT_START

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DOUT_START		Time between Trigger low and DOUT signal high in number of DAC clock cycles. Increment = 1.	0x0003	R$\overline{W}$
		0x0003	3 DAC clock cycles (minimum)		
		0xFFFF	65535 DAC clock cycles (maximum)		

DOUT Configuration Register (DOUT_CONFIG, Address 0x2D)

Table 46. Bit Descriptions for DOUT_CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:6]	RESERVED			0x000	R$\overline{W}$
5	DOUT_VAL		Manually sets DOUT signal value, only valid when DOUT_MODE = 0 (manual mode).	0	R$\overline{W}$
4	DOUT_MODE		Sets different enable signal mode.	0	R$\overline{W}$
		0	DOUT pin is output from SDO/SDI2/DOUT pin and is manually controlled by Bit 5 (DOUT_ENM) and Bit 10 (DOUT_EN) in Register 0x00, which must be set to use this feature.		
		1	DOUT pin is output from SDO/SDI2/DOUT. The pin is controlled by DOUT_START and DOUT_STOP fields. Bit 5 (DOUT_ENM) and Bit 10 (DOUT_EN) in Register 0x00 must be set to use this feature.		
[3:0]	DOUT_STOP		Time between pattern end and DOUT signal low in number of DAC clock cycles. Increment = 1.	0x0	R$\overline{W}$
		0x0	0 DAC clock cycles (minimum)		
		0xF	15 DAC clock cycles (maximum)		

DAC4 Constant Value Register (DAC4_CST, Address 0x2E)

Table 47. Bit Descriptions for DAC4_CST

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC4_CONST		Most significant byte of DAC4 constant value.	0x000	R$\overline{W}$
		0x7FF	Digital constant = IOUTFS - 1 LSB		
		0x000	Digital constant = 0		
		0x800	Digital constant = −IOUTFS + 1 LSB		
[3:0]	RESERVED			0x0	R$\overline{W}$

REGISTER MAP

DAC3 Constant Value Register (DAC3_CST, Address 0x2F)

Table 48. Bit Descriptions for DAC3_CST

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC3_CONST		Most significant byte of DAC3 constant value.	0x000	R$\overline{W}$
		0x7FF	Digital constant = IOUTFS - 1 LSB		
		0x000	Digital constant = 0		
		0x800	Digital constant = −IOUTFS + 1 LSB		
[3:0]	RESERVED			0x0	R$\overline{W}$

DAC2 Constant Value Register (DAC2_CST, Address 0x30)

Table 49. Bit Descriptions for DAC2_CST

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC2_CONST		Most significant byte of DAC2 constant value.	0x000	R$\overline{W}$
		0x7FF	Digital constant = IOUTFS - 1 LSB		
		0x000	Digital constant = 0		
		0x800	Digital constant = −IOUTFS + 1 LSB		
[3:0]	RESERVED			0x0	R$\overline{W}$

DAC1 Constant Value Register (DAC1_CST, Address 0x31)

Table 50. Bit Descriptions for DAC1_CST

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC1_CONST		Most significant byte of DAC1 constant value.	0x000	R$\overline{W}$
		0x7FF	Digital constant = IOUTFS - 1 LSB		
		0x000	Digital constant = 0		
		0x800	Digital constant = −IOUTFS + 1 LSB		
[3:0]	RESERVED			0x0	R$\overline{W}$

DAC4 Digital Gain Register (DAC4_DGAIN, Address 0x32)

Table 51. Bit Descriptions for DAC4_DGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC4_DIG_GAIN		DAC4 digital gain. Range of +2 to −2.	0x000	R$\overline{W}$
		0x400	Multiplies digital data at DAC channel path by +1		
		0x7FF	Multiplies digital data at DAC channel path by +2		
		0x800	Multiplies digital data at DAC channel path by -2		
		0xC00	Multiplies digital data at DAC channel path by -1		
[3:0]	RESERVED			0x0	R$\overline{W}$

DAC3 Digital Gain Register (DAC3_DGAIN, Address 0x33)

Table 52. Bit Descriptions for DAC3_DGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC3_DIG_GAIN		DAC3 digital gain. Range of +2 to −2.	0x000	R$\overline{W}$
		0x400	Multiplies digital data at DAC channel path by +1		
		0x7FF	Multiplies digital data at DAC channel path by +2		
		0x800	Multiplies digital data at DAC channel path by -2		
		0xC00	Multiplies digital data at DAC channel path by -1		

REGISTER MAP

Table 52. Bit Descriptions for DAC3_DGAIN (Continued)

Bits	Bit Field Name	Settings	Description	Reset	Access
[3:0]	RESERVED			0x0	R$\overline{W}$

DAC2 Digital Gain Register (DAC2_DGAIN, Address 0x34)

Table 53. Bit Descriptions for DAC2_DGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC2_DIG_GAIN		DAC2 digital gain. Range of +2 to −2.	0x000	R$\overline{W}$
		0x400	Multiplies digital data at DAC channel path by +1		
		0x7FF	Multiplies digital data at DAC channel path by +2		
		0x800	Multiplies digital data at DAC channel path by -2		
		0xC00	Multiplies digital data at DAC channel path by -1		
[3:0]	RESERVED			0x0	R$\overline{W}$

DAC1 Digital Gain Register (DAC1_DGAIN, Address 0x35)

Table 54. Bit Descriptions for DAC1_DGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC1_DIG_GAIN		DAC1 digital gain. Range of +2 to −2.	0x000	R$\overline{W}$
		0x400	Multiplies digital data at DAC channel path by +1		
		0x7FF	Multiplies digital data at DAC channel path by +2		
		0x800	Multiplies digital data at DAC channel path by -2		
		0xC00	Multiplies digital data at DAC channel path by -1		
[3:0]	RESERVED			0x0	R$\overline{W}$

DAC3/DAC4 Sawtooth Configuration Register (SAW4_3CONFIG, Address 0x36)

Table 55. Bit Descriptions for SAW4_3CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:10]	SAW_STEP4		Number of samples per step for DAC4. Up to 64 samples per step.	0x01	R$\overline{W}$
[9:8]	SAW_TYPE4		The type of sawtooth (positive, negative, or triangle) for DAC4.	0x0	R$\overline{W}$
		0x0	Ramp up saw wave.		
		0x1	Ramp down saw wave.		
		0x2	Triangle saw wave.		
		0x3	No wave, zero.		
[7:2]	SAW_STEP3		Number of samples per step for DAC3. Up to 64 samples per step.	0x01	R$\overline{W}$
[1:0]	SAW_TYPE3		The type of sawtooth (positive, negative, or triangle) for DAC3.	0x0	R$\overline{W}$
		0x0	Ramp up saw wave.		
		0x1	Ramp down saw wave.		
		0x2	Triangle saw wave.		
		0x3	No wave, zero.		

DAC1/DAC2 Sawtooth Configuration Register (SAW2_1CONFIG, Address 0x37)

Table 56. Bit Descriptions for SAW2_1CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:10]	SAW_STEP2		Number of samples per step for DAC2. Up to 64 samples per step.	0x01	R$\overline{W}$
[9:8]	SAW_TYPE2		The type of sawtooth (positive, negative, or triangle) for DAC2.	0x0	R$\overline{W}$
		0x0	Ramp up saw wave.		

REGISTER MAP

Table 56. Bit Descriptions for SAW2_1CONFIG (Continued)

Bits	Bit Field Name	Settings	Description	Reset	Access
		0x1	Ramp down saw wave.		
		0x2	Triangle saw wave.		
		0x3	No wave, zero.		
[7:2]	SAW_STEP1		Number of samples per step for DAC1. Up to 64 samples per step.	0x01	R$\overline{W}$
[1:0]	SAW_TYPE1		The type of sawtooth (positive, negative, or triangle) for DAC1.	0x0	R$\overline{W}$
		0x0	Ramp up saw wave.		
		0x1	Ramp down saw wave.		
		0x2	Triangle saw wave.		
		0x3	No wave, zero.		

DDS Tuning Word MSB Register (DDS_TW32, Address 0x3E)

Table 57. Bit Descriptions for DDS_TW32

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDSTW_MSB		DDS tuning word MSB.	0x0000	R$\overline{W}$

DDS Tuning Word LSB Register (DDS_TW1, Address 0x3F)

Table 58. Bit Descriptions for DDS_TW1

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	DDSTW_LSB		DDS tuning word LSB.	0x00	R$\overline{W}$
[7:0]	RESERVED			0x00	R$\overline{W}$

DDS4 Phase Offset Register (DDS4_PW, Address 0x40)

Table 59. Bit Descriptions for DDS4_PW

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS4_PHASE		DDS4 phase offset.	0x0000	R$\overline{W}$
		0x0000	DDS phase offset = 0°		
		0x4000	DDS phase offset = 90°		
		0x8000	DDS phase offset = 180°		
		0xC000	DDS phase offset = 270°		

DDS3 Phase Offset Register (DDS3_PW, Address 0x41)

Table 60. Bit Descriptions for DDS3_PW

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS3_PHASE		DDS3 phase offset.	0x0000	R$\overline{W}$
		0x0000	DDS phase offset = 0°		
		0x4000	DDS phase offset = 90°		
		0x8000	DDS phase offset = 180°		
		0xC000	DDS phase offset = 270°		

DDS2 Phase Offset Register (DDS2_PW, Address 0x42)

Table 61. Bit Descriptions for DDS2_PW

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS2_PHASE		DDS2 phase offset.	0x0000	R$\overline{W}$

REGISTER MAP

Table 61. Bit Descriptions for DDS2_PW (Continued)

Bits	Bit Field Name	Settings	Description	Reset	Access
		0x0000	DDS phase offset = 0°		
		0x4000	DDS phase offset = 90°		
		0x8000	DDS phase offset = 180°		
		0xC000	DDS phase offset = 270°		

DDS1 Phase Offset Register (DDS1_PW, Address 0x43)

Table 62. Bit Descriptions for DDS1_PW

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS1_PHASE		DDS1 phase offset.	0x0000	R$\overline{W}$
		0x0000	DDS phase offset = 0°		
		0x4000	DDS phase offset = 90°		
		0x8000	DDS phase offset = 180°		
		0xC000	DDS phase offset = 270°		

Pattern Control 1 Register (TRIG_TW_SEL, Address 0x44)

Table 63. Bit Descriptions for TRIG_TW_SEL

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:2]	RESERVED			0x0000	R$\overline{W}$
1	TRIG_DELAY_EN		Enable start delay as trigger delay for all four channels.	0	R$\overline{W}$
		0	Delay repeats for all patterns.		
		1	Delay is only at the start of first pattern.		
0	RESERVED			0	R$\overline{W}$

Pattern Control 2 Register (DDSx_CONFIG, Address 0x45)

Table 64. Bit Descriptions for DDSx_CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
15	DDS_COS_EN4		Enables DDS4 cosine output of DDS instead of sine wave.	0	R$\overline{W}$
14	DDS_MSB_EN4		Enables the clock for the SRAM address counter. Increment is coming from the DDS4 MSB.	0	R$\overline{W}$
		0	DAC Clock CLKP/CLKN (default)		
		1	Rising edge of the DDS4 output MSB. This can be used when the SRAM contains a list of DDS tuning words.		
13	RESERVED			0	R$\overline{W}$
12	RESERVED			0	R$\overline{W}$
11	DDS_COS_EN3		Enables DDS3 cosine output of DDS instead of sine wave.	0	R$\overline{W}$
10	DDS_MSB_EN3		Enables the clock for the SRAM address counter. Increment is coming from the DDS3 MSB.	0	R$\overline{W}$
		0	DAC Clock CLKP/CLKN (default)		
		1	Rising edge of the DDS4 output MSB. This can be used when the SRAM contains a list of DDS tuning words.		
9	PHASE_MEM_EN3		Enables DDS3 phase offset input coming from SRAM reading START_ADDR3. Because phase word is 8 bits and SRAM data is 12 bits, only 8 MSB of SRAM are taken into account.	0	R$\overline{W}$
		0	Selects DDS3_PW as the source of DDS offset.		
		1	Selects the SRAM as source of DDS phase offset input.		
8	RESERVED			0	R$\overline{W}$

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Table 64. Bit Descriptions for DDSx_CONFIG (Continued)

Bits	Bit Field Name	Settings	Description	Reset	Access
7	DDS_COS_EN2		Enables DDS2 cosine output of DDS instead of sine wave.	0	R$\overline{W}$
6	DDS_MSB_EN2		Enables the clock for the SRAM address counter. Increment is coming from the DDS2 MSB. Default is coming from DAC clock.	0	R$\overline{W}$
		0	DAC Clock CLKP/CLKN (default)		
		1	Rising edge of the DDS4 output MSB. This can be used when the SRAM contains a list of DDS tuning words.		
5	RESERVED			0	R$\overline{W}$
4	RESERVED			0	R$\overline{W}$
3	DDS_COS_EN1		Enables DDS1 cosine output of DDS instead of sine wave.	0	R$\overline{W}$
2	DDS_MSB_EN1		Enables the clock for the SRAM address counter. Increment is coming from the DDS1 MSB. Default is coming from DAC clock.	0	R$\overline{W}$
		0	DAC Clock CLKP/CLKN (default)		
		1	Rising edge of the DDS4 output MSB. This can be used when the SRAM contains a list of DDS tuning words.		
1	RESERVED			0	R$\overline{W}$
0	TW_MEM_EN		Enables DDS tuning word input coming from SRAM reading using START_ADDR1. Because tuning word is 24 bits and SRAM data is 12 bits, 12 bits are set to 0s depending on the value of the TW_MEM_SHIFT bits in the TW_RAM_CONFIG register.	0	R$\overline{W}$
		0	Selects the DDS_TW registers as the source for DDS tuning words (default)		
		1	Selects the SRAM and DDS_TW registers as configured in the TW_RAM_CONFIG register as the source of DDS tuning word input.		

TW_RAM_CONFIG Register (TW_RAM_CONFIG, Address 0x47)

Table 65. Bit Descriptions for TW_RAM_CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x000	R$\overline{W}$
[4:0]	TW_MEM_SHIFT		TW_MEM_EN must be set to 1 to use this bit field.	0x00	R$\overline{W}$
		0x00	DDSTW = (RAM[11:0],12'b0)		
		0x01	DDSTW = (DDSTW[23],RAM[11:0],11'b0)		
		0x02	DDSTW = (DDSTW[23:22],RAM[11:0],10'b0)		
		0x03	DDSTW = (DDSTW[23:21],RAM[11:0],9'b0)		
		0x04	DDSTW = (DDSTW[23:20],RAM[11:0],8'b0)		
		0x05	DDSTW = (DDSTW[23:19],RAM[11:0],7'b0)		
		0x06	DDSTW = (DDSTW[23:18],RAM[11:0],6'b0)		
		0x07	DDSTW = (DDSTW[23:17],RAM[11:0],5'b0)		
		0x08	DDSTW = (DDSTW[23:16],RAM[11:0],4'b0)		
		0x09	DDSTW = (DDSTW[23:15],RAM[11:0],3'b0)		
		0x0A	DDSTW = (DDSTW[23:14],RAM[11:0],2'b0)		
		0x0B	DDSTW = (DDSTW[23:13],RAM[11:0],1'b0)		
		0x0C	DDSTW = (DDSTW[23:12],RAM[11:0])		
		0x0D	DDSTW = (DDSTW[23:11],RAM[11:1])		
		0x0E	DDSTW = (DDSTW[23:10],RAM[11:2])		
		0x0F	DDSTW = (DDSTW[23:9],RAM[11:3])		
		0x10	DDSTW = (DDSTW[23:8],RAM[11:4])		
		0x11 to 0x1F	Reserved.		

Start Delay4 Register (START_DLY4, Address 0x50)

Table 66. Bit Descriptions for START_DLY4

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	START_DELAY4		Start delay of DAC4.	0x0000	R$\overline{W}$

Start Address4 Register (START_ADDR4, Address 0x51)

Table 67. Bit Descriptions for START_ADDR4

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	START_ADDR4		RAM address where DAC4 starts to read waveform.	0x000	R$\overline{W}$
[3:0]	RESERVED			0x0	R$\overline{W}$

Stop Address4 Register (STOP_ADDR4, Address 0x52)

Table 68. Bit Descriptions for STOP_ADDR4

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	STOP_ADDR4		RAM address where DAC4 stops to read waveform.	0x000	R$\overline{W}$
[3:0]	RESERVED			0x0	R$\overline{W}$

DDS Cycle4 Register (DDS_CYC4, Address 0x53)

Table 69. Bit Descriptions for DDS_CYC4

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS_CYC4		Number of sine wave cycles when DDS Prestored waveform using START_DELAYx and PATTERN_PERIOD is selected for DAC4 output.	0x0001	R$\overline{W}$

Start Delay3 Register (START_DLY3, Address 0x54)

Table 70. Bit Descriptions for START_DLY3

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	START_DELAY3		Start delay of DAC3.	0x0000	R$\overline{W}$

Start Address3 Register (START_ADDR3, Address 0x55)

Table 71. Bit Descriptions for START_ADDR3

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	START_ADDR3		RAM address where DAC3 starts to read waveform.	0x000	R$\overline{W}$
[3:0]	RESERVED			0x0	R$\overline{W}$

Stop Address3 Register (STOP_ADDR3, Address 0x56)

Table 72. Bit Descriptions for STOP_ADDR3

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	STOP_ADDR3		RAM address where DAC3 stops to read waveform.	0x000	R$\overline{W}$
[3:0]	RESERVED			0x0	R$\overline{W}$

REGISTER MAP

DDS Cycles3 Register (DDS_CYC3, Address 0x57)

Table 73. Bit Descriptions for DDS_CYC3

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS_CYC3		Number of sine wave cycles when DDS Prestored waveform using START_DELAYx and PATTERN_PERIOD is selected for DAC3 output.	0x0001	RW̄

Start Delay2 Register (START_DLY2, Address 0x58)

Table 74. Bit Descriptions for START_DLY2

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	START_DELAY2		Start delay of DAC2.	0x0000	RW̄

Start Address2 Register (START_ADDR2, Address 0x59)

Table 75. Bit Descriptions for START_ADDR2

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	START_ADDR2		RAM address where DAC2 starts to read waveform.	0x000	RW̄
[3:0]	RESERVED			0x0	RW̄

Stop Address2 Register (STOP_ADDR2, Address 0x5A)

Table 76. Bit Descriptions for STOP_ADDR2

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	STOP_ADDR2		RAM address where DAC2 stops to read waveform.	0x000	RW̄
[3:0]	RESERVED			0x0	RW̄

DDS Cycle2 Register (DDS_CYC2, Address 0x5B)

Table 77. Bit Descriptions for DDS_CYC2

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS_CYC2		Number of sine wave cycles when DDS Prestored waveform using START_DELAYx and PATTERN_PERIOD is selected for DAC2 output.	0x0001	RW̄

Start Delay1 Register (START_DLY1, Address 0x5C)

Table 78. Bit Descriptions for START_DLY1

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	START_DELAY1		Start delay of DAC1.	0x0000	RW̄

Start Address1 Register (START_ADDR1, Address 0x5D)

Table 79. Bit Descriptions for START_ADDR1

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	START_ADDR1		RAM address where DAC1 starts to read waveform.	0x000	RW̄
[3:0]	RESERVED			0x0	RW̄

REGISTER MAP

Stop Address1 Register (STOP_ADDR1, Address 0x5E)

Table 80. Bit Descriptions for STOP_ADDR1

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	STOP_ADDR1		RAM address where DAC1 stops to read waveform.	0x000	R$\overline{W}$
[3:0]	RESERVED			0x0	R$\overline{W}$

DDS Cycle1 Register (DDS_CYC1, Address 0x5F)

Table 81. Bit Descriptions for DDS_CYC1

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS_CYC1		Number of sine wave cycles when DDS Prestored waveform using START_DELAYx and PATTERN_PERIOD is selected for DAC1 output.	0x0001	R$\overline{W}$

Configuration Error Register (CFG_ERROR, Address 0x60)

Table 82. Bit Descriptions for CFG_ERROR

Bits	Bit Field Name	Settings	Description	Reset	Access
15	ERROR_CLEAR		Writing this bit clears all errors.	0	R$\overline{W}$
[14:6]	RESERVED			0x000	R
5	DOUT_START_LG_ERR		When the DOUT_START value is larger than the pattern delay, this error is toggled.	0	R
4	PAT_DLY_SHORT_ERR		When the pattern delay value is smaller than the default value, this error is toggled. The actual PATTERN_DELAY_SHORT is 65536 − (14 − PATTERN_DELAY_SHORT).	0	R
3	DOUT_START_SHORT_ERR		When the DOUT_START value is smaller than the default value, this error is toggled. The actual DOUT_START is 65536 − (3 − DOUT_START).	0	R
2	PERIOD_SHORT_ERR		When the period register setting value is smaller than the pattern play cycle, this error is toggled.	0	R
1	ODD_ADDR_ERR		When the memory pattern play is not even in length in trigger delay mode, this error flag is toggled.	0	R
0	MEM_READ_ERR		When there is a memory read conflict, this error flag is toggled.	0	R

SRAM Data Register (SRAM_DATA, Address 0x6000 to Address 0x6FFF)

Table 83. Bit Descriptions for SRAM_DATA

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	SRAM_DATA		SRAM_DATA[11:4]. The 8 MSBs of the programmable 12-bit SRAM_DATA.	0x00	R$\overline{W}$
[7:4]	SRAM_DATA		SRAM_DATA[3:0]. The 4 LSBs of the programmable 12-bit SRAM_DATA.	0x0	R$\overline{W}$
[3:0]	RESERVED			0x0	R$\overline{W}$

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CP-32-12	LFCSP	32-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD9106BCPZ	−40°C to +85°C	32-Lead LFCSP	Tray, 490	CP-32-12
AD9106BCPZRL7	−40°C to +85°C	32-Lead LFCSP	Reel, 1500	CP-32-12

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
AD9106ARDZ-EBZ	Evaluation Board

[1] Z = RoHS Compliant Part.