Data Sheet

AD9176S

Commercial Space Product

Dual, 16-Bit, 12.6 GSPS RF DAC with Wideband Channelizers

FEATURES

- Supports multiband wireless applications
  - 3 bypassable, complex data input channels per RF DAC
  - 3.08 GSPS maximum complex input data rate per input channel
  - 1 independent NCO per input channel
- Proprietary, low spurious and distortion design
  - 2-tone IMD3 = −83 dBc at 1.84 GHz, −7 dBFS/tone RF output
  - SFDR < −80 dBc at 1.84 GHz, −7 dBFS RF output
- Flexible 8-lane, 15.4 Gbps JESD204B interface
  - Supports single-band and multiband use cases
  - Supports 12-bit high density mode for increased data throughput
- Multiple chip synchronization
  - Supports JESD204B Subclass 1
- Selectable interpolation filter for a complete set of input data rates
  - 1×, 2×, 3×, 4×, 6×, and 8× configurable data channel interpolation
  - 1×, 2×, 4×, 6×, 8×, and 12× configurable final interpolation
- Final 48-bit NCO that operates at the DAC rate to support frequency synthesis up to 6 GHz
- Transmit enable function allows extra power saving and downstream circuitry protection
- High performance, low noise PLL clock multiplier
  - Supports 12.6 GSPS DAC update rate
  - Observation ADC clock driver with selectable divide ratios
- Low power
  - 2.54 W with 2 DACs at 12 GSPS, DAC PLL on
- 10 mm × 10 mm, 144-ball BGA_ED with metal enhanced thermal lid, 0.80 mm pitch

COMMERCIAL SPACE FEATURES

- Supports aerospace applications
- Certificate of Conformance
- Wafer diffusion lot traceability
- Burn-in, life test, and deltas analysis
- Radiation lot acceptance test (RLAT):
  - Total ionizing dose (TID)
- Radiation benchmark:
  - Single event latch-up (SEL)

APPLICATIONS

- Geosynchronous high throughput satellite (GEO HTS)
- Wireless communications infrastructure
  - Multiband base station radios
  - Microwave/E-band backhaul systems
- Instrumentation, automatic test equipment (ATE)
- Radars and jammers

FUNCTIONAL BLOCK DIAGRAM

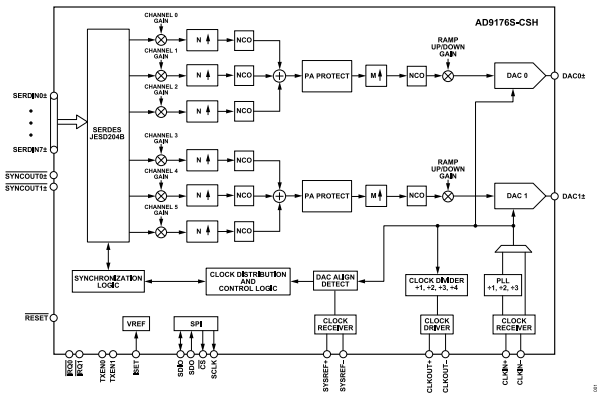

Figure 1.

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

TABLE OF CONTENTS

REVISION HISTORY

3/2023—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9176S-CSH is a high performance, dual, 16-bit, digital-to-analog converter (DAC) that supports DAC sample rates up to 12.6 GSPS. The device features an 8-lane, 15.4 Gbps JESD204B data input port, a high performance, on-chip DAC clock multiplier, and digital signal processing capabilities targeted at single-band and multiband direct to RF wireless applications.

The AD9176S-CSH features three complex data input channels per RF DAC datapath. Each input channel is fully bypassable. Each data input channel (or channelizer) includes a configurable gain stage, an interpolation filter, and a channel numerically controlled oscillator (NCO) for flexible, multiband frequency planning. The AD9176S-CSH supports an input data rate of up to a 3.08 GSPS complex (inphase/quadrature (I/Q)), or up to 6.16 GSPS non-complex (real), and is capable of allocating multiple complex input data streams to the assigned channels for individual processing. Each group of three channelizers is summed into a respective main datapath for additional processing when needed. Each main datapath includes an interpolation filter and one 48-bit main NCO ahead of the RF DAC core. Using the modulator switch, the outputs of a main datapath can be either routed to DAC0 alone for operating as a single DAC, or routed to both DAC0 and DAC1 for operating as a dual, intermediate frequency DAC (IF DAC).

The AD9176S-CSH also supports ultrawide data rate modes that allow bypassing the channelizers and main datapaths to provide maximum data rates of up to 6.16 GSPS as a single, 16-bit DAC, up to 3.08 GSPS as a dual, 16-bit DAC, or up to 4.1 GSPS as a dual, 12-bit DAC.

The AD9176S-CSH is available in a 144-ball BGA_ED package.

Additional application and technical information can be found in the Commercial Space Products Program brochure and the AD9176 data sheet.

PRODUCT HIGHLIGHTS

1. A low power, multichannel, dual DAC design reduces power consumption in higher bandwidth and multichannel applications, while maintaining performance.
2. Supports single-band and multiband wireless applications with three bypassable complex data channels per RF DAC, or configurations that use the two main datapaths as two wide-band complex data channels when using the built in modulator switch.
3. A maximum complex data rate (per I or Q) of up to 3.08 GSPS with 16-bit resolution, and up to 4.1 GSPS with 12-bit resolution. The AD9176S-CSH can be alternatively configured as a dual DAC, with each DAC operating across an independent JESD204B link, at the previously described data rates.
4. Ultrawide bandwidth single-DAC modes, supporting up to 6.16 GSPS data rates with 16-bit resolution.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 1.

Parameter	Test Conditions/Comments	Temperature (T_A)[1]	Min	Typ	Max	Unit
RESOLUTION		Full	16			Bit
ACCURACY						
Integral Nonlinearity (INL)		Full	−30		+23	LSB
		25°C	−30	±7	+23	LSB
Differential Nonlinearity (DNL)		Full	−18		+18	LSB
		25°C	−18	±7	+18	LSB
ANALOG OUTPUTS (DAC0+, DAC0−, DAC1+, DAC1−)						
Gain Error (with Internal ISET Reference)		Full	−7		+13	%
		25°C	−7		+13	%
Full-Scale Output Current						
Minimum	R_{SET} = 5 kΩ	Full	14.2	16	17.8	mA
Maximum	R_{SET} = 5 kΩ	Full	23.6	26	28.8	mA
Common-Mode Voltage		25°C		0		V
Differential Impedance		25°C		100		Ω
DAC DEVICE CLOCK INPUT (CLKIN+, CLKIN−)						
Differential Input Power	R_{LOAD} = 100 Ω differential on-chip					
Minimum		25°C		0		dBm
Maximum		25°C		6		dBm
Differential Input Impedance[2]		25°C		100		Ω
Common-Mode Voltage	AC-coupled	25°C		0.5		V
CLOCK OUTPUT DRIVER (CLKOUT+, CLKOUT−)						
Differential Output Power						
Minimum		25°C		−9		dBm
Maximum		25°C		0		dBm
Differential Output Impedance		25°C		100		Ω
Common-Mode Voltage	AC-coupled	Full		0.5		V
		25°C	0.23		0.78	V
Output Frequency		Full	727.5		3000	MHz
TEMPERATURE DRIFT						
Gain		25°C		10		ppm/°C
REFERENCE						
Internal Reference Voltage		Full		0.495		V
ANALOG SUPPLY VOLTAGES						
AVDD1.0		Full	0.95	1.0	1.05	V
AVDD1.8		Full	1.71	1.8	1.89	V

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Temperature (T_A)[1]	Min	Typ	Max	Unit
DIGITAL SUPPLY VOLTAGES						
DVDD1.0		Full	0.95	1.0	1.05	V
DAVDD1.0		Full	0.95	1.0	1.05	V
DVDD1.8		Full	1.71	1.8	1.89	V
SERIALIZER/DESERIALIZER (SERDES) SUPPLY VOLTAGES						
SVDD1.0		Full	0.95	1.0	1.05	V

[1] Full means T_A = −40°C to +85°C.

[2] See the AD9176 data sheet for more details.

DIGITAL SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC UPDATE RATE					
Minimum				2.91	GSPS
Maximum[1]	16-bit resolution, with interpolation	12.6			GSPS
	16-bit resolution, no interpolation	6.16			GSPS
Adjusted[2]	16-bit resolution, with interpolation	3.08			GSPS
	16-bit resolution, no interpolation	6.16			GSPS
DAC PHASE-LOCKED LOOP (PLL) VOLTAGE CONTROLLED OSCILLATOR (VCO) FREQUENCY RANGES					
VCO Output Divide by 1		8.74		12.42	GSPS
VCO Output Divide by 2		4.37		6.21	GSPS
VCO Output Divide by 3		2.91		4.14	GSPS
PHASE FREQUENCY DETECT INPUT FREQUENCY RANGE		25		770	MHz
DAC DEVICE CLOCK INPUT (CLKIN+, CLKIN−) FREQUENCY RANGES					
PLL Off		2.91		12.6	GHz
PLL On	M divider set to divide by 1	25		770	MHz
	M divider set to divide by 2	50		1540	MHz
	M divider set to divide by 3	75		2310	MHz
	M divider set to divide by 4	100		3080	MHz

[1] The maximum DAC update rate varies depending on the selected JESD204B mode and the lane rate for the given configuration used. The maximum DAC rate according to lane rate and voltage supply levels is listed in Maximum DAC Sampling Rate Specifications.

[2] For adjusted DAC update rate, see the AD9176 data sheet for more details.

SPECIFICATIONS

MAXIMUM DAC SAMPLING RATE SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DAC UPDATE RATE					
SVDD1.0 = 1.0 V ± 5%	Lane rate > 11 Gbps	11.67			GSPS
	Lane rate ≤ 11 Gbps	12.37			GSPS
SVDD1.0 = 1.0 V ± 2.5%	Lane rate > 11 Gbps	11.79			GSPS
	Lane rate ≤ 11 Gbps[1]	12.6			GSPS

[1] If using the on-chip PLL, the maximum DAC speed is limited to the maximum PLL speed of 12.42 GSPS, as listed in Table 2.

POWER SUPPLY DC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 4.

Parameter	Test Conditions/Comments	Temperature (T_A)[1]	Min	Typ	Max	Unit
DUAL LINK MODES						
Mode 1 (L = 2, M = 4, NP = 16, N = 16)	11.7965 GSPS DAC rate, 184.32 MHz PLL reference clock, 32× total interpolation (4×, 8×), 40 MHz tone at −3 dBFS, channel gain = −6 dB, channel NCOs = ±150 MHz, main NCO = 2 GHz, $\overline{\text{SYNCOUTx±}}$ in LVDS mode					
AVDD1.0	All supply levels set to nominal values	Full	540		1020	mA
		25°C	540		895	mA
	All supply levels set to 5% tolerance	Full		775	1120	mA
AVDD1.8		Full	88		130	mA
		25°C	88		127	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply					
	All supply levels set to nominal values	Full	550		1670	mA
		25°C	550		1525	mA
	All supplies at 5% tolerance	Full		1170	1850	mA
DVDD1.8		Full	19		50	mA
		25°C	19		35	mA
SVDD1.0	All supply levels set to nominal values	Full	170		510	mA
		25°C	170		390	mA
	All supplies at 5% tolerance	Full		305	560	mA
Total Power Dissipation		Full	1.90		3.38	W
		25°C	1.90		3.10	W
Mode 4 (L = 4, M = 4, NP = 16, N = 16)	11.7965 GSPS DAC rate, 491.52 MHz PLL reference clock, 24× total interpolation (3×, 8×), 40 MHz tone at −3 dBFS, channel gain = −6 dB, channel NCOs = ±150 MHz, main NCO = 2 GHz, $\overline{\text{SYNCOUTx±}}$ in LVDS mode					
AVDD1.0		25°C		725		mA
AVDD1.8		25°C		110		mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply	25°C		1150		mA

SPECIFICATIONS

Table 4. (Continued)

Parameter	Test Conditions/Comments	Temperature (T_A)[1]	Min	Typ	Max	Unit
DVDD1.8		25°C		35		mA
SVDD1.0		25°C		425		mA
Total Power Dissipation		25°C		2.56		W
Mode 0 (L = 1, M = 2, NP = 16, N = 16)	5.89824 GSPS DAC rate, 184.32 MHz PLL reference clock, 16× total interpolation (2×, 8×), 40 MHz tone at −3 dBFS, channel NCO disabled, main NCO = 1.8425 GHz, $\overline{\text{SYNCOUTx±}}$ in LVDS mode					
AVDD1.0	All supply levels set to nominal values	Full		400	670	mA
	All supplies at 5% tolerance	Full		425	745	mA
AVDD1.8		Full		110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply					
	All supply levels set to nominal values	Full		570	960	mA
	All supplies at 5% tolerance	Full		610	1070	mA
DVDD1.8		Full		35	50	mA
SVDD1.0		Full		175	340	mA
Total Power Dissipation		Full		1.40	2.15	W
Mode 3 (L = 2, M = 2, NP = 16, N = 16)	11.7965 GSPS DAC rate, 184.32 MHz PLL reference clock, 24× total interpolation (3×, 8×), 40 MHz tone at −3 dBFS, channel NCO disabled, main NCO = 2.655 GHz, $\overline{\text{SYNCOUTx±}}$ in LVDS mode					
AVDD1.0	All supply levels set to nominal values	25°C		725		mA
	All supplies at 5% tolerance	25°C		775		mA
AVDD1.8		25°C		110		mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply					
	All supply levels set to nominal values	25°C		1020		mA
	All supplies at 5% tolerance	25°C		1070		mA
DVDD1.8		25°C		35		mA
SVDD1.0	All supply levels set to nominal values	25°C		245		mA
	All supplies at 5% tolerance	25°C		250		mA
Total Power Dissipation		25°C		2.25		W
Mode 9 (L = 4, M = 2, NP = 16, N = 16)	12 GSPS DAC rate, 187.5 MHz PLL reference clock, 8× total interpolation (1×, 8×), 10 MHz tone at −3 dBFS, channel NCO disabled, main NCO = 3.072 GHz, $\overline{\text{SYNCOUTx±}}$ in LVDS mode					
AVDD1.0	All supply levels set to nominal values	Full		740	1030	mA
	All supplies at 5% tolerance	Full		785	1135	mA
AVDD1.8		Full		110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply					
	All supply levels set to nominal values	Full		1010	1580	mA
	All supplies at 5% tolerance	Full		1070	1740	mA
DVDD1.8		Full		35	50	mA
SVDD1.0	All supply levels set to nominal values	Full		530	840	mA
	All supplies at 5% tolerance	Full		550	910	mA
Total Power Dissipation		Full		2.54	3.63	W
Mode 2 (L = 3, M = 6, NP = 16, N = 16)	12 GSPS DAC rate, 375 MHz PLL reference clock, 48× total interpolation (6×, 8×), 30 MHz tone at −3 dBFS, channel gain = −11 dB, channel NCOs = 20 MHz, main NCO = 2.1 GHz					
AVDD1.0	All supply levels set to nominal values	Full		735	1030	mA
	All supplies at 5% tolerance	Full		785	1135	mA

SPECIFICATIONS

Table 4. (Continued)

Parameter	Test Conditions/Comments	Temperature (T_A)[1]	Min	Typ	Max	Unit
AVDD1.8		Full		110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply					
	All supply levels set to nominal values	Full		1370	1800	mA
	All supplies at 5% tolerance	Full		1460	1980	mA
DVDD1.8		Full		35	50	mA
SVDD1.0	All supply levels set to nominal values	Full		410	680	mA
	All supplies at 5% tolerance	Full		430	755	mA
Total Power Dissipation		Full		2.77	3.69	W
SINGLE-LINK MODES						
Mode 20 (L = 8, M = 1, NP = 16, N = 16)	6 GSPS DAC rate, 187.5 MHz PLL reference clock, 1× total interpolation (1×, 1×), 1.8 GHz tone at −3 dBFS, channel and main NCOs disabled					
AVDD1.0	All supply levels set to nominal values	Full		400	670	mA
	All supplies at 5% tolerance	Full		430	745	mA
AVDD1.8		Full		75	100	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply					
	All supply levels set to nominal values	Full		390	700	mA
	All supplies at 5% tolerance	Full		410	810	mA
DVDD1.8		Full		35	50	mA
SVDD1.0	All supply levels set to nominal values	Full		525	820	mA
	All supplies at 5% tolerance	Full		550	880	mA
Total Power Dissipation		Full		1.51	2.34	W
Mode 12 (L = 8, M = 2, NP = 12, N = 12)	4 GSPS DAC rate, 187.5 MHz PLL reference clock, 1× total interpolation (1×, 1×), 1 GHz tone at −3 dBFS, channel and main NCOs disabled					
AVDD1.0	All supply levels set to nominal values	Full		300	550	mA
	All supplies at 5% tolerance	Full		315	620	mA
AVDD1.8		Full		75	100	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply					
	All supply levels set to nominal values	Full		320	630	mA
	All supplies at 5% tolerance	Full		350	725	mA
DVDD1.8		Full		35	50	mA
SVDD1.0	All supply levels set to nominal values	Full		525	820	mA
	All supplies at 5% tolerance	Full		550	880	mA
Total Power Dissipation		Full		1.34	2.15	W
DUAL-LINK, MODE 3 (NCO ONLY, SINGLE-CHANNEL MODE, NO SERDES)	6 GSPS DAC rate, 300 MHz PLL reference clock, 8× total interpolation (1×, 8×), no input tone (dc internal level = 0x50FF), channel NCO = 40 MHz, main NCO = 1.8425 GHz					
AVDD1.0						
	All supply levels set to nominal values	Full		410	660	mA
	All supplies at 5% tolerance	Full		435	750	mA
AVDD1.8		Full		110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply					
	All supply levels set to nominal values	Full		500	780	mA
	All supplies at 5% tolerance	Full		515	950	mA
DVDD1.8		Full		0.3	1	mA
SVDD1.0	All supply levels set to nominal values	Full		5	100	mA
	All supplies at 5% tolerance	Full		3	120	mA

SPECIFICATIONS

Table 4. (Continued)

Parameter	Test Conditions/Comments	Temperature (T_A)[1]	Min	Typ	Max	Unit
Total Power Dissipation		Full		1.11	1.671	W
DUAL-LINK, MODE 4 (NCO ONLY, DUAL-CHANNEL MODE, NO SERDES)	12 GSPS DAC rate, 500 MHz PLL reference clock, 32× total interpolation (4×, 8×), no input tone (DC internal level = 0x2AFF), channel NCOs = ±150 MHz, main NCO = 2 GHz					
AVDD1.0	All supply levels set to nominal values	Full		750	1030	mA
	All supplies at 5% tolerance	Full		790	1130	mA
AVDD1.8		Full		110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply					
	All supply levels set to nominal values	Full		1200	1590	mA
	All supplies at 5% tolerance	Full		1300	1750	mA
DVDD1.8		Full		0.3	1	mA
SVDD1.0		Full		5	100	mA
Total Power Dissipation		Full		2.15	2.851	W

[1] Full means T_A = −40°C to +85°C.

SERIAL PORT AND CMOS PIN SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 5.

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
WRITE OPERATION		See the AD9176 data sheet for more details				
Maximum SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$		80			MHz
SCLK Clock High	t_{PWH}	SCLK = 20 MHz	5.03			ns
SCLK Clock Low	t_{PWL}	SCLK = 20 MHz	1.6			ns
SDIO to SCLK Setup Time	t_{DS}		1.154			ns
SCLK to SDIO Hold Time	t_{DH}		0.577			ns
$\overline{CS}$ to SCLK Setup Time	t_S		1.036			ns
SCLK to $\overline{CS}$ Hold Time	t_H		−5.3			ps
READ OPERATION		See the AD9176 data sheet for more details				
SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$				48.58	MHz
SCLK Clock High	t_{PWH}		5.03			ns
SCLK Clock Low	t_{PWL}		1.6			ns
SDIO to SCLK Setup Time	t_{DS}		1.158			ns
SCLK to SDIO Hold Time	t_{DH}		0.537			ns
$\overline{CS}$ to SCLK Setup Time	t_S		1.036			ns
SCLK to SDIO Data Valid Time	t_{DV}		9.6			ns
SCLK to SDO Data Valid Time	t_{DV}		13.7			ns
$\overline{CS}$ to SDIO Output Valid to High-Z		See the AD9176 data sheet for more details	5.4			ns
$\overline{CS}$ to SDO Output Valid to High-Z		See the AD9176 data sheet for more details	9.59			ns
INPUTS (SDIO, SCLK, $\overline{CS}$, $\overline{RESET}$, TXEN0, and TXEN1)						

SPECIFICATIONS

Table 5. (Continued)

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
Voltage Input						
High	V_{IH}		1.48			V
Low	V_{IL}				0.425	V
Current Input						
High	I_{IH}				±100	nA
Low	I_{IL}		±100			nA
OUTPUTS (SDIO, SDO)						
Voltage Output						
High	V_{OH}					
0 mA load			1.69			V
4 mA load			1.52			V
Low	V_{OL}					
0 mA load					0.045	V
4 mA load					0.175	V
Current Output						
High	I_{OH}			4		mA
Low	I_{OL}			4		mA
INTERRUPT OUTPUTS ($\overline{IRQ0}$, $\overline{IRQ1}$)						
Voltage Output						
High	V_{OH}		1.71			V
Low	V_{OL}				0.075	V

DIGITAL INPUT DATA TIMING SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LATENCY[1]					
Channel Interpolation Factor, Main Datapath Interpolation Factor	LMFC_VAR_x = 12, LMFC_DELAY_x = 12, unless otherwise noted				
1×, 1×[2]	JESD204B Mode 10,[3] Mode 18[3]		420		DAC clock cycles
	JESD204B Mode 11, Mode 19		440		DAC clock cycles
	JESD204B Mode 12, Mode 19		590		DAC clock cycles
	JESD204B Mode 20[3]		700		DAC clock cycles
	JESD204B Mode 21		750		DAC clock cycles
1×, 2×[2]	JESD204B Mode 8[3]		670		DAC clock cycles
	JESD204B Mode 9		700		DAC clock cycles
1×, 4×[2]	JESD204B Mode 8[3]		1090		DAC clock cycles
	JESD204B Mode 9		1140		DAC clock cycles
1×, 6×[2]	JESD204B Mode 8[3]		1460		DAC clock cycles
	JESD204B Mode 9		1530		DAC clock cycles
1×, 8×[2]	JESD204B Mode 3		1390		DAC clock cycles
	JESD204B Mode 8[3]		1820		DAC clock cycles
	JESD204B Mode 9		1920		DAC clock cycles
1×, 12×[2]	JESD204B Mode 8[3]		2700		DAC clock cycles
	JESD204B Mode 9		2840		DAC clock cycles

SPECIFICATIONS

Table 6. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
2×, 6×[2]	JESD204B Mode 3, Mode 4		1970		DAC clock cycles
	JESD204B Mode 5		1770		DAC clock cycles
2×, 8×[2]	JESD204B Mode 0		2020		DAC clock cycles
	JESD204B Mode 3, Mode 4		2500		DAC clock cycles
3×, 6×[2]	JESD204B Mode 3, Mode 4		2880		DAC clock cycles
	JESD204B Mode 5, Mode 6		2630		DAC clock cycles
3×, 8×[2]	JESD204B Mode 3, Mode 4		3310		DAC clock cycles
	JESD204B Mode 5, Mode 6		2980		DAC clock cycles
4×, 6×[2]	JESD204B Mode 0, Mode 1, Mode 2		2410		DAC clock cycles
4×, 8×[2]	JESD204B Mode 0, Mode 1, Mode 2		3090		DAC clock cycles
6×, 6×[2]	JESD204B Mode 0, Mode 1, Mode 2		3190		DAC clock cycles
6×, 8×[2]	JESD204B Mode 0, Mode 1, Mode 2		4130		DAC clock cycles
8×, 6×[2]	JESD204B Mode 7		3300		DAC clock cycles
8×, 8×[2]	JESD204B Mode 7		4270		DAC clock cycles
DETERMINISTIC LATENCY					
Fixed				13	PCLK[4]
Variable				2	PCLK cycles
SYSREF± TO LMFC DELAY			0		DAC clock cycles

[1] Total latency (or pipeline delay) through the device is calculated as follows: total latency = interface latency + fixed latency + variable latency + pipeline delay.

[2] The first value listed in this specification is the channel interpolation factor, and the second value is the main datapath interpolation factor.

[3] LMFC_VAR_x = 7 and LMFC_DELAY_x = 4

[4] PCLK is the internal processing clock for the AD9176S-CSH and equals the lane rate ÷ 40.

JESD204B INTERFACE ELECTRICAL AND SPEED SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B SERIAL INTERFACE RATE (SERIAL LANE RATE)			3		15.4	Gbps
JESD204B DATA INPUTS						
Input Leakage Current		T_A = 25°C				
Logic High		Input level = 1.0 V ± 0.25 V		10		µA
Logic Low		Input level = 0 V		−4		µA
Unit Interval	UI		333		66.7	ps
Common-Mode Voltage	V_{RCM}	AC-coupled	−0.05		+1.1	V
Differential Voltage	R_V_{DIFF}		110		1050	mV
Differential Impedance	Z_{RDIFF}	At DC	80	100	120	Ω
SYSREF± INPUT						
Differential Impedance				100		Ω
DIFFERENTIAL OUTPUTS ($\overline{SYNCOUT0±}$, $\overline{SYNCOUT1±}$)[1]		Driving 100 Ω differential load				
Output Differential Voltage	V_{OD}		320	390	460	mV
Output Offset Voltage	V_{OS}		1.08	1.12	1.15	V
SINGLE-ENDED OUTPUTS ($\overline{SYNCOUT0±}$, $\overline{SYNCOUT1}$)		Driving 100 Ω differential load				
Output Voltage						
High	V_{OH}		1.69			V

SPECIFICATIONS

Table 7. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Low	V_{OL}				0.045	V
Current Output						
High	I_{OH}			0		mA
Low	I_{OL}			0		mA

[1] IEEE Standard 1596.3 LVDS compatible.

INPUT DATA RATES AND SIGNAL BANDWIDTH SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 8.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT DATA RATE PER INPUT CHANNEL					
	Channel datapaths bypassed (1× interpolation), single DAC mode, 16-bit resolution			6160	MSPS
	Channel datapaths bypassed (1× interpolation), dual DAC mode, 16-bit resolution			3080	MSPS
	Channel datapaths bypassed (1× interpolation), dual DAC mode, 12-bit resolution			4100	MSPS
	1 complex channel enabled			3080	MSPS
	2 complex channels enabled			770	MSPS
	3 complex channels enabled			385	MSPS
COMPLEX SIGNAL BANDWIDTH PER INPUT CHANNEL					
	1 complex channel enabled (0.8 × f_{DATA})			1232	MHz
	2 complex channels enabled (0.8 × f_{DATA})			616	MHz
	3 complex channels enabled (0.8 × f_{DATA})			308	MHz
MAXIMUM NCO CLOCK RATE					
Channel NCO				1540	MHz
Main NCO				12.6	GHz
MAXIMUM NCO SHIFT FREQUENCY RANGE					
Channel NCO	Channel summing node = 1.575 GHz, channel interpolation rate > 1×	−770		+770	MHz
Main NCO	f_{DAC} = 12.6 GHz, main interpolation rate > 1×	−6.3		+6.3	GHz
MAXIMUM FREQUENCY SPACING ACROSS INPUT CHANNELS	Maximum NCO output frequency × 0.8			1232	MHz

[1] Values listed for these parameters are the maximum possible when considering all JESD204B modes of operation. Some modes are more limiting, based on other parameters.

AC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 9.

Parameter	Test Conditions/Comments	Temperature (T_A)[1]	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)						

SPECIFICATIONS

Table 9. (Continued)

Parameter	Test Conditions/Comments	Temperature (T_A)[1]	Min	Typ	Max	Unit
Single Tone, f_{DAC} = 12000 MSPS, Mode 1 (L = 2, M = 4)	−7 dBFS, shuffle enabled					
f_{OUT} = 100 MHz		25°C		−81		dBc
f_{OUT} = 500 MHz		25°C		−80		dBc
f_{OUT} = 950 MHz		25°C		−75		dBc
f_{OUT} = 1840 MHz		25°C		−80		dBc
f_{OUT} = 2650 MHz		25°C		−75		dBc
f_{OUT} = 3700 MHz		25°C		−67		dBc
Single Tone, f_{DAC} = 6000 MSPS, Mode 0 (L = 1, M = 2)	−7 dBFS, shuffle enabled					
f_{OUT} = 100 MHz		25°C		−85		dBc
f_{OUT} = 500 MHz		25°C		−85		dBc
f_{OUT} = 950 MHz		25°C		−78		dBc
f_{OUT} = 1840 MHz		25°C		−75		dBc
f_{OUT} = 2650 MHz		25°C		−69		dBc
Single Tone, f_{DAC} = 3000 MSPS, Mode 10 (L = 8, M = 2)	−7 dBFS, shuffle enabled					
f_{OUT} = 100 MHz		25°C		−87		dBc
f_{OUT} = 500 MHz		25°C		−84		dBc
f_{OUT} = 950 MHz		25°C		−81		dBc
Single-Band Application, Band 3 (1805 MHz to 1880 MHz)	Mode 0, 2× to 8×, f_{DAC} = 6000 MSPS, 368.64 MHz reference clock					
SFDR Harmonics	−7 dBFS, shuffle enabled					
In-Band		25°C		−82		dBc
Digital Predistortion (DPD) Band	DPD bandwidth = data rate × 0.8	25°C		−80		dBc
Second Harmonic		Full			−61	dBc
		25°C		−82	−61	dBc
Third Harmonic		Full			−66	dBc
		25°C		−80	−66	dBc
Fourth Harmonic		Full			−77	dBc
		25°C		−95	−77	dBc
Fifth Harmonic		Full			−79	dBc
		25°C		−95	−79	dBc
SFDR Nonharmonics	−7 dBFS, shuffle enabled					
In-Band		25°C		−74		dBc
DPD Band		25°C		−74		dBc
ADJACENT CHANNEL LEAKAGE RATIO						
4-Channel Wideband Code Division Multiple Access (WCDMA)	−1 dBFS digital backoff					
f_{DAC} = 1200 MSPS, Mode 1 (L = 2, M = 4)	f_{OUT} = 1840 MHz	25°C		−70		dBc
	f_{OUT} = 2650 MHz	25°C		−68		dBc
	f_{OUT} = 3500 MHz	25°C		−66		dBc
f_{DAC} = 6000 MSPS, Mode 0 (L = 1, M = 2)	f_{OUT} = 1840 MHz	25°C		−71		dBc
	f_{OUT} = 2650 MHz	25°C		−66		dBc
THIRD-ORDER INTERMODULATION DISTORTION (IMD3)	Two-tone test, −7 dBFS/tone, 1 MHz spacing					
f_{DAC} = 12000 MSPS, Mode 1 (L = 2, M = 4)	f_{OUT} = 1840 MHz	Full			−67	dBc
		25°C		−83	−67	dBc
	f_{OUT} = 2650 MHz	25°C		−85		dBc

SPECIFICATIONS

Table 9. (Continued)

Parameter	Test Conditions/Comments	Temperature (T_A)[1]	Min	Typ	Max	Unit
	f_{OUT} = 3700 MHz	25°C		−77		dBc
f_{DAC} = 6000 MSPS, Mode 0 (L = 1, M = 2)	f_{OUT} = 1840 MHz	25°C		−74		dBc
	f_{OUT} = 2650 MHz	25°C		−72		dBc
NOISE SPECTRAL DENSITY (NSD)	0 dBFS, NSD measurement taken at 10% away from f_{OUT}, shuffle on					
Single Tone, f_{DAC} = 12000 MSPS						
f_{OUT} = 200 MHz		25°C		−163		dBc/Hz
f_{OUT} = 500 MHz		25°C		−163		dBc/Hz
f_{OUT} = 950 MHz		25°C		−162		dBc/Hz
f_{OUT} = 1850 MHz		25°C		−160		dBc/Hz
f_{OUT} = 2150 MHz		25°C		−158		dBc/Hz
Single Tone, f_{DAC} = 6000 MSPS						
f_{OUT} = 200 MHz		25°C		−164		dBc/Hz
f_{OUT} = 500 MHz		25°C		−163		dBc/Hz
f_{OUT} = 950 MHz		25°C		−161		dBc/Hz
f_{OUT} = 1850 MHz		25°C		−157		dBc/Hz
f_{OUT} = 2150 MHz		25°C		−155		dBc/Hz
Single Tone, f_{DAC} = 3000 MSPS						
f_{OUT} = 100 MHz		25°C		−163		dBc/Hz
f_{OUT} = 500 MHz		25°C		−159		dBc/Hz
f_{OUT} = 950 MHz		25°C		−155		dBc/Hz
SINGLE-SIDEBAND PHASE NOISE OFFSET	See the AD9176 data sheet for more details					
1 kHz		25°C		−97		dBc/Hz
10 kHz		25°C		−105		dBc/Hz
100 kHz		25°C		−114		dBc/Hz
600 kHz		25°C		−126		dBc/Hz
1.2 MHz		25°C		−133		dBc/Hz
1.8 MHz		25°C		−137		dBc/Hz
6 MHz		25°C		−148		dBc/Hz
DAC TO DAC OUTPUT ISOLATION	Taken using the AD9176-FMC-EBZ					
Dual Band, f_{DAC} = 12000 MSPS, Mode 1 (L = 2, M = 4)						
	f_{OUT} = 1840 MHz	25°C		−77		dB
	f_{OUT} = 2650 MHz	25°C		−70		dB
	f_{OUT} = 3700 MHz	25°C		−68		dB

[1] Full means T_A = −40°C to +85°C.

BURN-IN DELTA LIMIT SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. Delta limits apply at room temperature (T_A = 25°C) for post 240 hour burn-in test. Delta calculation is based on absolute maximum changes.

Table 10.

Parameter	Test Conditions/Comments	Delta	Unit
ANALOG OUTPUTS (DAC0+, DAC0−, DAC1+, DAC1−)			
Gain Error		±3.6	%
POWER SUPPLY DC SPECIFICATIONS			
Mode 1 (L = 2, M = 4, NP = 16, N = 16)	11.7965 GSPS DAC rate, 184.32 MHz PLL reference clock, 32× total interpolation (4×, 8×), 40 MHz tone at −3 dBFS, channel		

SPECIFICATIONS

Table 10. (Continued)

Parameter	Test Conditions/Comments	Delta	Unit
	gain = −6 dB, channel NCOs = ±150 MHz, main NCO = 2 GHz, SYNCOUTx± in LVDS mode		
AVDD1.0	All supply levels set to nominal values	±61	mA
AVDD1.8		±7	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply	±175	mA
	All supply levels set to nominal values		
DVDD1.8		±3	mA
SVDD1.0	All supply levels set to nominal values	±40	mA

RADIATION TEST AND LIMIT SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. Radiation testing is performed at room temperature (T_A = 25°C) only, which corresponds to T_J = 51°C. Total ionizing dose (TID) characterized to 100 krads.

Parameter	Test Conditions/Comments	Min	Max	Unit
DC SPECIFICATIONS				
INL		−30	+23	LSB
DNL		−18	+18	LSB
Gain Error		−18	+18	%
POWER SUPPLY SPECIFICATIONS				
Mode 1 (L = 2, M = 4, NP = 16, N = 16)	11.7965 GSPS DAC rate, 184.32 MHz PLL reference clock, 32× total interpolation (4×, 8×), 40 MHz tone at −3 dBFS, channel gain = −6 dB, channel NCOs = ±150 MHz, main NCO = 2 GHz, $\overline{\text{SYNCOUTx±}}$ in LVDS mode			
AVDD1.0	All supply levels set to nominal values		895	mA
AVDD1.8			150	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply		1525	mA
	All supply levels set to nominal values			
DVDD1.8			50	mA
SVDD1.0	All supply levels set to nominal values		390	mA
AC SPECIFICATIONS				
SFDR Harmonics				
Second Harmonic			−61	dBc
Third Harmonic			−66	dBc
Fourth Harmonic			−72	dBc
Fifth Harmonic			−77	dBc

ABSOLUTE MAXIMUM RATINGS

Table 11.

Parameter	Rating
ISET, FILT_COARSE, FILT_BYP, FILT_VCM	−0.3 V to AVDD1.8 + 0.3 V
SERDINx±	−0.2 V to SVDD1.0 + 0.2 V
SYNCOUT0±, SYNCOUT1±, RESET, TXEN0, TXEN1, IRQ0, IRQ1, CS, SCLK, SDIO, SDO	−0.3 V to DVDD1.8 + 0.3 V
DAC0±, DAC1±, CLKIN±, CLKOUT±, FILT_FINE	−0.2 V to AVDD1.0 + 0.2 V
SYSREF±	−0.2 V to DVDD1.0 + 0.2 V
AVDD1.0, DVDD1.0, SVDD1.0 to GND	−0.2 V to +1.2 V
AVDD1.8, DVDD1.8 to GND	−0.3 V to 2.2 V
Maximum Junction Temperature (T_J)[1]	118°C
Storage Temperature Range	−65°C to +150°C
Peak Reflow	235°C

[1] Some operating modes of the device may cause the device to approach or exceed the maximum junction temperature during operation at supported ambient temperatures. Removal of heat from the device may require additional measures such as active airflow, heat sinks, or other measures.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Thermal resistances and thermal characterization parameters are specified vs. the number of PCB layers in different airflow velocities (in m/sec). The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 11.

Use the values in Table 12 in compliance with JEDEC 51-12.

Table 12. Simulated Thermal Resistance vs. PCB Layers[1]

Package Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
BP-144-1					
JEDEC 2s2p Board	0.0	25.3	2.4[2]	3.0[3]	°C/W
	1.0	22.6	N/A	N/A	°C/W
	2.5	21.0	N/A	N/A	°C/W
12-Layer PCB[4]	0.0	15.4	2.4	2.6	°C/W
	1.0	13.1	N/A	N/A	°C/W
	2.5	11.6	N/A	N/A	°C/W

[1] N/A means not applicable.

[2] 1SOP PCB with no vias in PCB.

[3] 1SOP PCB with 7 × 7 standard JEDEC vias.

[4] Non JEDEC thermal resistance.

OUTGAS TESTING

The criteria used for the acceptance and rejection of materials must be determined by the user and based upon specific component and system requirements. Historically, a total mass loss (TML) of 1.00% and collected volatile condensable material (CVCM) of 0.10% have been used as screening levels for rejection of spacecraft materials.

Table 13. Outgas Testing

Specification (Tested per ASTM E595-15)	Value	Unit
Total Mass Lost	0.04	%
Collected Volatile Condensable Material	<0.01	%
Water Vapor Recovered	0.02	%

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 2. Pin Configuration

Table 14. Pin Function Descriptions

Pin No.	Mnemonic	Description
1.0 V Supply		
H3 to H5, H8 to H10, J6, M2, M11	AVDD1.0	1.0 V Clock and Analog Supplies. These pins supply the clock receivers, clock distribution, the on-chip DAC clock multiplier, and the DAC analog core. Clean power supply rail sources are required on these pins.
F5 to F8	DVDD1.0	1.0 V Digital Supplies. These pins supply power to the DAC digital circuitry. Clean power supply rail sources are required on these pins.
F4, F9	DAVDD1.0	1.0 V Digital to Analog Supplies. These pins can share a supply rail with the DVDD1.0 supply (electrically connected) but must have separate supply plane and decoupling capacitors for the PCB layout to improve isolation for these two pins. Clean power supply rail sources are required on these pins.
C1, C2, C5, C7, C8, C11, C12, D6	SVDD1.0	1.0 V SERDES Supplies to the JESD204B Data Interface. Clean power supply rail sources are required on these pins.
1.8 V Supply		
K3, K5, K7, K10, L3, L6, L7, L10	AVDD1.8	1.8 V Analog Supplies to the On-Chip DAC Clock Multiplier and the DAC Analog Core. Clean power supply rail sources are required on these pins.
C6, D3, D10, E3, E10	DVDD1.8	1.8 V Digital Supplies to the JESD204B Data Interface and the Other Input/Output Circuitry, Such as the SPI. Clean power supply rail sources are required on these pins.
Ground		
A1, A6, A7, A12, B1, B6, B7, B12, C3, C4, C9, C10, D5, D7, F1 to F3, F10 to F12, G1 to G12, H11, J1, J3 to J5, J8 to J11, K2, K8, K9, K11, K12, L2, L4, L5, L8, L9, L11, M1, M3, M6, M7, M10, M12	GND	Device Common Ground.
RF Clock		
J12	CLKIN+	Positive Device Clock Input. This pin is the clock input for the on-chip DAC clock multiplier, reference clock, when the DAC PLL is on. This pin is also the clock input for the DAC sample clock

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 14. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
		or device clock when the DAC PLL is off. AC couple this input. There is an internal 100 Ω resistor between this pin and CLKIN−.
H12	CLKIN−	Negative Device Clock Input.
K1	CLKOUT+	Positive Device Clock Output. This pin is the clock output of a divided down device clock and is available with the DAC PLL on and off. The divide down ratios are by 1, 2, 3, or 4.
L1	CLKOUT−	Negative Device Clock Output.
System Reference		
H1	SYSREF+	Positive System Reference Input. It is recommended to AC couple this pin, but DC coupling is also acceptable. See Table 7 for the Dc common-mode voltage.
H2	SYSREF−	Negative System Reference Input. It is recommended to AC couple this pin, but DC coupling is also acceptable. See Table 7 for the DC common-mode voltage.
On-Chip DAC PLL Loop Filter		
H6	FILT_FINE	On-Chip DAC Clock Multiplier and PLL Fine Loop Filter Input. If the PLL is not in use, leave this pin floating and disable the PLL via the control registers.
H7	FILT_COARSE	On-Chip DAC Clock Multiplier and PLL Coarse Loop Filter Input. If the PLL is not in use, leave this pin floating and disable the PLL via the control registers.
J7	FILT_BYP	On-Chip DAC Clock Multiplier and Low Dropout (LDO) Bypass. Add a high quality ceramic bypass capacitor between 2 µF and 10 µF at this node. Ideally, this capacitor is 10 µF X7R or better. If the PLL is not in use, leave this pin floating and disable the PLL via the control registers.
K6	FILT_VCM	On-Chip DAC Clock Multiplier and VCO Common-Mode Input. If the PLL is not in use, leave this pin floating and disable the PLL via the control registers.
SERDES Data Bits		
A2	SERDIN7+	SERDES Data Bit 7, Positive.
B2	SERDIN7−	SERDES Data Bit 7, Negative.
A3	SERDIN6+	SERDES Data Bit 6, Positive.
B3	SERDIN6−	SERDES Data Bit 6, Negative.
A4	SERDIN5+	SERDES Data Bit 5, Positive.
B4	SERDIN5−	SERDES Data Bit 5, Negative.
A5	SERDIN4+	SERDES Data Bit 4, Positive.
B5	SERDIN4−	SERDES Data Bit 4, Negative.
A8	SERDIN3+	SERDES Data Bit 3, Positive.
B8	SERDIN3−	SERDES Data Bit 3, Negative.
A9	SERDIN2+	SERDES Data Bit 2, Positive.
B9	SERDIN2−	SERDES Data Bit 2, Negative.
A10	SERDIN1+	SERDES Data Bit 1, Positive.
B10	SERDIN1−	SERDES Data Bit 1, Negative.
A11	SERDIN0+	SERDES Data Bit 0, Positive.
B11	SERDIN0−	SERDES Data Bit 0, Negative.
Synchronization Output		
D12	$\overline{\text{SYNCOUT0+}}$	Positive Synchronization (Active Low) Output Signal, Channel Link 0. This pin is LVDS or CMOS selectable.
D11	$\overline{\text{SYNCOUT0−}}$	Negative Synchronization (Active Low) Output Signal, Channel Link 0. This pin is LVDS or CMOS selectable.
D1	$\overline{\text{SYNCOUT1+}}$	Positive Synchronization (Active Low) Output Signal, Channel Link 1. This pin is LVDS or CMOS selectable.
D2	$\overline{\text{SYNCOUT1−}}$	Negative Synchronization (Active Low) Output Signal, Channel Link 1. This pin is LVDS or CMOS selectable.
Serial Port Interface		
E4	SDO	Serial Port Data Output (CMOS Levels with Respect to DVDD1.8).
E7	SDIO	Serial Port Data Input/Output (CMOS Levels with Respect to DVDD1.8).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 14. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
E5	SCLK	Serial Port Clock Input (CMOS Levels with Respect to DVDD1.8).
E6	$\overline{CS}$	Serial Port Chip Select, Active Low (CMOS Levels with Respect to DVDD1.8).
E8	$\overline{RESET}$	Reset, Active Low (CMOS Levels with Respect to DVDD1.8).
Interrupt Request		
D9	$\overline{IRQ0}$	Interrupt Request 0. This pin is an open-drain, active low output (CMOS levels with respect to DVDD1.8). Connect a pull-up resistor to DVDD1.8 to prevent this pin from floating when inactive.
E9	$\overline{IRQ1}$	Interrupt Request 1. This pin is an open-drain, active low output (CMOS levels with respect to DVDD1.8). Connect a pull-up resistor to DVDD1.8 to prevent this pin from floating when inactive.
CMOS Input/Outputs		
D8	TXEN0	Transmit Enable for DAC0. The CMOS levels are determined with respect to DVDD1.8.
D4	TXEN1	Transmit Enable for DAC1. The CMOS levels are determined with respect to DVDD1.8.
DAC Analog Outputs		
M9	DAC0+	DAC0 Positive Current Output.
M8	DAC0−	DAC0 Negative Current Output.
M4	DAC1+	DAC1 Positive Current Output.
M5	DAC1−	DAC1 Negative Current Output.
Reference		
L12	ISET	Device Bias Current Setting Pin. Connect a 5 kΩ resistor from this pin to GND, preferably with <0.1% tolerance and <±25 ppm/°C temperature coefficient.
Do Not Connect		
E1, E2, E11, E12, J2, K4	DNC	Do Not Connect. Do not connect to these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

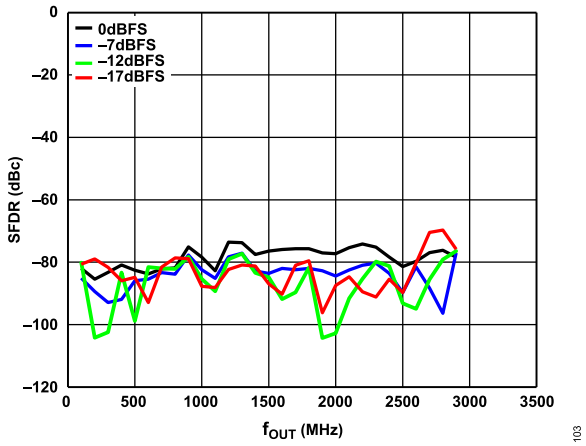

Figure 3. Second Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×

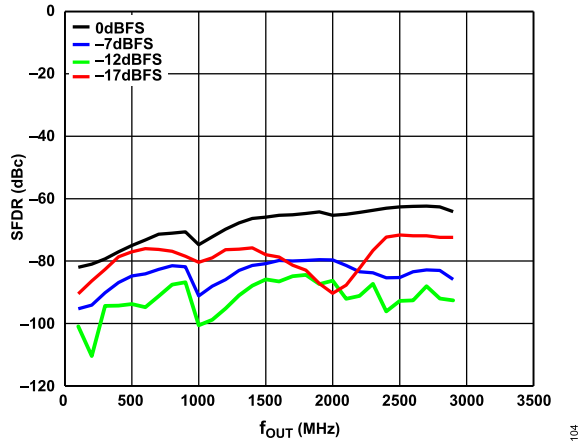

Figure 4. Third Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×

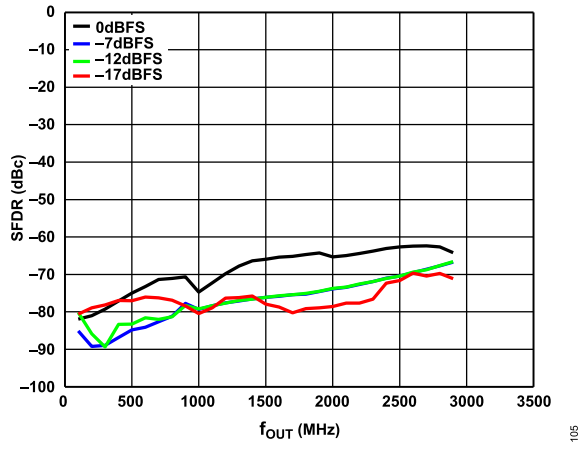

Figure 5. Worst Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×

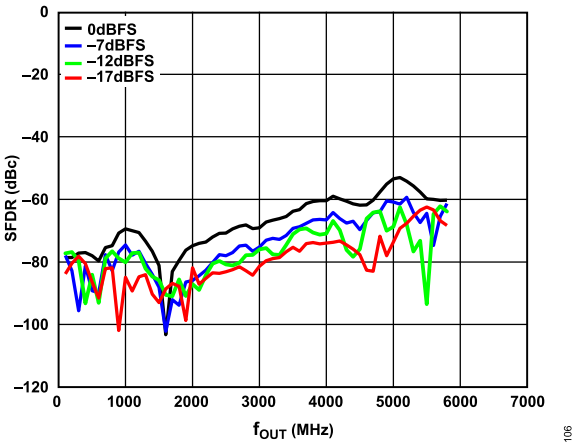

Figure 6. Second Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 1), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

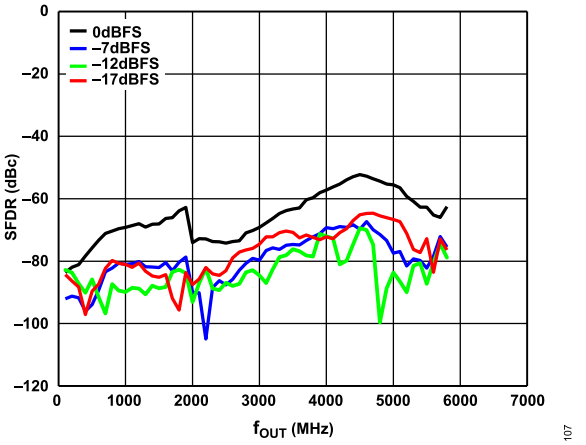

Figure 7. Third Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 1), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

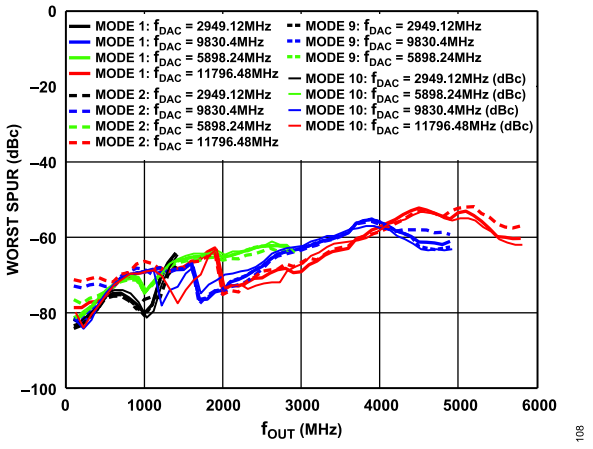

Figure 8. Worst Spur vs. f_{OUT} over f_{DAC} (All Modes), 0 dB Digital Scale

TYPICAL PERFORMANCE CHARACTERISTICS

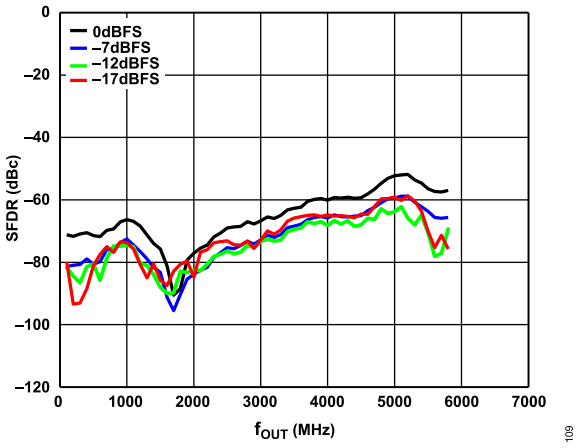

Figure 9. Second Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

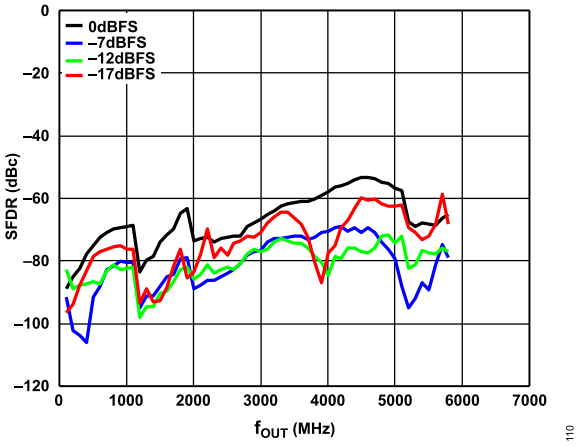

Figure 10. Third Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

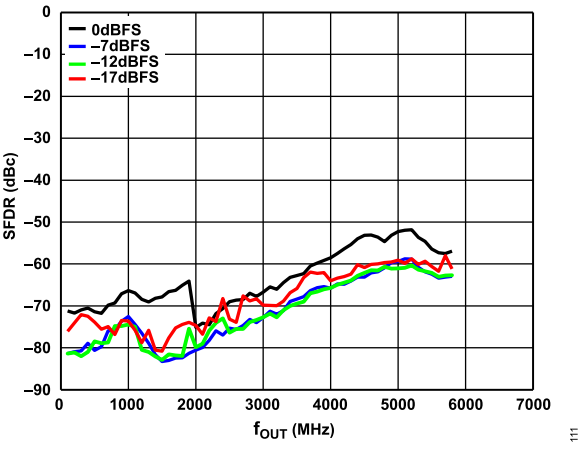

Figure 11. Worst Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

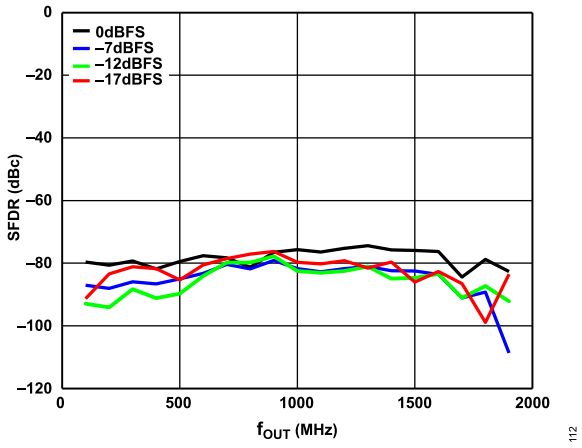

Figure 12. Second Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 12), 4 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 1×, 12-Bit Resolution

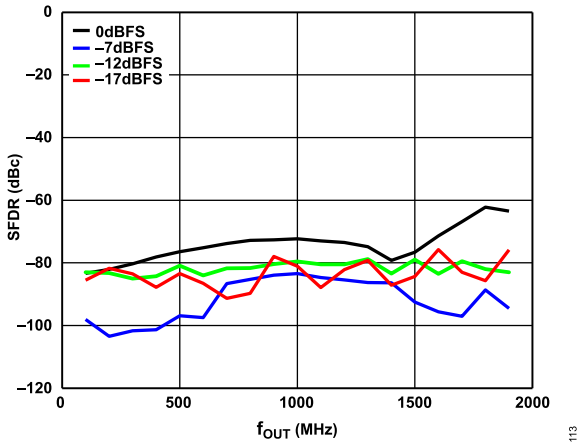

Figure 13. Third Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 12), 4 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 1×, 12-Bit Resolution

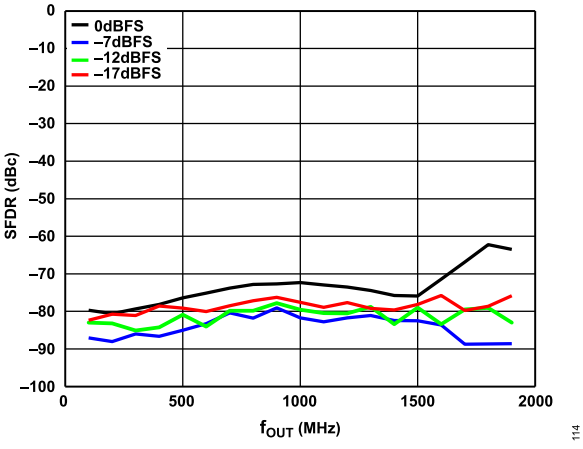

Figure 14. Worst Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 12), 4 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 1×, 12-Bit Resolution

TYPICAL PERFORMANCE CHARACTERISTICS

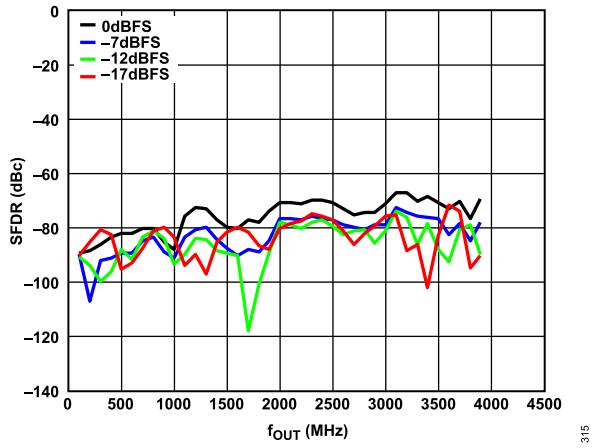

Figure 15. Second Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 12), 8 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 2×, 12-Bit Resolution

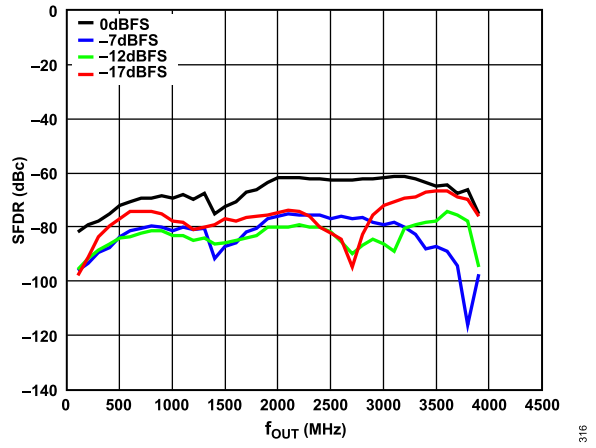

Figure 16. Third Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 12), 8 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 2×, 12-Bit Resolution

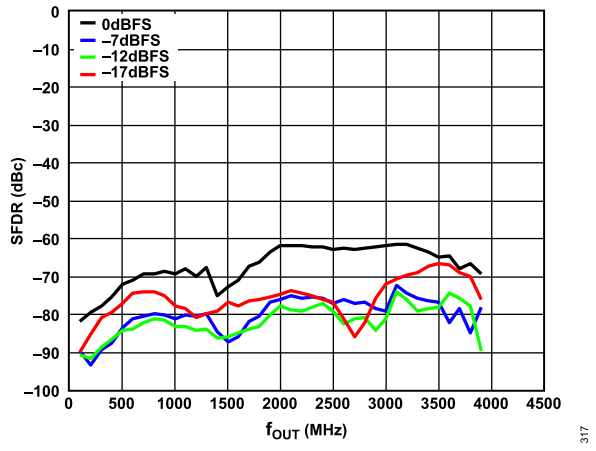

Figure 17. Worst Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 12), 8 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 2×, 12-Bit Resolution

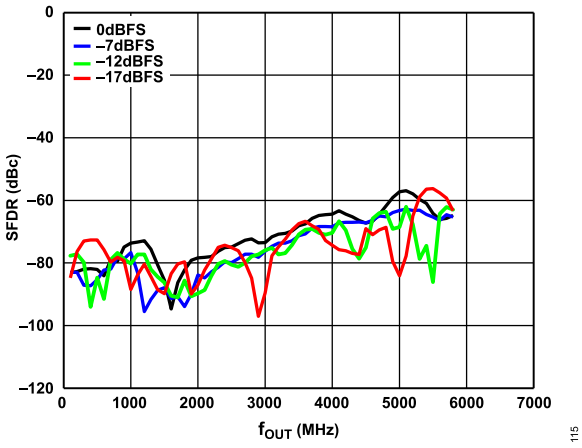

Figure 18. Second Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 9), 12 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×

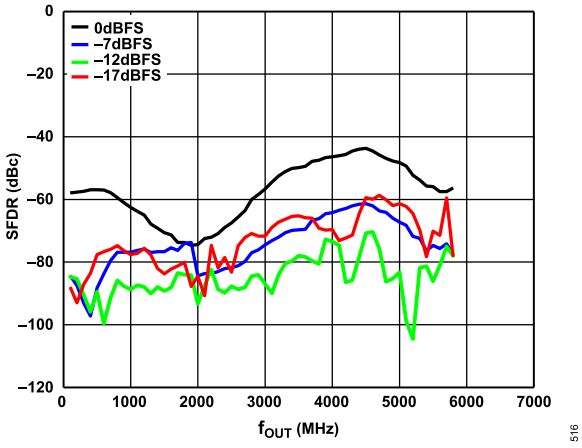

Figure 19. Third Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 9), 12 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×

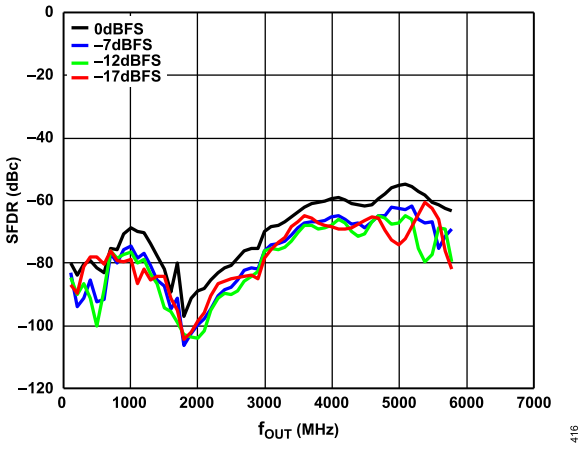

Figure 20. Second Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 10), 12 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×

TYPICAL PERFORMANCE CHARACTERISTICS

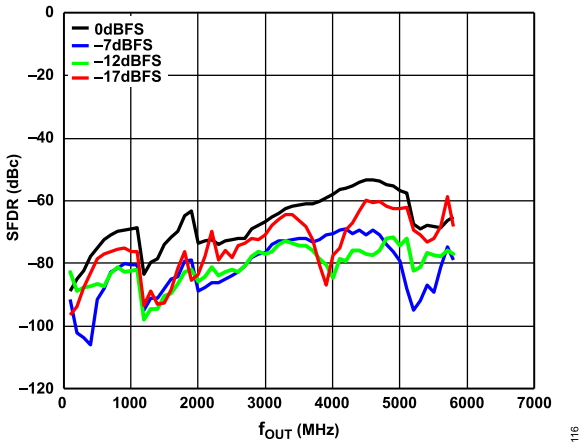

Figure 21. Third Harmonic (SFDR) vs. f_{OUT} over Digital Scale (Mode 10), 12 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×

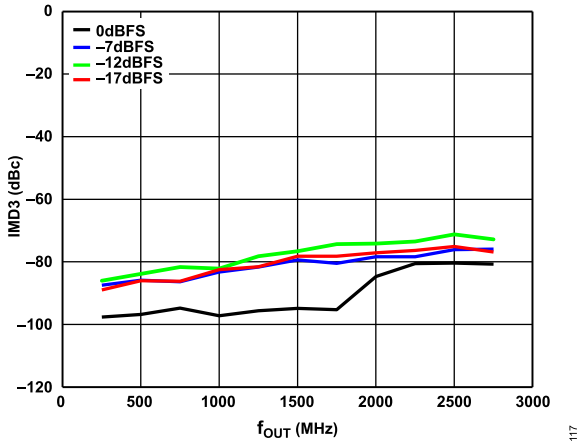

Figure 22. IMD3 vs. f_{OUT} over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×, 1 MHz Tone Spacing

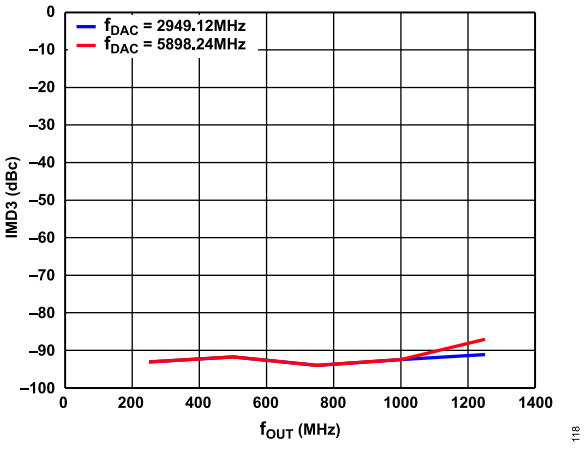

Figure 23. IMD3 vs. f_{OUT} over f_{DAC} (Mode 0), Channel Interpolation 2×, Main Interpolation 8×, 1 MHz Tone Spacing

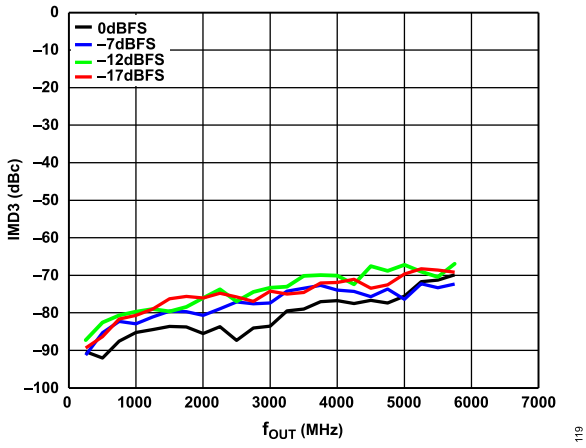

Figure 24. IMD3 vs. f_{OUT} over Digital Scale (Mode 1), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×, 1 MHz Tone Spacing

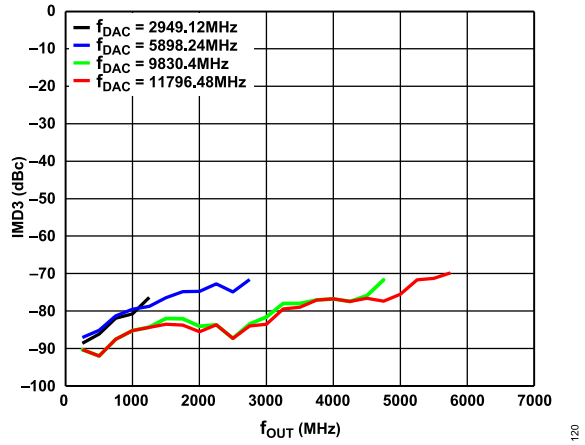

Figure 25. IMD3 vs. f_{OUT} over f_{DAC} (Mode 1), Channel Interpolation 4×, Main Interpolation 8×, 1 MHz Tone Spacing, −7 dB Digital Scale

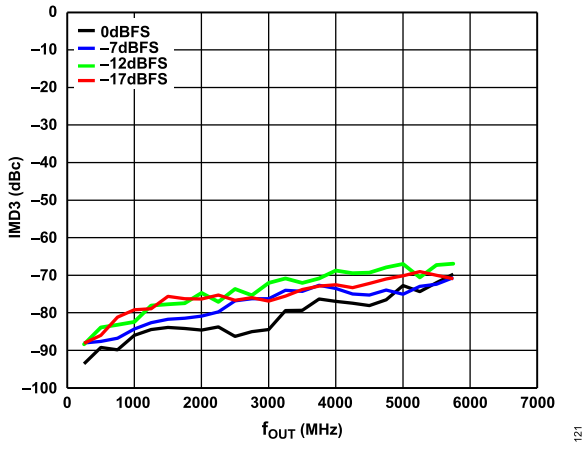

Figure 26. IMD3 vs. f_{OUT} over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×, 1 MHz Tone Spacing

TYPICAL PERFORMANCE CHARACTERISTICS

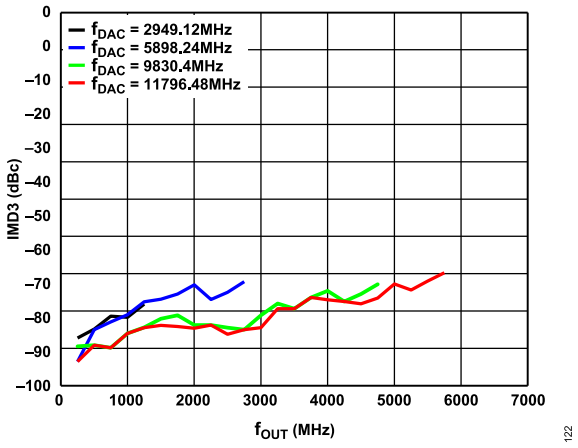

Figure 27. IMD3 vs. f_{OUT} over f_{DAC} (Mode 2), Channel Interpolation 4×, Main Interpolation 8×, 1 MHz Tone Spacing

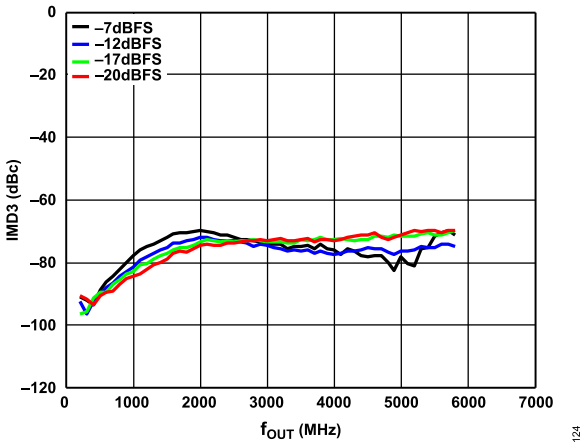

Figure 30. IMD3 vs. f_{OUT} over Digital Scale (Mode 10), 12 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×, 1 MHz Tone Spacing

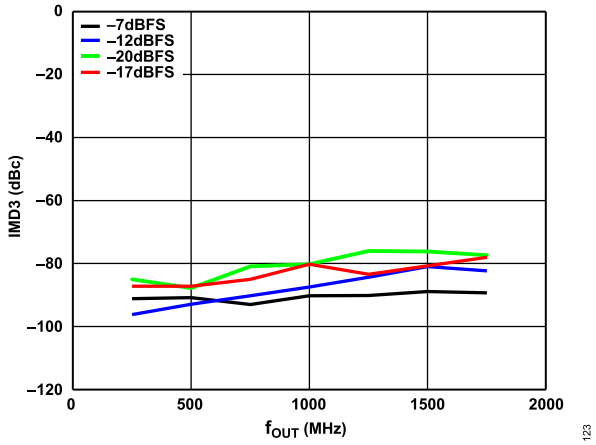

Figure 28. IMD3 vs. f_{OUT} over Digital Scale (Mode 12), 4 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 1×, 1 MHz Tone Spacing, 12-Bit Resolution

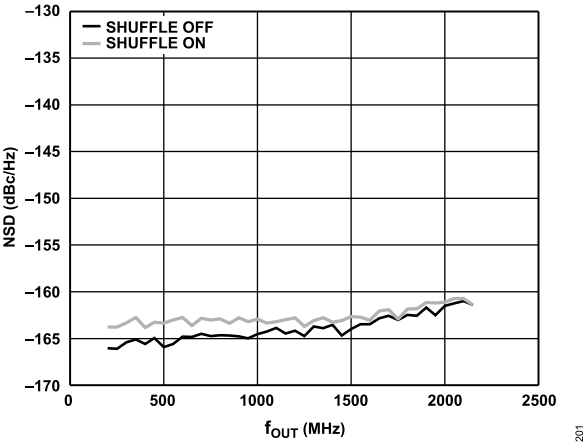

Figure 31. NSD vs. f_{OUT}, 11796.48 MHz f_{DAC}, 16-Bit Resolution, for Different Shuffle Options, Single Tone Measured at 70 MHz

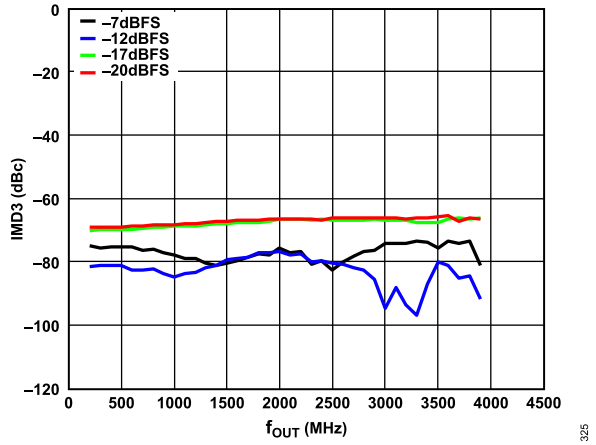

Figure 29. IMD3 vs. f_{OUT} over Digital Scale (Mode 12), 8 GHz DAC Sampling Rate, Channel Interpolation 1×, Main Interpolation 2×, 1 MHz Tone Spacing

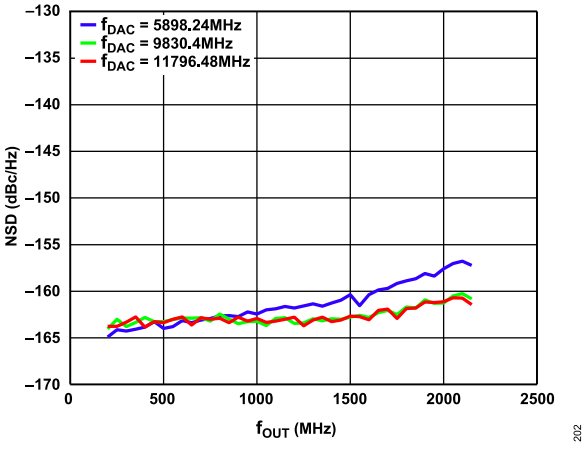

Figure 32. NSD vs. f_{OUT} over f_{DAC}, 16-Bit Resolution, Shuffle On, Single Tone Measured at 70 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

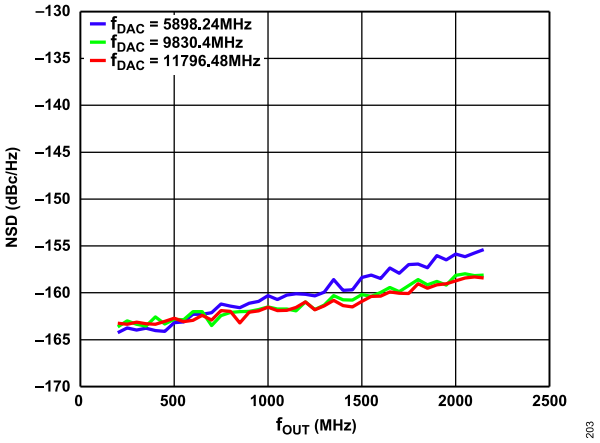

Figure 33. NSD vs. f_{OUT} over f_{DAC}, 16-Bit Resolution, Shuffle On, Single-Tone, Measured at 10% Offset from f_{OUT}

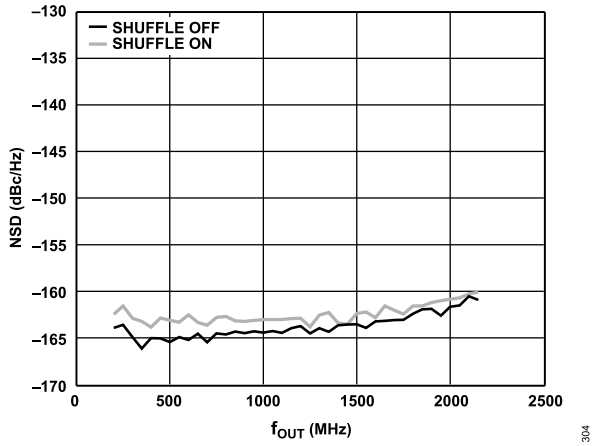

Figure 34. NSD vs. f_{OUT}, 11796.48 MHz f_{DAC}, 12-Bit Resolution, for Different Shuffle Options, Single-Tone, Measured at 70 MHz

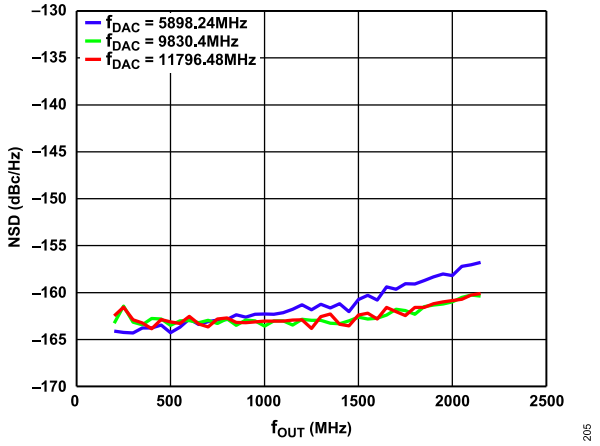

Figure 35. NSD vs. f_{OUT} over f_{DAC}, 12-Bit Resolution, Shuffle On, Single-Tone, Measured at 70 MHz

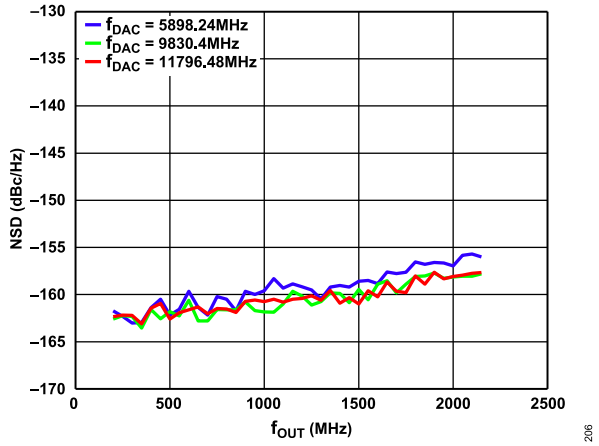

Figure 36. NSD vs. f_{OUT} over f_{DAC}, 12-Bit Resolution, Shuffle On, Single-Tone, Measured at 10% Offset from f_{OUT}

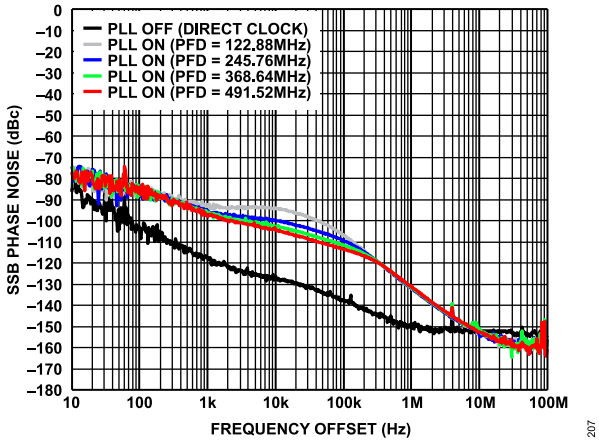

Figure 37. Single-Sideband (SSB) Phase Noise vs. Frequency Offset over f_{OUT}, over PFD Frequency, f_{DAC} = 12 GHz, f_{OUT} = 1.8 GHz, PLL On, PLL Reference Clock = 500 MHz

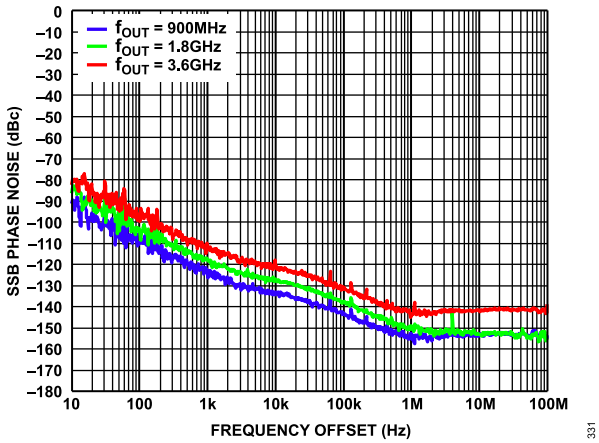

Figure 38. SSB Phase Noise vs. Frequency Offset over f_{OUT}, f_{DAC} = 12 GHz, Direct Clock (PLL Off)

TYPICAL PERFORMANCE CHARACTERISTICS

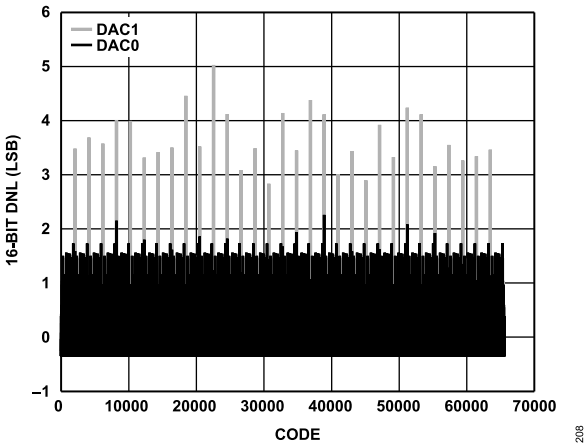

Figure 39. DNL, I_{OUTFS} = 26 mA, 16-Bit Resolution

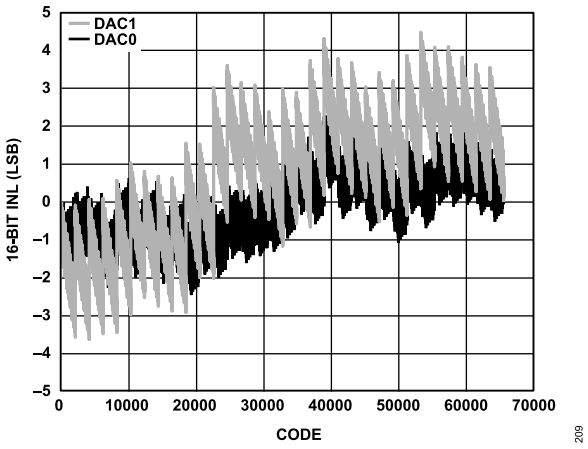

Figure 40. INL, I_{OUTFS} = 26 mA, 16-Bit Resolution

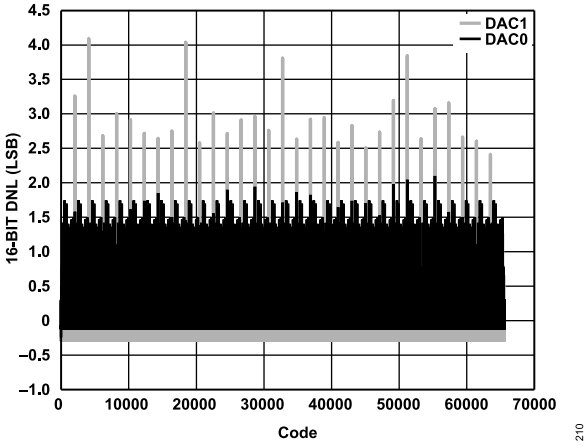

Figure 41. DNL, I_{OUTFS} = 20 mA, 16-Bit Resolution

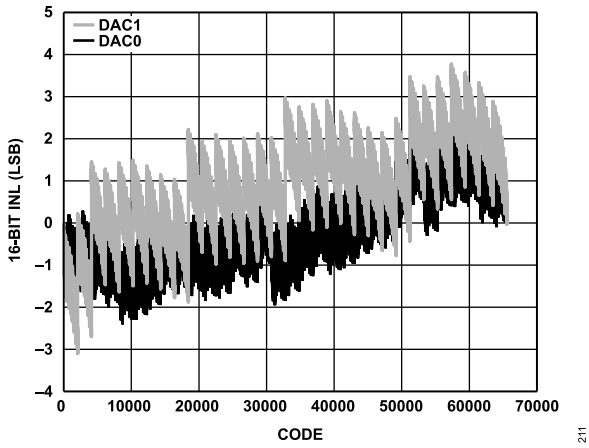

Figure 42. INL, I_{OUTFS} = 20 mA, 16-Bit Resolution

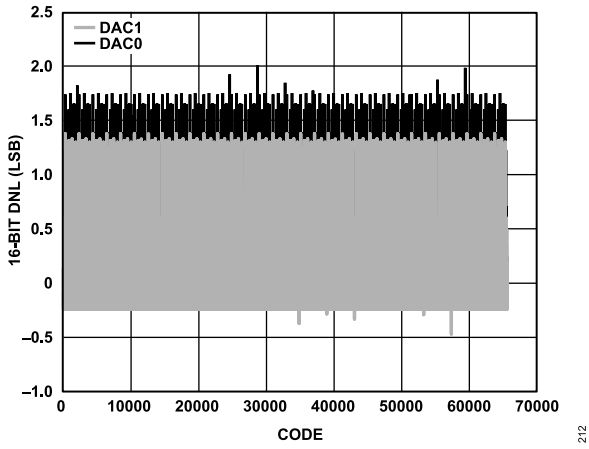

Figure 43. DNL, I_{OUTFS} = 15.6 mA, 16-Bit Resolution

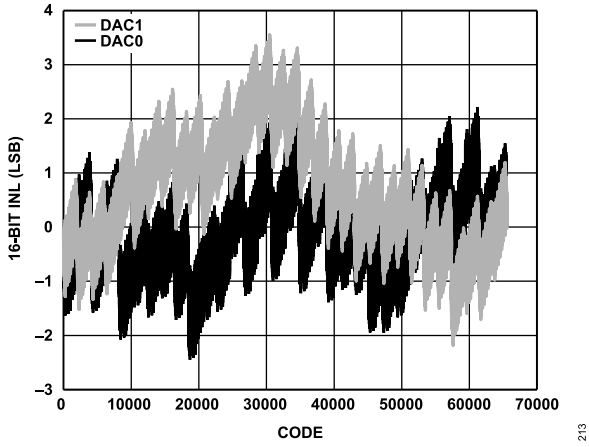

Figure 44. INL, I_{OUTFS} = 15.6 mA, 16-Bit Resolution

TYPICAL PERFORMANCE CHARACTERISTICS

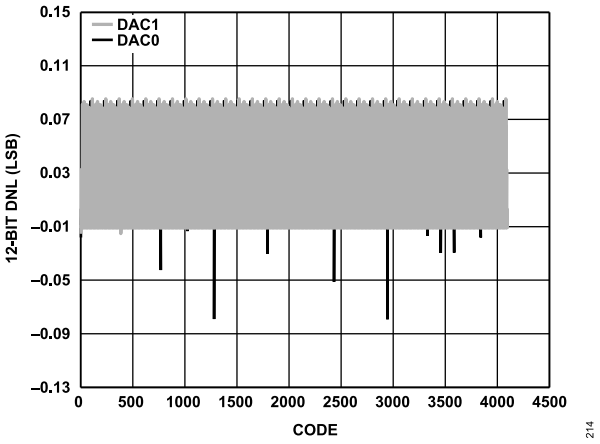

Figure 45. DNL, I_{OUTFS} = 20 mA, 12-Bit Resolution

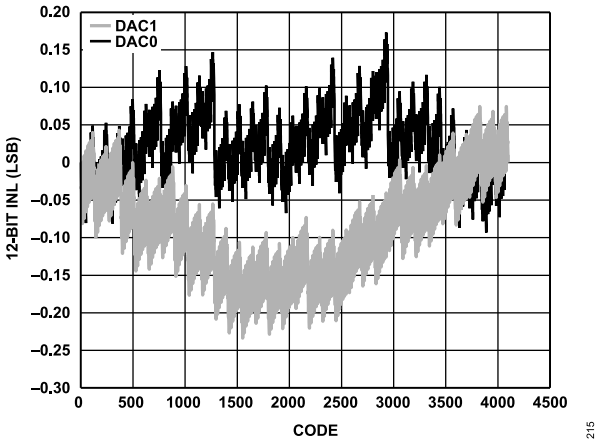

Figure 46. INL, I_{OUTFS} = 20 mA, 12-Bit Resolution

OUTLINE DIMENSIONS

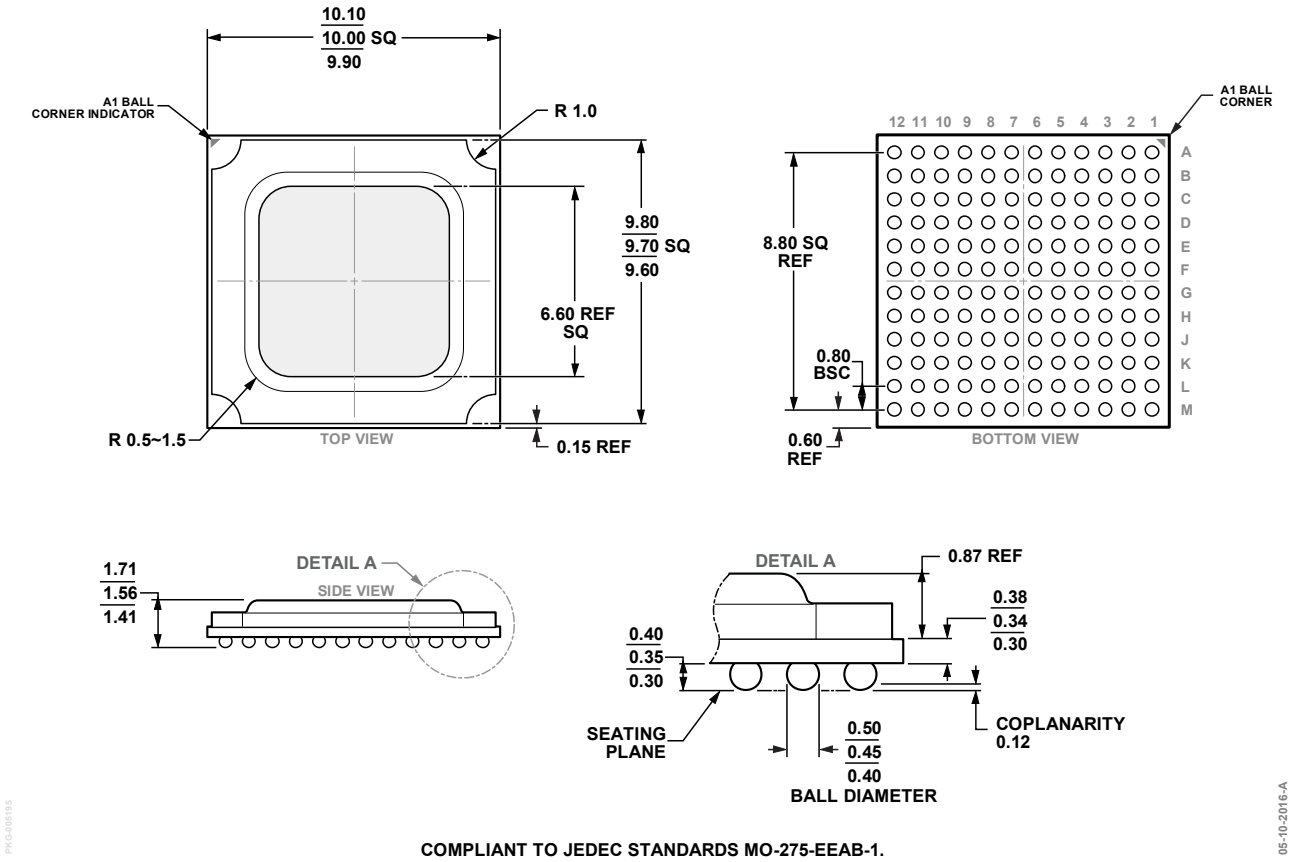

Figure 47. 144-Ball Ball Grid Array, Thermally Enhanced [BGA_ED] (BP-144-1) Dimensions shown in millimeters

Updated: March 11, 2023

ORDERING GUIDE

Model	Temperature Range	Package Description	Packing Quantity	Package Option
AD9176BBP-CSH	-40°C to +85°C	144 ball (10x10x1.71 w/6.6 mm EP)	Tray, 168	BP-144-1