DIGITAL AMPLIFIER POWER STAGE

Features

- PVDD range from 10.8V to 26.4V
- Support single-ended input audio PWM (AD) modulated signal
- Support differential input audio PWM (AD & BD) modulated signal
- Loudspeaker output power for stereo (BTL)
  - 10W x 2CH @ THD+N=0.15% into 8Ω at 24V
  - 10W x 2CH @ THD+N=0.23% into 8Ω at 18V
  - 10W x 2CH @ THD+N=0.5% into 8Ω at 15V
  - 8W x 2CH @ THD+N=5.6% into 8Ω at 12V
- Loudspeaker output power for mono (BTL)
  - 20W x 1CH @ THD+N=0.09% into 8Ω at 24V
  - 20W x 1CH @ THD+N=0.12% into 8Ω at 18V
  - 20W x 1CH @ THD+N=0.3% into 8Ω at 15V
- Over-temperature protection
- Over-current protection
- Under-voltage detection
- Error report
- Built-in anti-pop function
- Support both of 24-pin E-TSSOP and 48-pin 7x7mm E-LQFP thermally-enhanced package

Applications

- TV audio
- DVD Receiver
- Home Theaters

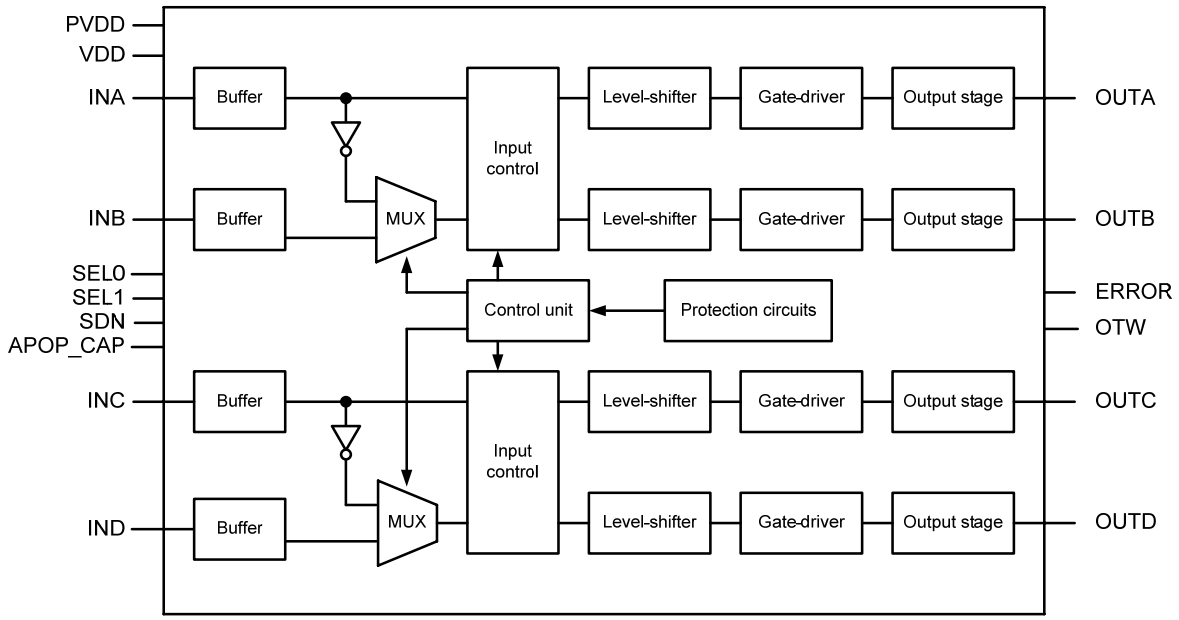
Description

The AD92580 is a high performance stereo digital amplifier power stage. It can deliver 10W x 2CH output power into 8Ω loudspeaker for stereo or 20W x 1ch output power into 4Ω loudspeaker for mono in BTL configuration within <1% THD+N at 15V ~ 24V supply.

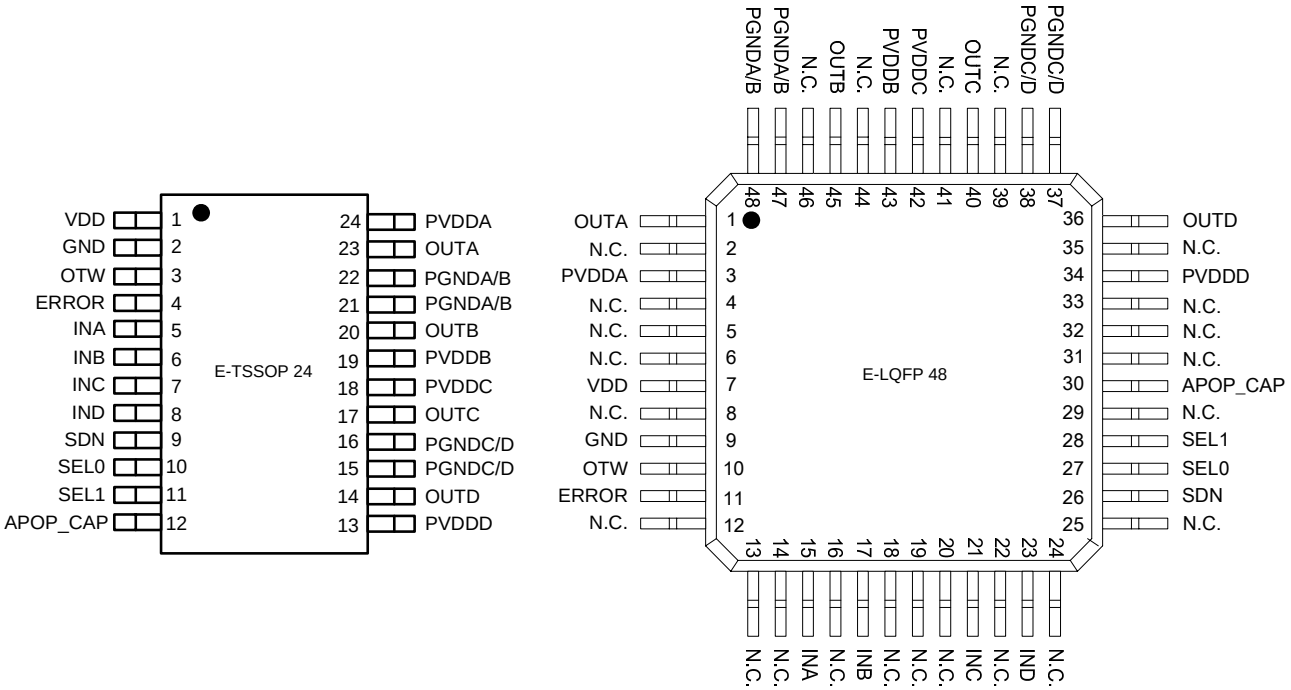
A patented, built-in anti-pop function can reduce the speaker's pop noise without requiring complex anti-pop sequence in PWM input.

The AD92580's chip is integrated with over-temperature, over-current, and under-voltage protection circuits. These additions safeguard the AD92580 against fault conditions that could damage the chip and system catastrophically.

Functional Block Diagram



Pin Assignments



Pin Description

NAME	PIN		TYP	DESCRIPTION
	E-TSSOP 24	E-LQFP 48		
VDD	1	7	P	Power supply for digital circuit
GND	2	9	P	Ground for digital circuit
OTW	3	10	O	Over temperature warning
ERROR	4	11	O	Error pointer
INA	5	15	I	PWM input A
INB	6	17	I	PWM input B
INC	7	21	I	PWM input C
IND	8	23	I	PWM input D
SDN	9	26	I	Shutdown (active-low) with soft pulled resistor 100kohm to ground
SEL0	10	27	I	Mode select pin 0
SEL1	11	28	I	Mode select pin 1
APOP_CAP	12	30	O	Anti-pop capacitor
PVDDD	13	34	P	Power supply for half bridge D
OUTD	14	36	O	Half-bridge output D
PGNDC/D	15	37	P	Ground for half bridge C/D
PGNDC/D	16	38	P	Ground for half bridge C/D
OUTC	17	40	O	Half-bridge output C

PVDDC	18	42	P	Power supply for half bridge C
PVDDB	19	43	P	Power supply for half bridge B
OUTB	20	45	O	Half-bridge output B
PGNDA/B	21	47	P	Ground for half bridge A/B
PGNDA/B	22	48	P	Ground for half bridge A/B
OUTA	23	1	O	Half-bridge output A
PVDDA	24	3	P	Power supply for half bridge A
N.C.	N/A	2, 4, 5, 6 8, 12, 13, 14 16, 18, 19, 20 22, 24, 25, 29 31, 32, 33, 35 39, 41, 44, 46		

Ordering Information

Product ID	Package	Packing	Comments
AD92580-QE24NAT	E-TSSOP 24L	6.2K units / Box Tube	Green
AD92580-LE48NAY	E-LQFP-48L 7x7 mm	2.5K Units / Box Tray	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jc}(℃/W)	Exposed Thermal Pad
E-TSSOP 24L	AD92580	31.5	2.16	7.5	Yes ***(Note 1)***
E-LQFP 7x7 48L		29.9	1.33	6.0	

Note 1.1: ***The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.***

Note 1.2: ***θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.***

Note 1.3: ***θ_{jc} represents the heat resistance for the heat flow between the chip and the package's top surface.***

Note 1.4: ***Ψ_{jt} represents the heat resistance for the heat flow between the chip and the exposed pad's center.***