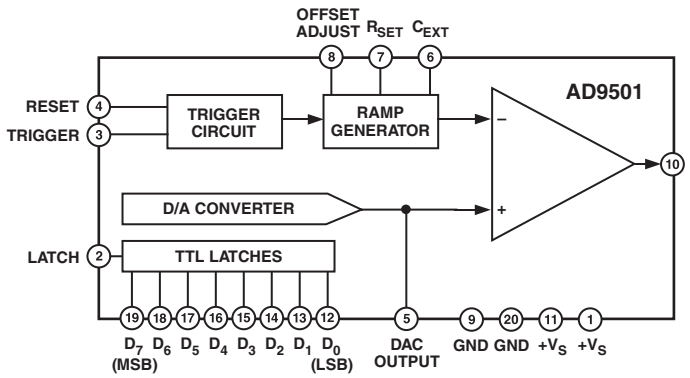
Digitally Programmable Delay Generator

AD9501

FEATURES
Single 5 V Supply
TTL- and CMOS-Compatible
10 ps Delay Resolution
2.5 ns to 10 μs Full-Scale Range
Maximum Trigger Rate 50 MHz

APPLICATIONS
Disk Drive Deskewing
Data Communications
Test Equipment
Radar I and Q Matching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9501 is a digitally programmable delay generator that provides programmed time delays of an input pulse. Operating from a single 5 V supply, the AD9501 is TTL- or CMOS-compatible and capable of providing accurate timing adjustments with resolutions as low as 10 ps. Its accuracy and programmability make it ideal for use in data deskewing and pulse delay applications, as well as clock timing adjustments.

Full-scale delay range is set by the combination of an external resistor and capacitor and can range from 2.5 ns to 10 μs for a single AD9501. An 8-bit digital word selects a time delay within the full-scale range. When triggered by the rising edge of an input pulse, the output of the AD9501 will be delayed by an amount equal to the selected time delay (t_D) plus an inherent propagation delay (t_{PD}).

The AD9501 is available for a commercial temperature range of 0°C to 70°C in a 20-lead plastic DIP and a 20-lead plastic leaded chip carrier (PLCC).

REV. B

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AD9501–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

($+V_S$ = 5 V; C_{EXT} = Open; R_{SET} = 3090 Ω [Full-Scale Range = 100 ns]; Pin 8 grounded and device output connected to Pin 4 RESET input, unless otherwise noted.)

Parameter	Temp	Test Level	0°C to 70°C AD9501JN/JP Min	Typ	Max	Unit
RESOLUTION			8			Bits
ACCURACY						
Differential Nonlinearity	25°C	I			0.5	LSB
Integral Nonlinearity	25°C	I			1	LSB
Monotonicity	25°C	I		Guaranteed		
DIGITAL INPUTS						
Latch Input 1 Voltage	Full	VI	2.0			V
Latch Input 0 Voltage	Full	VI			0.8	V
Logic 1 Voltage	Full	VI	2.0			V
Logic 0 Voltage	Full	VI			0.8	V
Logic 1 Current	Full	VI			60	µA
Logic 0 Current	Full	VI			3	µA
Digital Input Capacitance	25°C	IV			5.5	pF
Data Setup Time (t_S)[1]	25°C	V		2.5		ns
Data Hold Time (t_H)[2]	25°C	V		2.5		ns
Latch Pulse Width (t_L)	25°C	V		3.5		ns
Reset/Trigger Pulse Width (t_R, t_T)	25°C	V		2		ns
DYNAMIC PERFORMANCE						
Maximum Trigger Rate[3]	25°C	IV	18	22		MHz
Minimum Propagation Delay (t_{PD})[4]	25°C	I		25	30	ns
Propagation Delay Tempco[5]	Full	V		25		ps/°C
Full-Scale Range Tempco	Full	V		36		ps/°C
Delay Uncertainty	25°C	V		53		ps
Reset Propagation Delay (t_{RD})[6]	25°C	I		14.5	17.5	ns
Reset-to-Trigger Holdoff (t_{THO})[7]	25°C	V		4.5		ns
Trigger-to-Reset Holdoff (t_{RHO})[8]	25°C	V		19		ns
Minimum Output Pulse Width[9]	25°C	V		7.5		ns
Output Rise Time[10]	25°C	I		2.3	3.5	ns
Output Fall Time[10]	25°C	I		1.0	2.0	ns
DAC Settling Time (t_{LD})[11]	25°C	V		30		ns
Linear Ramp Settling Time (t_{LRS})[12]	25°C	V		20		ns
DIGITAL OUTPUT						
Logic 1 Voltage (Source 1 mA)	Full	VI	2.4			V
Logic 0 Voltage (Sink 4 mA)	Full	VI		0.24	0.4	V
POWER SUPPLY[13]						
Positive Supply Current (5.0 V)	Full	VI		69.5	83	mA
Power Dissipation	Full	VI			415	mW
Power Supply Rejection Ratio[14]						
Full-Scale Range Sensitivity	25°C	I		0.7	2.0	ns/V
Minimum Prop Delay Sensitivity	25°C	I		0.45	1.7	ns/V

NOTES

[1]Digital data inputs must remain stable for the specified time prior to the positive transition of the LATCH signal.

[2]Digital data inputs must remain stable for the specified time after the positive transition of the LATCH signal.

[3]Programmed delay (t_D) = 0 ns. Maximum self-resetting trigger rate is limited to 6.9 MHz with 100 ns programmed delay. If t_D = 0 ns and external RESET signal is used, maximum trigger rate is 23 MHz.

[4]Programmed delay (t_D) = 0 ns. In operation, any programmed delays are in addition to the minimum propagation delay (t_{PD}).

[5]Programmed delay (t_D) = 0 ns. Minimum propagation delay (t_{PD}).

[6]Measured from 50% transition point of the RESET signal input to the 50% transition point of the falling edge of the output.

[7]Minimum time from the falling edge of RESET to the triggering input to ensure valid output pulse, using external RESET pulse.

[8]Minimum time from triggering event to rising edge of RESET to ensure valid output event, using external RESET pulse. Extends to 125 ns when programmed delay is 100 ns.

[9]When self-resetting with a full-scale programmed delay.

[10]Measured from 0.4 V to 2.4 V; source = 1 mA; sink = 4 mA.

[11]Measured from the data input to the time when the AD9501 becomes 8-bit accurate, after a full-scale change in the program delay data word.

[12]Measured from the RESET input to the time when the AD9501 becomes 8-bit accurate, after a full-scale programmed delay.

[13]Supply voltage should remain stable within ±5% for normal operation.

[14]Measured at $+V_S$ = 5.0 V ± 5%; specification shown is for worst case.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage	7 V
Digital Input Voltage Range	–0.5 V to $+V_S$
Trigger/Reset Input Voltage Range	–0.5 V to $+V_S$
Minimum R_{SET}	30 Ω
Digital Output Current (Sourcing)	10 mA
Digital Output Current (Sinking)	50 mA
Operating Temperature Range	
AD9501JN/JP	0°C to 70°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature[2]	175°C
Lead Soldering Temperature (10 sec)	300°C

NOTES

[1]Absolute Maximum Ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances: 20-lead plastic leaded chip carrier, θ_{JA} = 73°C/W; θ_{JC} = 29°C/W. 20-lead plastic DIP, θ_{JA} = 65°C/W; θ_{JC} = 26°C/W.

ORDERING GUIDE

Device	Temperature	Description	Package Option*
AD9501JN	0°C to 70°C	20-Lead Plastic DIP	N-20
AD9501JP	0°C to 70°C	20-Lead Plastic Leaded Chip Carrier	P-20A
AD9501JP-REEL	0°C to 70°C	20-Lead Plastic Leaded Chip Carrier	P-20A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at 25°C, and sample tested at specified temperatures.

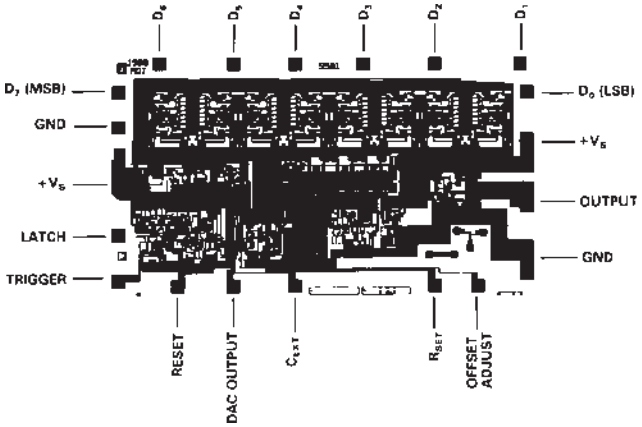
III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

DIE LAYOUT AND MECHANICAL INFORMATION



MECHANICAL INFORMATION

Die Dimensions	89 × 153 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	Ground
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold; Gold Ball Bonding

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1, 11	$+V_S$	Positive Voltage Supply; Nominally 5 V.
2	LATCH	TTL/CMOS Register Control Line. Logic HIGH latches input data D_0–D_7. Register is transparent for logic LOW.
3	TRIGGER	TTL/CMOS-Compatible Input. Rising edge triggers the internal ramp generator and begins the delay cycle.
4	RESET	TTL/CMOS-Compatible Input. Logic HIGH resets the ramp voltage and OUTPUT.
5	DAC OUTPUT	Output Voltage of the Internal Digital-to-Analog Converter.
6	C_{EXT}	Optional External Capacitor Connected to $+V_S$. Used with R_{SET} and 8.5 pF internal capacitor to determine full-scale delay range (t_{DFS}).
7	R_{SET}	External Resistor to Ground. Used to determine full-scale delay range (t_{DFS}).
8	OFFSET ADJUST	Normally Connected to GROUND. Can be used to adjust minimum propagation delay (t_{PD}); see Theory of Operation section.
9, 20	GROUND	Circuit Ground Return.
10	OUTPUT	TTL-Compatible Delayed Output Pulse.
12–19	D_0–D_7	TTL/CMOS-Compatible Inputs. Used to set the programmed delay of the AD9501 delayed output. D_0 is the LSB and D_7 is the MSB.

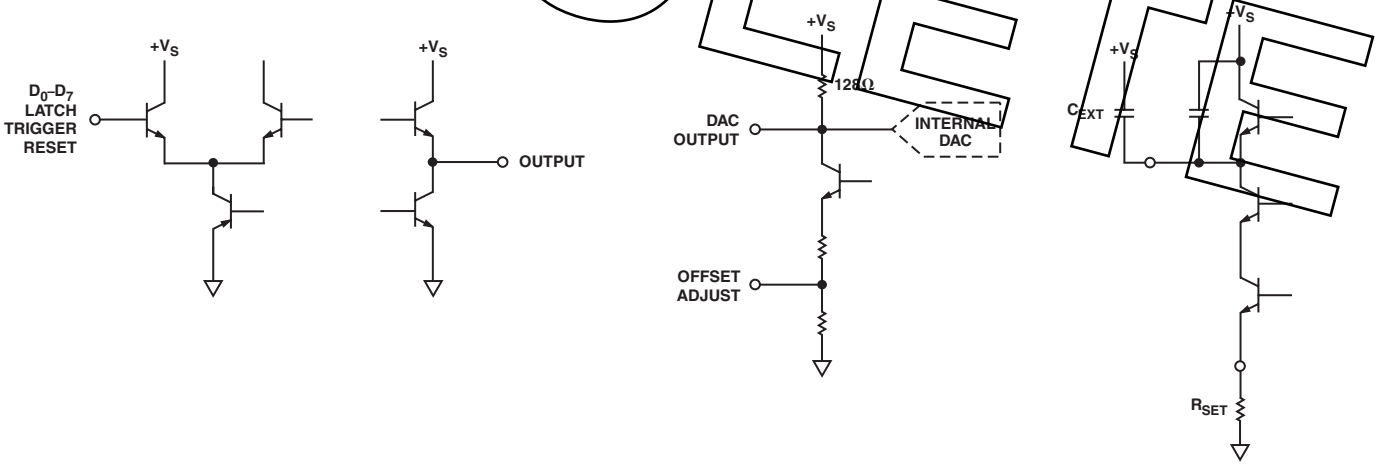


Figure 1. Equivalent Circuits

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9501 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

The AD9501 is a digitally programmable delay device. Its function is to provide a precise incremental delay between input and output, proportional to an 8-bit digital word applied to its delay control port. Incremental delay resolution is 10 ps at the minimum full-scale range of 2.5 ns. Digital delay data inputs, latch, trigger, and reset are all TTL/CMOS-compatible. Output is TTL-compatible.

Refer to the AD9501 Functional Block Diagram.

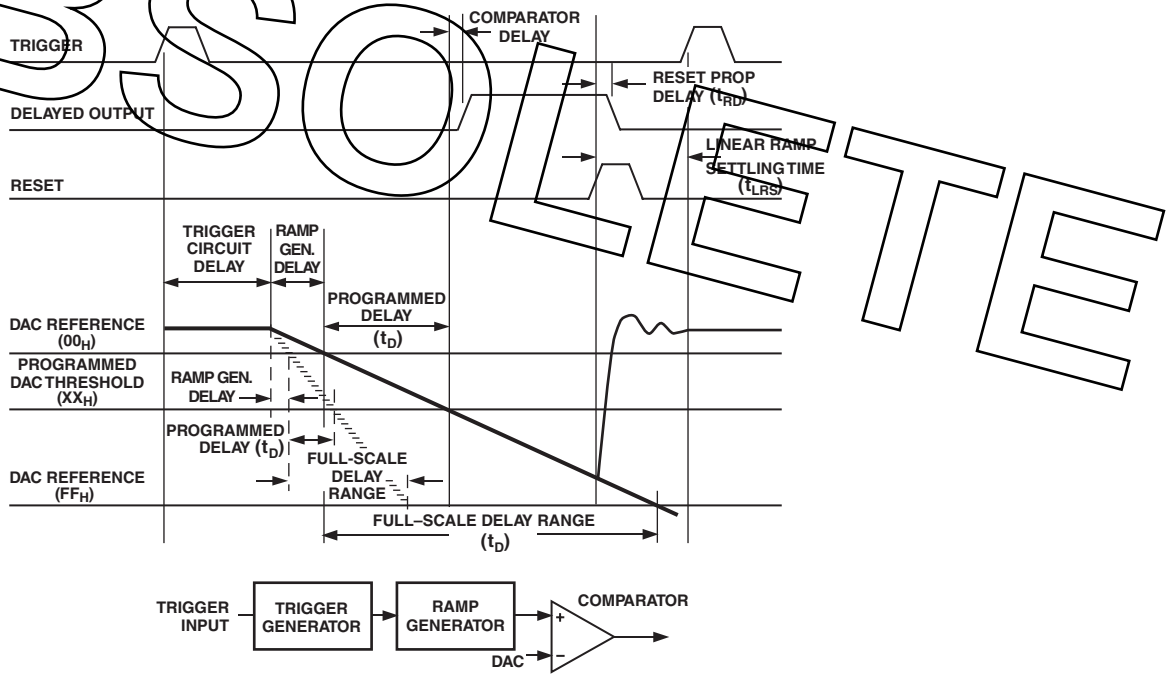
Inside the unit, there are three main subcircuits: a linear ramp generator, an 8-bit digital-to-analog converter (DAC), and a voltage comparator. The rising edge of the input (TRIGGER) pulse initiates the delay cycle by triggering the ramp generator. The voltage comparator monitors the ramp voltage and switches the delayed output (Pin 10) HIGH when the ramp voltage crosses the threshold set by the DAC output voltage. The DAC threshold voltage is programmed by the user with digital inputs.

Figure 2 illustrates in detail how the delay is determined. Minimum delay (t_{PD}) is the sum of trigger circuit delay, ramp generator delay, and comparator delay.

The trigger circuit delay and comparator delay are fixed; ramp generator delay is a variable affected by the rate of change of the linear ramp and (to a lesser degree) the value of the offset voltage described below.

Maximum delay is the sum of minimum delay (t_{PD}) and full-scale program delay (t_{DFS}).

Ramp generator delay is the time required for the ramp to slew from its reset voltage to the most positive DAC reference voltage (00_H). The difference in these two voltages is nominally 18 mV (with OFFSET ADJUST open) or 34 mV (OFFSET ADJUST grounded).



MINIMUM PROPAGATION DELAY = (t_{PD}) = TRIGGER CIRCUIT DELAY + RAMP GENERATOR DELAY + COMPARATOR DELAY

MAXIMUM PROPAGATION DELAY = MINIMUM PROPAGATION DELAY (t_{PD}) + FULL–SCALE RANGE (t_{DFS})

$$\text{PROGRAMMED DELAY } (t_D) = \left(\frac{\text{DIGITAL VALUE}}{256}\right)$$

TOTAL DELAY = (t_{PD}) + (t_D)

AD9501 TESTED WITH C_{EXT} = 0 pF; R_{SET} = 3.09 kΩ (100 ns PROGRAMMED DELAY)

Figure 2. Internal Timing

Offset between the two levels is necessary for three reasons. First, offset allows the ramp to reset and settle without re-entering the voltage range of the DAC. Second, the DAC may overshoot as it switches to its most positive value (00_H); this can lead to false output pulses if there is no offset between the ramp reset voltage and the upper reference. Overshoot on the ramp can also lead to false outputs without the offset. Finally, the ramp is slightly nonlinear for a short interval when it is first started; the offset shifts the most positive DAC level below this nonlinear region and maintains ramp linearity for short programmed delay settings.

Pin 8 of the AD9501 is called OFFSET ADJUST (see Functional Block Diagram) and allows the user to control the amount of offset separating the initial ramp voltage and the most positive DAC reference. This, in turn, causes the ramp generator delay to vary.

Figure 3 shows differences in timing that occur if OFFSET ADJUST Pin 8 is grounded or open. The variable ramp generator delay is the major component of the three components that comprise minimum delay (t_{PD}) and, therefore, is affected by the connection to Pin 8.

It is preferable to ground Pin 8 because the smaller offset that results from leaving it open increases the possibility of false output pulses. When grounding the pin, it should be grounded directly or connected to the ground through a resistor or potentiometer with a value of 10 kΩ or less.

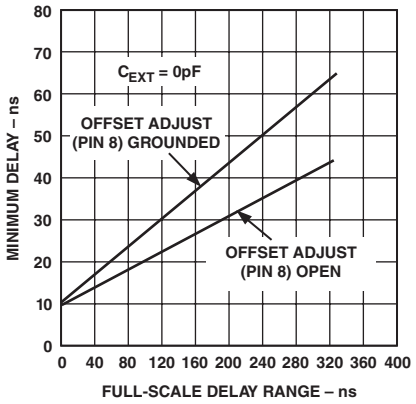


Figure 3. Minimum Delay (t_{PD}) vs. Full-Scale Delay Range (t_{DFS})

Caution is urged when using resistance in series with Pin 8. The possibility of false output pulses, as discussed above, is increased under these circumstances. Using resistance in series with Pin 8 is recommended only when matching minimum delays between two or more AD9501 devices; it is not recommended if using a single AD9501. Changing the resistance between Pin 8 and ground from 0 kΩ to 10 kΩ varies the ramp generator delay by approximately 35%.

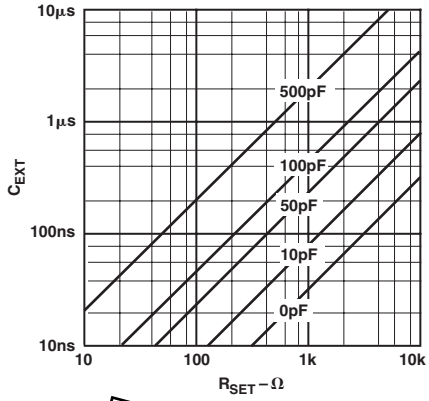


Figure 4. RC Values vs. Full-Scale Delay Range (t_{DFS})

The full-scale delay range (t_{DFS}) can be calculated from the equation:

$$t_{DFS} = R_{SET} \times (C_{EXT} + 8.5\ pF) \times 3.84$$

Whenever full-scale delay range is 326 ns or less, C_{EXT} should be left open. Additional capacitance and/or larger values of R_{SET} increase the linear ramp settling time, which reduces the maximum trigger rate. When delays longer than 326 ns are required, up to 500 pF can be connected from C_{EXT} to $+V_S$. To preserve the unit's low drift performance, both R_{SET} and C_{EXT} should have low temperature coefficients. Resistors that are used should be 1% metal film types.

The programmed delay (t_D) is set by the DAC inputs, D_0–D_7.

The minimum delay through the AD9501 corresponds to an input code of 00_H, and FF_H gives the full-scale delay. Any programmed delay can be approximated by

$$t_D = (DAC\ code / 256) \times t_{DFS}$$

Total delay through the AD9501 for any given DAC code is equal to

$$t_{TOTAL} = t_D + t_{PD}$$

As shown on the Functional Block Diagram, TTL/CMOS latches are included to store the digital delay data. Data is latched when LATCH is HIGH. When LATCH is LOW, the latches are transparent, and the DAC will attempt to follow any changes on inputs D_0–D_7.

Figure 5 shows the timing relationship between the input data and the LATCH. The DAC settling time (t_{LD}) is approximately 30 ns. After the digital (programmed delay) data is updated, a minimum 30 ns must elapse between the time LATCH goes HIGH and the arrival of a TRIGGER pulse to assure rated pulse delay accuracy.

When RESET goes HIGH, the ramp timing capacitor (C_{EXT} + 8.5 pF) is discharged. The RESET input is level-sensitive and overrides the TRIGGER input. Therefore, any trigger pulse that occurs when RESET is HIGH will not produce an output pulse. As shown in Figure 5, the next trigger pulse should not occur before the linear ramp settling time (t_{LRS}) interval is completed to assure rated pulse delay accuracy.

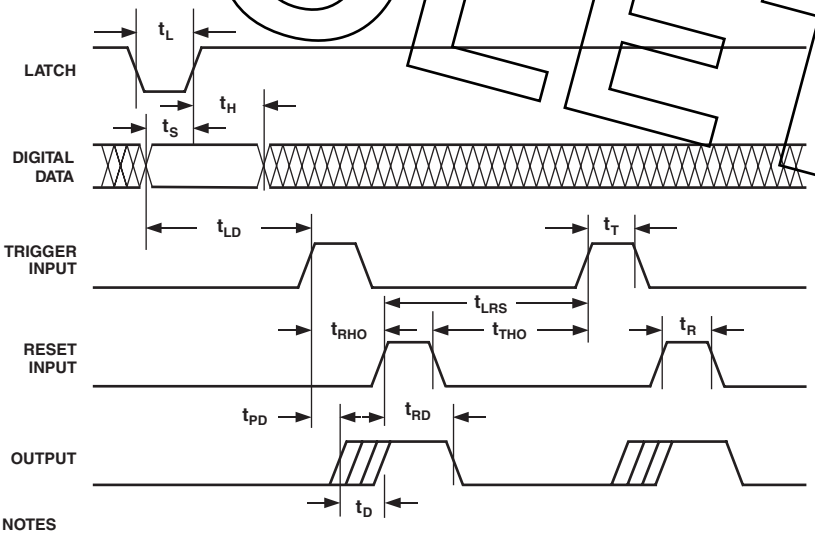
For most applications, OUTPUT can be tied to RESET. This causes the output pulse to be narrow (equal to the reset propagation delay, t_{RD}). Alternatively, an external pulse can be applied to RESET. To assure a valid output pulse, however, the delay between TRIGGER and RESET should be equal to or greater than the total delay of t_{PD} + t_D illustrated in Figure 2.

As shown in Figure 2, the capacitor voltage discharges rapidly and includes a small amount of overshoot and ringing. Rated timing delay will not be realized unless subsequent trigger events are delayed until after the linear ramp settles to its reset voltage value.

The values for the various delay increments in the specification table are based on a full-scale delay range of 100 ns with OUTPUT tied to RESET (self-resetting operation).

When full-scale delay range is set for intervals shorter than 100 ns, the rate of change of the linear ramp is increased. This faster rate means the maximum trigger rate shown in the specification table is increased because the ramp generator delay, and consequently, minimum propagation delay, t_{PD}, become smaller.

Linear ramp settling time (t_{LRS}) also becomes shorter as full-scale delay range is decreased. Minimum delays for various full-scale delay range values are shown in Figure 3.



NOTES
A TRIGGERING EVENT MAY OCCUR AT ANY TIME THE DAC (PROGRAMMED DELAY) IS BEING CHANGED. TRIGGERING EVENTS DURING THE INTERNAL DAC SETTLING TIME MAY NOT GENERATE AN ACCURATE PULSE DELAY.

t_L – LATCH PULSE WIDTH
t_H – DIGITAL HOLD TIME
t_S – DIGITAL DATA SETUP TIME
t_{LD} – DAC SETTLING TIME
t_T – TRIGGER PULSE WIDTH
t_{LRS} – LINEAR RAMP SETTLING TIME
t_{RHO} – TRIGGER-TO-RESET HOLD-OFF
t_{THO} – RESET-TO-TRIGGER HOLD-OFF
t_R – RESET PULSE WIDTH
t_{PD} – MINIMUM PROPAGATION DELAY
t_{RD} – RESET PROPAGATION DELAY
t_D – PROGRAMMED DELAY

Figure 5. System Timing

APPLICATIONS

The AD9501 is useful in a wide variety of precision timing applications because of its ability to delay TTL/CMOS pulse edges by increments as small as 10 ps.

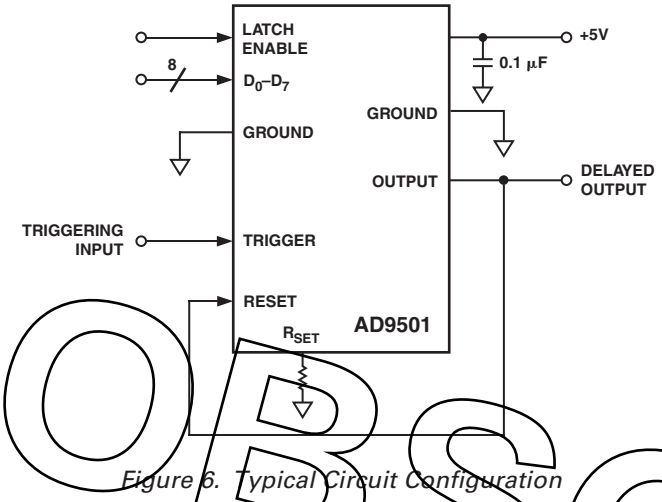


Figure 6. Typical Circuit Configuration

In Figure 6, the delayed output is tied back to the RESET input. This produces a narrow output pulse whose leading edge is delayed by an amount proportional to the 8-bit digital word stored in the on-board latches. For the configuration shown, the output pulse width will be equal to the reset propagation delay (t_{RD}). If wider pulses are required, a delay can be inserted between OUTPUT and RESET. If preferred, an external pulse can be used as a reset input to control the timing of the falling edge (and, consequently, the width) of the delayed output.

Multiple Signal Path Deskewing

High speed electronic systems with parallel signal paths require that close delay matching be maintained. If delay mismatch (time skew) occurs, errors can occur during data transfer. For these situations, the matching of delays is generally accomplished by carefully matching lead lengths.

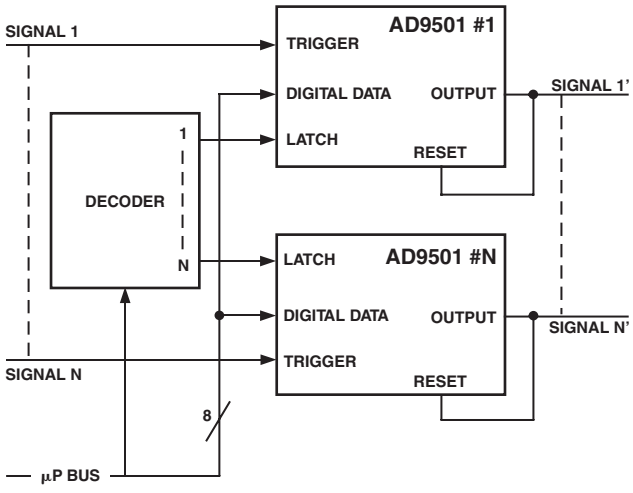


Figure 7. Multiple Signal Path Deskewing

This delay matching is often difficult when using high speed, high pin count testers because lead length and circuit impedance can change when the tester setup is changed for different types of devices. The skew that might result from these changes can be compensated for by using AD9501 units, as shown in Figure 7.

When deskewing multiple signal paths, a single stimulus pulse is applied to all inputs of the AD9501s that are used. The delay for each signal path is then measured by the tester's delay measurement circuit. Using a closed-loop technique, all delays are equalized by changing the digital value held in the register of each AD9501. Once all delays have been matched to the desired tolerance, the calibration loop is opened, and the tester is ready to test the new type of device.

Digitally Programmable Oscillator

Two AD9501s can be configured as a stable oscillator, as shown in Figure 8.

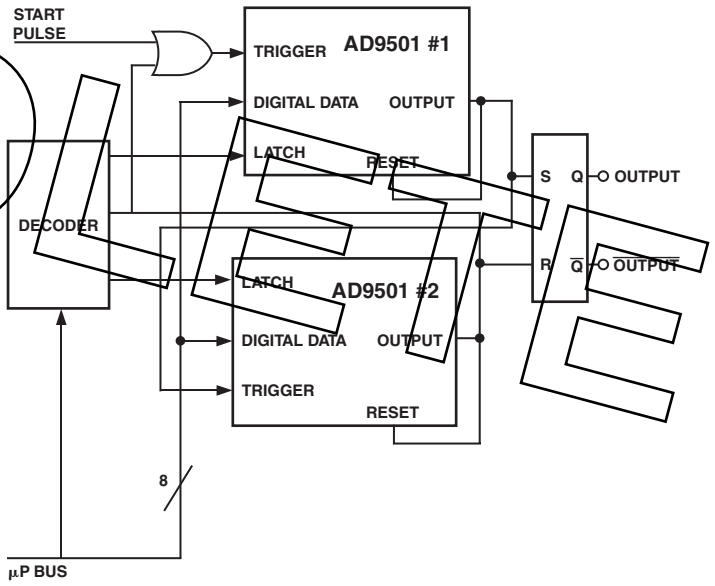


Figure 8. Digitally Programmable Oscillator

Delay through each side of the oscillator is determined by the programmed delay (t_D) of each AD9501 plus the minimum propagation delay (t_{PD}) of each. Increasing the digital value applied to either AD9501 decreases frequency, just as increasing RC decreases frequency in an analog ring oscillator.

Using a pair of AD9501 delay generators, as shown, allows the user great flexibility because both the frequency and the duty cycle of the oscillator are easily controlled.

Frequency of the oscillator output can be established with the equation

$$f = 1/(2t_{PD} + t_{D1} + t_{D2})$$

when t_{D1} and t_{D2} are the programmed delays of AD9501 #1 and AD9501 #2, respectively.

Programmable Pulse Generator

In Figure 9, two AD9501 units are triggered from a common clock signal. Their outputs go to the inputs of an RS flip-flop. A digital delay value is applied as an input to each with AD9501 #2 typically having a larger value than AD9501 #1.

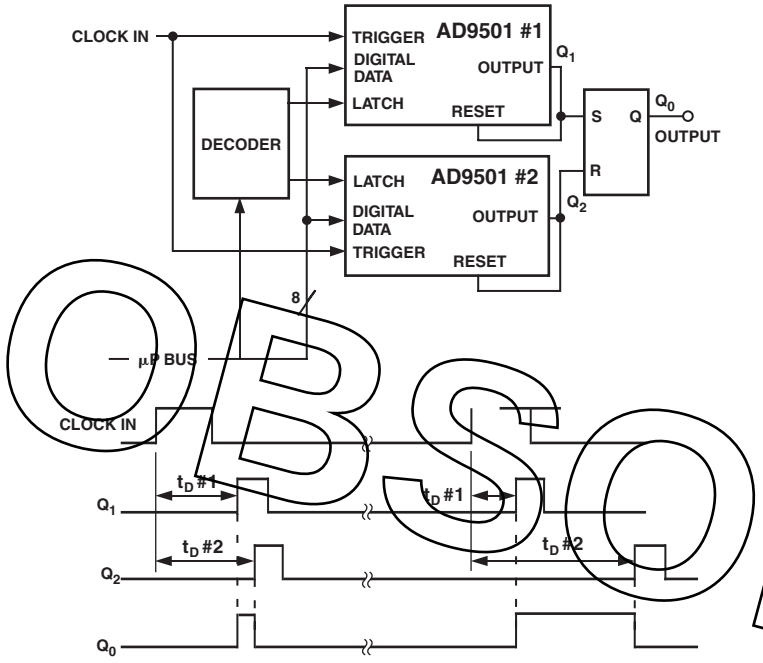


Figure 9. Programmable Pulse Delay Generator

As shown by the timing portion of the diagram, changing the delay value from one clock cycle to the next generates a pseudo-random pulse whose leading and trailing edge delays are controlled relative to Clock In. The dashed lines illustrate how the programmed delays of the AD9501 components control both the timing and width of the generator output.

The frequency (f) and pulse width (t_{pw}) of the pulse generator can be determined as follows:

$$f = f_{CLOCK\ IN}$$

and:

$$t_{pw} = t_{TOT\,2} - t_{TOT\,1}$$

with t_{TOT} being equal to each AD9501's minimum propagation delay (t_{PD}) plus programmed delay (t_D). If both AD9501s are set for the same full-scale delay range, their minimum propagation delays will be approximately the same, and the pulse width will be approximately equal to the difference in programmed delays.

Digital Delay Detector

An unknown digital delay can be measured by applying a repetitive clock to the circuit shown in Figure 10.

The pictured delay detector works in a manner similar to a successive-approximation ADC; in this circuit, however, a D-type flip-flop replaces the ADC's voltage comparator.

To calibrate the circuit, short out the unknown delay and apply the clock input to both AD9501 units.

AD9501 #1 should be programmed so its delay is greater than the zero-set programmed delay of AD9501 #2. To accomplish this, continue to apply clock pulses and increment the digital data into AD9501 #1 until the output of the successive-approximation register (SAR) is 02H (00000010) or greater. At this point, the delay through AD9501 #1 is slightly longer than the delay through AD9501 #2, making it possible to use the SAR output as the zero reference point for measuring the unknown delay when it is reinserted into the circuit.

This calibration procedure compensates for the setup time of the flip-flop, stray circuit delays, and other nonideal characteristics that are an inherent part of any circuit.

Eight cycles of the clock input are required to determine the value of the unknown delay.

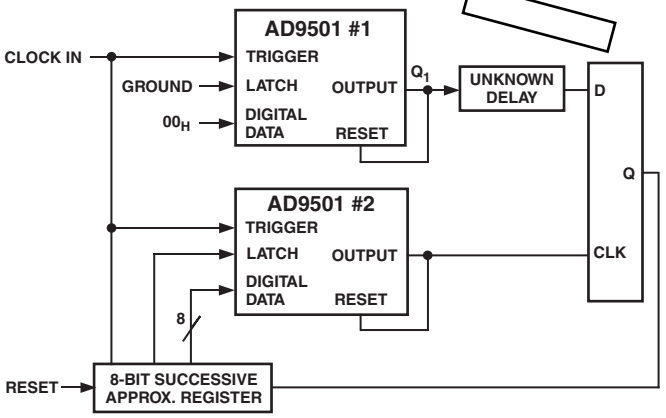


Figure 10. Digital Delay Detector

Analog Settling Time Measurement

The circuit shown in Figure 11 functions in a manner similar to the digital delay detector; for this application, the clock must be repetitive also. As in the delay detector, AD9501 #1 is used to cancel the propagation delay of AD9501 #2, propagation delay of the comparators, and stray delays. To accomplish this, use the calibration procedure described earlier for the digital delay generator.

The difference between the two circuits is in the detection method. The register of the digital delay is replaced by a window comparator for the analog settling measurement.

Threshold voltages V_1 and V_2 are set for the desired tolerance around the final value of the DUT output signal. As shown in the lower portion of the diagram, the output of the detector is HIGH when the analog output signal of the converter is within the limits set by V_1 and V_2.

Therefore, the settling time can be measured by starting the delay of AD9501 #2 at its maximum setting and decrementing it until the window comparator goes low. The difference between the DAC codes applied to AD9501 #2 and AD9501 #1 is a measure of the settling time of the D/A converter being tested.

Layout Considerations

Although the inputs and output of the AD9501 are digital, the delay is determined by analog circuits. This makes it critical to use high speed analog circuit layout techniques to achieve rated performance.

The ground plane should be on the component side of the board and extend under the AD9501 to shield it from digital switching signals. Most socket assemblies add significant inter-lead capacitance and should be avoided whenever possible. If sockets must be used, individual pin sockets, such as TYCO part numbers 5-330808-3 (closed end) or 5-330808-6 (open end), should be used.

Power supply decoupling is also critical for high speed design; a 0.1 µF capacitor should be connected as close as possible to each supply pin.

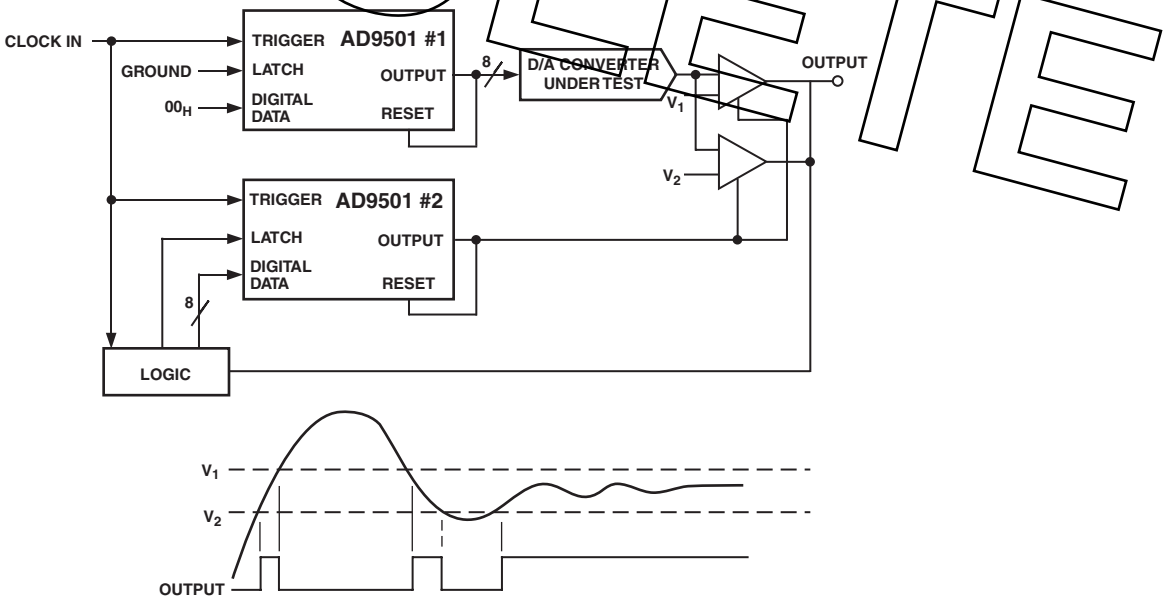
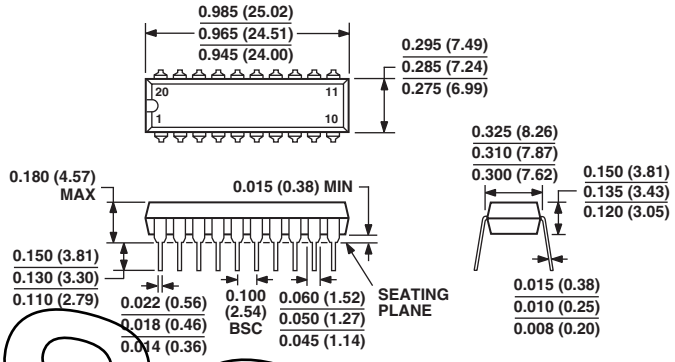


Figure 11. Analog Settling Time Measurement

OUTLINE DIMENSIONS

20-Lead Plastic Dual In-Line Package [PDIP]
(N-20)

Dimensions shown in inches and (millimeters)

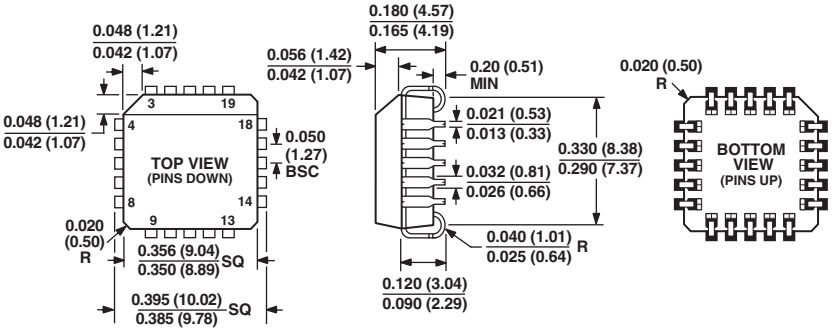


COMPLIANT TO JEDEC STANDARDS MO-095-AE

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

20-Lead Plastic Leaded Chip Carrier [PLCC]
(P-20A)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
3/04–Data Sheet changed from REV. A to REV. B.	
Changes to GENERAL DESCRIPTION	1
Military package deleted	1
Edit to SPECIFICATIONS	2
Edits to ABSOLUTE MAXIMUM RATINGS	3
Edits to ORDERING GUIDE	3
Edit to Figure 1	4
Edit to Figure 4	6
Q-20 package deleted	11

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