# 14-Bit CCD/CIS Signal Processor

# AD9814S

## 1.0 Scope

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD9814.

## 2.0 Part Number. The complete part number(s) of this specification follow:

| Part Number | Description |
|---|---|
| **AD9814-703F** | Complete 14-Bit CCD/CIS Signal Processor |

## 3.0 Case Outline

| Letter | Descriptive designator | Case Outline (Lead Finish per MIL-PRF-38535) |
|---|---|---|
| F | CDFP3-F28 | 28 lead bottom-brazed flatpack |

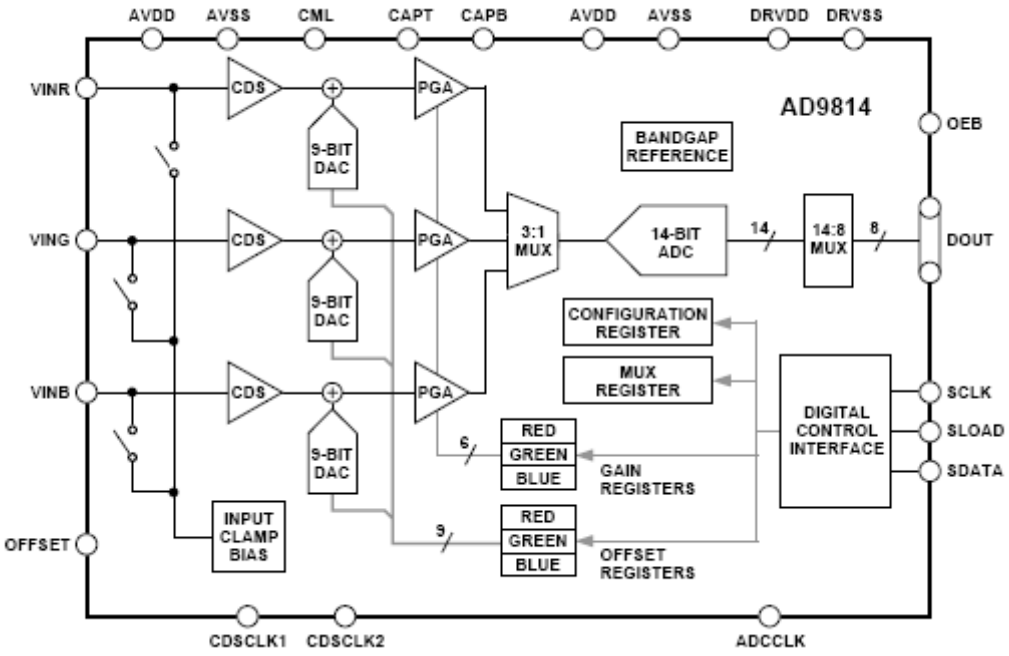


Figure 1 - Functional Block Diagram





**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.326.8703** 

| Pin Number | Name | Type | Description |
|---|---|---|---|
| 1 | CDSCLK1 | DI | CDS Reference Level Sampling Clock |
| 2 | CDSCLK2 | DI | CDS Data Level Sampling Clock |
| 3 | ADCCLK | DI | A/D Converter Sampling Clock |
| 4 | OEB | DI | Output Enable, Active Low |
| 5 | DRVDD | P | Digital Output Driver Supply |
| 6 | DRVSS | P | Digital Output Driver Ground |
| 7 | D7 | DO | Data Output MSB. ADC DB13 High Byte, ADC DB5 Low Byte |
| 8 | D6 | DO | Data Output. ADC DB12 High Byte, ADC DB4 Low Byte |
| 9 | D5 | DO | Data Output. ADC DB11 High Byte, ADC DB3 Low Byte |
| 10 | D4 | DO | Data Output. ADC DB10 High Byte, ADC DB2 Low Byte |
| 11 | D3 | DO | Data Output. ADC DB9 High Byte, ADC DB1 Low Byte |
| 12 | D2 | DO | Data Output. ADC DB8 High Byte, ADC DB0 Low Byte |
| 13 | D1 | DO | Data Output. ADC DB7 High Byte, Don’t Care Low Byte |
| 14 | D0 | DO | Data Output LSB. ADC DB6 High Byte, Don’t Care Low Byte |
| 15 | SDATA | DI/DO | Serial Interface Data Input/Output |
| 16 | SCLK | DI | Serial Interface Clock Input |
| 17 | SLOAD | DI | Serial Interface Load Pulse |
| 18 | AVDD | P | +5 V Analog Supply |
| 19 | AVSS | P | Analog Ground |
| 20 | CAPB | AO | ADC Bottom Reference Voltage Decoupling |
| 21 | CAPT | AO | ADC Top Reference Voltage Decoupling |
| 22 | VINB | AI | Analog Input, Blue Channel |
| 23 | CML | AO | Internal Bias Level Decoupling |
| 24 | VING | AI | Analog Input, Green Channel |
| 25 | OFFSET | AO | Clamp Bias Level Decoupling |
| 26 | VINR | AI | Analog Input, Red Channel |
| 27 | AVSS | P | Analog Ground |
| 28 | AVDD | P | +5 V Analog Supply |

Type: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

Figure 2 – Terminal Connections and Pin Function Descriptions

## 4.0 Absolute Maximum Ratings. ($T_A$ = 25°C, unless otherwise noted)

| Parameter | With respect to | Min | Max | Units |
|---|---|---|---|---|
| VIN, CAPT, CAPB | AVSS | -0.3 | AVDD + 0.3 | V |
| Digital Inputs | AVSS | -0.3 | AVDD + 0.3 | V |
| AVDD | AVSS | -0.5 | +6.5 | V |
| DRVDD | DRVSS | -0.5 | +6.5 | V |
| AVSS | DRVSS | -0.3 | +0.3 | V |
| Digital Outputs | DRVSS | -0.3 | DRVDD + 0.3 | V |
| Junction Temperature | | | +150 | °C |
| Storage Temperature | | -65 | +150 | °C |
| Lead Temperature (10 sec) | | | +300 | °C |

NOTES:

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

The input limits are defined as maximum tolerable voltage levels into the AD9814. These levels are not intended to be in the linear input range of the device. Signals beyond the input limits will turn on the overvoltage protection diodes.

## 5.0 Thermal Characteristics:

| Package Type | Junction-to-Case ($\Theta_{JC}$) | Junction-to-Ambient ($\Theta_{JA}$) | Units |
|---|---|---|---|
| Thermal Resistance, Bottom Brazed (F) | 22 | 60 | °C/W Max |

## 6.0 Table I. Electrical Table:

| Table I | | | | | | |
|---|---|---|---|---|---|---|
| Parameter<br>See notes at end of table | Symbol | Conditions 1/<br>Unless Otherwise Specified | Sub Group | Limit Min | Limit Max | Units |
| RESOLUTION | RES | No Missing Codes | 1,2,3 | 14 | | Bits |
| Supply Currents | IAVDD | | 1,2,3 | | 80 | mA |
| | IDRVDD | | 1,2,3 | | 10 | mA |
| Power dissipation | PD | | 1,2,3 | | 450 | mW |
| Power supply rejection | PSR | AVDD= +5.0V ± 0.25V | 1,2 | | 0.3 | %FSR |
| | | | 3 | | 0.5 | %FSR |
| ACCURACY (Entire Signal Path)<br>Integral Nonlinearity 2/ | INL | | 1,2 | -11 | 11 | LSB |
| | | | 3 | -18 | 11 | LSB |
| ACCURACY (Entire Signal Path)<br>Differential Nonlinearity | DNL | | 1 | -1 | 1.25 | LSB |
| | | | 2 | -1 | 1 | LSB |
| | | | 3 | -1 | 1.5 | LSB |
| ACCURACY (Entire Signal Path)<br>Offset Error | VOS | | 1,2,3 | -104 | 104 | mV |
| ACCURACY (Entire Signal Path)<br>Gain Error 3/ | GAIN | | 1,2,3 | -5.3 | 5.3 | %FSR |
| PGA Gain Ratio 4/ | PGA GAIN | | 1,2,3 | 5.7 | 5.9 | |
| DIFFERENTIAL VREF<br>CAPT-CAPB (4V Input Range) | VREF4 | | 1,2,3 | 1.9 | 2.1 | V |
| DIFFERENTIAL VREF<br>CAPT-CAPB (2V Input Range) | VREF2 | | 1,2,3 | 0.94 | 1.06 | V |

TABLE I NOTES:

1/ $T_A$ = +25 °C, $T_A$ Max = +125 °C, $T_A$ Min = -55 °C. AVDD = +5 V, DRVDD = +5 V, 3-Channel CDS, $F_{ADCCLK}$ = 6 MHz, $F_{CDSCLK1}$ = $F_{CDSCLK2}$ = 2 MHz, PGA Gain = 1, Input Range = 4V, unless otherwise noted.

2/ INL is measured using the “fixed endpoint” method, NOT using a “best-fit” calculation.

3/ The Gain Error specification is dominated by the tolerance of the internal differential voltage reference.

4/ The PGA Gain is approximately “linear in dB” and follows the equation: PGA Gain = (5.8 / (1 + 4.8 (63 – G) / 63)) where G is the register value.

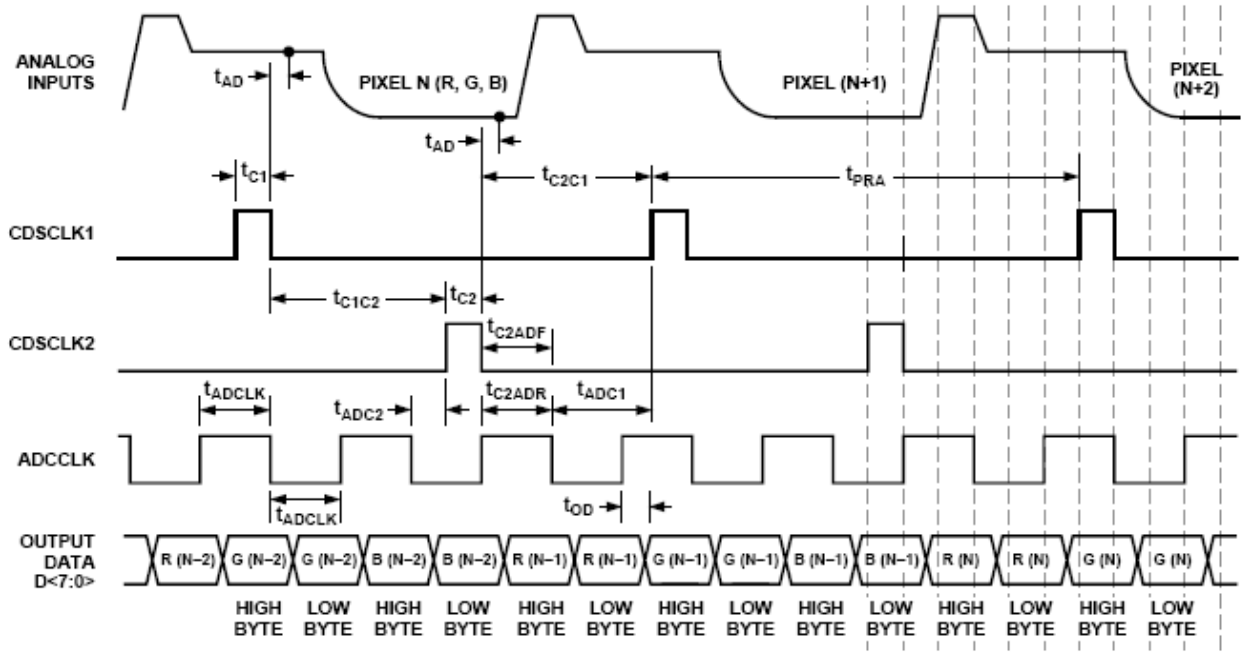


Figure 3 – 3-Channel CDS Mode Timing Diagram

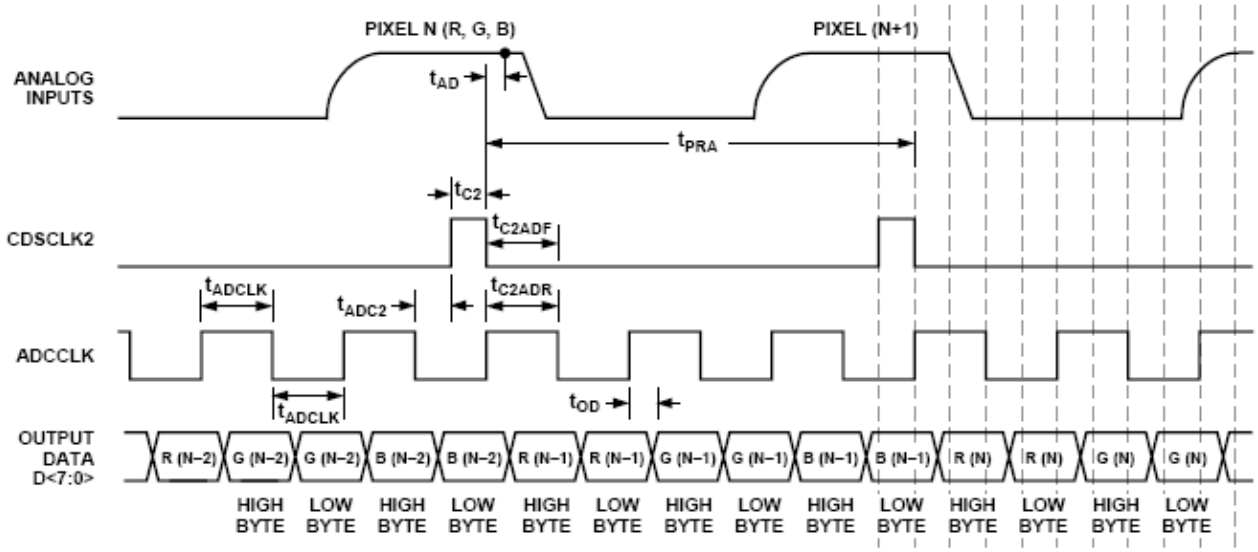


Figure 4 – 3-Channel SHA Mode Timing Diagram

## 6.0 Table II. Electrical Test Requirements:

| Table II | |
|---|---|
| Test Requirements | Subgroups (in accordance with MIL-PRF-38535, Table III) |
| Interim Electrical Parameters | 1 |
| Final Electrical Parameters | 1, 2, 3 1/ 2/ |
| Group A Test Requirements | 1, 2, 3 |
| Group C end-point electrical parameters | 1 2/ |
| Group D end-point electrical parameters | 1 |
| Group E end-point electrical parameters | N/A |

Notes:
1/ PDA applies to Subgroup 1. Delta's excluded from PDA.
2/ See Table III for Delta limits.

## 7.0 Table III. Life Test / Burn-in Delta limits:

| Table III | | |
|---|---|---|
| **Test Symbol** | **Delta Limit** | **Units** |
| IAVDD | +/-2 | mA |
| VOS | +/-13.2 (+/-54) | mV (LSB) |
| GAIN | +/-0.56 (+/-91) | % (LSB) |
| +INL | +/-6 | LSB |
| -INL | +/-5 | LSB |
| +DNL | +/-0.5 | LSB |
| -DNL | +/-0.35 | LSB |

## 8.0 Life Test / Burn-In Circuit:

8.1 HTRB is not applicable for this drawing.
8.2 Burn-in is per MIL-STD-883 Method 1015, test condition D.
8.3 Steady state life test is per MIL-STD-883 Method 1005, test condition D.

## 9.0 MIL-STD-38535 QMLV exceptions:

9.1 Full WLA per MIL-STD-883 TM 5007 is not available for this product. SEM Inspection only is available per MIL-STD-883, TM2018.
9.2 This product is manufactured in a MIL-PRF-38535 QMLQ certified wafer fab facility.

| Rev | Description of Change | Date |
|---|---|---|
| A | Initiate | Sept 9, 2007 |
| B | Update header/footer and add to 1.0 Scope description. | March 7, 2008 |
| C | Add reference notations to Section 4.0, Table I | April 7, 2008 |
| D | Remove post Group C specification limits in Table III such that only Delta limits are listed. Remove QMLV exception for testing in QMLQ facility. Add Figure 2 pin descriptions. Formatting improvements. | March 24, 2010 |
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