Low Power, 12.65 mW, 2.3 V to 5.5 V, Programmable Waveform Generator

Enhanced Product

AD9833-EP

FEATURES

- Digitally programmable frequency and phase
- 12.65 mW power consumption at 3 V
- 0 MHz to 12.5 MHz output frequency range
- 28-bit resolution: 0.1 Hz at 25 MHz reference clock
- Sinusoidal, triangular, and square wave outputs
- 2.3 V to 5.5 V power supply
- No external components required
- 3-wire SPI interface
- Power-down option
- 10-lead MSOP package
- Enhanced product features
  - Supports defense and aerospace applications (AQEC)
  - Temperature range: −55°C to +125°C
  - Controlled manufacturing baseline
  - 1 assembly/test site
  - 1 fabrication site
  - Enhanced product change notification
  - Qualification data available upon request

APPLICATIONS

- Frequency stimulus/waveform generation
- Liquid and gas flow measurement
- Sensory applications: proximity, motion, defect detection
- Line loss/attenuation
- Test and medical equipment
- Sweep/clock generators
- Time domain reflectometry (TDR) applications

GENERAL DESCRIPTION

The AD9833-EP is a low power, programmable waveform generator capable of producing sine, triangular, and square wave outputs. Waveform generation is required in various types of sensing, actuation, and time domain reflectometry (TDR) applications. The output frequency and phase are software programmable, allowing easy tuning. No external components are needed. The frequency registers are 28 bits wide. With a 25 MHz clock rate, a resolution of 0.1 Hz can be achieved; with a 1 MHz clock rate, the AD9833-EP can be tuned to 0.004 Hz resolution.

The AD9833-EP is written to via a 3-wire serial interface. This serial interface operates at clock rates up to 40 MHz and is compatible with DSP and microcontroller standards. The device operates with a power supply from 2.3 V to 5.5 V.

The AD9833-EP has a power-down function (SLEEP). This function allows sections of the device that are not being used to be powered down, thus minimizing the current consumption of the part. For example, the DAC can be powered down when a clock output is being generated.

The AD9833-EP is available in a 10-lead MSOP package. Additional application and technical information can be found in the AD9833 data sheet.

FUNCTIONAL BLOCK DIAGRAM

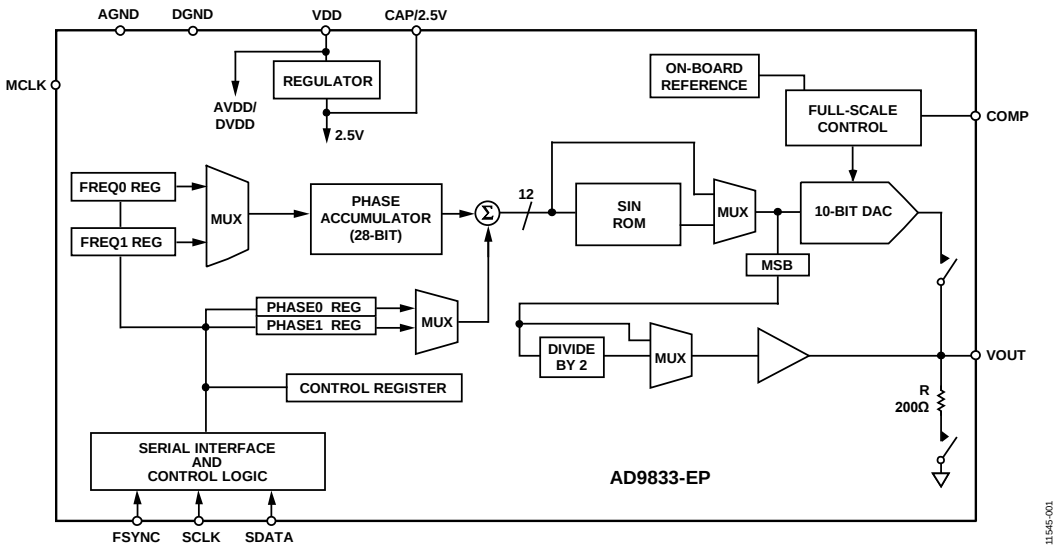

Figure 1.

Rev. 0 Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

8/13—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, $T_A = T_{MIN}$ to T_{MAX}, R_{SET} = 6.8 kΩ for VOUT, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS					
Resolution		10		Bits	
Update Rate			25	MSPS	
VOUT Maximum		0.65		V	
VOUT Minimum		38		mV	
VOUT Temperature Coefficient		200		ppm/°C	
DC Accuracy					
Integral Nonlinearity		±1.0		LSB	
Differential Nonlinearity		±0.5		LSB	
DDS SPECIFICATIONS (SFDR)					
Dynamic Specifications					
Signal-to-Noise Ratio (SNR)	53.5	60		dB	f_{MCLK} = 25 MHz, $f_{OUT} = f_{MCLK}/4096$
Total Harmonic Distortion (THD)		−66	−53.5	dBc	f_{MCLK} = 25 MHz, $f_{OUT} = f_{MCLK}/4096$
Spurious-Free Dynamic Range (SFDR)					
Wideband (0 to Nyquist)		−60		dBc	f_{MCLK} = 25 MHz, $f_{OUT} = f_{MCLK}/50$
Narrow-Band (±200 kHz)		−78		dBc	f_{MCLK} = 25 MHz, $f_{OUT} = f_{MCLK}/50$
Clock Feedthrough		−60		dBc	
Wake-Up Time		1		ms	
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.7			V	2.3 V to 2.7 V power supply
	2.0			V	2.7 V to 3.6 V power supply
	2.8			V	4.5 V to 5.5 V power supply
Input Low Voltage, V_{INL}			0.5	V	2.3 V to 2.7 V power supply
			0.7	V	2.7 V to 3.6 V power supply
			0.8	V	4.5 V to 5.5 V power supply
Input Current, I_{INH}/I_{INL}			10	µA	
Input Capacitance, C_{IN}		3		pF	
POWER SUPPLIES					f_{MCLK} = 25 MHz, $f_{OUT} = f_{MCLK}/4096$
VDD	2.3		5.5	V	
I_{DD}		4.5	5.5	mA	I_{DD} code dependent; see Figure 7
Low Power Sleep Mode		0.5		mA	DAC powered down, MCLK running

[1] Operating temperature range is −55°C to +125°C; typical specifications are at 25°C.

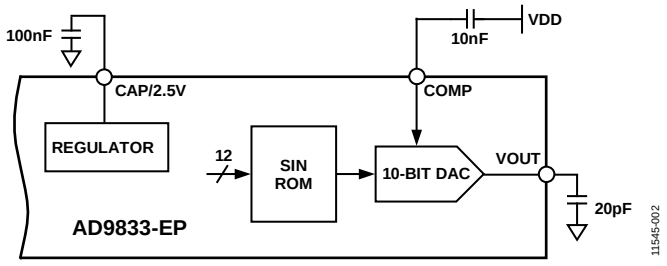

Figure 2. Test Circuit Used to Test Specifications

TIMING CHARACTERISTICS

VDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, unless otherwise noted.[1]

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_1	40	ns min	MCLK period
t_2	16	ns min	MCLK high duration
t_3	16	ns min	MCLK low duration
t_4	25	ns min	SCLK period
t_5	10	ns min	SCLK high duration
t_6	10	ns min	SCLK low duration
t_7	5	ns min	FSYNC to SCLK falling edge setup time
$t_{8\ min}$	10	ns min	FSYNC to SCLK hold time
$t_{8\ max}$	$t_4 - 5$	ns max	
t_9	5	ns min	Data setup time
t_{10}	3	ns min	Data hold time
t_{11}	5	ns min	SCLK high to FSYNC falling edge setup time

[1] Guaranteed by design, not production tested.

Timing Diagrams

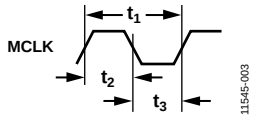

Figure 3. Master Clock

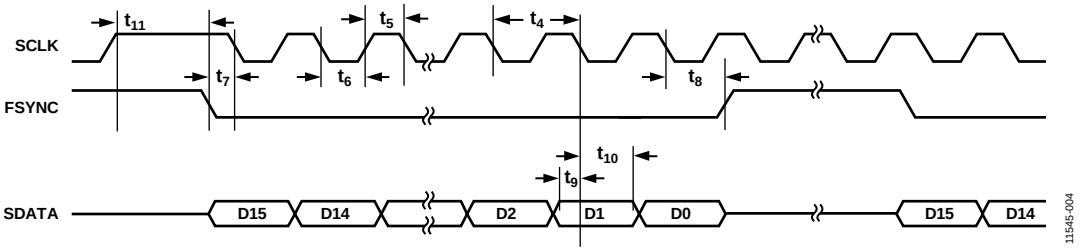

Figure 4. Serial Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to AGND	−0.3 V to +6 V
VDD to DGND	−0.3 V to +6 V
AGND to DGND	−0.3 V to +0.3 V
CAP/2.5V	2.75 V
Digital I/O Voltage to DGND	−0.3 V to VDD + 0.3 V
Analog I/O Voltage to AGND	−0.3 V to VDD + 0.3 V
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
MSOP Package	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

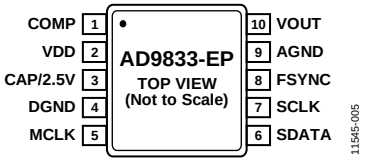

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COMP	DAC Bias Pin. This pin is used for decoupling the DAC bias voltage.
2	VDD	Positive Power Supply for the Analog and Digital Interface Sections. The on-board 2.5 V regulator is also supplied from VDD. VDD can have a value from 2.3 V to 5.5 V. A 0.1 µF and a 10 µF decoupling capacitor should be connected between VDD and AGND.
3	CAP/2.5V	The digital circuitry operates from a 2.5 V power supply. This 2.5 V is generated from VDD using an on-board regulator when VDD exceeds 2.7 V. The regulator requires a decoupling capacitor of 100 nF typical, which is connected from CAP/2.5V to DGND. If VDD is less than or equal to 2.7 V, CAP/2.5V should be tied directly to VDD.
4	DGND	Digital Ground.
5	MCLK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. The output frequency accuracy and phase noise are determined by this clock.
6	SDATA	Serial Data Input. The 16-bit serial data-word is applied to this input.
7	SCLK	Serial Clock Input. Data is clocked into the AD9833-EP on each falling edge of SCLK.
8	FSYNC	Active Low Control Input. FSYNC is the frame synchronization signal for the input data. When FSYNC is taken low, the internal logic is informed that a new word is being loaded into the device.
9	AGND	Analog Ground.
10	VOUT	Voltage Output. The analog and digital output from the AD9833-EP is available at this pin. An external load resistor is not required because the device has a 200 Ω resistor on board.

TYPICAL PERFORMANCE CHARACTERISTICS

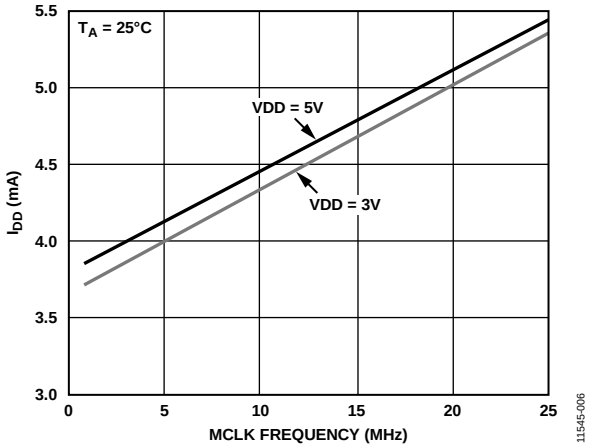

Figure 6. Typical Current Consumption (I_{DD}) vs. MCLK Frequency for f_{OUT} = MCLK/10

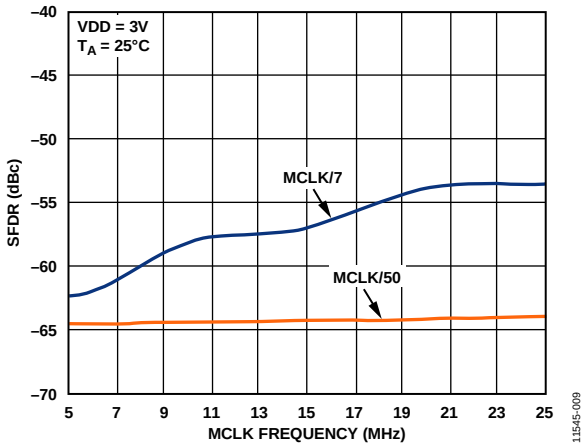

Figure 9. Wideband SFDR vs. MCLK Frequency

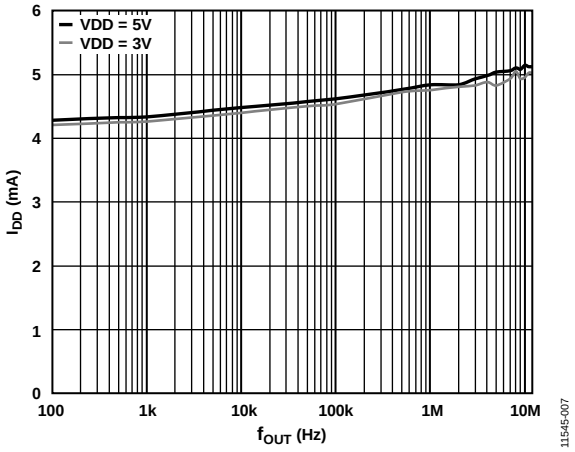

Figure 7. Typical I_{DD} vs. f_{OUT} for f_{MCLK} = 25 MHz

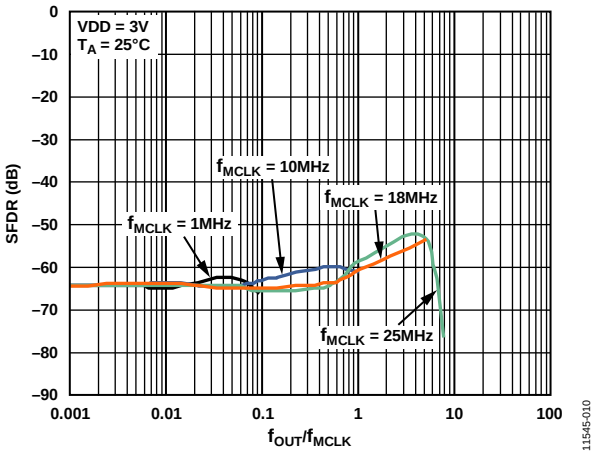

Figure 10. Wideband SFDR vs. f_{OUT}/f_{MCLK} for Various MCLK Frequencies

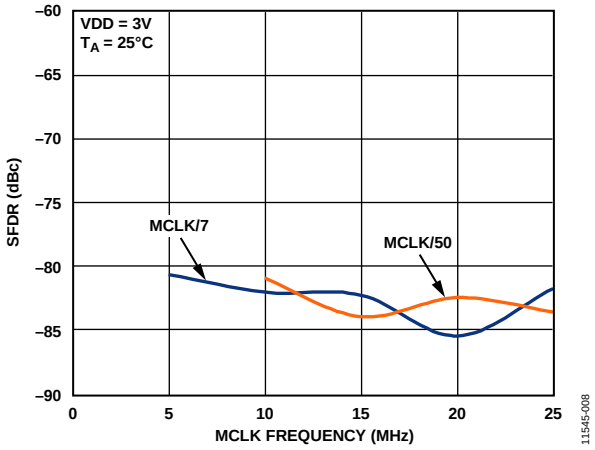

Figure 8. Narrow-Band SFDR vs. MCLK Frequency

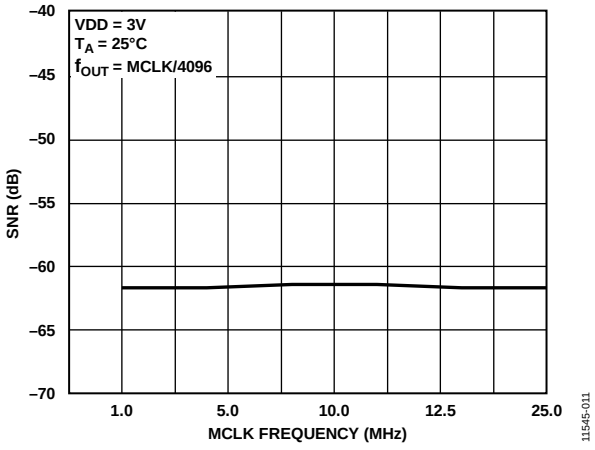

Figure 11. SNR vs. MCLK Frequency

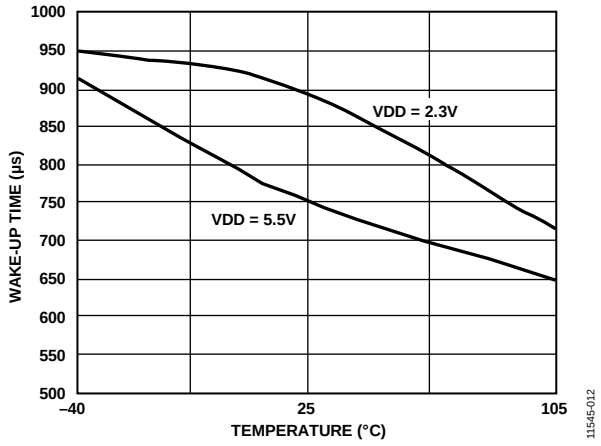

Figure 12. Wake-Up Time vs. Temperature

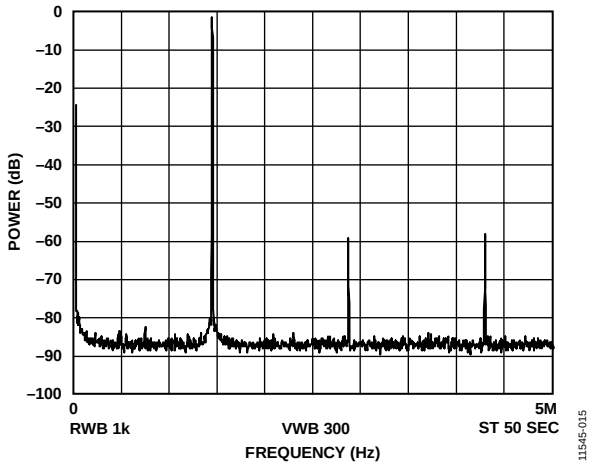

Figure 15. Power vs. Frequency, f_{MCLK} = 10 MHz, f_{OUT} = 1.43 MHz = $f_{MCLK}/7$, Frequency Word = 0x2492492

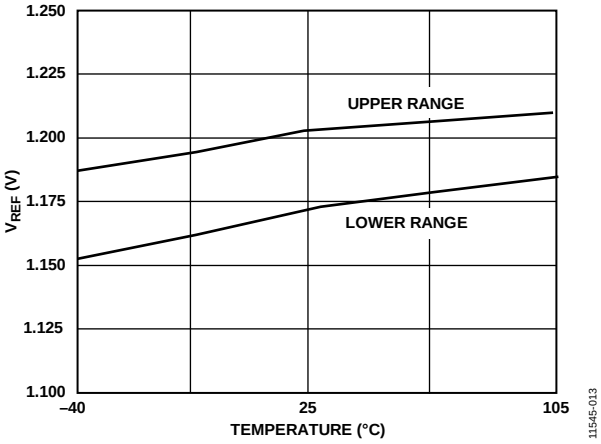

Figure 13. V_{REF} vs. Temperature

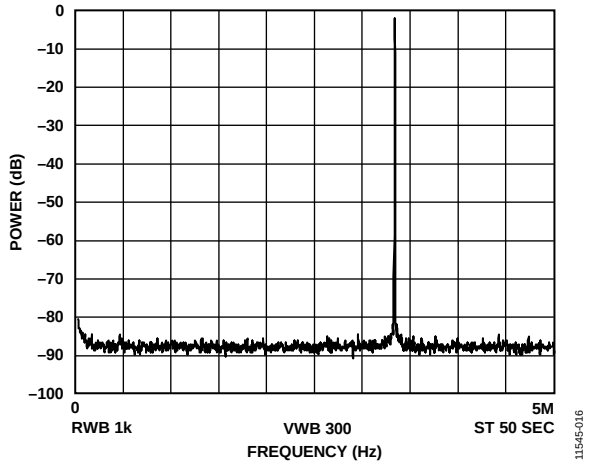

Figure 16. Power vs. Frequency, f_{MCLK} = 10 MHz, f_{OUT} = 3.33 MHz = $f_{MCLK}/3$, Frequency Word = 0x5555555

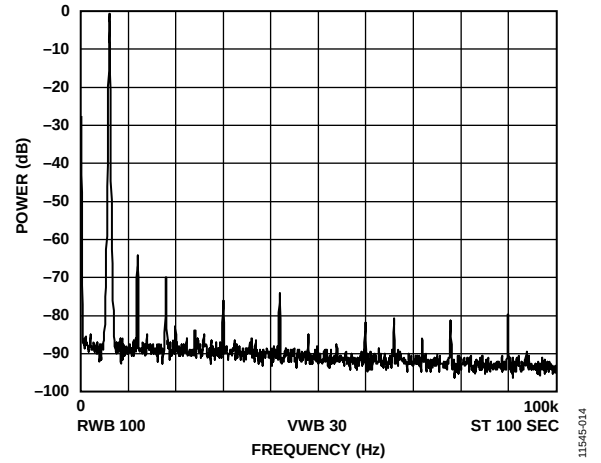

Figure 14. Power vs. Frequency, f_{MCLK} = 10 MHz, f_{OUT} = 2.4 kHz, Frequency Word = 0x000FBA9

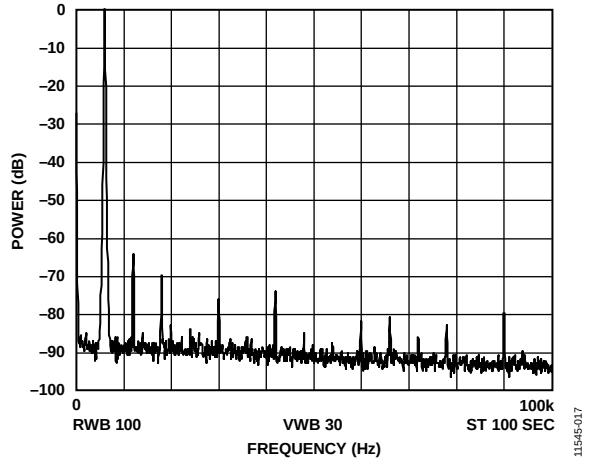

Figure 17. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 6 kHz, Frequency Word = 0x000FBA9

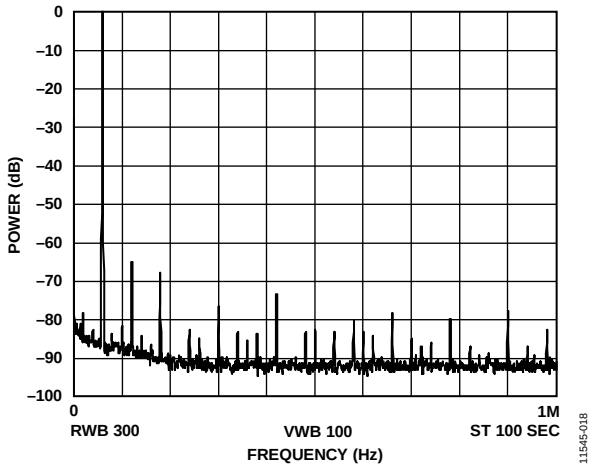

Figure 18. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 60 kHz, Frequency Word = 0x009D495

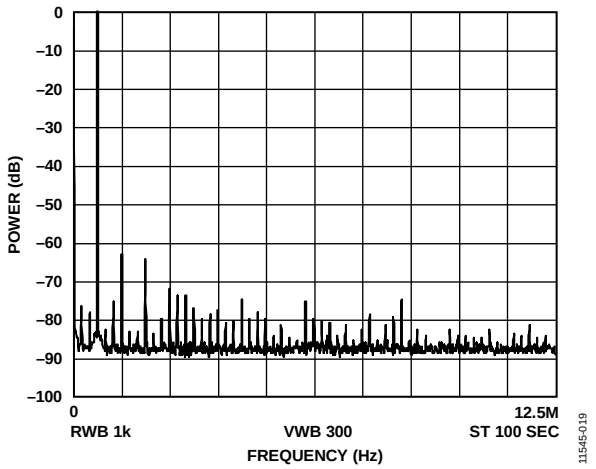

Figure 19. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 600 kHz, Frequency Word = 0x0624DD3

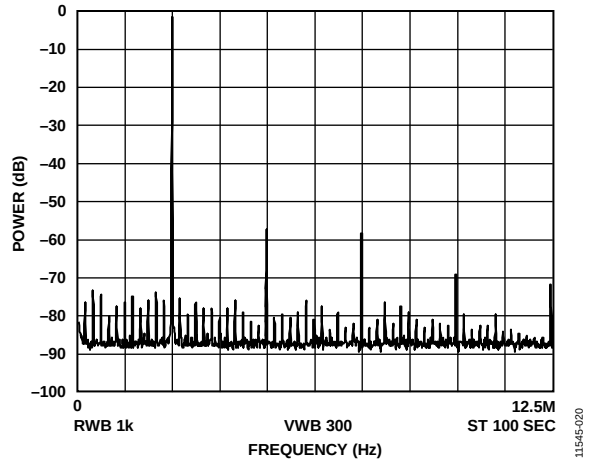

Figure 20. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 2.4 MHz, Frequency Word = 0x189374D

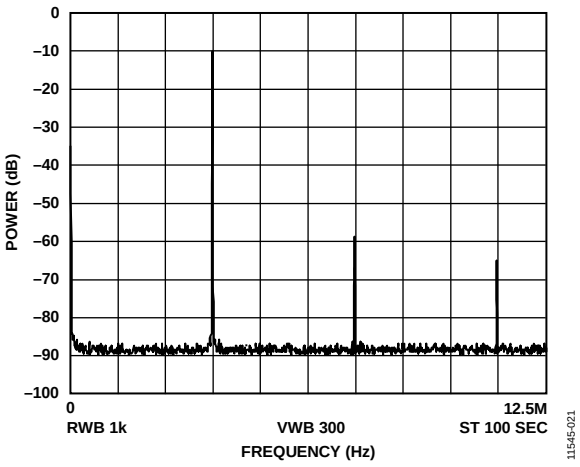

Figure 21. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 3.857 MHz = f_{MCLK}/7, Frequency Word = 0x2492492

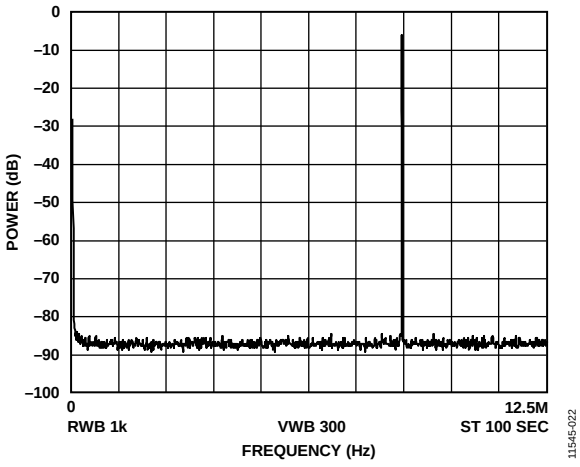

Figure 22. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 8.333 MHz = f_{MCLK}/3, Frequency Word = 0x5555555

OUTLINE DIMENSIONS

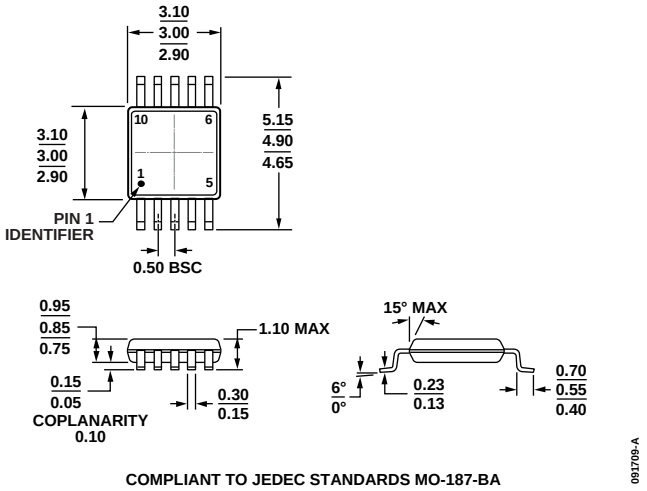

Figure 23. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD9833SRMZ-EP-RL7	−55°C to +125°C	10-Lead MSOP	RM-10	DMR

[1] Z = RoHS Compliant Part.

NOTES

NOTES