National Semiconductor

ADVANCE INFORMATION
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ADC08B3000
High Performance, Low Power, 8-Bit, 3 GSPS A/D Converter with 4K Buffer

General Description

Note: This product is currently in development. - ALL specifications are design targets and are subject to change.

The ADC08B3000 is a single, low power, high performance CMOS analog-to-digital converter that digitizes signals to 8 bits resolution at sampling rates up to 3.4 GSPS. Consuming a typical 1.8 Watts at 3 GSPS from a single 1.9 Volt supply, this device is guaranteed to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier and the self-calibration scheme enable a very flat response of all dynamic parameters upto Nyquist, producing a high 7.0 ENOB with a 748 MHz input signal and a 3 GHz sample rate while providing a 10^{-18} B.E.R. 3 GSPS is achieved through using a 1.5GHz clock. Output formatting is offset binary. The device contains a 4K FIFO Capture Buffer which is used to feed two 8 bit CMOS output busses at a rate up to 200MHz.

The converter typically consumes less than 20 mW in the Power Down Mode and is available in a 128-lead, thermally enhanced exposed pad LQFP and operates over the Industrial ($-40^{\circ}C \le T_A \le +85^{\circ}C$) temperature range.

Features

- Internal Sample-and-Hold
- Single +1.9V ±0.1V Operation
- Choice of SDR or DDR output clocking
- Internal selectable 4K Data Buffer
- Clock Phase Adjust for Multiple ADC Synchronization
- Guaranteed No Missing Codes
- Serial Interface for Extended Control
- Fine Adjustment of Input Full-Scale Range and Offset
- Duty Cycle Corrected Sample Clock

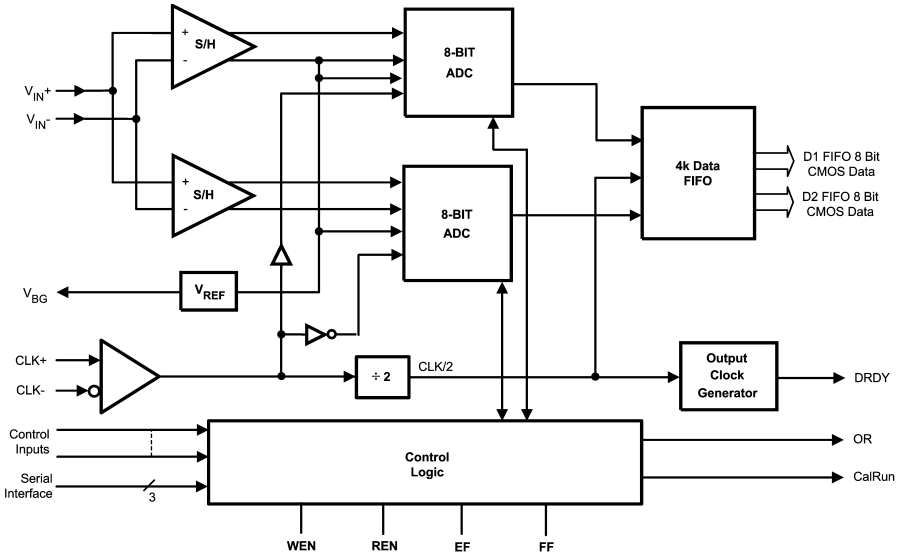
Key Specifications

■ Resolution	8 Bits
■ Max Conversion Rate	3 GSPS (min)
■ Bit Error Rate	10^{-18} (typ)
■ ENOB @ 748 MHz Input	7.0 Bits (typ)
■ SNR @ 748 MHz	44 dB (typ)
■ Full Power Bandwidth	TBD
■ Power Consumption	
— Operating	1.8 W (typ)
— Power Down Mode	20 mW (typ)

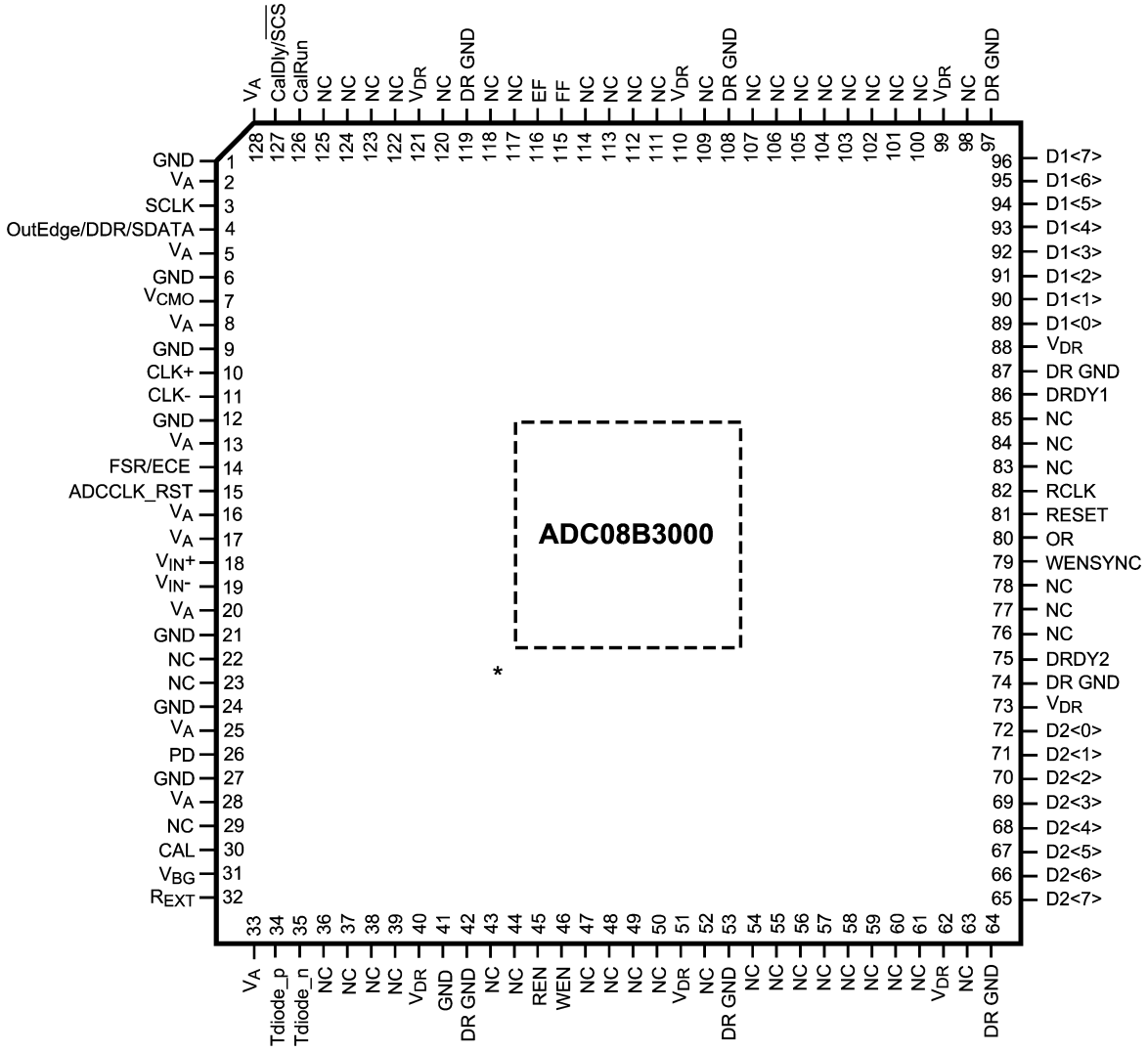
Applications

- Ranging Applications
- Test and measurement Applications

Block Diagram



Pin Configuration



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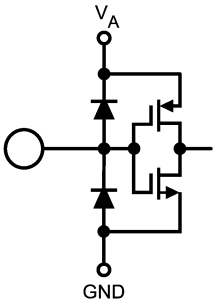
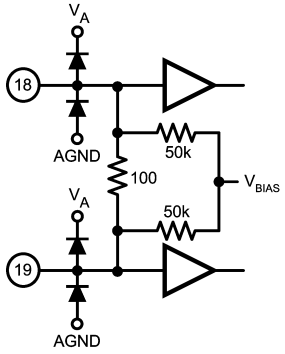
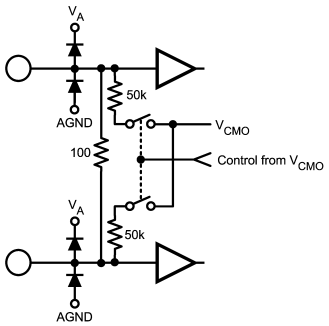
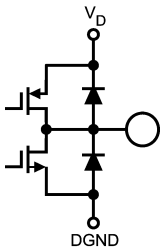
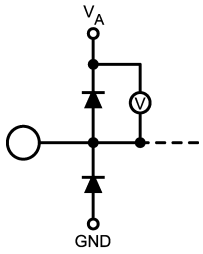
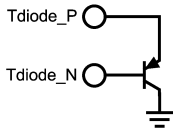
* Exposed pad on back of package must be soldered to ground plane to ensure rated performance.

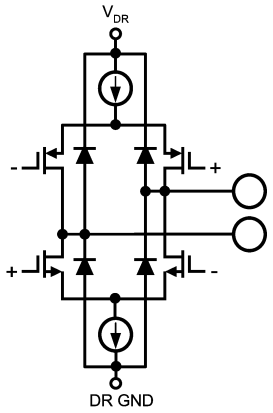
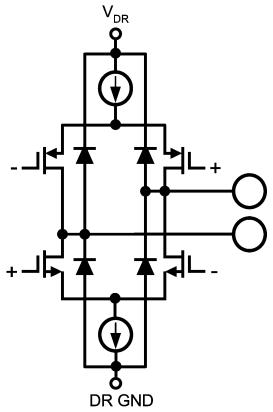
Pin Descriptions and Equivalent Circuits

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
3	SCLK		Serial Interface Clock. When the extended control mode is enabled, this pin functions as the SCLK input which clocks in the serial data.See Section 1.2 for details on the extended control mode. See Section 1.3 for description of the serial interface. When not in extended control mode, tie to ground.
4	OutEdge / DDR / SDATA		Edge Select, Double Data Rate Enable and Serial Data Input. This input sets the edge of DRDY at which the output data transitions. (See Section 1.1.5.2). When this pin is floating or connected to 1/2 the supply voltage, DDR clocking is enabled. When the extended control mode is enabled, this pin functions as the SDATA input. See Section 1.2 for details on the extended control mode. See Section 1.3 for description of the serial interface.
15	ADCCLK_RST		ADC Sample Clock Reset. A positive pulse on this pin is used to reset and synchronize the ADC sampling clock.
26	PD		Power Down Pins. A logic high on the PD pin puts the entire device into the Power Down Mode.
30	CAL		Calibration Cycle Initiate. A minimum 80 input clock cycles logic low followed by a minimum of 80 input clock cycles high on this pin initiates the self calibration sequence. See Section 2.4.2 for an overview of self-calibration and Section 2.4.2.2 for a description of on-command calibration.
14	FSR/ECE		Full Scale Range Select and Extended Control Enable. In non-extended control mode, a logic low on this pin sets the full-scale differential input range to 600 mV_{P-P}. A logic high on this pin sets the full-scale differential input range to 800 mV_{P-P}. See Section 1.1.4. To enable the extended control mode, whereby the serial interface and control registers are employed, allow this pin to float or connect it to a voltage equal to $V_A/2$. See Section 1.2 for information on the extended control mode.
127	CalDly / $\overline{SCS}$		Calibration Delay and Serial Interface Chip Select. With a logic high or low on pin 14, this pin functions as Calibration Delay and sets the number of input clock cycles after power up before calibration begins (See Section 1.1.1). With pin 14 floating, this pin acts as the enable pin for the serial interface input and the CalDly value becomes "0" (short delay with no provision for a long power-up calibration delay).
10 11	CLK+ CLK-		LVDS Clock input pins for the ADC. The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on the falling edge of CLK+. See Section 1.1.2 for a description of acquiring the input and Section 2.3 for an overview of the clock inputs.

Pin Descriptions and Equivalent Circuits (Continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
18 19	V_{IN}+ V_{IN}–		Analog signal inputs to the ADC. The differential full-scale input range is 600 mV_{P-P} when the FSR pin is low, or 800 mV_{P-P} when the FSR pin is high.
7	V_{CMO}		Common Mode Voltage. The voltage output at this pin is required to be the common mode input voltage at V_{IN}+ and V_{IN}– when d.c. coupling is used. This pin should be grounded when a.c. coupling is used at the analog input. This pin is capable of sourcing or sinking 100µA. See Section 2.2.
31	V_{BG}		Bandgap output voltage capable of 100 µA source/sink.
126	CalRun		Calibration Running indication. This pin is at a logic high when calibration is running.
32	R_{EXT}		External bias resistor connection. Nominal value is 3.3k-Ohms (±0.1%) to ground. See Section 1.1.1.
34 35	Tdiode_P Tdiode_N		Temperature Diode Positive (Anode) and Negative (Cathode) for die temperature measurements. See Section 2.6.2.
45	REN		Read Enable. A logic high on this input causes a byte of data to be read from the Capture Buffer with each RCLK cycle. This signal must not be asserted while the WEN is already asserted. This signal may be asserted asynchronously as it is internally synchronized with the internal sampling clock.
46	WEN		Write Enable. A logic high on this input causes a byte of data to be written into the Capture Buffer with each sampling clock cycle.This signal may be asserted asynchronously as it is internally synchronized with the internal sampling clock.

Pin Descriptions and Equivalent Circuits (Continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
72 71 70 69 68 67 66 65	D2<0> D2<1> D2<2> D2<3> D2<4> D2<5> D2<6> D2<7>		Digital Data Output 2. When the REN input is asserted and 2X8 Output Enable is set in the FIFO register, data from banks Da and Dc are read from the capture buffer and presented on this port synchronous with each rising edge of RCLK. When 2X8 Output Enable is not set in the FIFO register, data output 2 is high-Z.
75	DRDY2		Data Ready 2. DRDY is generated by RCLK and is synchronized to the output data. The use of this pin assists in eliminating the latency uncertainty between when RCLK transitions and when data transitions on the output
89 90 91 92 93 94 95 96	D1<0> D1<1> D1<2> D1<3> D1<4> D1<5> D1<6> D1<7>		Digital Data Output 1. When the REN input is asserted, data is read from the capture buffer and presented on this port synchronous with each rising edge of RCLK. When 2X8 Output Eanble is set in the FIFO resgister, data from banks Db and Dd only are presented on this port. When REN is deasserted, this output holds the data from the previous read. When 2X8 Output Enable is not set in the FIFO register, port presents data from Da, Db, Dc, Dd banks.
86	DRDY1		Data Ready 1. DRDY is generated by RCLK and is synchronized to the output data. The use of this pin assists in eliminating the latency uncertainty between when RCLK transitions and when data transitions on the output
79	WENSYNC		Synchronized WEN. The control input WEN is synchronized on-chip with the internal Sampling Clock and is provided at this output.
80	OR		Out Of Range output. A logic high on this pin indicates that the differential input is out of range (outside the range ±300 mV or ±400 mV as defined by the FSR pin). This signal is asserted if the input signal has over ranged at any time during the data capture operation. This pin is cleared after the Capture Buffer is read or after asserting the RESET pin.
81	RESET		A logic high at this input resets all Capture Buffer control logic in the chip.
82	RCLK		Read Clock. Free running clock that is used to read data from the Capture Buffer. The parallel data on the data output port and the EF flag are asserted synchronous to this clock.

Pin Descriptions and Equivalent Circuits (Continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
115	FF		Buffer Full Flag. This signal is asserted synchronous to the internal sampling clock when the capture buffer is full. If the WEN input remains asserted, the next CLK will cause an overflow, whereby the pointer will wrap around and begin overwriting the old data if the ASW bit is set to 0 in the Capture Buffer Control register. This signal is deasserted when a read cycle is initiated and the data buffer is no longer 'full'.
116	EF		Buffer Empty Flag. This signal is asserted synchronous to the RCLK signal when the Capture Buffer is empty. It is deasserted when a write cycle is initiated and the data buffer is no longer 'empty'.
2, 5, 8, 13, 16, 17, 20, 25, 28, 33, 128	V_A		Analog power supply pins. Bypass these pins to ground.
40, 51 ,62, 73, 88, 99, 110, 121	V_{DR}		Output Driver power supply pins. Bypass these pins to DR GND.
1, 6, 9, 12, 21, 24, 27, 41	GND		Ground return for V_A.
42, 53, 64, 74, 87, 97, 108, 119	DR GND		Ground return for V_{DR}.

Pin Descriptions and Equivalent Circuits (Continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
22, 23, 29, 36, 37, 38, 39, 43, 44, 47, 48, 49, 50, 52, 54, 55, 56, 57, 58, 59, 60, 61, 63, 76, 77, 78, 83, 84, 85, 98, 100, 101, 102, 103, 104, 105, 106, 107, 109, 111, 112, 113, 114, 117, 118, 120, 122, 123, 124, 125	NC		No Connection. Make no connection to these pins

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_{DR})	2.2V
Voltage on Any Input Pin	−0.15V to (V_A +0.15V)
Ground Difference |GND - DR GND|	0V to 100 mV
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Power Dissipation at $T_A \leq 85^\circ C$	TBD W
ESD Susceptibility (Note 4)	
Human Body Model	2500V
Machine Model	250V
Soldering Temperature, Infrared, 10 seconds, (Note 5), (Applies to standard plated package only)	235˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Ambient Temperature Range	$-40^\circ C \leq T_A \leq +85^\circ C$
Supply Voltage (V_A)	+1.8V to +2.0V
Driver Supply Voltage (V_{DR})	+1.8V to V_A
Analog Input Common Mode Voltage	V_{CMO} ±50mV
V_{IN}+, V_{IN}- Voltage Range (Maintaining Common Mode)	200mV to V_A
Ground Difference (|GND - DR GND|)	0V
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	$0.4V_{P-P}$ to $2.0V_{P-P}$

Package Thermal Resistance

Package	θ_{JA}	θ_{JC} (Top of Package)	θ_{J-PAD} (Thermal Pad)
128-Lead Exposed Pad LQFP	26˚C / W	10˚C / W	2.8˚C / W

Converter Electrical Characteristics

NOTE: This product is currently in development and the parameters specified in this section are DESIGN TARGETS. The specifications in this section cannot be guaranteed until device characterization has taken place. The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $870mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Input Clock, f_{CLK} = 1.5 GHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits $T_A = 25^\circ C$, unless otherwise noted. (Notes 6, 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
INL	Integral Non-Linearity (Best fit)	DC Coupled, 1MHz Sine Wave Overanged	±0.35	**±TBD**	LSB (max)
DNL	Differential Non-Linearity	DC Coupled, 1MHz Sine Wave Overanged	±0.25	**±TBD**	LSB (max)
	Resolution with No Missing Codes			**8**	Bits
V_{OFF}	Offset Error		-0.45	**−TBD** **TBD**	LSB (min) LSB (max)
V_{OFF_ADJ}	Input Offset Adjustment Range	Extended Control Mode	±45		mV
PFSE	Positive Full-Scale Error (Note 9)		−0.6	**±TBD**	mV (max)
NFSE	Negative Full-Scale Error (Note 9)		−1.31	**±TBD**	mV (max)
FS_ADJ	Full-Scale Adjustment Range	Extended Control Mode	±20	**±15**	%FS
DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth		TBD		GHz
B.E.R.	Bit Error Rate		10^{-18}		Error/Sample
	Gain Flatness	d.c. to 1500 MHz	±TBD		dBFS
		d.c. to 3 GHz	±TBD		dBFS
ENOB	Effective Number of Bits	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	TBD	**TBD**	Bits (min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	7.0	**TBD**	Bits (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	TBD	**TBD**	Bits (min)

Converter Electrical Characteristics (Continued)

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Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
DYNAMIC CONVERTER CHARACTERISTICS					
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	TBD	**TBD**	dB (min)
		f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB	TBD	**TBD**	dB (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR – 0.5 dB	TBD	**TBD**	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	TBD	**TBD**	dB (min)
		f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB	44.0	**TBD**	dB (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR – 0.5 dB	TBD	**TBD**	dB (min)
THD	Total Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	TBD	**-TBD**	dB (max)
		f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB	TBD	**-TBD**	dB (max)
		f_{IN} = 1498 MHz, V_{IN} = FSR – 0.5 dB	TBD	**-TBD**	dB (max)
2nd Harm	Second Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	TBD		dB
		f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB	TBD		dB
		f_{IN} = 1498 MHz, V_{IN} = FSR – 0.5 dB	TBD		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	TBD		dB
		f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB	TBD		dB
		f_{IN} = 1498 MHz, V_{IN} = FSR – 0.5 dB	TBD		dB
SFDR	Spurious-Free dynamic Range	f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	TBD	**TBD**	dB (min)
		f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB	TBD	**TBD**	dB (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR – 0.5 dB	TBD	**TBD**	dB (min)
IMD	Intermodulation Distortion	f_{IN1} = 321 MHz, V_{IN} = FSR – 7 dB f_{IN2} = 326 MHz, V_{IN} = FSR – 7 dB	TBD		dB
	Out of Range Output Code (In addition to OR Output high)	$(V_{IN}+) - (V_{IN}-) >$ + Full Scale		**255**	
		$(V_{IN}+) - (V_{IN}-) <$ – Full Scale		**0**	
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
V_{IN}	Full Scale Analog Differential Input Range	FSR pin 14 Low	600	**520**	mV_{P-P} (min)
				680	mV_{P-P} (max)
		FSR pin 14 High	800	**720**	mV_{P-P} (min)
				880	mV_{P-P} (max)
V_{CMI}	Analog Input Common Mode Voltage		V_{CMO}	**V_{CMO} – 50** **V_{CMO} + 50**	mV (min) mV (max)
C_{IN}	Analog Input Capacitance, Normal operation (Notes 10, 11)	Differential	0.02		pF
		Each input pin to ground	1.6		pF
	Analog Input Capacitance, DES Mode (Notes 10, 11)	Differential	0.08		pF
		Each input pin to ground	2.2		pF
R_{IN}	Differential Input Resistance		100	**94**	Ω (min)
				106	Ω (max)
ANALOG OUTPUT CHARACTERISTICS					
V_{CMO}	Common Mode Output Voltage		1.26	**0.95** **1.45**	V (min) V (max)
V_{CMO_LVL}	V_{CMO} input threshold to set DC Coupling mode	V_A = 1.8V	0.60		V
		V_A = 2.0V	0.66		V
TC V_{CMO}	Common Mode Output Voltage Temperature Coefficient	T_A = –40˚C to +85˚C	118		ppm/˚C

Converter Electrical Characteristics (Continued)

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Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
ANALOG OUTPUT CHARACTERISTICS					
C_{LOAD} V_{CMO}	Maximum V_{CMO} load Capacitance			80	pF
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA	1.26	**1.20** **1.33**	V (min) V (max)
TC V_{BG}	Bandgap Reference Voltage Temperature Coefficient	T_A = –40˚C to +85˚C, I_{BG} = ±100 µA	28		ppm/˚C
C_{LOAD} V_{BG}	Maximum Bandgap Reference load Capacitance			80	pF
TEMPERATURE DIODE CHARACTERISTICS					
ΔV_{BE}	Temperature Diode Voltage	192 µA vs. 12 µA, T_J = 25˚C	71.23		mV
		192 µA vs. 12 µA, T_J = 85˚C	85.54		mV
CLOCK INPUT CHARACTERISTICS					
V_{ID}	Differential Clock Input Level	Sine Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
		Square Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
I_I	Input Current	V_{IN} = 0 or V_{IN} = V_A	±1		µA
C_{IN}	Input Capacitance (Notes 10, 11)	Differential	0.02		pF
		Each input to ground	1.5		pF
DIGITAL CONTROL PIN CHARACTERISTICS					
V_{IH}	Logic High Input Voltage	(Note 12)		**0.85 x V_A**	V (min)
V_{IL}	Logic Low Input Voltage	(Note 12)		**0.15 x V_A**	V (max)
C_{IN}	Input Capacitance (Notes 11, 13)	Each input to ground	1.2		pF
DIGITAL OUTPUT CHARACTERISTICS					
Z_O	Differential Output Impedance		100		Ohms
V_{OH}	CMOS H level output	I_{OH} = -400uA (Note 12)	1.65	**1.5**	V
V_{OL}	CMOS L level output	I_{OH} = 400uA (Note 12)	0.15	**0.3**	V
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD = Low PD = High	745 10.2	**TBD** **TBD**	mA (max) mA (max) mA
I_{DR}	Output Driver Supply Current	PD = Low PD = High	200 0.012	**TBD** **TBD**	mA (max) mA (max) mA
P_D	Power Consumption	PD = Low PD = High	1.8 20	**TBD** **TBD**	W (max) W (max) mW
PSRR1	D.C. Power Supply Rejection Ratio	Change in Full Scale Error with change in V_A from 1.8V to 2.0V	30		dB
PSRR2	A.C. Power Supply Rejection Ratio	248 MHz, $50mV_{P-P}$ riding on V_A	51		dB

Converter Electrical Characteristics (Continued)

NOTE: This product is currently in development and the parameters specified in this section are DESIGN TARGETS. The specifications in this section cannot be guaranteed until device characterization has taken place. The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $870mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Input Clock, f_{CLK} = 1.5 GHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25˚C, unless otherwise noted. (Notes 6, 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
AC ELECTRICAL CHARACTERISTICS					
f_{CLK1}	Maximum Input Clock Frequency	Sampling rate is 2x clock input	1.7	**1.5**	GHz (min)
f_{CLK2}	Minimum Input Clock Frequency	Sampling rate is 2x clock input	500		MHz
	Input Clock Duty Cycle	500MHz ≤ Input clock frequency ≤ 1.5 GHz (Note 12)	50	20 80	% (min) % (max)
t_{CL}	Input Clock Low Time	(Note 11)	333	**133**	ps (min)
t_{CH}	Input Clock High Time	(Note 11)	333	**133**	ps (min)
t_{RS}	Reset Setup Time	(Note 11)	150		ps
t_{RH}	Reset Hold Time	(Note 11)	250		ps
t_{RPW}	Reset Pulse Width	(Note 11)		**4**	Clock Cycles (min)
t_{LHT}	Differential Low to High Transition Time	10% to 90%, C_L = 2.5 pF	250		ps
t_{HLT}	Differential High to Low Transition Time	10% to 90%, C_L = 2.5 pF	250		ps
t_{AD}	Sampling (Aperture) Delay	Input CLK+ Fall to Acquisition of Data	1.3		ns
t_{AJ}	Aperture Jitter		0.4		ps rms
t_{OD}	Input Clock to Data Output Delay (in addition to Pipeline Delay)	50% of Input Clock transition to 50% of Data transition	3.1		ns
	Pipeline Delay (Latency) (Note 11)	Dd Outputs		**13**	Input Clock Cycles
		Db Outputs		**14**	
		Dc Outputs		**13.5**	
		Da Outputs		**14.5**	
	Over Range Recovery Time	Differential V_{IN} step from ±1.2V to 0V to get accurate conversion	1		Input Clock Cycle
t_{WU}	PD low to Rated Accuracy Conversion (Wake-Up Time)		500		ns
f_{SCLK}	Serial Clock Frequency	(Note 11)	100		MHz
t_{SSU}	Data to Serial Clock Setup Time	(Note 11)	2.5		ns (min)
t_{SH}	Data to Serial Clock Hold Time	(Note 11)	1		ns (min)
	Serial Clock Low Time			**4**	ns (min)
	Serial Clock High Time			**4**	ns (min)
t_{CAL}	Calibration Cycle Time		1.4×10^5		Clock Cycles
t_{CAL_L}	CAL Pin Low Time	See *Figure 3* (Note 11)		80	Clock Cycles (min)
t_{CAL_H}	CAL Pin High Time	See *Figure 3* (Note 11)		80	Clock Cycles (min)
t_{CalDly}	Calibration delay determined by pin 127	See Section 1.1.1, *Figure 3*, (Note 11)		2^{25}	Clock Cycles (min)

Converter Electrical Characteristics (Continued)

NOTE: This product is currently in development and the parameters specified in this section are DESIGN TARGETS. The specifications in this section cannot be guaranteed until device characterization has taken place. The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $870mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Input Clock, f_{CLK} = 1.5 GHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25˚C, unless otherwise noted. (Notes 6, 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
AC ELECTRICAL CHARACTERISTICS					
t_{CalDly}	Calibration delay determined by pin 127	See Section 1.1.1, *Figure 3*, (Note 11)		2^{31}	Clock Cycles (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no guarantee of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

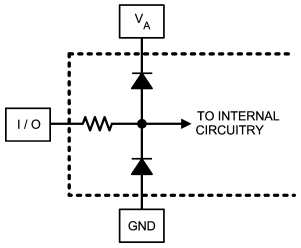
Note 2: All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supply limits (that is, less than GND or greater than V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two. This limit is not placed upon the power, ground and digital output pins.

Note 4: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

Note 5: See AN-450, "Surface Mounting Methods and Their Effect on Product Reliability".

Note 6: The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



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Note 7: To guarantee accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded.

Note 8: Typical figures are at T_A = 25˚C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See *Figure 1*. For relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

Note 10: The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 11: This parameter is guaranteed by design and is not tested in production.

Note 12: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 13: The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 14: Tying V_{BG} to the supply rail will increase the output offset voltage (V_{OS}) by 400mv (typical), as shown in the V_{OS} specification above. Tying V_{BG} to the supply rail will also affect the differential LVDS output voltage (V_{OD}), causing it to increase by 40mV (typical).

Specification Definitions

APERTURE (SAMPLING) DELAY is that time required after the fall of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode the aperture delay time (t_{AD}) after the input clock goes low.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

Bit Error Rate (B.E.R.) is the probability of error and is defined as the probable number of errors per unit of time divided by the number of bits seen in that amount of time. A B.E.R. of 10^{-18} corresponds to a statistical error in one bit about every four (4) years.

CLOCK DUTY CYCLE is the ratio of the time that the clock wave form is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at 3 GSPS with a ramp input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

Specification Definitions (Continued)

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors:

Positive Gain Error = Offset Error – Positive Full-Scale Error

Negative Gain Error = –(Offset Error – Negative Full-Scale Error)

Gain Error = Negative Full-Scale Error – Positive Full-Scale Error = Positive Gain Error + Negative Gain Error

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The best fit method is used.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^n$$

where V_{FS} is the differential full-scale amplitude of 600 mV or 800 mV as set by the FSR input and "n" is the ADC resolution in bits, which is 8 for the ADC08B3000.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the last code transition is from the ideal 1/2 LSB above a differential –435 mV with the FSR pin high, or 1/2 LSB above a differential –325 mV with the FSR pin low. For the ADC08B3000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 127.5.

OUTPUT DELAY (t_{OD}) is the time delay after the falling edge of DRDY before the data update is present at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of input clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential +435 mV with the FSR pin high, or 1-1/2 LSB below a differential +325 mV with the FSR pin low. For the ADC08B3000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. PSRR1 (DC PSRR) is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8V to 2.0V. PSRR2 (AC PSRR) is a measure of how well an a.c. signal riding upon the power supply is rejected from the output and is measured with a 248 MHz, 50 mV_{P-P} signal riding upon the power supply. It is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the input clock frequency, including harmonics but excluding d.c.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$\text{THD} = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

Transfer Characteristic

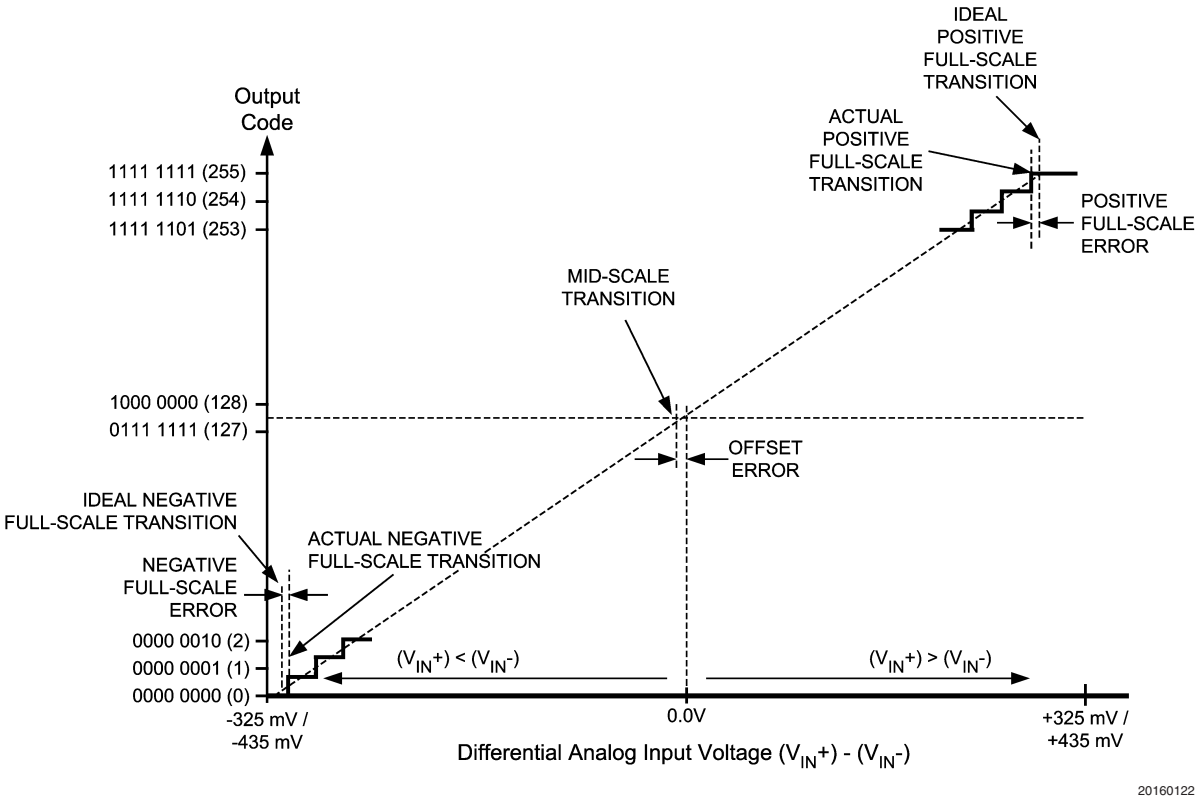


FIGURE 1. Input / Output Transfer Characteristic

Timing Diagrams

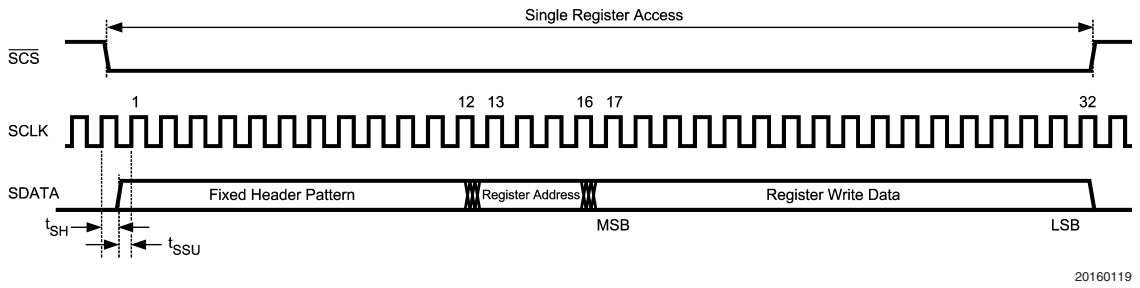


FIGURE 2. Serial Interface Timing

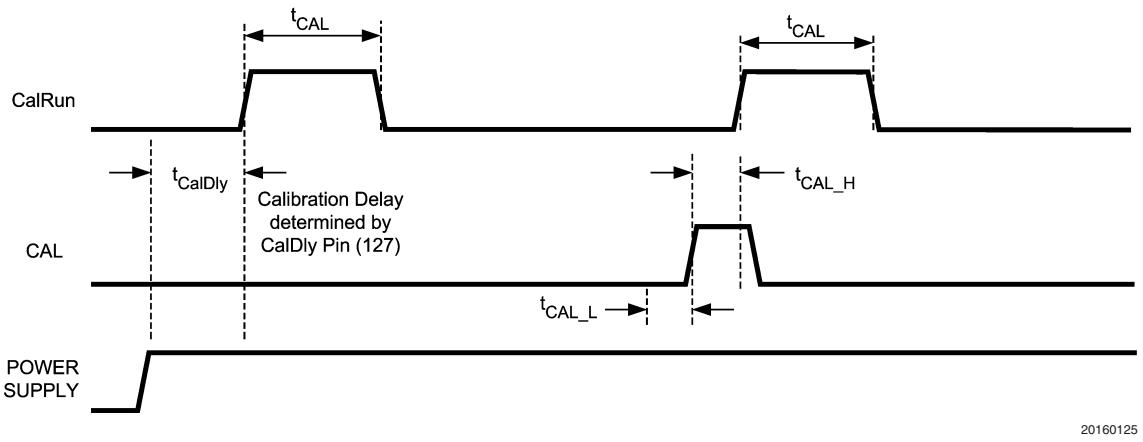


FIGURE 3. Self Calibration and On-Command Calibration Timing

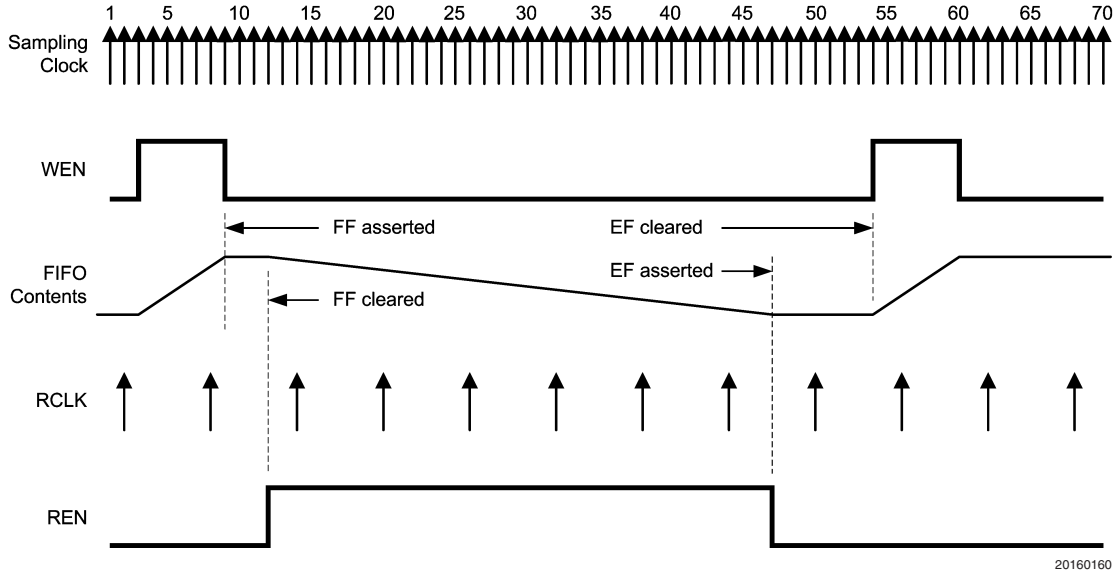


FIGURE 4. Data Capture and Data Offload Operation

Timing Diagrams (Continued)

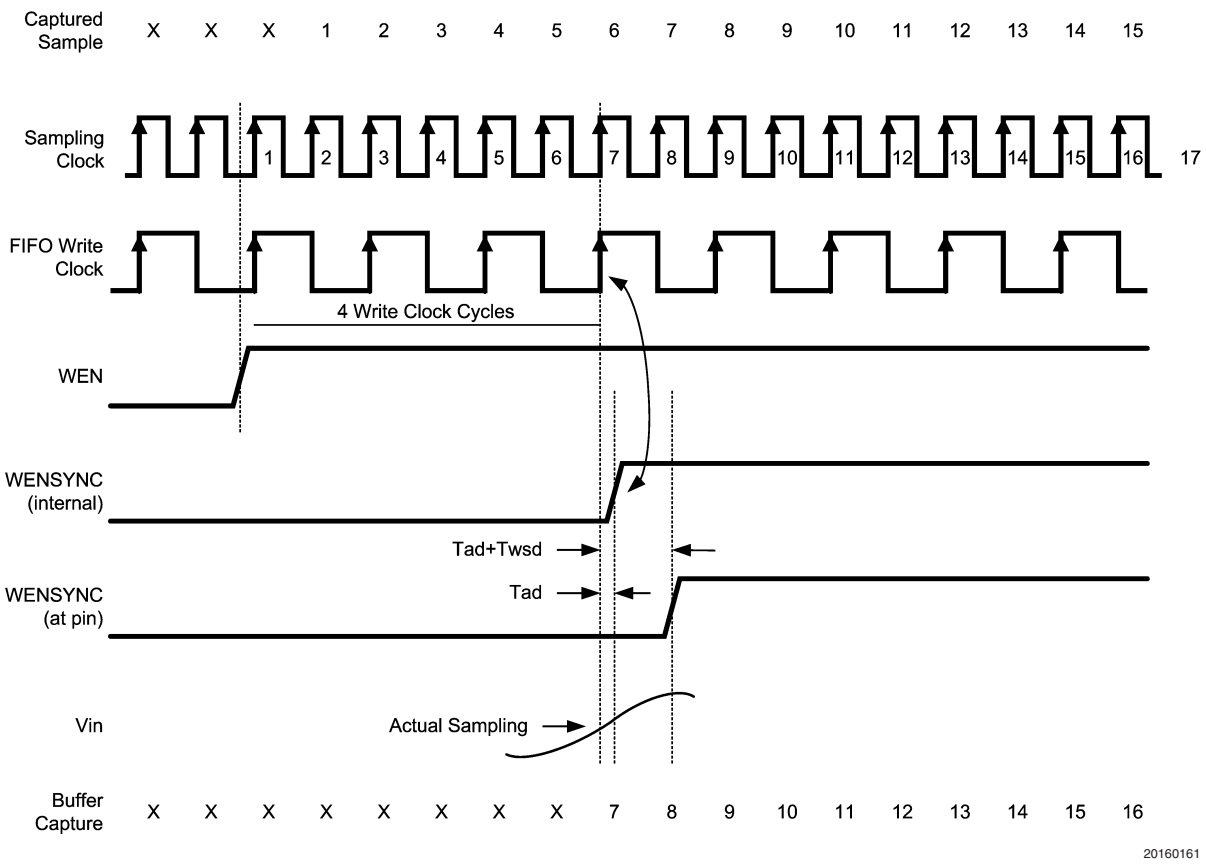


FIGURE 5. Data Capture and Write Enable Timing - 7 Input Clock Cycles

Timing Diagrams (Continued)

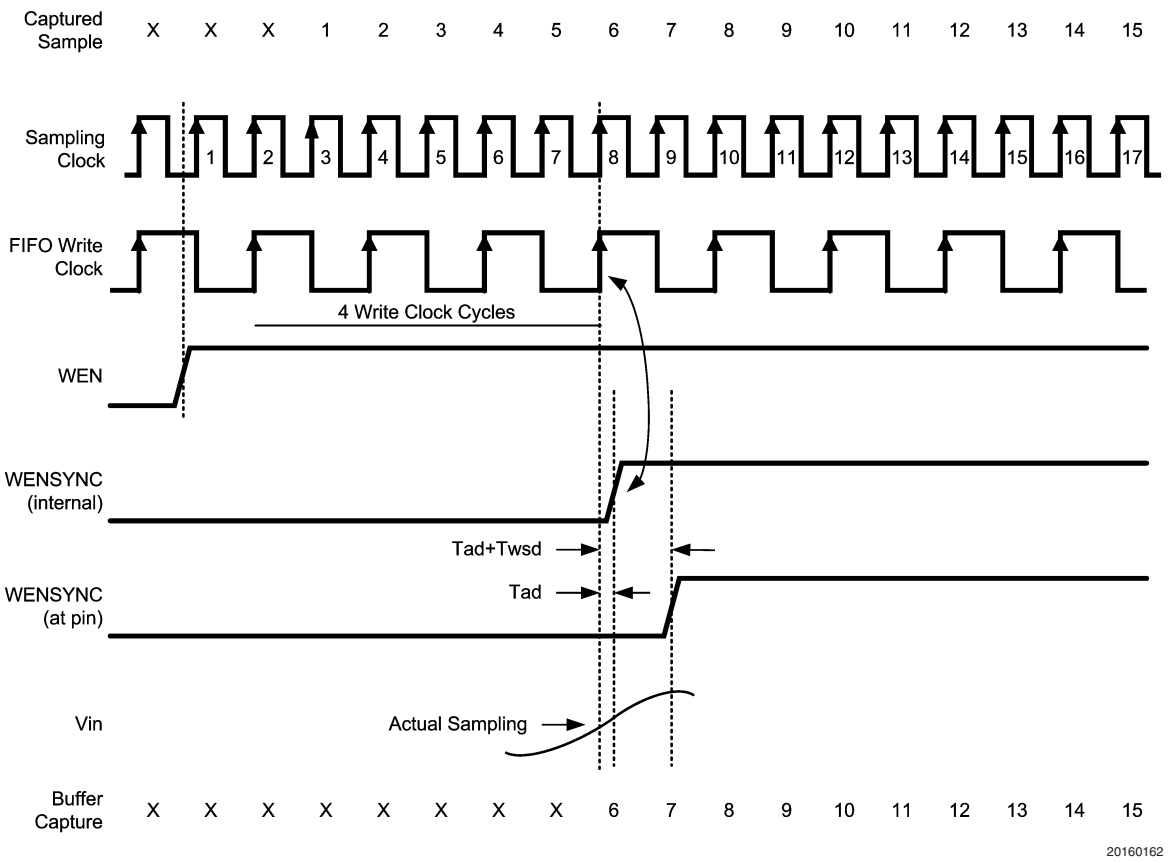


FIGURE 6. Data Capture and Write Enable Timing - 8 Input Clock Cycles

1.0 Functional Description

The ADC08B3000 is a versatile A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section.

While it is generally poor practice to allow an active pin to float, pins 4 and 14 of the ADC08B3000 are designed to be left floating without jeopardy. In all discussions throughout this data sheet, whenever a function is called by allowing a control pin to float, connecting that pin to a potential of one half the V_A supply voltage will have the same effect as allowing it to float.

1.1 OVERVIEW

The ADC08B3000 uses a calibrated folding and interpolating architecture that achieves over TBD effective bits. The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to other things, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal that is within the converter's input voltage range is digitized to eight bits at speeds of 500 MSPS to 3.0 GSPS, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at the analog input will cause the OR (Out of Range) output to be activated. This single OR output indicates when the output code from the converter is below negative full scale or above positive full scale.

1.1.1 Self-Calibration

A self-calibration is performed upon power-up and can also be invoked by the user upon command. Calibration trims the 100Ω analog input differential termination resistor and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR) and ENOB. Internal bias currents are also set with the calibration process. All of this is true whether the calibration is performed upon power up or is performed upon command. Running the self calibration is an important part of this chip's functionality and is required in order to obtain adequate performance. In addition to the requirement to be run at power-up, self calibration must be re-run whenever the sense of the FSR pin is changed. For best performance, we recommend that self calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly relative to the specific system performance requirements. See Section 2.4.2.2 for more information. Calibration can not be initiated or run while the device is in the power-down mode. See Section 1.1.7 for information on the interaction between Power Down and Calibration.

During the calibration process, the input termination resistor is trimmed to a value that is equal to R_{EXT} / 33. This external resistor is located between pin 32 and ground. R_{EXT} must be 3300 Ω ±0.1%. With this value, the input termination resistor is trimmed to be 100 Ω. Because R_{EXT} is also used to set the proper current for the Track and Hold amplifier, for the preamplifiers and for the comparators, other values of R_{EXT} should not be used.

In normal operation, calibration is performed just after application of power and whenever a valid calibration command is given, which is holding the CAL pin low for at least 80 input clock cycles, then hold it high for at least another 80 input clock cycles. The time taken by the calibration procedure is specified in the A.C. Characteristics Table. Holding the CAL pin high upon power up will prevent the calibration process from running until the CAL pin experiences the above-mentioned 80 input clock cycles low followed by 80 cycles high.

CalDly (pin 127) is used to select one of two delay times after the application of power to the start of calibration. This calibration delay is 2^{25} input clock cycles (about 22 ms at 3 GSPS) with CalDly low, or 2^{31} input clock cycles (about 1.4 seconds at 3 GSPS) with CalDly high. These delay values allow the power supply to come up and stabilize before calibration takes place. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

The CalRun output is high whenever the calibration procedure is running. This is true whether the calibration is done at power-up or on-command.

1.1.2 Acquiring the Input

Data is acquired at the falling edge of CLK+ (pin 10) and the digital equivalent of that data is available at the digital outputs 13 input clock cycles later for the Dd and Dc output buses and 14 input clock cycles later for the Db and Da output buses. There is an additional internal delay called t_{OD} before the data is available at the outputs. See the Timing Diagram. The ADC08B3000 will convert as long as the input clock signal is present. The fully differential comparator design and the innovative design of the sample-and-hold amplifier, together with self calibration, enables a very flat SINAD/ENOB response beyond 1.5 GHz. The ADC08B3000 output data signaling is CMOS and the output format is offset binary.

1.1.3 Control Modes

Much of the user control can be accomplished with several control pins that are provided. Examples include initiation of the calibration cycle, power down mode and full scale range setting. However, the ADC08B3000 also provides an Extended Control mode whereby a serial interface is used to access register-based control of several advanced features. The Extended Control mode is not intended to be enabled and disabled dynamically. Rather, the user is expected to employ either the normal control mode or the Extended Control mode at all times. When the device is in the Extended Control mode, pin-based control of several features is replaced with register-based control and those pin-based controls are disabled. These pins are OutEdge/DDR (pin 4), FSR (pin 14) and CalDly (pin 127). See Section 1.2 for details on the Extended Control mode.

1.1.4 The Analog Inputs

The ADC08B3000 must be driven with a differential input signal. Operation with a single-ended signal is not recommended. It is important that the input signals are either a.c. coupled to the inputs with the V_{CMO} pin grounded, or d.c. coupled with the V_{CMO} pin left floating. An input common mode voltage equal to the V_{CMO} output must be provided when d.c. coupling is used.

1.0 Functional Description (Continued)

Two full-scale range settings are provided with pin 14 (FSR). A high on pin 14 causes an input full-scale range setting of 800 mV_{P-P}, while grounding pin 14 causes an input full-scale range setting of 600 mV_{P-P}. The full-scale range setting operates equally on both ADCs.

In the Extended Control mode, the full-scale input range can be set to values between 560 mV_{P-P} and 840 mV_{P-P} through a serial interface. See Section 2.2

1.1.5 Clocking

The ADC08B3000 must be driven with an a.c. coupled, differential clock signal. Section 2.3 describes the use of the clock input pins. To assist the user in offloading captured data from the Capture Buffer, the ADC08B3000 has an RCLK input. RCLK is a free-running clock which can be applied asynchronously to the analog input clock and can operate up to 200MHz. The data output, DRDY signals and EF flag are asserted synchronous to RCLK. See Section 1.7.

1.1.5.1 Dual-Edge Sampling

One ADC samples the input on the positive edge of the input clock and the other ADC samples the same input on the other edge of the input clock. The input is thus sampled twice per input clock cycle, resulting in an overall sample rate of twice the input clock frequency.

The ADC08B3000 uses dual edge sampling to achieve a sampling frequency of 3 GSPS with a 1.5 GHz input clock.

The ADC08B3000 includes an automatic clock phase background calibration feature which automatically and continuously adjusts the phase of the relative rising and falling edge pahses. This feature removes the need to manually adjust the clock phase and provides optimal ENOB performance

1.1.5.2 OutEdge Setting

To help ease data capture in the SDR mode, the output data may be caused to transition on either the positive or the negative edge of the Data Ready (DRDY) Pins. This is chosen with the OutEdge input (pin 4). A high on the OutEdge input pin causes the output data to transition on the rising edge of DRDY, while grounding this input causes the output to transition on the falling edge of DRDY. See Section 2.4.3.

1.1.7 Power Down

The ADC08B3000 is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode. In this power down mode the data output pins (positive and negative) including DRDY and OR +/- are put into a high impedance state and the devices power consumption is reduced to a minimal level.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

1.2 NORMAL/EXTENDED CONTROL

The ADC08B3000 may be operated in one of two modes. In the simpler standard control mode, the user affects available configuration and control of the device through several control pins. The "extended control mode" provides additional configuration and control options through a serial interface and a set of 6 registers. The two control modes are selected with pin 14 (FSR/ECE: Extended Control Enable). The choice of control modes is required to be a fixed selection and is not intended to be switched dynamically while the device is operational.

Table 1 shows how several of the device features are affected by the control mode chosen.

TABLE 1. Features and modes

Feature	Normal Control Mode	Extended Control Mode
RCLK Data transitions with rising or falling RCLK edge	Selected with pin 4	Selected with the OE bit in the Configuration Register
Power-On Calibration Delay	Delay Selected with pin 127	Short delay only.
Full-Scale Range	Options (600 mV_{P-P} or 800 mV_{P-P}) selected with pin 14. Selected range applies to both channels.	Up to 512 step adjustments over a nominal range of 560 mV to 840 mV. Selected using register 3H
Input Offset Adjust	Not possible	±45 mV adjustments in 512 steps using register 2h
Clock Phase Adjustment	Not possible	The clock phase can be adjusted manually through the Coarse & Fine registers (Eh and Dh)
Test Pattern	Not possible	A test pattern can be made present at the data outputs by programming register Fh.

1.0 Functional Description (Continued)

The default state of the Extended Control Mode is set upon power-on reset (internally performed by the device) and is shown in *Table 2*.

TABLE 2. Extended Control Mode Operation (Pin 14 Floating)

Feature	Extended Control Mode Default State
Calibration Delay	Short Delay
Full-Scale Range	700 mV nominal for both channels
Input Offset Adjust	No adjustment for either channel

1.3 THE SERIAL INTERFACE

The 3-pin serial interface is enabled only when the device is in the Extended Control mode. The pins of this interface are Serial Clock (SCLK), Serial Data (SDATA) and Serial Interface Chip Select ($\overline{SCS}$) Eight write only registers are accessible through this serial interface.

$\overline{SCS}$: This signal should be asserted low while accessing a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

SCLK: Serial data input is accepted with the rising edge of this signal.

SDATA: Each register access requires a specific 32-bit pattern at this input. This pattern consists of a header, register address and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed. See the Timing Diagram.

Each Register access consists of 32 bits, as shown in *Figure 2* of the Timing Diagrams. The fixed header pattern is 0000 0000 0001 (eleven zeros followed by a 1). The loading sequence is such that a "0" is loaded first. These 12 bits form the header. The next 4 bits are the address of the register that is to be written to and the last 16 bits are the data written to the addressed register. The addresses of the various registers are indicated in *Table 3*.

Refer to the Register Description (Section 1.4) for information on the data to be written to the registers.

Subsequent register accesses may be performed immediately, starting with the 33rd SCLK. This means that the $\overline{SCS}$ input does not have to be de-asserted and asserted again between register addresses. It is possible, although not recommended, to keep the $\overline{SCS}$ input permanently enabled (at a logic low) when using extended control.

IMPORTANT NOTE: The Serial Interface should not be used when calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Programming the serial registers will also reduce dynamic performance of the ADC for the duration of the register access time.

1.0 Functional Description (Continued)

TABLE 3. Register Addresses

4-Bit Address					
Loading Sequence: A3 loaded after H0, A0 loaded last					
A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0h	Reserved
0	0	0	1	1h	Configuration
0	0	1	0	2h	Offset
0	0	1	1	3h	Full-Scale Voltage Adjust
0	1	0	0	4h	Reserved
0	1	0	1	5h	Reserved
0	1	1	0	6h	Reserved
0	1	1	1	7h	Reserved
1	0	0	0	8h	Reserved
1	0	0	1	9h	Reserved
1	0	1	0	Ah	Reserved
1	0	1	1	Bh	Reserved
1	1	0	0	Ch	Reserved
1	1	0	1	Dh	Extended Clock Phase Adjust Fine
1	1	1	0	Eh	Extended Clock Phase Adjust Coarse
1	1	1	1	Fh	FIFO

1.4 REGISTER DESCRIPTION

Eight write-only registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Normal Control Mode. Each register description below also shows the Power-On Reset (POR) state of each control bit.

Configuration Register

Addr: 1h (0001b) **W only (0xBEFF)**

D15	D14	D13	D12	D11	D10	D9	D8
1	0	1	DCS	DCP	nDE	1	OE

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15 Must be set to 1b

Bit 14 Must be set to 0b

Bit 13 Must be set to 1b

Bit 12 DCS: Duty Cycle Stabilizer. When this bit is set to 1b , a duty cycle stabilzation circuit is applied to the clock input. When this bit is set to 0b the stabilzation circuit is disabled.

POR State: 1b

Bit 11 DCP: DDR Clock Phase. This bit only has an effect in the DDR mode. When this bit is set to 0b, the DRDY edges are time-aligned with the data bus edges (“0˚ Phase”). When this bit is set to 1b, the DRDY edges are placed in the middle of the data bit-cells (“90˚ Phase”).

POR State: 1b

Bit 10 nDE: DDR Enable. When this bit is set to 0b, data bus clocking follows the DDR (Dual Data Rate) mode whereby a data word is output with each rising and falling edge of DRDY. When this bit is set to a 1b, data bus clocking follows the SDR (Single Data Rate) mode whereby each data word is output with either the rising or falling edge of DRDY, as determined by the OutEdge bit.

POR State: 1b

Bit 9 Must be set to 1b

Bit 8 OE: Output Edge. This bit selects the edge of the DRDY pins with which the data words transition in the SDR mode and has the same effect as the OutEdge pin in the normal control mode. When this bit is set to 1b, the data outputs change with the rising edge of the DRDY pins. When this bit is set to 0b, the data outputs change with the falling edge of the DRDY pins.

POR State: 0b

Bits 7:6 Must be set to 1b.

Bits 5:0 Must be set to 1b

1.0 Functional Description (Continued)

Offset Adjust

Addr: 2h (0010b) **W only (0x007F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)			Offset Value				(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8 Offset Value. The input offset of the ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides 0.176 mV of offset.

POR State: 0000 0000 b

Bit 7 Sign bit. 0b gives positive offset, 1b gives negative offset.

POR State: 0b

Bit 6:0 Must be set to 1b

Full-Scale Voltage Adjust

Addr: 3h (0011b) **W only (0x807F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)			Adjust Value				

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15:7 Full Scale Voltage Adjust Value. The input full-scale voltage or gain of the ADC is adjusted linearly and monotonically with a 9 bit data value. The adjustment range is ±20% of the nominal 700 mV_{P-P} differential value.

0000 0000 0 560mV_{P-P}

1000 0000 0 700mV_{P-P}

Default Value

1111 1111 1 840mV_{P-P}

For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.

POR State: 1000 0000 0b (no adjustment)

Bits 6:0 Must be set to 1b

Extended Clock Phase Adjust Fine

Addr: Dh (1101b) **W only (0x3FFF)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)			FAM				

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15:7 Fine Adjust Magnitude. With all bits set, total adjust = 110ps of non-linear clock adjust. The default setting is 000000000b

Bit 6:0 Must be set to 1b

Extended Clock Phase Adjust Coarse

Addr: Eh (1110b) **W only (0x07FF)**

D15	D14	D13	D12	D11	D10	D9	D8
ENA		CAM			1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15 Enable, default is 0b

Bit 14:11 Coarse Adjust Magnitude. Each LSB results in approximately 70ps of clock adjust. The default setting is 0000b

Bits 10:0 Must be set to 1b

FIFO Register

Addr: Fh (1111b) **W only (0xE7FF)**

D15	D14	D13	D12	D11	D10	D9	D8
BZO	BZZ	ASW	O2E	TP	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 14 BZZ: BSIZE0. Bit 14 in combination with BSIZE1 (BIT 15) is used to select the buffer size of the Capture Buffer. The Capture Buffer is size adjustable and it cannot be split between the two CMOS data output ports. See Section 1.6 for a table which relates the Capture Buffer size to BSIZE1 and BSIZE0 programming.

POR State: 1b

Bit 13 ASW: Auto-Stop Write. When ASW is logic 1, the Capture Buffer writes will stop automatically when the Capture Buffer is full of captured data and the FF flag is asserted. If this bit is logic 0, the device will continuously write data to the Capture Buffer while overwriting previously captured data.

POR State: 1b

1.0 Functional Description (Continued)

Bit 12 O2E: 02X8 Output Enable. When this bit is a logic 1, data stored in the Capture Buffer will appear on two 8 bit output ports. When this bit is asserted logic 0, data will only appear on the D1 8 bit output port.

POR State: 0b

Bit 11 TP: Test Pattern Output Enable. When this bit is set 1b, the ADC is disengaged and a test pattern generator is connected to the outputs including OR. This test pattern will work with the device in the SDR and DDR modes.

POR State: 0b

Bits10:0 Must be set to 1b

1.4.1 Note Regarding Extended Mode Offset Correction

When using the Offset Adjust registers, the following information should be noted.

For offset values of +0000 0000 and -0000 0000, the actual offset is not the same. By changing only the sign bit in this case, an offset step in the digital output code of about 1/10th of an LSB is experienced. This is shown more clearly in the Figure below.

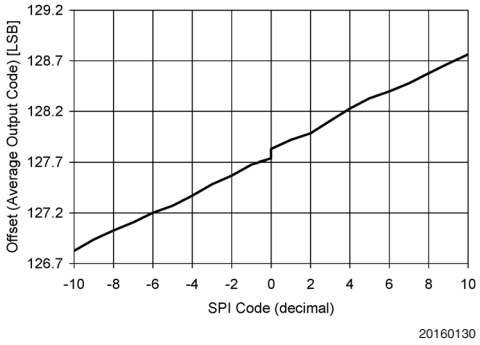


FIGURE 7. Extended Mode Offset Behaviour

1.5 ADC Test Pattern

To aid in system debug, the ADC08B3000 has the capability of providing a test pattern at the 2 outputs completely independent of the input signal. By default, the test pattern will only appear on the D1 port. To have the test pattern appear on both D1 and D2 ports, bit 12 in the FIFO Register must be programmed to 1b. Refer to section 1.4. To engage the test pattern, bit 11 must be programmed to 1b in the FIFO Register. When the test pattern is enabled, the ADC is disengaged and a test pattern generator is connected to the output ports including OR. OR is asserted high at the start of the test pattern output and will remain high until the data is read out of the Capture Buffer and the Emtpy Flag (EF) is asserted high. Each port can output a unique pattern sequences as described in table *Table 4* and *Table 5*. The test pattern appears on the output port with the transition of DRDY.

1.0 Functional Description (Continued)

TABLE 4. Test Pattern Output By Port in 1x8 SDR Mode

Mode	Time	Port D1	Port D2	OR	Comments
1X8	T0	01h		1	Pattern Sequence n
	T1	02h		1	
	T2	03h		1	
	73	04h		1	
	T4	FEh		1	
	T5	FDh		1	
	T6	FCh		1	
	T7	FBh		1	
	T8	01h		1	
	T9	02h		1	
	T10	03h		1	
	T11	04h		1	
	T12	FEh		1	
	T13	FDh		1	
	T14	FCh		1	
	T15	FBh		1	
	T16	01h		1	
	T17	02h		1	
	T18	03h		1	
	T19	04h		1	
	T20	01h		1	Pattern Sequence n+1
	T21	02h		1	
	T22	03h		1	
	T23	04h		1	
	T24	FEh		1	
	T25	FDh		1	
	T26	FCh		1	
	T27	FBh		1	
	T28	01h		1	
	T29	02h		1	
	T30	...		...	

TABLE 5. Test Pattern Output By Port in 2x8 SDR Mode

Mode	Time	Port D1	Port D2	OR	Comments
2X8	T0	02h	01h	1	Pattern Sequence n
	T1	04h	03h	1	
	T2	FDh	FEh	1	
	T3	FBh	FCh	1	
	T4	02h	01h	1	
	T5	04h	03h	1	
	T6	FDh	FEh	1	
	T7	FBh	FCh	1	
	T8	02h	01h	1	
	T9	04h	03h	1	

1.0 Functional Description (Continued)

TABLE 5. Test Pattern Output By Port in 2x8 SDR Mode (Continued)

Mode	Time	Port D1	Port D2	OR	Comments
	T10	02h	01h	1	Pattern Sequence
	T11	04h	03h	1	n+1
	T12	FDh	FEh	1	
	T13	FBh	FCh	1	
	T14	02h	01h	1	
	T15	...	...	...	

1.6 Capture Buffer Functional Description

With the integration of the Capture Buffer, the ADC08B3000 allows sampling and processing tasks to be decoupled. The intent is that the input signal can be sampled at a high rate and collected samples can be offloaded for digital processing at a slower rate. There are 5 main signals which are used to coordinate the handshaking between the Capture Buffer data capture operation and the Capture Buffer data offload operation. These five signals are WEN, REN, EF, FF and RESET. It is important to note that the Capture Buffer implemented on this product is not a general purpose Capture Buffer. The Capture Buffer size is programmable in the Extended Control Mode using bit 15 and bit 14 in the FIFO Register. See *Table 6*. In order for a Capture Buffer read to commence, the entire buffer has to be filled. It is not possible to write to and read from the Capture Buffer simultaneously.

TABLE 6. Programmable Capture Buffer Size

BSIZE1	BSIZE0	Buffer Size (Bytes)
0	0	512
0	1	1024
1	0	2048
1	1	4096

1.6.1 Error Flags

The ADC08B3000 provides two output control signals, Full Flag (FF) and Empty Flag (EF) to aid in data capture and offload operations. An Empty Flag (EF) will be asserted by the device to indicate that the last data was read and the Capture Buffer is now empty. Only when Empty Flag (EF) is asserted high can a Capture Buffer data capture operation begin. The assertion of WEN clears the Empty Flag (EF). The data can only be read from the Capture Buffer when the FF (Full Flag) is asserted high by the device indicating that the Capture Buffer is full. Once the FF is asserted high, the data is ready to be read from the Capture Buffer on the rising edge of RCLK. The RESET signal clears Full Flag (FF) and sets Empty Flag (EF) and clears both the data capture and data offload operations.

1.6.2 Writing to the Capture Buffer

An internally generated write clock is used to write the converted data into the Capture Buffer. The write clock is the same speed as the ADC Sampling Clock. Unless the chip is in a power-down state, the ADC is always converting the input signal. The data is stored in the Capture Buffer only when the Write Enable (WEN) signal is asserted. After the assertion of the Full Flag (FF), the Capture Buffer will start writing over the oldest data because the Write Pointer will wrap-around. The user has the option to stop the writing of the Capture Buffer automatically upon full condition with the use of the ASW (Auto-Stop Write) input. This is programmed by setting bit 13 to 1b in the FIFO register in the Extended Control Mode. Refer to Section 1.4. An Empty Flag (EF) will be asserted by the device to indicate that the last data was read out of the Capture and the Capture Buffer is now empty. Only at this point can another data capture sequence can begin with the assertion of WEN. The assertion and internal synchronization of WEN clears the Empty Flag (EF).

1.6.3 Reading from the Capture Buffer

Once the Full Flag (FF) is asserted high, the data is ready to be read from the Capture Buffer on the rising edge of RCLK. RCLK is an externally applied free-running clock which can be asynchronous to the ADC input clock. To read the data out of the Capture Buffer, the Read Enable (REN) signal must be asserted. The Full Flag (FF) is cleared with the assertion and internal synchronizing of REN. An Empty Flag (EF) will be asserted by the device to indicate that the last data was read and the Capture Buffer is now empty.

1.6.4 Coordinating Read Enable (REN) and Write Enable (WEN)

It is not possible to write to and read from the Capture Buffer simultaneously. This means that the Write Enable (WEN) and the Read Enable (REN) signals should not be asserted simultaneously. If the Read Enable (REN) and Write Enable (WEN) signals are asserted at the same time, the Write Enable (WEN) signal supercedes and the Read Enable (REN) signal is ignored. This is true even if the Read Enable (REN) signal is asserted first and the data offload operation is progressing normally. If the Write Enable (WEN) signal is asserted while Read Enable (REN) is asserted, the Capture Buffer will freeze its operation until a RESET is applied. Recall that RESET allows the Capture Buffer pointers to be reset so a new data capture operation can begin.

1.6.5 Capture Buffer Reset

The RESET signal clears FF and sets EF and clears both the data capture and data offload operations. The RESET signal can be useful during a partial read scenario where the data offload operation stops early and the EF is not asserted by the device. In this case the RESET signal allows the FIFO pointers to be reset so a new data capture operation can begin. The RESET signal has no effect on the ADC operation which has its own internal Power-On Reset circuit.

1.6.6 Data Ready and Write Enable Sync

The ADC08B3000 has three other signals available to coordinate the Capture Buffer data capture and data offload operations. These signals are Data Ready Port 1 (DRDY1), Date Ready Port 2 (DRDY2), and Write Enable Sync (WENSYNC). Data Ready Port 1 (DRDY1) and Data Ready Port 2 (DRDY2) can be used as a latching clock for an external

1.0 Functional Description (Continued)

system. There are applications where using RCLK alone to capture the data on the data output ports D1 and D2 is not a possibility. In which case, Data Ready Port 1 (DRDY1) and Data Ready Port 2 (DRDY2) can be used. The Data Ready (DRDY) pins offer improved data capture capability by eliminating the impact of the RCLK trace delay and the internal RCLK-to-DataOut delay. Data Ready (DRDY) is presented on the output ports at the same time as the data output. In many applications, the user will be providing RCLK which can operate up to 200MHz. RCLK is used by the device to produce the data and DRDY signals on the output ports. During the data offload operation, the REN signal is asserted. After three rising clock edges of RCLK, the data and the DRDY signals appear on the output ports.

Write Enable Sync (WENSYNC) is another signal used for handshaking between the ADC and an external system. Write Enable Sync (WENSYNC) is a synchronized version of Write Enable (WEN) and is synchronized with the ADC sampling clock. Write Enable Sync (WENSYNC) is provided as an output because Write Enable (WEN) can be asserted completely asynchronous to the ADC sampling clock, therefore it would be difficult for the user to know exactly on which data sample the data capture operation actually began. Write Enable Sync (WENSYNC) allows the user to determine when the actual data capture began and on which sample.

1.6.7 Over Range

Over Range (OR) is a signal used to determine if the input signal has over ranged at any time during a data capture operation. It is asserted if an over ranged condition occurred during the data capture operation and is cleared only after the Capture Buffer data offload operation is complete and the Empty Flag (EF) is asserted.

2.0 Applications Information

2.1 THE REFERENCE VOLTAGE

The voltage reference for the ADC08B3000 is derived from a 1.254V bandgap reference, a buffered version of which is made available at pin 31, V_{BG} for user convenience and has an output current capability of ±100 µA. This reference voltage should be buffered if more current is required.

The internal bandgap-derived reference voltage has a nominal value of 600 mV or 800 mV, as determined by the FSR pin and described in Section 1.1.4.

There is no provision for the use of an external reference voltage, but the full-scale input voltage can be adjusted through a Configuration Register in the Extended Control mode, as explained in Section 1.2.

Differential input signals up to the chosen full-scale level will be digitized to 8 bits. Signal excursions beyond the full-scale range will be clipped at the output.

2.2 THE ANALOG INPUT

The analog input is a differential one to which the signal source may be a.c. coupled or d.c. coupled. The full-scale input range is selected with the FSR pin to be 600 mV_{P-P} or 800 mV_{P-P}, or can be adjusted to values between 560 mV_{P-P} and 840 mV_{P-P} in the Extended Control mode through the Serial Interface. For best performance, it is recommended that the full-scale range be kept between 595 mV_{P-P} and 805 mV_{P-P} in the Extended Control mode.

Table 7 gives the input to output relationship with the FSR pin high and the normal (non-extended) mode is used. With the FSR pin grounded, the millivolt values in *Table 7* are reduced to 75% of the values indicated. In the Enhanced Control Mode, these values will be determined by the full scale range and offset settings in the Control Registers.

TABLE 7. DIFFERENTIAL INPUT TO OUTPUT RELATIONSHIP (Non-Extended Control Mode, FSR High)

V_{IN}+	V_{IN}−	Output Code
V_{CM} − 217.5mV	V_{CM} + 217.5mV	0000 0000
V_{CM} − 109 mV	V_{CM} + 109 mV	0100 0000
V_{CM}	V_{CM}	0111 1111 / 1000 0000
V_{CM} + 109 mV	V_{CM} −109 mV	1100 0000
V_{CM} + 217.5mV	V_{CM} − 217.5mV	1111 1111

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

Note that a precise d.c. common mode voltage must be present at the ADC inputs. This common mode voltage, V_{CMO}, is provided on-chip when a.c. input coupling is used and the input signal is a.c. coupled to the ADC.

When the inputs are a.c. coupled, the V_{CMO} output *must* be grounded, as shown in *Figure 8*. This causes the on-chip V_{CMO} voltage to be connected to the inputs through on-chip 50k-Ohm resistors.

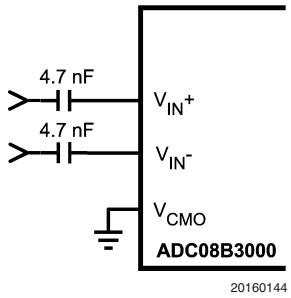


FIGURE 8. Differential Input Drive

When the d.c. coupled mode is used, a common mode voltage must be provided at the differential inputs. This common mode voltage should track the V_{CMO} output pin. Note that the V_{CMO} output potential will change with temperature. The common mode output of the driving device should track this change.

Full-scale distortion performance falls off rapidly as the input common mode voltage deviates from V_{CMO}. This is a direct result of using a very low supply voltage to minimize power. Keep the input common voltage within 50 mV of V_{CMO}.

Performance is as good in the d.c. coupled mode as it is in the a.c. coupled mode, provided the input common mode voltage at both analog inputs remain within 50 mV of V_{CMO}.

2.0 Applications Information

(Continued)

If d.c. coupling is used, it is best to servo the input common mode voltage, using the V_{CMO} pin, to maintain optimum performance. An example of this type of circuit is shown in *Figure 9*.

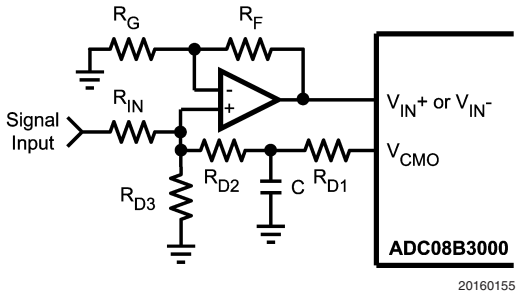


FIGURE 9. Example of Serving the Analog Input with V_{CMO}

One such circuit should be used in front of the V_{IN}+ input and another in front of the V_{IN}– input. In that figure, R_{D1}, R_{D2} and R_{D3} are used to divide the V_{CMO} potential so that, after being gained up by the amplifier, the input common mode voltage is equal to V_{CMO} from the ADC. R_{D1} and R_{D2} are split to allow the bypass capacitor to isolate the input signal from V_{CMO}. R_{IN}, R_{D2} and R_{D3} will divide the input signal, if necessary. Capacitor "C" in *Figure 9* should be chosen to keep any component of the input signal from affecting V_{CMO}.

Be sure that the current drawn from the V_{CMO} output does not exceed 100 µA.

The Input impedance in the d.c. coupled mode (V_{CMO} pin not grounded) consists of a precision 100Ω resistor between V_{IN}+ and V_{IN}– and a capacitance from each of these inputs to ground. In the a.c. coupled mode the input appears the same except there is also a resistor of 50K between each analog input pin and the V_{CMO} potential.

Driving the inputs beyond full scale will result in a saturation or clipping of the reconstructed output.

2.2.1 Handling Single-Ended Input Signals

There is no provision for the ADC08B3000 to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-connected transformer, as shown in *Figure 10*.

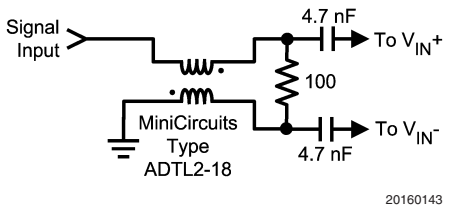


FIGURE 10. Single-Ended to Differential signal conversion with a balun-connected transformer

The 100 Ohm external resistor placed accross the output terminals of the balun in parallel with the ADC08B3000's on-chip 100 Ohm resistor makes a 50 Ohms differential impedance at the balun output. Or, 25 Ohms to virtual ground at each of the balun output terminals.

Looking into the balun, the source sees the impedance of the first coil in series with the impedance at the output of that coil. Since the transformer has a 1:1 turns ratio, the impedance across the first coil is exactly the same as that at the output of the second coil, namely 25 Ohms to virtual ground. So, the 25 Ohms across the first coil in series with the 25 Ohms at its output gives 50 Ohms total impedance to match the source.

2.2.2 Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the ADC08B3000 is derived from an internal bandgap reference. The FSR pin controls the effective reference voltage of the ADC08B3000 such that the differential full-scale input range at the analog inputs is 800 mV_{P-P} with the FSR pin high, or is 600 mV_{P-P} with FSR pin low. Best SNR is obtained with FSR high, but better distortion and SFDR are obtained with the FSR pin low.

2.3 THE CLOCK INPUTS

The ADC08B3000 has differential LVDS clock inputs, CLK+ and CLK-, which must be driven with an a.c. coupled, differential clock signal. Although the ADC08B3000 is tested and its performance is guaranteed with a differential 1.5 GHz clock, it typically will function well with input clock frequencies indicated in the Electrical Characteristics Table. The clock inputs are internally terminated and biased. The input clock signal must be capacitively coupled to the clock pins as indicated in *Figure 11*.

Operation up to the sample rates indicated in the Electrical Characteristics Table is typically possible if the maximum ambient temperatures indicated are not exceeded. Operating at higher sample rates than indicated for the given ambient temperature may result in reduced device reliability and product lifetime. This is because of the higher power consumption and die temperatures at high sample rates. Important also for reliability is proper thermal management . See Section 2.6.2.

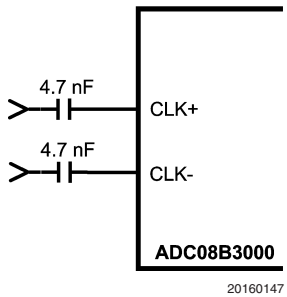


FIGURE 11. Differential (LVDS) Input Clock Connection

The differential input clock line pair should have a characteristic impedance of 100Ω and (when using a balun), be terminated at the clock source in that (100Ω) characteristic impedance. The input clock line should be as short and as direct as possible. The ADC08B3000 clock input is internally terminated with an untrimmed 100Ω resistor.

Insufficient input clock levels will result in poor dynamic performance. Excessively high input clock levels could

2.0 Applications Information

(Continued)

cause a change in the analog input offset voltage. To avoid these problems, keep the input clock level within the range specified in the Electrical Characteristics Table.

The low and high times of the input clock signal can affect the performance of any A/D Converter. The ADC08B3000 features a duty cycle clock correction circuit which can maintain performance over temperature. The ADC will meet its performance specification if the input clock high and low times are maintained within the range (20/80% ratio) as specified in the Electrical Characteristics Table.

High speed, high performance ADCs such as the ADC08B3000 require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{IN(P-P)}/V_{INFSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN}))$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{INFSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, to the ADC analog input.

Note that the maximum jitter described above is the arithmetic sum of the jitter from all sources, including that in the ADC input clock, that added by the system to the ADC input clock and input signals and that added by the ADC itself. Since the effective jitter added by the ADC is beyond user control, the best the user can do is to keep the sum of the externally added input clock jitter and the jitter added by the analog circuitry to the analog signal to a minimum.

Input clock amplitudes above those specified in the Electrical Characteristics Table may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 127/128 when both input pins are at the same potential.

2.4 CONTROL PINS

Six control pins (without the use of the serial interface) provide a wide range of possibilities in the operation of the ADC08B3000 and facilitate its use. These control pins provide Full-Scale Input Range setting, Self Calibration, Calibration Delay, Output Edge Synchronization choice, and a Power Down feature.

2.4.1 Full-Scale Input Range Setting

The input full-scale range can be selected to be either 600 mV_{P-P} or 800 mV_{P-P}, as selected with the FSR control input (pin 14) in the Normal Mode of operation. In the Extended Control Mode, the input full-scale range may be set to be anywhere from 560 mV_{P-P} to 840 mV_{P-P}. See Section 2.2 for more information.

2.4.2 Self Calibration

The ADC08B3000 self-calibration must be run to achieve specified performance. The calibration procedure is run upon power-up and can be run any time on command. The calibration procedure is exactly the same whether there is an input clock present upon power up or if the clock begins some time after application of power. The CalRun output indicator is high while a calibration is in progress.

2.4.2.1 Power-On Calibration

Power-on calibration begins after a time delay following the application of power. This time delay is determined by the setting of CalDly, as described in the Calibration Delay Section, below.

The calibration process will be not be performed if the CAL pin is high at power up. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The ADC08B3000 will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired. A manual calibration, however, may be performed after powering up with the CAL pin high. See On-Command Calibration Section 2.4.2.2.

The internal power-on calibration circuitry comes up in an unknown logic state. If the input clock is not running at power up and the power on calibration circuitry is active, it will hold the analog circuitry in power down and the power consumption will typically be less than 200 mW. The power consumption will be normal after the clock starts.

2.4.2.2 On-Command Calibration

To initiate an on-command calibration, bring the CAL pin high for a minimum of 80 input clock cycles after it has been low for a minimum of 80 input clock cycles. Holding the CAL pin high upon power up will prevent execution of power-on calibration until the CAL pin is low for a minimum of 80 input clock cycles, then brought high for a minimum of another 80 input clock cycles. The calibration cycle will begin 80 input clock cycles after the CAL pin is thus brought high. The CalRun signal should be monitored to determine when the calibration cycle has completed.

The minimum 80 input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned in section 1.1 for best performance, a self calibration should be performed 20 seconds or more after power up and repeated when the operating temperature changes significantly relative to the specific system design performance requirements. ENOB changes slightly with increasing junction temperature and can be easily corrected by performing an on-command calibration.

2.4.2.3 Calibration Delay

The CalDly input (pin 127) is used to select one of two delay times after the application of power to the start of calibration, as described in Section 1.1.1. The calibration delay values allow the power supply to come up and stabilize before calibration takes place. With no delay or insufficient delay, calibration would begin before the power supply is stabilized at its operating value and result in non-optimal calibration coefficients. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

Note that the calibration delay selection is not possible in the Extended Control mode and the short delay time is used.

2.4.3 Output Edge Synchronization

OutEdge is a pin available to help latch the converter output data into external circuitry. This pin may make data capture easier, especially when output clock and data trace lengths are not matched. This pin allows the user to shift the phase of the Data Ready pins (DRDY1 and DRDY2) with respect to the data outputs.

2.0 Applications Information

(Continued)

2.4.4 Power Down Feature

The Power Down pin (PD) allow the ADC08B3000 to be entirely powered down (PD). See Section 1.1.7 for details on the power down feature.

The digital data output pins are put into a high impedance state when the PD pin for the respective channel is high. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

2.5 THE DIGITAL OUTPUTS

The output format is CMOS and Offset Binary. Accordingly, a full-scale input level with V_{IN}+ positive with respect to V_{IN}– will produce an output code of all ones, a full-scale input level with V_{IN}– positive with respect to V_{IN}+ will produce an output code of all zeros and when V_{IN}+ and V_{IN}– are equal, the output code will vary between codes 127 and 128.

2.6 POWER CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 µF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins. A 0.1 µF capacitor should be placed as close as possible to each V_A pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance.

The V_A and V_{DR} supply pins should be isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A ferrite choke, such as the JW Miller FB20009-3B, is recommended between these supply lines when a common source is used for them.

As is the case with all high speed converters, the ADC08B3000 should be assumed to have little power supply noise rejection. Any power supply used for digital circuitry in a system where a lot of digital power is being consumed should not be used to supply power to the ADC08B3000. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

2.6.1 Supply Voltage

The ADC08B3000 is specified to operate with a supply voltage of 1.9V ±0.1V. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08B3000 power pins.

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the ADC08B3000. The circuit of *Figure 12* will provide supply overshoot protection.

Many linear regulators will produce output spiking at power-on unless there is a minimum load provided. Active devices draw very little current until their supply voltages reach a few hundred millivolts. The result can be a turn-on spike that can destroy the ADC08B3000, unless a minimum load is provided for the supply. The 100Ω resistor at the regulator output provides a minimum output current during power-up to ensure there is no turn-on spiking.

In the circuit of *Figure 12*, an LM317 linear regulator is satisfactory if its input supply voltage is 4V to 5V . If a 3.3V supply is used, an LM1086 linear regulator is recommended.

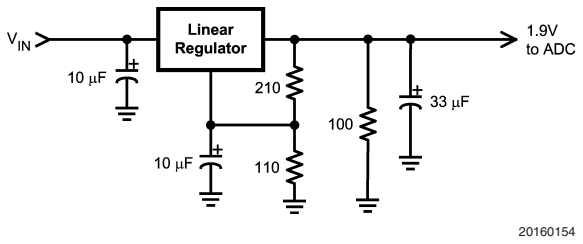


FIGURE 12. Non-Spiking Power Supply

The output drivers should have a supply voltage, V_{DR}, that is within the range specified in the Operating Ratings table. This voltage should not exceed the V_A supply voltage.

If the power is applied to the device without an input clock signal present, the current drawn by the device might be below 200 mA. This is because the ADC08B3000 gets reset through clocked logic and its initial state is unknown. If the reset logic comes up in the "on" state, it will cause most of the analog circuitry to be powered down, resulting in less than 100 mA of current draw. This current is greater than the power down current because not all of the ADC is powered down. The device current will be normal after the input clock is established.

2.6.2 Thermal Management

The ADC08B3000 is capable of impressive speeds and performance at very low power levels for its speed. However, the power consumption is still high enough to require attention to thermal management. For reliability reasons, the die temperature should be kept to a maximum of 130˚C. That is, T_A (ambient temperature) plus ADC power consumption times θ_{JA} (junction to ambient thermal resistance) should not exceed 130˚C. This is not a problem if the ambient temperature is kept to a maximum of +85˚C as specified in the Operating Ratings section.

Please note that the following are general recommendations for mounting exposed pad devices onto a PCB. This should be considered the starting point in PCB and assembly process development. It is recommended that the process be developed based upon past experience in package mounting.

The package of the ADC08B3000 has an exposed pad on its back that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. The land pattern design for lead attachment to the PCB should be the same as for a conventional LQFP, but the exposed pad must be attached to the board to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

2.0 Applications Information

(Continued)

To maximize the removal of heat from the package, a thermal land pattern must be incorporated on the PC board within the footprint of the package. The exposed pad of the device must be soldered down to ensure adequate heat conduction out of the package. The land pattern for this exposed pad should be at least as large as the 5 x 5 mm of the exposed pad of the package and be located such that the exposed pad of the device is entirely over that thermal land pattern. This thermal land pattern should be electrically connected to ground. A clearance of at least 0.5 mm should separate this land pattern from the mounting pads for the package pins.

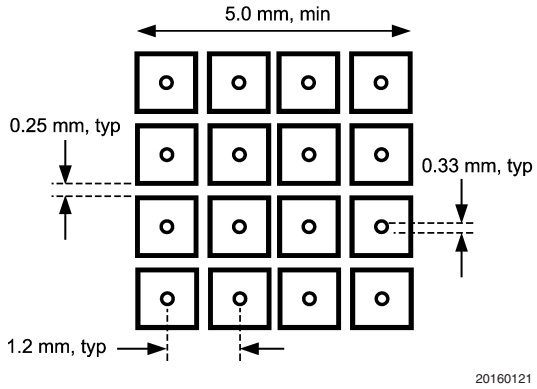


FIGURE 13. Recommended Package Land Pattern

Since a large aperture opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the land pattern of *Figure 13*.

To minimize junction temperature, it is recommended that a simple heat sink be built into the PCB. This is done by including a copper area of about 2 square inches (6.5 square cm) on the opposite side of the PCB. This copper area may be plated or solder coated to prevent corrosion, but should not have a conformal coating, which could provide some thermal insulation. Thermal vias should be used to connect these top and bottom copper areas. These thermal vias act as "heat pipes" to carry the thermal energy from the device side of the board to the opposite side of the board where it can be more effectively dissipated. The use of 9 to 16 thermal vias is recommended.

The thermal vias should be placed on a 1.2 mm grid spacing and have a diameter of 0.30 to 0.33 mm. These vias should be barrel plated to avoid solder wicking into the vias during the soldering process as this wicking could cause voids in the solder between the package exposed pad and the thermal land on the PCB. Such voids could increase the thermal resistance between the device and the thermal land on the board, which would cause the device to run hotter.

If it is desired to monitor die temperature, a temperature sensor may be mounted on the heat sink area of the board near the thermal vias. .Allow for a thermal gradient between the temperature sensor and the ADC08B3000 die of $\theta_{J\text{-}PAD}$ times typical power consumption = 2.8 x 1.9 = 5.3˚C. Allowing for 6.3˚C, including some margin for temperature drop from the pad to the temperature sensor, then, would mean that maintaining a maximum pad temperature reading of 123.7˚C will ensure that the die temperature does not exceed 130˚C, assuming that the exposed pad of the ADC08B3000 is properly soldered down and the thermal vias are adequate. (The inaccuracy of the temperature sensor is addtional to the above calculation).

2.7 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A single ground plane should be used, instead of splitting the ground plane into analog and digital areas.

Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near any linear component or power supply trace or plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC, causing excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90˚ to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines should be isolated from ALL other lines, analog AND digital. The generally accepted 90˚ crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the ADC08B3000. Any external component (e.g., a filter capacitor) connected between the converter’s input and ground should be connected to a very clean point in the analog ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

2.8 DYNAMIC PERFORMANCE

The ADC08B3000 is a.c. tested and its dynamic performance is guaranteed. To meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in Section 2.3.

It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the input clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

Best dynamic performance is obtained when the exposed pad at the back of the package has a good connection to ground. This is because this path from the die to ground is a lower impedance than offered by the package pins.

2.0 Applications Information

(Continued)

2.9 USING THE SERIAL INTERFACE

The ADC08B3000 may be operated in the non-extended control (non-Serial Interface) mode or in the extended control mode. *Table 8* and *Table 9* describe the functions of pins 3, 4, 14 and 127 in the non-extended control mode and the extended control mode, respectively.

2.9.1 Non-Extended Control Mode Operation

Non-extended control mode operation means that the Serial Interface is not active and all controllable functions are controlled with various pin settings. That is, the full-scale range, single-ended or differential input and input coupling (a.c. or d.c.) are all controlled with pin settings. The non-extended control mode is used by setting pin 14 high or low, as opposed to letting it float. *Table 8* indicates the pin functions of the ADC08B3000 in the non-extended control mode.

TABLE 8. Non-Extended Control Mode Operation (Pin 14 High or Low)

Pin	Low	High	Floating
3	0.50 V_{P-P} Output	0.70 V_{P-P} Output	n/a
4	OutEdge = Neg	OutEdge = Pos	DDR
14	600 mV_{P-P} input range	800 mV_{P-P} input range	Extended Control Mode

Pin 3 can be either high or low in the non-extended control mode. Pin 14 must not be left floating to select this mode. See Section 1.2 for more information.

Pin 4 can be high or low or can be left floating in the non-extended control mode. In the non-extended control mode, pin 4 high or low defines the edge at which the output data transitions. See Section 2.4.3 for more information. If this pin is floating, the output clock (DRDY) is a DDR (Double Data Rate) clock (see Section 1.1.5.3) and the output edge synchronization is irrelevant since data is clocked out on both DRDY edges.

Pin 127, if it is high or low in the non-extended control mode, sets the calibration delay. If pin 127 is floating, the calibration delay is the same as it would be with this pin low and the converter performs dual edge sampling (DES).

TABLE 9. Extended Control Mode Operation (Pin 14 Floating)

Pin	Function
3	SCLK (Serial Clock)
4	SDATA (Serial Data)
127	$\overline{SCS}$ (Serial Interface Chip Select)

2.10 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, no input should go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot.

Care should be taken not to overdrive the inputs of the ADC08B3000. Such practice may lead to conversion inaccuracies and even to device damage.

Incorrect analog input common mode voltage in the d.c. coupled mode. As discussed in section 1.1.4 and 2.2, the Input common mode voltage must remain within 50 mV of the V_{CMO} output , which has a variability with temperature that must also be tracked. Distortion performance will be degraded if the input common mode voltage is more than 50 mV from V_{CMO} .

Using an inadequate amplifier to drive the analog input. Use care when choosing a high frequency amplifier to drive the ADC08B3000 as many high speed amplifiers will have higher distortion than will the ADC08B3000, resulting in overall system performance degradation.

Driving the V_{BG} pin to change the reference voltage. As mentioned in Section 2.1, the reference voltage is intended to be fixed to provide one of two different full-scale values (600 mV_{P-P} and 800 mV_{P-P}). Over driving this pin will not change the full scale value, but can be used to change the LVDS common mode voltage from 0.8V to 1.2V by tying the V_{BG} pin to V_A.

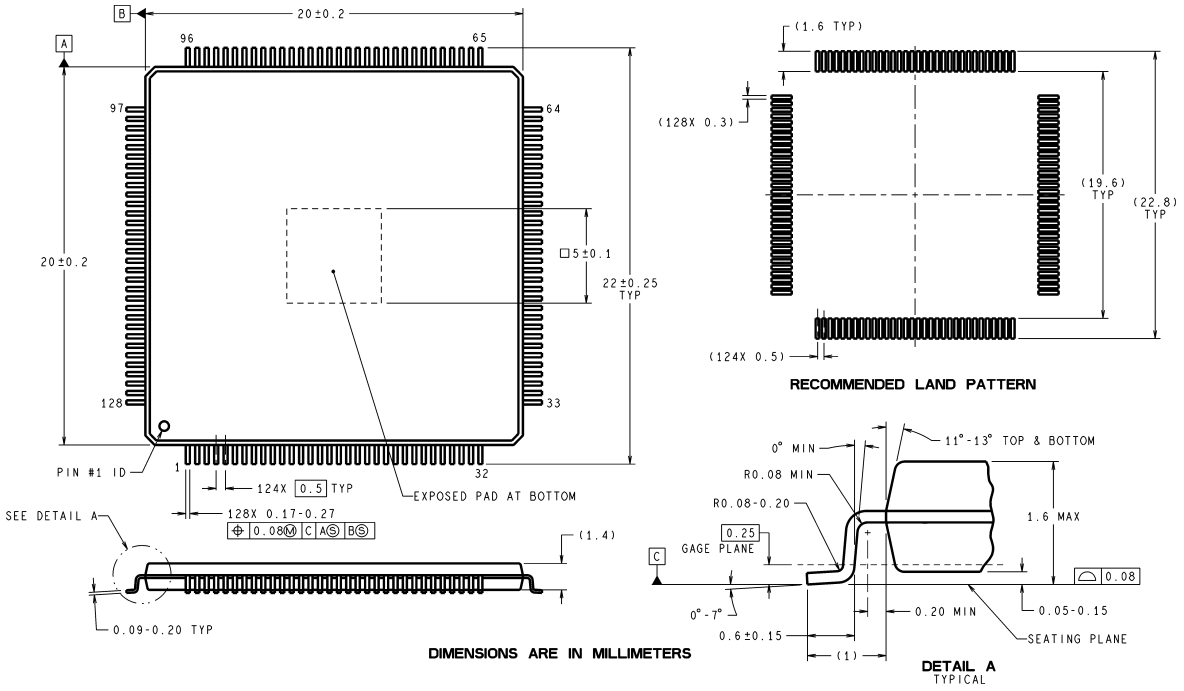
Driving the clock input with an excessively high level signal. The ADC input clock level should not exceed the level described in the Operating Ratings Table or the input offset could change.

Inadequate input clock levels. As described in Section 2.3, insufficient input clock levels can result in poor performance. Excessive input clock levels could result in the introduction of an input offset.

Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal. As described in Section 2.6.2, it is important to provide adequate heat removal to ensure device reliability. This can either be done with adequate air flow or the use of a simple heat sink built into the board. The backside pad should be grounded for best performance.

Physical Dimensions inches (millimeters) unless otherwise noted



VNX128A (Rev A)

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE JEDEC REGISTRATION MS-026, VARIATION BFB.

128-Lead Exposed Pad LQFP
NS Package Number VNX128A

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