National Semiconductor

PRELIMINARY

ADC1080, ADC1280 12-Bit Successive Approximation A/D Converter

General Description

The ADC1080 and ADC1280 are complete successive approximation analog-to-digital converters that include an internal clock, reference and comparator.

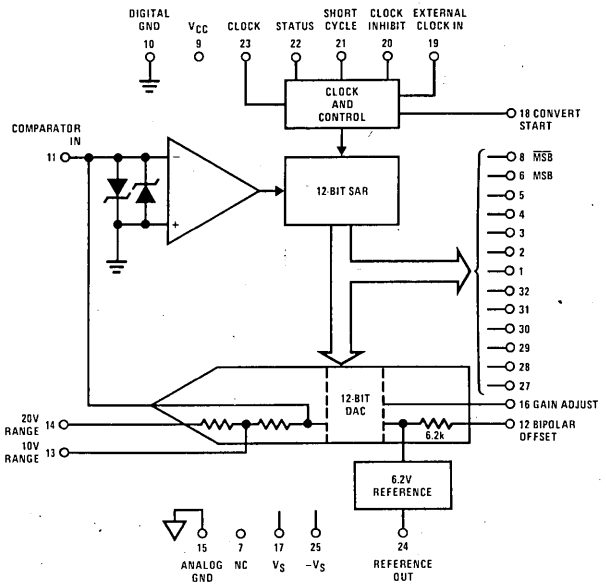
The design of the ADC1080 and ADC1280 includes scaling resistors that provide analog signal ranges of ±2.5V, ±5.0V, ±10V, 0V to 5V, or 0V to 10V. The 6.2V precision reference may be used for external applications. All digital signals are fully TTL compatible; output data may be read in both serial and parallel form.

The ADC1280 has a maximum linearity of 0.012% of FSR and the ADC1080 has a maximum linearity of 0.048% of FSR. Both grades are specified for use over the −25°C to +85°C temperature range and both are available in a 32-pin DIP.

Features

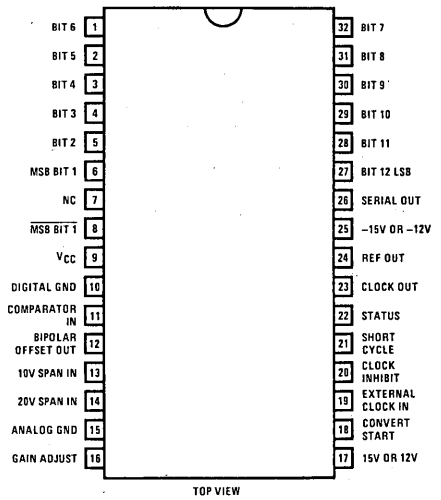
- Completely self-contained with internal reference, clock, and comparator
- High reliability exact replacement for ADC80
- ±1/2 LSB linearity for ADC1280
- Input voltage ranges of ±2.5V, ±5V, ±10V, 0V to 5V, and 0V to 10V
- 6.2V reference available for external use at 1.5 mA
- Conversion speed—22 μs
- Short cycle and external clock options for faster conversion time

Block Diagram



Connection Diagram

Dual-In-Line Package



Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±18V	Operating Temperature Range	−55°C to +100°C
Logic Supply Voltage	7V	Storage Temperature Range	−65°C to +150°C
Reference Input Voltage (V_{REF})	0V, 18V	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$T_A = -25°C$ to $+85°C$, $V_S = \pm 11.4V$ to $\pm 16.00V$, $V_{CC} = 4.75V$ to $5.25V$ unless otherwise noted.

Parameter	Conditions	ADC1280 Min	ADC1280 Typ (Note 1)	ADC1280 Max	ADC1080 Min	ADC1080 Typ (Note 1)	ADC1080 Max	Units
CONVERTER CHARACTERISTICS								
Resolution		12			10			Bits
Linearity Error	$T_A = 25°C$			±0.012			±0.048	% FSR (Note 3)
Linearity Error Tempco				±3			±3	ppm of FSR/°C
Differential Linearity Error			±1/2			±1/2		LSB
No Missing Codes	(Note 2)	12			10			Bits
Full-Scale (Gain) Error	$T_A = 25°C$ (Note 4)		±0.1			±0.1		% FSR
Zero-Scale (Offset) Error	$T_A = 25°C$ (Note 4) Unipolar		±0.05			±0.05		%FSR
	$T_A = 25°C$ (Note 4) Bipolar		±0.1			±0.1		%FSR
Full-Scale (Gain) Tempco				±30			±30	ppm/°C
Zero-Scale (Offset) Tempco	Unipolar			±3			±3	ppm of FSR/°C
	Bipolar			±15			±15	ppm of FSR/°C
Analog Input Voltage Range	Unipolar	0V to 5V, 0V to 10V						V
	Bipolar	±2.5V, ±5V, ±10V						V
Input Impedance (Direct Input)	0V to 5V, ±2.5V		2.5k			2.5k		Ω
	0V to 10V, ±5V		5k			5k		Ω
	±10V		10k			10k		Ω
REFERENCE CHARACTERISTICS								
Reference Voltage		6.07	6.2	6.33	6.07	6.2	6.33	V
Tempco of Drift			10	20		10	20	ppm/°C
External Use Current				1.5			1.5	mA
Output Impedance			0.05	1.0		0.05	1.0	Ω
DIGITAL AND DC CHARACTERISTICS								
Logic 1 Input Voltage (Bit Off)	Incl Ext Clock Input	2.0			2.0			V
Logic 0 Input Voltage (Bit On)	Incl Ext Clock Input			0.8			0.8	V
Logic 1 Input Current	Incl Ext Clock Input, $V_{IN} = 2.5V$		0.05	1		0.05	1	μA
Logic 0 Input Current	Incl Ext Clock Input, $V_{IN} = 0V$			−100			−100	μA
Logic 0 Output Voltage	$I_{OUT} = 3.2$ mA			0.4			0.4	V
Logic 1 Output Voltage	$I_O = 360\ \mu A$	2.4			2.4			V
Short Circuit Output Current	$V_{CC} = Max$	−18		−57	−18		−57	mA
Power Supply Current	$T_A = 25°C$ I^+		16			16		mA
	$T_A = 25°C$ I^-		12			12		mA
	$T_A = 25°C$ I_{CC}		92			92		mA
Power Supply Sensitivity	V_S		0.003			0.003		FSR/% V_S
	V_{CC}		0.0015			0.0015		FSR/% V_{CC}

Electrical Characteristics (Continued)

$T_A = -25°C$ to $+85°C$, $V_S = \pm 11.4V$ to $\pm 16.00V$, $V_{CC} = 4.75V$ to $5.25V$ unless otherwise noted.

Parameter	Conditions		ADC1280			ADC1080			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
AC CHARACTERISTICS									
Conversion Time	$T_A = 25°C$	Internal Clock		22	25			21	μs
		External Clock		16	18			12	
Clock Frequency	Internal			575			575		kHz
Convert Command			100			100			ns

Note 1: All typical values are for $T_A = 25°C$.

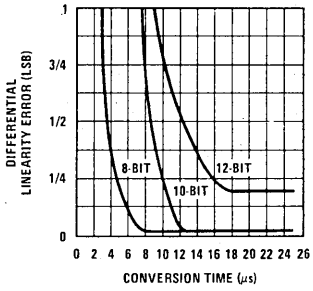
Note 2: Guarantees that for increasing analog voltage, the digital code increases. This specification guarantees monotonicity.

Note 3: FSR means "full-scale range" and is 20V for ±10V range, 10V for ±5V range.

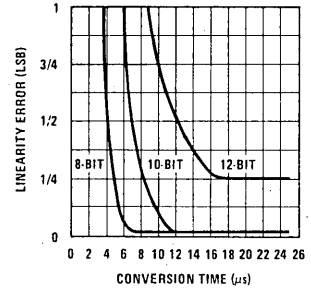
Note 4: Externally adjustable to zero.

Typical Performance Curves

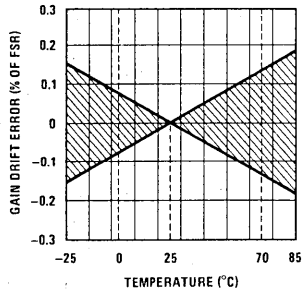
Linearity Error vs Conversion Time (Normalized)



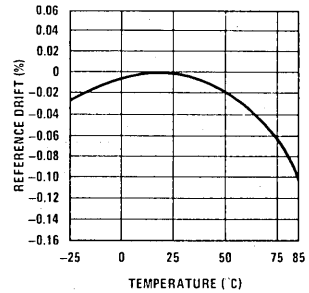
Differential Linearity Error vs Conversion Time (Normalized)



Maximum Gain Drift Error—% of FSR vs Temperature



Reference Drift—% Error vs Temperature



1.0 Definition of Terms and Applications

The accuracy of an A/D converter is described by the transfer function shown in *Figure 1.* There is an inherent quantization uncertainty of ± 1/2 LSB associated with the resolution.

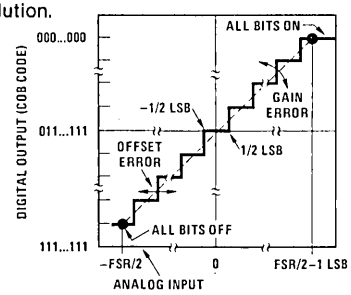


FIGURE 1. Transfer Characteristics for an Ideal Bipolar A/D

The remaining errors in the A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error, and power supply rejection. The matching and tracking errors in the ADC1080 and ADC1280 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ± 0.1% FSR for gain and ± 0.05% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in *Figures 2 and 3.* Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full-scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size *(Figure 1).*

Monotonic behavior requires that the differential linearity error be less than 1 LSB; however, a monotonic converter can have missing codes.

There are three types of drift error over temperature: offset, gain, and linearity. Offset drift causes a shift of the transfer characteristics left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full-scale point.

1.1 Gain and Offset Error

Initial gain and offset errors are factory trimmed to ± 0.1% of FSR (± 0.05% for unipolar offset) at 25°C.

Gain and offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC1080 and ADC1280 as shown in *Figures 2 and 3.* Multiturn potentiometers with 100 ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10 kΩ to 100 kΩ. All resistors should be 20% or better. Pin 16 (gain adjust) may be left open if no external adjustment is required.

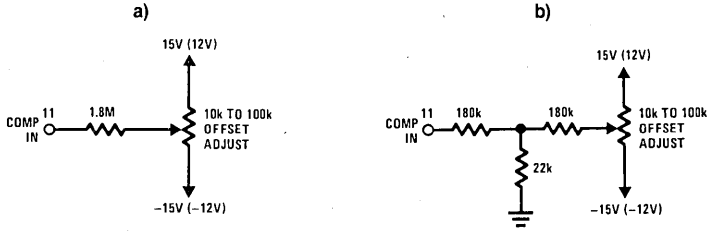


FIGURE 2. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment

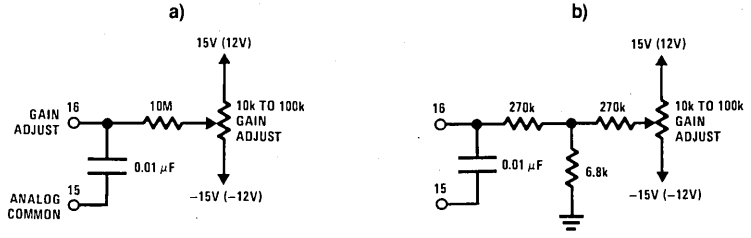


FIGURE 3. Two Methods of Connecting Optional Gain Adjust with a 0.6% Range of Adjustment

Adjustment Procedure

Offset—Connect the offset potentiometer as shown in *Figure 2*. Sweep the input through the end point transition voltage that should cause an output transition to all ones.

Adjust the offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

Gain—Connect the gain adjust potentiometer as shown in *Figure 3*. Sweep the input through the end point transition voltage that should cause an output transition to all zeros.

Adjust the gain potentiometer until the actual end point transition voltage occurs E_{IN}^{ON}. Table I details the transition voltage levels required.

1.2 Accuracy Drift vs Temperature

Three major drift parameters degrade A/D converter accuracy over temperature: they are gain, offset and linearity drift. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\in g^2 + \in o^2 + \in e^2}$$

where $\in g$ = gain drift error (ppm/°C)

$\in o$ = offset drift error (ppm of FSR/°C)

$\in e$ = linearity error (ppm of FSR/°C)

For *unipolar* operation, the total RSS drift is ±30.3 ppm/°C and for *bipolar* operation, the total RSS drift is ±33.7 ppm/°C.

1.3 Accuracy vs Speed

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC1080 and ADC1280 are shown in *Figures 3 and 4.*

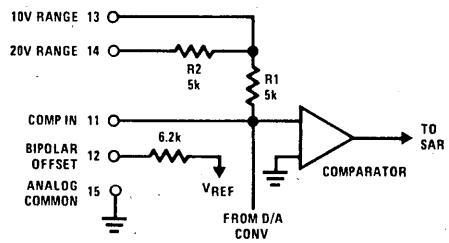


FIGURE 4. Input Scaling Circuit

The ADC1080 and ADC1280 conversion speeds are specified for a maximum linearity error of ± 1/2 LSB and a differential linearity error of ± 1/2 LSB with the internal clock. Faster conversion speeds up to 23 μs for 12 bits, 12 μs for 10 bits, and 6 μs for 8 bits are possible with an external clock.

1.4 Power Supply Sensitivity

Changes in the DC power supplies will affect the accuracy of the ADC1080 and ADC1280. Normally, regulated power supplies with 1% or less ripple are recommended.

1.5 Layout Precautions

Analog and digital commons are not connected internally in the ADC1080 and ADC1280, but should be connected together as close to the unit as possible, preferably to a large ground plane under the A/D. If these grounds must be run separately, use a wide conductor pattern between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

1.6 Input Scaling

The ADC1080 and ADC1280 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table I. See *Figure 4* for circuit details.

TABLE I. INPUT SCALING CONNECTIONS

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
± 10V	COB or CTC	11	Input Signal	14
± 5V	COB or CTC	11	Open	13
± 2.5V	COB or CTC	11	Pin 11	13
0V to 5V	CSB	15	Pin 11	13
0V to 10V	CSB	15	Open	13

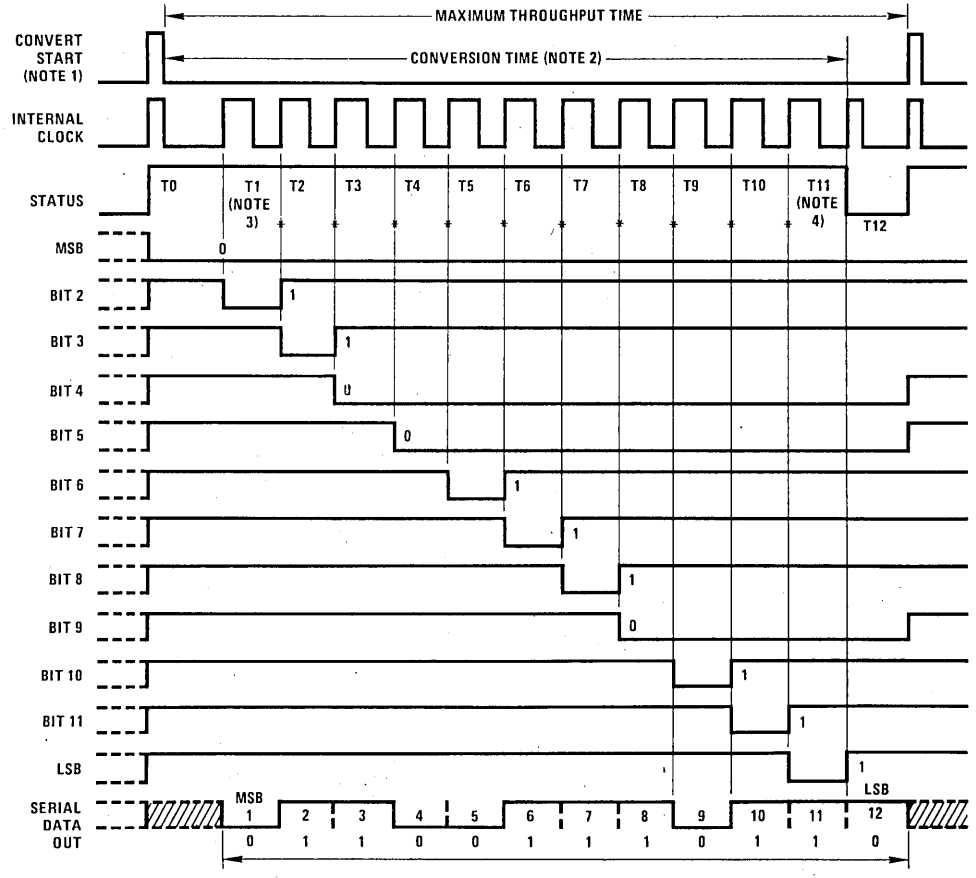
2.0 Functional Description

On receipt of a CONVERT START command, the ADC1080 and ADC1280 convert the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

2.1 Timing

The Timing Diagram is shown in *Figure 5*. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t0, B1 is reset and B2-B12 are set unconditionally. At t1 the bit 1 decision is made (keep) and bit 2 is unconditionally reset. At t2, the bit 2 decision is made (keep) and bit 3 is reset unconditionally. This sequence continues until the bit 12 (LSB) decision (keep) is made at t12. After a 40 ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic 0 state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see *Figure 5*).



Note 1: The convert start pulse width is 100 ns min and must remain low during a conversion. The conversion is initiated by the rising edge of the convert command.

Note 2: 25 μs for 12 bits and 21 μs for 10 bits (max).

Note 3: MSB decision

Note 4: LSB decision 40 ns prior to the status going low.

*Bit decisions

FIGURE 5. Timing Diagram (Binary Code 011001110110)

Incorporation of this 40 ns delay guarantees that the parallel (and serial) data are valid at the Logic 1 to Logic 0 transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

2.2 Digital Output Data

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether bit 1 (pin 6) or its logical inverse bit 1 (pin 8) is used as the MSB. Parallel data becomes valid approximately 40 ns before the STATUS flag returns to Logic 0, permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200 ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in *Figure 5.* There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in *Figure 5.* The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

2.3 Short Cycle Input

A short cycle input, pin 21, permits the timing cycle shown in *Figure 5* to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 21 is connected to 5V (pin 9). When 10-bit resolution is desired, pin 21 is connected to bit 11 output pin 28. The conversion cycle then terminates, and the STATUS flag resets after the bit 10 decision (t10 + 40 ns in the Timing Diagram of *Figure 5*). Short cycle pin connections and associated maximum 12-bit, 10-bit and 8-bit conversion times are summarized in Table II.

TABLE II. SHORT CYCLE CONNECTIONS

Connect Short Cycle Pin 21 To Pin	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
9	12	0.024	25	t12 + 40 ns
28	10	0.100	21	t10 + 40 ns
30	8	0.390	17	t8 + 40 ns

2.4 Control Modes

The timing sequence of the ADC1080 and ADC1280 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in *Figures 6-9.*

2.5 Calibration

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in *Figures 10 and 11*, are used for device calibration. To prevent interaction of these two adjustments, zero is always adjusted first and then gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and − FS for bipolar input ranges). Gain is adjusted with the analog input near the most postive end of the analog range.

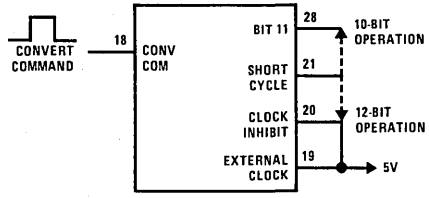


FIGURE 6. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

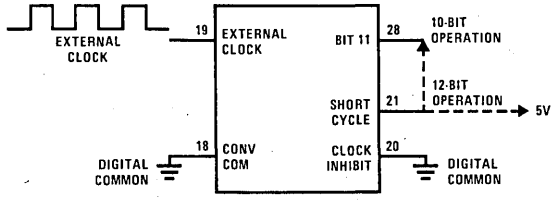


FIGURE 7. Continuous Conversion with External Clock. Conversion is Initiated by 14th Clock Pulse. Clock Runs Continuously.

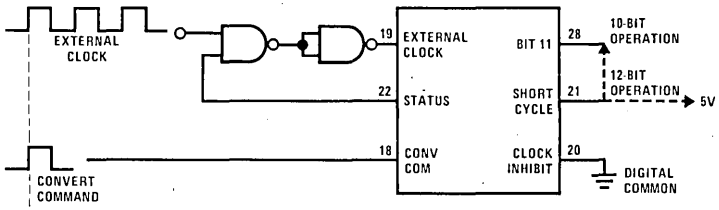


FIGURE 8. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command Must be Synchronized with Clock.

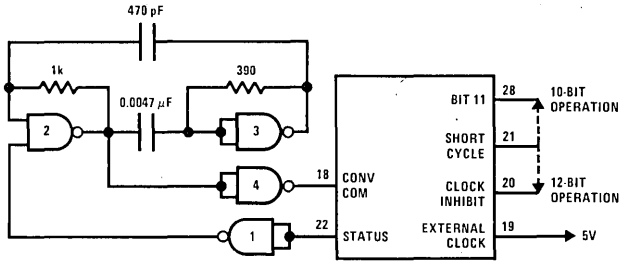


FIGURE 9. Continuous Conversion with Internal Clock. Conversion is Initiated by the 14th Clock Pulse. Clock Runs Continuously. The Oscillator Formed by Gates 2 and 3 Insures that the Conversion Process will Start When Logic Power is First Turned On.

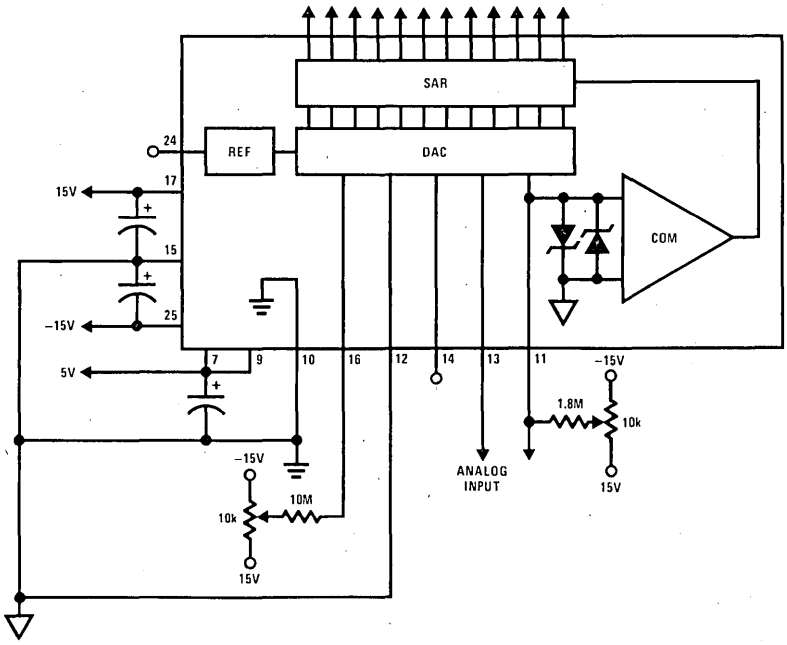


FIGURE 10. Analog and Power Connections for Unipolar 0V–10V Input Range

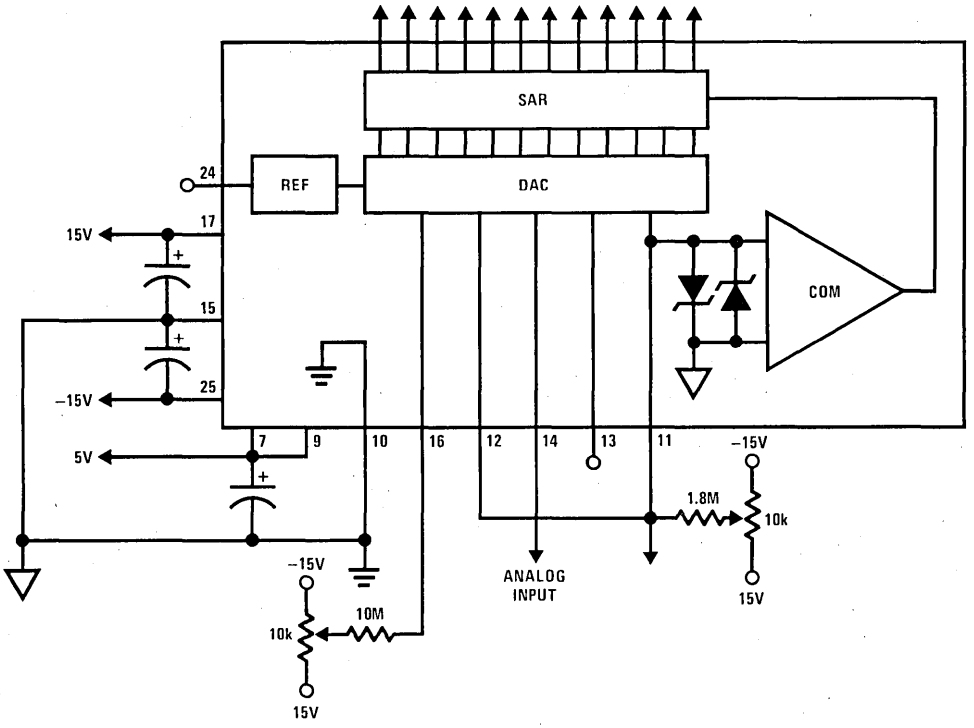


FIGURE 11. Analog and Power Connections for Bipolar ±10V Input Range

0V to 10V Range: Set analog input to +1 LSB = +0.0024V. Adjust zero for digital output = 1 1 1 1 1 1 1 1 1 1 1 1 0. Zero is now calibrated. Set analog input to +FSR −2 LSB = +9.9952V. Adjust gain for 0 0 0 0 0 0 0 0 0 0 0 0 1 digital output code; full-scale (gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 0 1 1 1 1 1 1 1 1 1 1 1.

−10V to +10V Range: Set analog input to −9.9951V; adjust zero for 1 1 1 1 1 1 1 1 1 1 1 0 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust gain for 0 0 0 0 0 0 0 0 0 0 0 0 1 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0 1 1 1 1 1 1 1 1 1 1 1.

Other Ranges: Representative digital coding for 0V to 10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0V to 5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0V to 10V and −10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4 LSB using the static adjustment procedure described in paragraph 1.1. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level.

TABLE III. INPUT VOLTAGES AND CODE DEFINITIONS

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	± 10V	± 5V	± 2.5V	0V to 20V	0V to 10V	0V to 5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	78.13 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	19.53 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	4.88 mV	2.44 mV	1.22 mV
Transition Values							
MSB LSB							
0 0 0...0 0 0****	+ Full-Scale	10V − 3/2 LSB	5V − 3/2 LSB	2.5V − 3/2 LSB	20V − 3/2 LSB	10V − 3/2 LSB	5V − 3/2 LSB
0 1 1...1 1 1	Mid-Scale	0	0	0	10V	5V	2.5V
1 1 1...1 1 0	− Full-Scale	−10V + 1/2 LSB	−5V + 1/2 LSB	−2.5V + 1/2 LSB	0 + 1/2 LSB	0 + 1/2 LSB	0 + 1/2 LSB

*COB = Complementary Offset Binary.

**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.

***CSB = Complementary Straight Binary.

****Voltages given are the nominal value for transition to the code specified.

Ordering Information

Temperature Range		−25°C to +85°C
Linearity (Accuracy)	0.012%	*ADC1280HCD ADC80AG-12 ADC80AGZ-12
	0.048%	*ADC1080HCD ADC80AG-10 ADC80AGZ-10
Package		D32B

*Devices may be ordered by either part number

Contact National Semiconductor Corp., Product Marketing Group for Package and Ordering Information