GENERAL DESCRIPTION

The adc1295x is a CMOS 8bit A/D converter which combines an auto offset calibration comparator, high resolution R-string DAC, clock generator, 8bit successive approximation register (SAR), output register, and AINC which controls analog input selection. The adc1295x provides software-selection power-down mode. The device operates with a single +3.3V supply and A/D conversion rate is 800KSPS, external clock XP1 is 40MHz. The operating temperature range is -40–85 °C for commercial specification.

FEATURES

— Resolution : 8-bit

— Maximum Conversion Rate : 800kSPS

— Power Supply : 3.3V Single (Typ)

— Differential Linearity Error : ± 1.0 LSB

— Integral Linearity Error : ± 2.0 LSB

— Folding, Interpolation and Pipelined Scheme

— Low Power Consumption
: at operating, 3.3mW(typ)
: at standby, 330nW(typ)

— Guaranteed Monotonicity

— No Missing Code

— Latched Tri-state Output

— Operating Temperature Range : -40 °C – 85 °C

TYPICAL APPLICATIONS

— MICOM

— Battery Charger

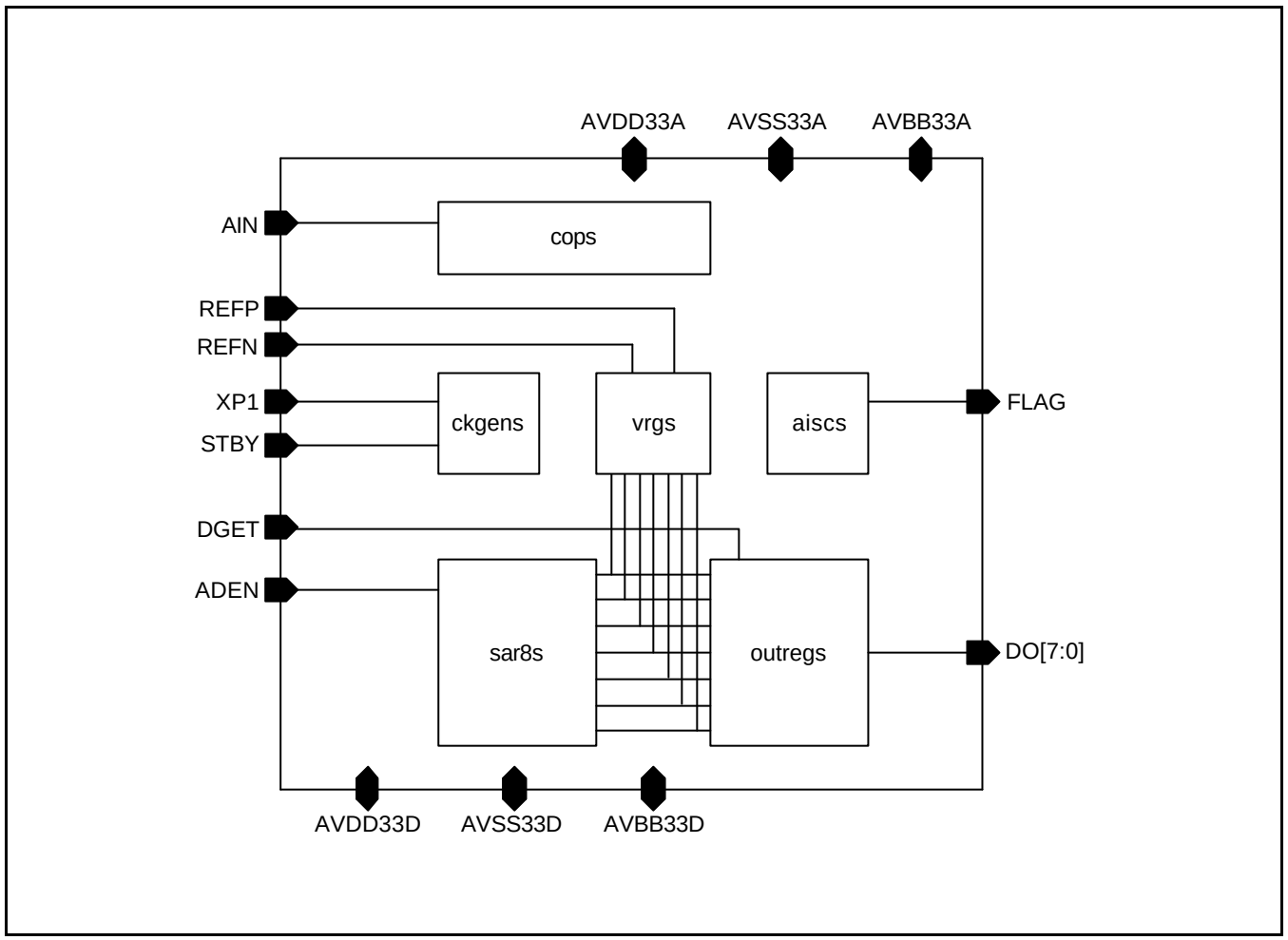
— Game Pack

— Digital Still Camera

— Hand Held Computer & Organizer.

— Other Low power equipments.

FUNCTIONAL BLOCK DIAGRAM



Ver 1.2 (Apr. 2002)

No responsibility is assumed by SEC for its use nor for any infringements of patents or other rights of third parties that may result from its use. The content of this data sheet is subject to change without any notice.

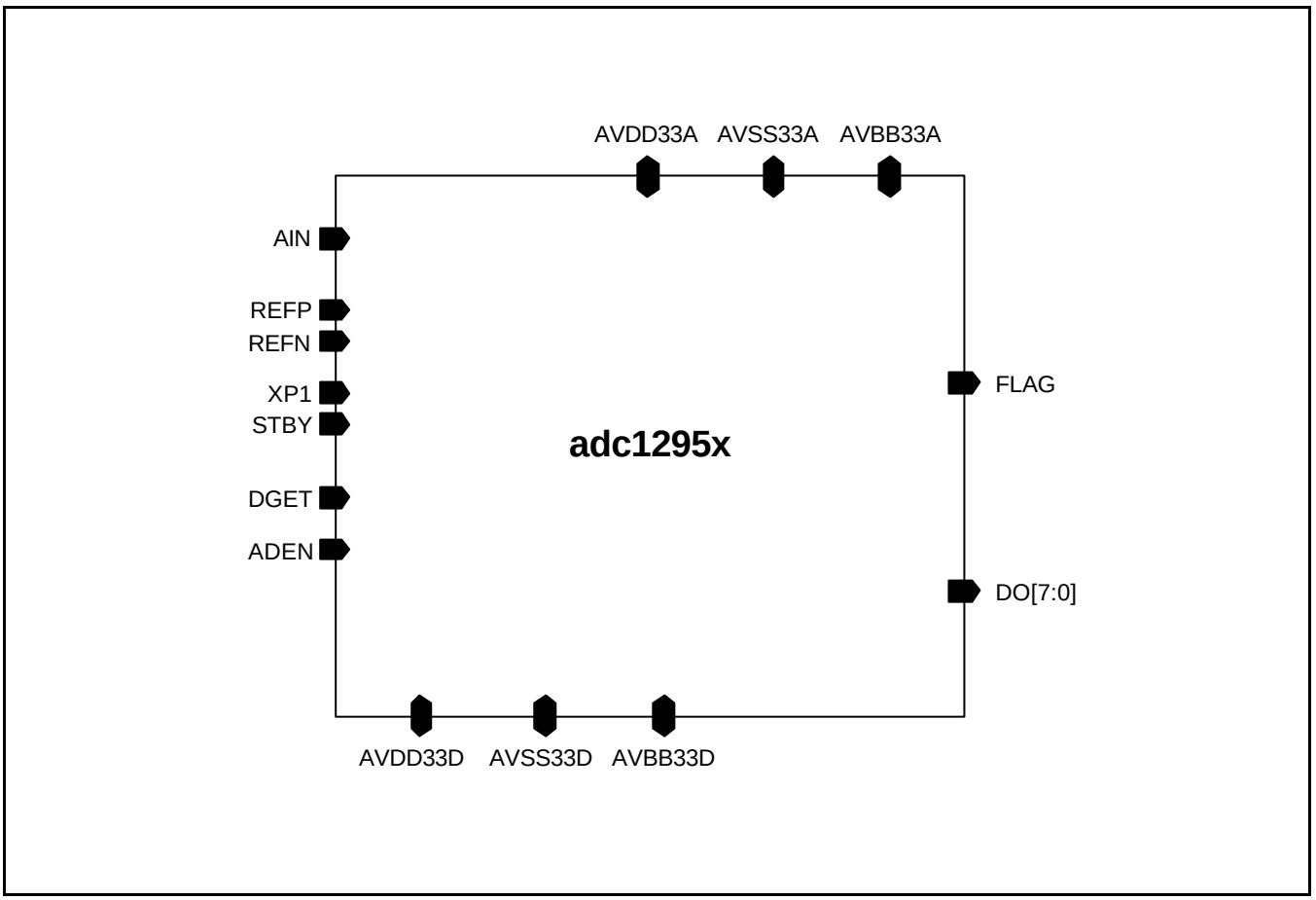
CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
REFP	AI	phia_abb	Internal Reference Top Bias. 3.3V
REFN	AI	phia_abb	Internal Reference Bottom Bias. 0V
AVDD33A	AP	vdd3t_abb	Analog Power(3.3V)
AVSS33A	AG	vss3t_abb	Analog Ground
AVBB33A	AG	vbb3_abb	Analog Substrate
AIN	AI	phiar50_abb	Analog Input
XP1	DI	phicc_abb	Main Clock(external)
STBY	DI	phicc_abb	System Power Down(Active High)
ADEN	DI	phicc_abb	A/D Conversion Enable
DO[7:0]	DO	phoa_abb	Digital Outputs
DGET	DI	phicc_abb	DOUTs Read Enable
FLAG	DO	phoa_abb	Test pin for checking the ADC state
AVBB33D	DG	vbb3_abb	Digital Substrate
AVSS33D	DG	vss3t_abb	Digital Ground
AVDD33D	DP	vdd3t_abb	Digital Power(3.3V)

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bi-direction
— DB: Digital Bi-direction
— AP: Analog Power
— AG: Analog Ground
— DP: Digital Power
— DG: Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	4.5	V
Analog Input Voltage	AIN	V_{SS} to V_{DD}	V
Digital Input Voltage	DIN	V_{SS} to V_{DD}	V
Digital Output Voltage	$V_{OH, VOL}$	V_{SS} to V_{DD}	V
Reference Voltage	REFP/REFN	V_{SS} to V_{DD}	V
Storage Temperature Range	Tstg	-55 to 125	°C
Operating Temperature Range	Topr	-40 to 85	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	AVDD33A AVDD33D	3.3-5%	3.3	3.3+5%	V
Supply Voltage Difference	AVDD33A AVSS33D	-0.1	0.0	0.1	V
Reference Input Voltage	REFP REFN	– –	AVDD33A 0	– –	V
Analog Input Voltage	AIN	REFN	–	REFP	V
Clock High Time Clock Low Time	Tpwh Tpwl	– –	19 19	– –	ns
Digital Input 'L' Voltage Digital Input 'H' Voltage	V_{IL} V_{IH}	0 0.9*AVDD33D	– –	0.1*AVDD33D AVDD33D	V
Operating Temperature	Topr	-40	–	85	°C

NOTE: It is strongly recommended that all the supply pins (AVDD33A, AVDD33D) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Conditions
Resolution	–	–	8	–	Bits	
Differential Linearity Error	DLE	–	±0.5	±1.0	LSB	XP1 : 40MHz
Integral Linearity Error	ILE	–	±0.5	±2.0	LSB	
Offset Voltage Error(top)	EOT	–	±2.0	±4.0	LSB	EOT = REFP-AIN(255,256)
Offset Voltage Error(bottom)	EOB	–	±2.0	±4.0	LSB	EOB = AIN(0,1)-REFN

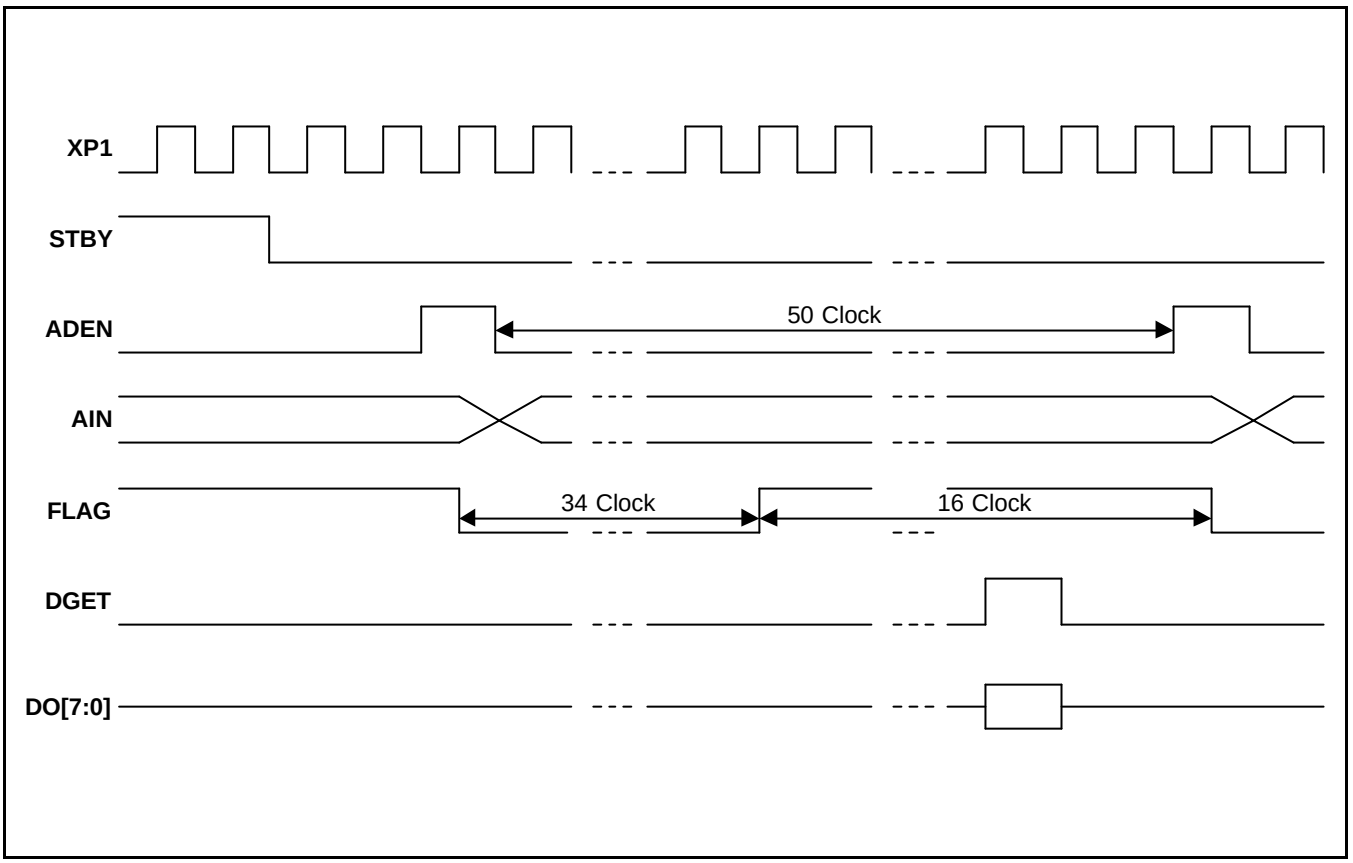
NOTES:

1. Converter Specifications (unless otherwise specified)
   AVDD33A=3.3V AVDD33D=3.3V
   AVSS33A=GND AVSS33D=GND
   AVBB33A=GND AVBB33D=GND
   REFP=3.3V REFN=0.0V
   Ta=25°C
2. TBD : To Be Determined

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Conditions
Clock High Time	Tpwh	–	19	–	ns	XP1 : 25MHz (Typ)
Clock Low Time	Tpwl	–	19	–	ns	40MHz (Max)
Conversion Rate	f_{AD}	–	500	800	KSPS	
Conversion Time	t_{AD}	1.25	2	–	us	
Dynamic Supply Current	Is	–	1	1.5	mA	Power Load Cap:10uF//0.1uF Output load cap.=1pF
	Isd	–	0.1	0.5	uA	at Power Down.
Power Dissipation	Pd	–	3.3	5.4	mW	during A/D operation
	Pdd	–	0.33	1.8	uW	at Power Down.
Digital Output Data Delay	t_D	–	20	25	ns	Output load cap.=1pF

TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

1. XP1

The XP1 is the system main clock. If 25MHz clock is applied, 10bit 500KSPS or 8bit 650KSPS outputs are produced. In case of 10MHz clock, 10bit 200KSPS or 8bit 250KSPS outputs are made.

2. STBY

This pin is used for keeping standby without A/D conversion operation. For A/D operation, its state must be changed from '1' to '0' after at least one XP1 period. In the timing chart, 3.5-XP1 period is drawn and this state transition can occur even at rising or falling edges. If not needed, it can be tied to GND.

3. ADEN

This is a A/D conversion enable signal. It is for one XP1 period at falling edge. In a 10bit, at least 45-XP1 periods are required until the next ADEN, and 37-XP1 periods are delayed until the next ADEN for an 8bit.

4. DO[7:0]

Digital output pins.

5. DGET

Data read signal. If DGET is applied during A/D conversion, selected AIN pin information is produced(refer to TIMING CHART). It is to check if the right analog input is selected. After A/D operation, the state of the test pin, FLAG, changes to '1', and A/D converted data are produced by applying DGET signal.

6. AIN

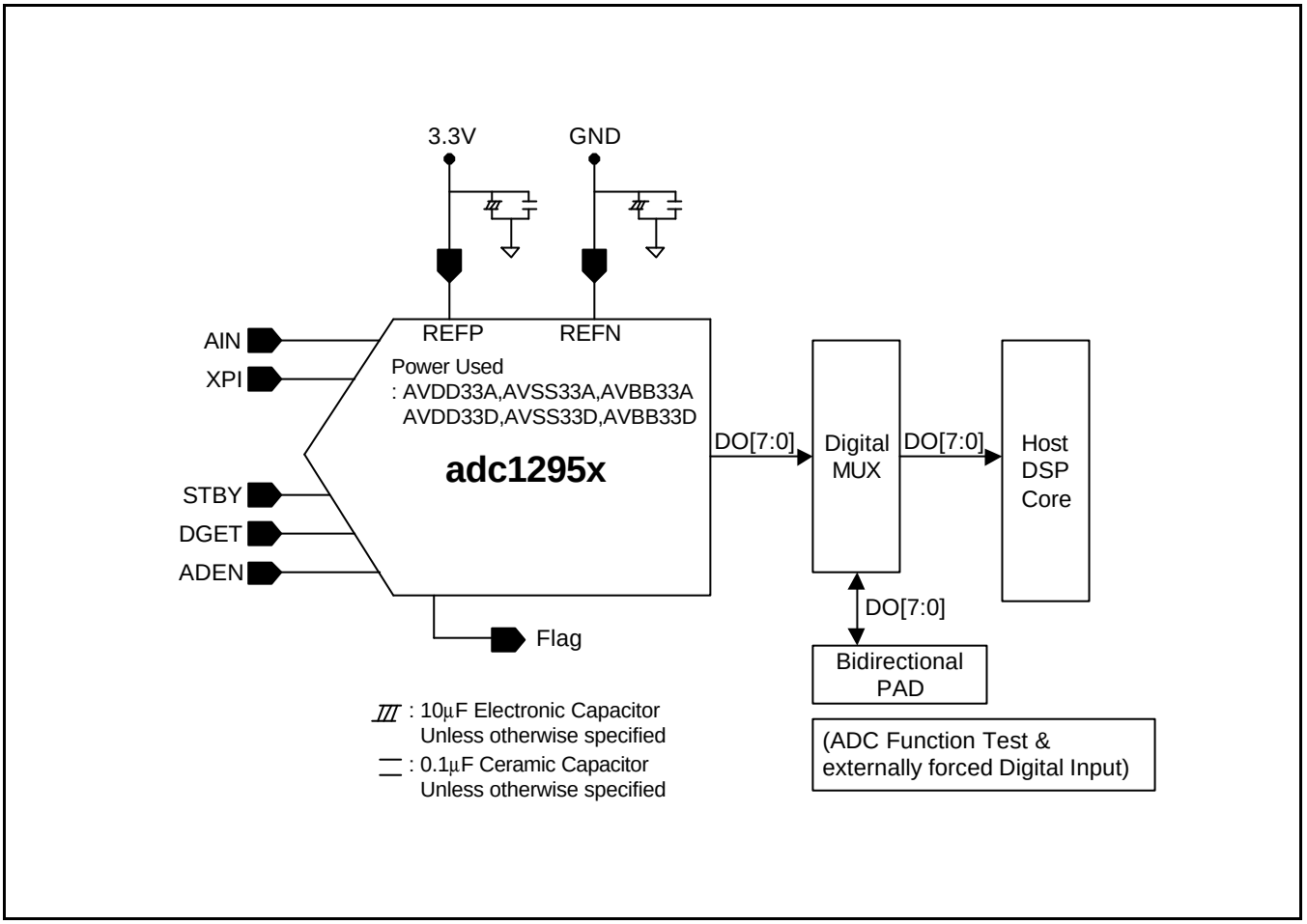
Analog Input

7. FLAG

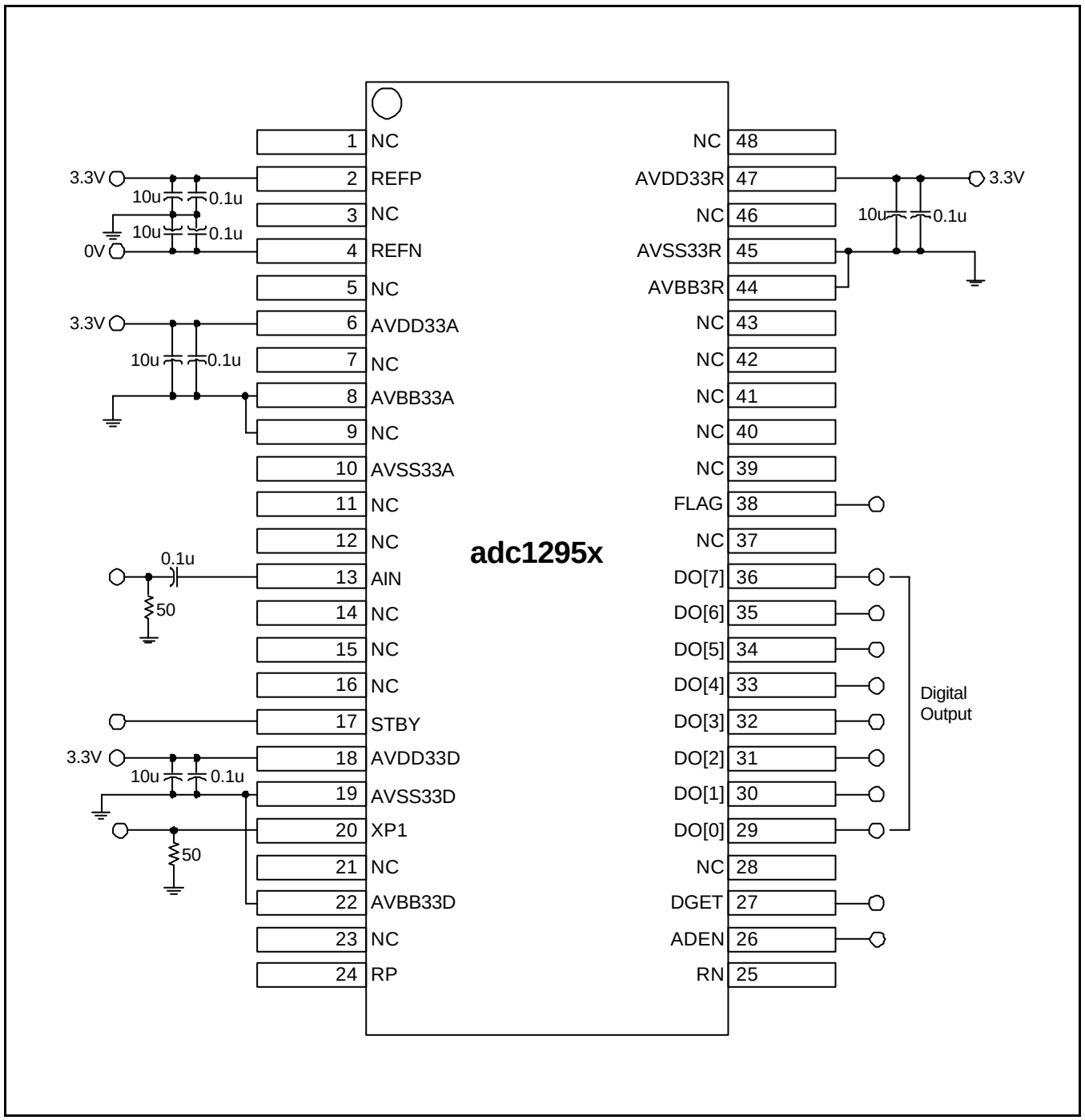
Test pin. Its state goes LOW during A/D conversion, and goes HIGH after the A/D conversion. If STBY signal is applied even at A/D conversion mode, its state goes HIGH immediately.

CORE EVALUATION GUIDE

1. You can test ADC function by the DGET. If you don't use the DGET pin, this ADC function is evaluated by external check on the bi-directional pads connected to input nodes of HOST DSP back-end circuit.
2. The reference voltages may be biased externally through REFP and REFN pins



PACKAGE CONFIGUATION



PACKAGE PIN DESCRIPTION

Pin Name	Pin No.	I/O Type	I/O PAD	Pin Description
REFP	2	AI	phia_abb	Internal Reference Top Bias. 3.3V
REFN	4	AI	phia_abb	Internal Reference Bottom Bias. 0V
AVDD33A	6	AP	vdd3t_abb	Analog Power(3.3V)
AVBB33A	8	AG	vbb3_abb	Analog Substrate
AVSS33A	10	AG	vss3t_abb	Analog Ground
AIN	13	AI	phiar10_abb	Analog Inputs. Input Span : REFP – REFN
STBY	17	DI	phicc_abb	System Power Down(Active High)
AVDD33D	18	DP	vdd3t_abb	Digital Power(3.3V)
AVSS33D	19	DG	vss3t_abb	Digital Ground
XP1	20	DI	phicc_abb	Main Clock(external)
AVBB33D	22	DG	vbb3_abb	Digital Substrate
ADEN	26	DI	phicc_abb	A/D Conversion Enable
DGET	27	DI	phicc_abb	Read Enable
DO[7:0]	29~36	DO	phot12_abb	Digital Outputs
FLAG	38	DO	phot12_abb	Testpin. ADC Operation Checking.
AVBB33R	44	DG	vbb3_abb	Driver Substrate
AVSS33R	45	DG	vss3t_abb	Driver Ground
AVDD33R	47	DP	vdd3t_abb	Driver Power(3.3V)

USER GUIDE

1. Speed Up

— The initial target speed(Conversion Rate) of adc1295x was 8bit 500KSPS~ 800KSPS, but it proved to operate well even at 8bit 900KSPS because of a lot of design margin. It would be realized by speed-up of XP1.

2. Input Range Variation

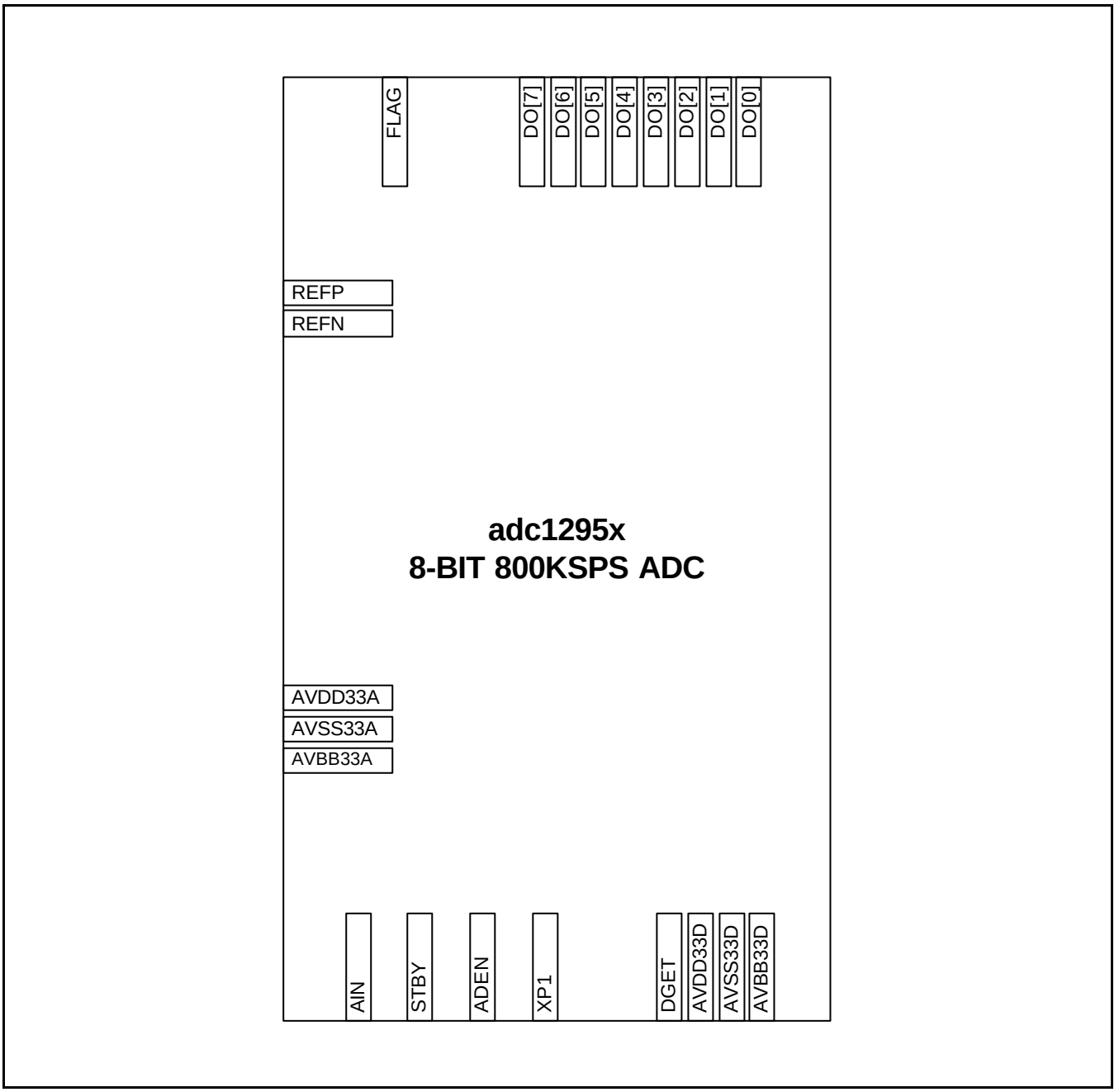
— The analog input of this ADC is single input and the range is from REFN to REFP. This AIN voltage follows reference voltage range fundamentally. Therefore, in order to alter into another input voltage range, change the voltage value of REFP.

— You can use the AIN voltage whose minimum range is 2.7V. In this case, the REFP is 2.7V and REFN is 0.0V. If the range is 3.0V, the REFP is 3.0V and REFN is 0.0V. It is an user selection item. In case of maximum voltage range, the REFP is the power level(3.3V) and the REFN is the ground level.

3. Note that this ADC has not the sample and hold circuit, therefore during the A/D conversion the analog input voltage variation should not deviate more than 1 LSB voltage range.

PHANTOM CELL INFORMATION

— Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
The term "External" implies that the pins should be assigned externally like power pins.
The term "External/internal" implies that the applications of these pins depend on the user.



Pin Name	Pin Usage	Pin Layout Guide
AVDD33A	External	- Maintain the large width of lines as far as the pads. - place the port positions to minimize the length of power lines. - Do not merge the analog powers with anoter power from other blocks. - Use good power and ground source on board.
AVSS33A	External	
AVBB33A	External	
AVDD33D	External	
AVSS33D	External	
AVBB33D	External	
AIN	External/Internal	- Do not overlap with digtal lines. - Maintain the shotest path to pads.
XP1	External/Internal	- Separate from all other analog signals
REFP	External/Internal	- Maintain the larger width and the shorter length as far as the pads. - Separate from all other digital lines.
REFB	External/Internal	
STBY	External/Internal	
ADEN	External/Internal	
DGET	External/Internal	
FLAG	External/Internal	
DO[7]	External/Internal	
DO[6]	External/Internal	
DO[5]	External/Internal	
DO[4]	External/Internal	
DO[3]	External/Internal	
DO[2]	External/Internal	
DO[1]	External/Internal	
DO[0]	External/Internal	

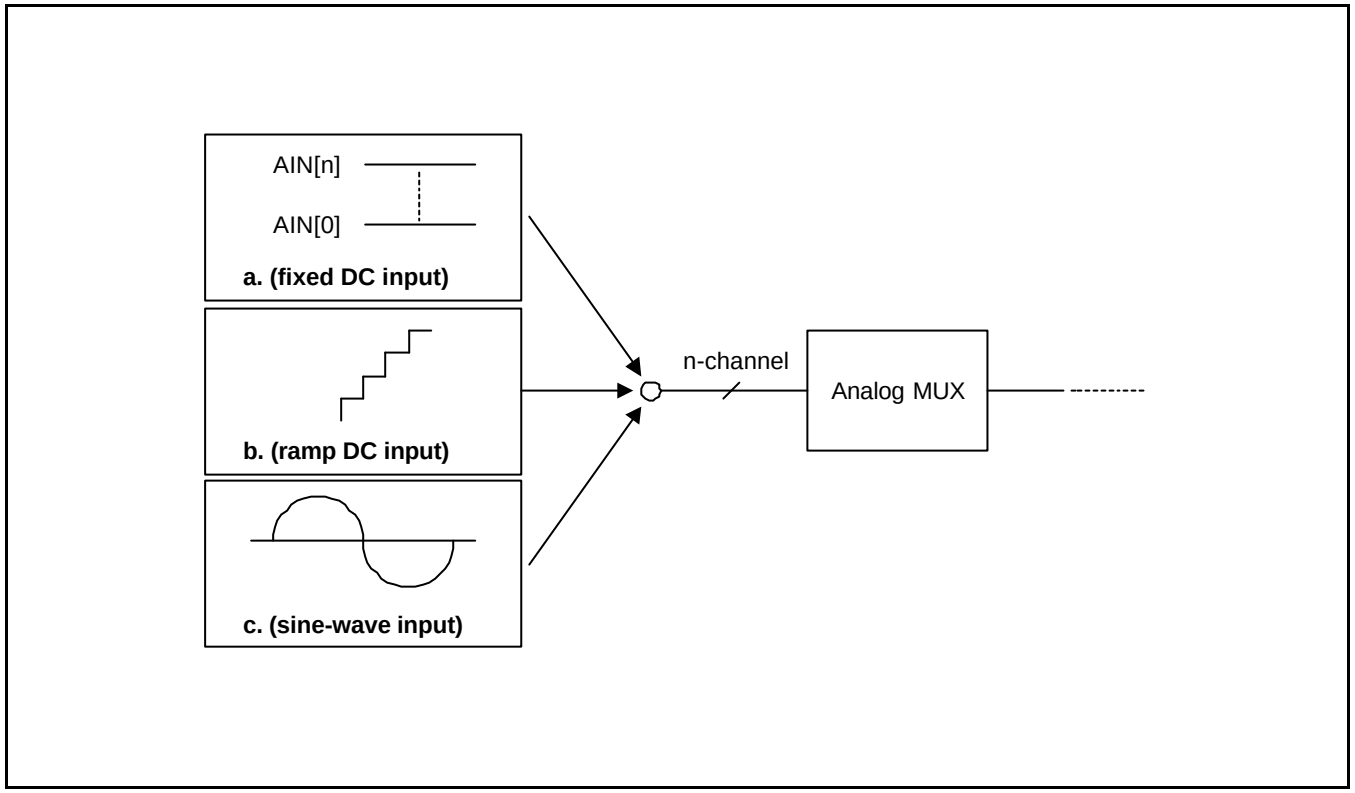
FEEDBACK REQUEST

It should be quite helpful to our ADC core development if you specify your system requirements on ADC in the following characteristic checking table and fill out the additional questions.
We appreciate your interest in our products. Thank you very much.

Characteristic	Min	Typ	Max	Unit	Remarks
Analog Power Supply Voltage				V	
Digital Power Supply Voltage				V	
Bit Resolution				Bit	
Reference Input Voltage				V	
Analog Input Voltage				V_{PP}	
Number of Analog Input Channel					
Operating Temperature				°C	
Integral Non-linearity Error				LSB	
Differential Non-linearity Error				LSB	
Bottom Offset Voltage Error				mV	
Top Offset Voltage Error				mV	
Conversion Rate				KSPS	
Conversion Time(ADEN~ADEN)				us	
Dynamic Supply Current				mA	
Power Dissipation				mW	
Power Dissipation at Power Down				uW	
Digital Output Format (Provide detailed description & timing diagram)					

FEEDBACK REQUEST-2

1. I want to know the detail of the analog input waveform. Which one is adequate for your analog input waveform among the a, b, and c below. If none of the three is adequate, please describe the analog input waveform to be used. If your analog input signal is sine-wave as c, please let me know what is your analog input signal's frequency and how many number of sampling points are required for 1-period?



2. Between single input-output and differential input-output configurations, which one is suitable for your system and why?
3. Please comment on the internal/external pin configurations and draw the timing diagram you want our ADC to have, if you have any reason to prefer some type of configuration.
4. Freely list those functions you want to be implemented in our ADC, if you have any.

HISTORY CARD

Version	Date	Modified Items	Comments
ver 1.0	00.6.30	Original version published (preliminary)	
ver 1.2	02.04.26	Add the phantom information (Final Version)	