GENERAL DESCRIPTION

The ADC1298X is a CMOS 10-bit low-voltage and high-speed A/D converter (ADC) for video and other applications. It has a four-step pipelined architecture, which consists of sample & hold amplifier, multiplying D/A converters (DACs), and subranging flash ADCs.
The maximum conversion rate of ADC1298X is 30MSPS and supply voltage is 3.3V single.

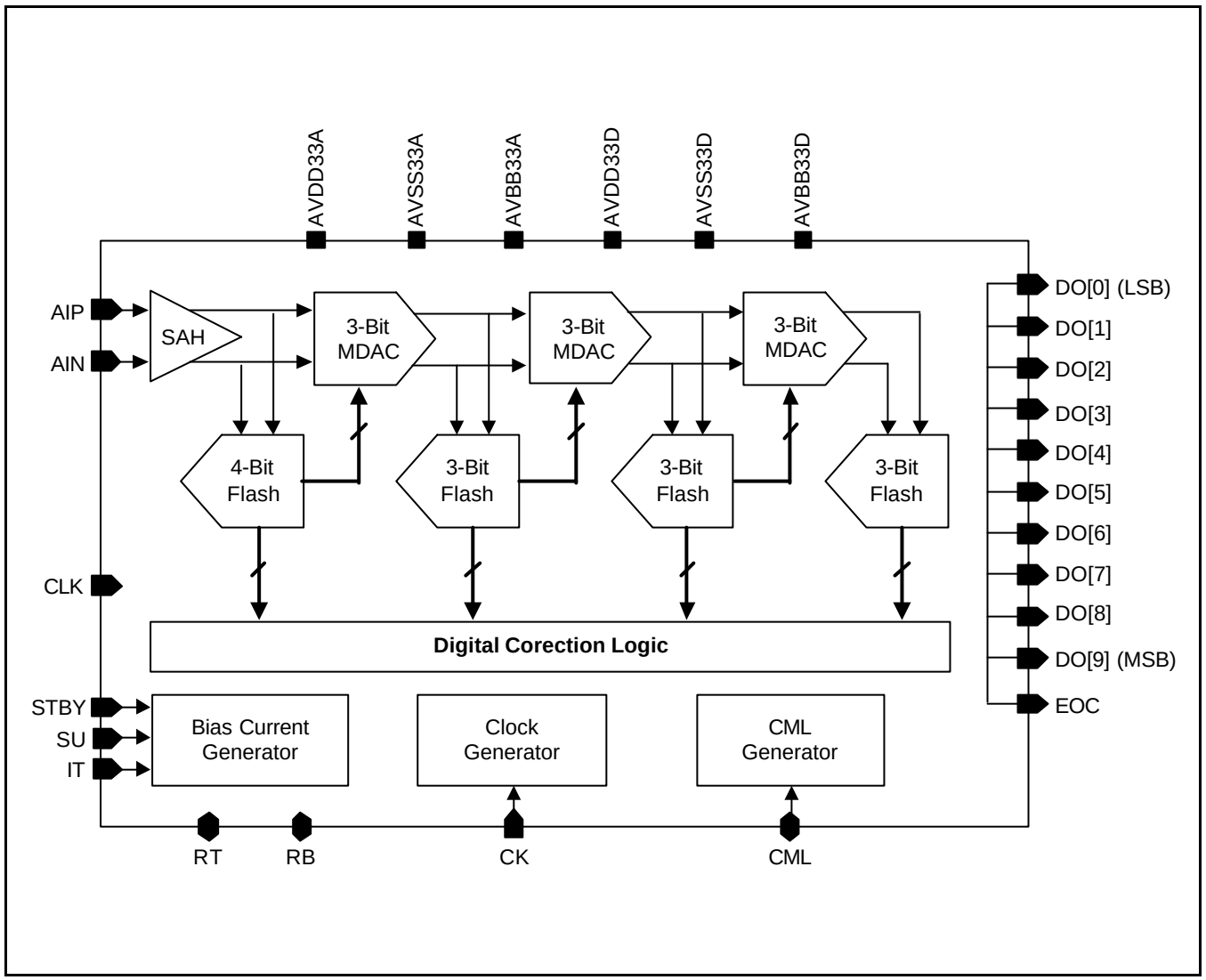
FEATURES

— Process : CMOS
— Resolution : 10-bit
— Maximum Conversion Rate : 30MSPS
— Power Supply : 3.3V Single
— Power Consumption : 60mW
— Differential Linearity Error : ± 1.0 LSB (Typ)
— Integral Linearity Error : ± 2.0 LSB (Typ)
— Internal Sample-and-Hold
— Operating Temperature Range : 0 °C – 70 °C

TYPICAL APPLICATIONS

— CCD imaging processors
  Camcorders, scanners, and security cameras.
— Read channel LSI
  HDD, DVD, and CD-ROM drives
— IF and baseband signal digitizers
— Portable equipments for low-power applications

FUNCTIONAL BLOCK DIAGRAM



Ver 1.1 (Apr. 2002)

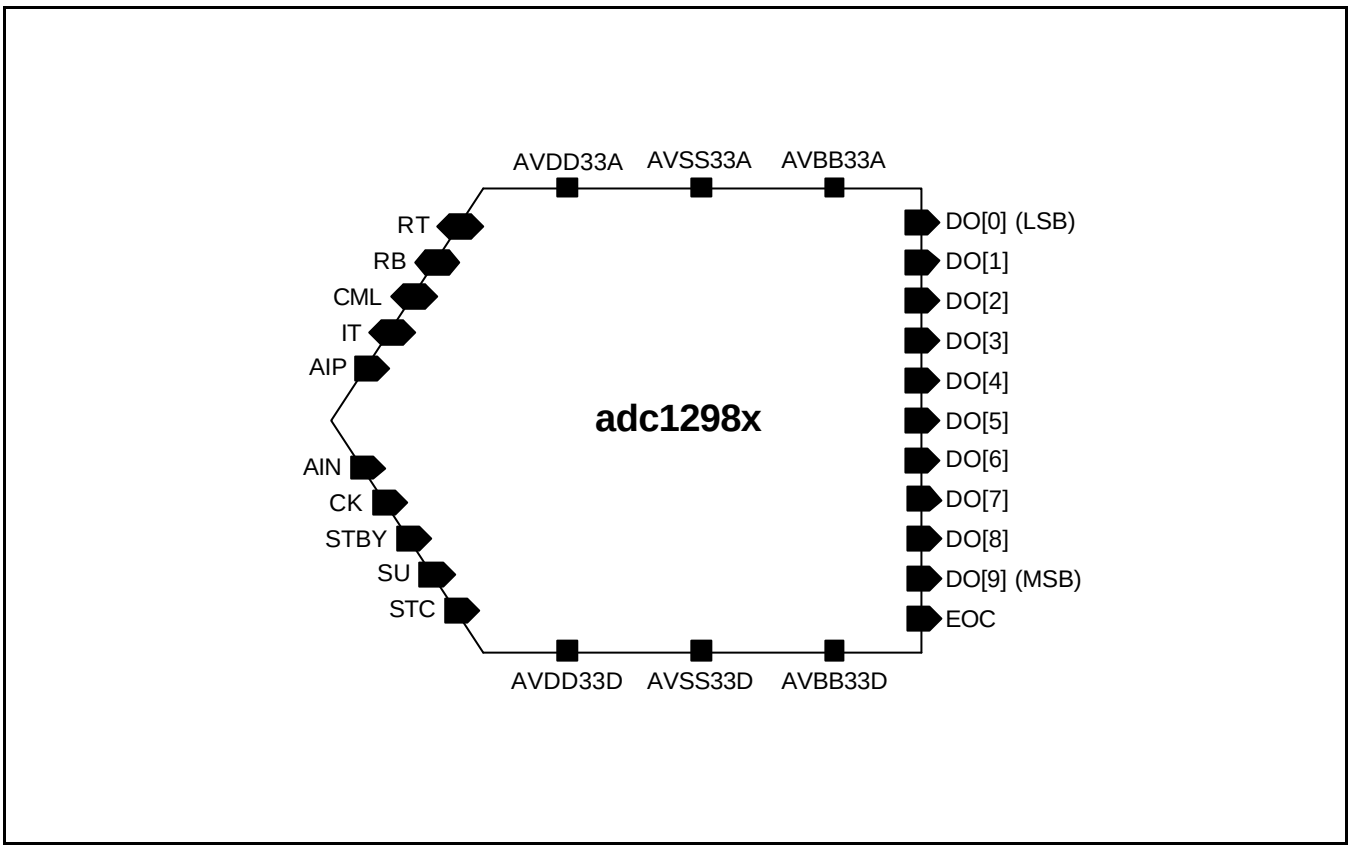
CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
AIP	AI	phiar50_abb	Analog Input (RB ~ RT)
AIN	AI	phiar50_abb	Analog Input (RT ~ RB)
STBY	DI	phicc_abb	STandBy (Active High)
SU	DI	phicc_abb	SpeedUp (Active High)
STC	DI	phicc_abb	STart of Conversion (Active High)
CK	DI	phicc_abb	Input Clock (30MHz)
DO[9:0]	DO	phob8_abb	Digital Output
EOC	DO	phob8_abb	End-Of-Conversion
RT	AB	phoa_abb	Reference Top Bias (+2.15V)
RB	AB	phoa_abb	Reference Bottom Bias (+1.15V)
CML	AB	phoa_abb	Common-Mode Level (+1.65V)
IT	AB	phiar50_abb	Bias Current Generator Test 100uA in Normal, 10uA in STBY mode
AVDD33A	AP	vdd3t_abb	Analog Power
AVSS33A	AG	vss3t_abb	Analog Ground
AVBB33A	AG	vbb3_abb	Analog Substrate Bias
AVDD33D	DP	vdd3t_abb	Digital Power
AVSS33D	DG	vss3t_abb	Digital Ground
AVBB33D	DG	vbb3_abb	Digital Substrate Bias

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bi-direction
— DB: Digital Bi-direction
— AP: Analog Power
— AG: Analog Ground
— DP: Digital Power
— DG: Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	AVDD33A AVDD33D	-0.3 to 4.5	V
Analog Input Voltage	AIP / AIN	-0.3 to AVDD33A+0.3	V
Digital Input Voltage	CK	-0.3 to AVDD33D+0.3	V
Digital Output Voltage	$V_{OH, VOL}$	-0.3 to AVDD33D+0.3	V
Storage Temperature Range	T_{stg}	-45 to 125	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to AVSS33A/AVSS33D unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model).

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	AVDD33A - AVSS33A AVDD33D - AVSS33D	3.15	3.3	3.45	V
Supply Voltage Difference	AVDD33A - AVDD33D	-0.1	0.0	0.1	V
Reference Input Voltage	RT RB	– AVSS33A	2.15 1.15	AVDD33A –	V
Analog Input Voltage	AIP/AIN	RB	–	RT	V
Clock High Time Clock Low Time	T_{pwh} T_{pwl}	– –	16.6 16.6	– –	ns
Digital Input 'L' Voltage Digital Input 'H' Voltage	V_{IL} V_{IH}	– 3.0	– –	0.3 –	V
Operating Temperature	T_{opr}	0	–	70	°C

NOTE: It is strongly recommended that all the supply pins (AVDD33A, AVDD33D) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Conditions
Resolution	–	–	10	–	Bits	
Differential Linearity Error	DLE	–	–	±1.0	LSB	AIP/AIN : RB – RT (Ramp Input)
Integral Linearity Error	ILE	–	–	±2.0	LSB	F_S : 1MHz 2MHz
Reference Current	IREF	–	1.25	2	mA	1.0V/800Ω = 1.25mA
Bottom Offset Voltage Error	EOB	–	–	±10	LSB	EOB = AI(0, 1) - (RB-RT)
Top Offset Voltage Error	EOT	–	–	±10	LSB	EOT = (RT-RB) - AI(1022, 1023)

NOTES:

1. Converter Specifications (unless otherwise specified)
   AVDD33A=3.3V AVDD33D=3.3V
   AVSS33A=GND AVSS33D=GND
   RT=2.15V RB=1.15V
   STBY=LOW STC=HIGH SU=LOW
   Ta = 25°C
2. AI(D1, D2) denotes the net voltage difference between AIP and AIN at the instant when of which the counterpart Digital Output code transits from D1 to D2.

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Conditions
Clock High Time	T_{pwh}	–	16.6	–	ns	–
Clock Low Time	T_{pwl}	–	16.6	–	ns	
Conversion Rate	F_S	30	–	–	MSPS	
Dynamic Supply Current	I_S	–	18	25	mA	I_S = (IREF) + I(AVDD33A) + I(AVDD33D) F_S : 30MHz
Analog Input Range	V_{IN}	AVSS	2.0	AVDD	V_{PP}	SNDR varies according to V_{IN}
Analog Input Capacitance	C_{IN}	–	10	–	pF	–
Analog Input Bandwidth	F_{IN}	–	1	6	MHz	–
Digital Output Data Delay	t_D	–	10	–	ns	See "DELAY TIMING DIAGRAM"
Signal to Noise Distortion Ratio (SNDR)	SNDR1 SNDR2 SNDR3	–	48	–	dB	AIN : 1, 2, 4MHz respectively (Sine Input) FS : 30MHz

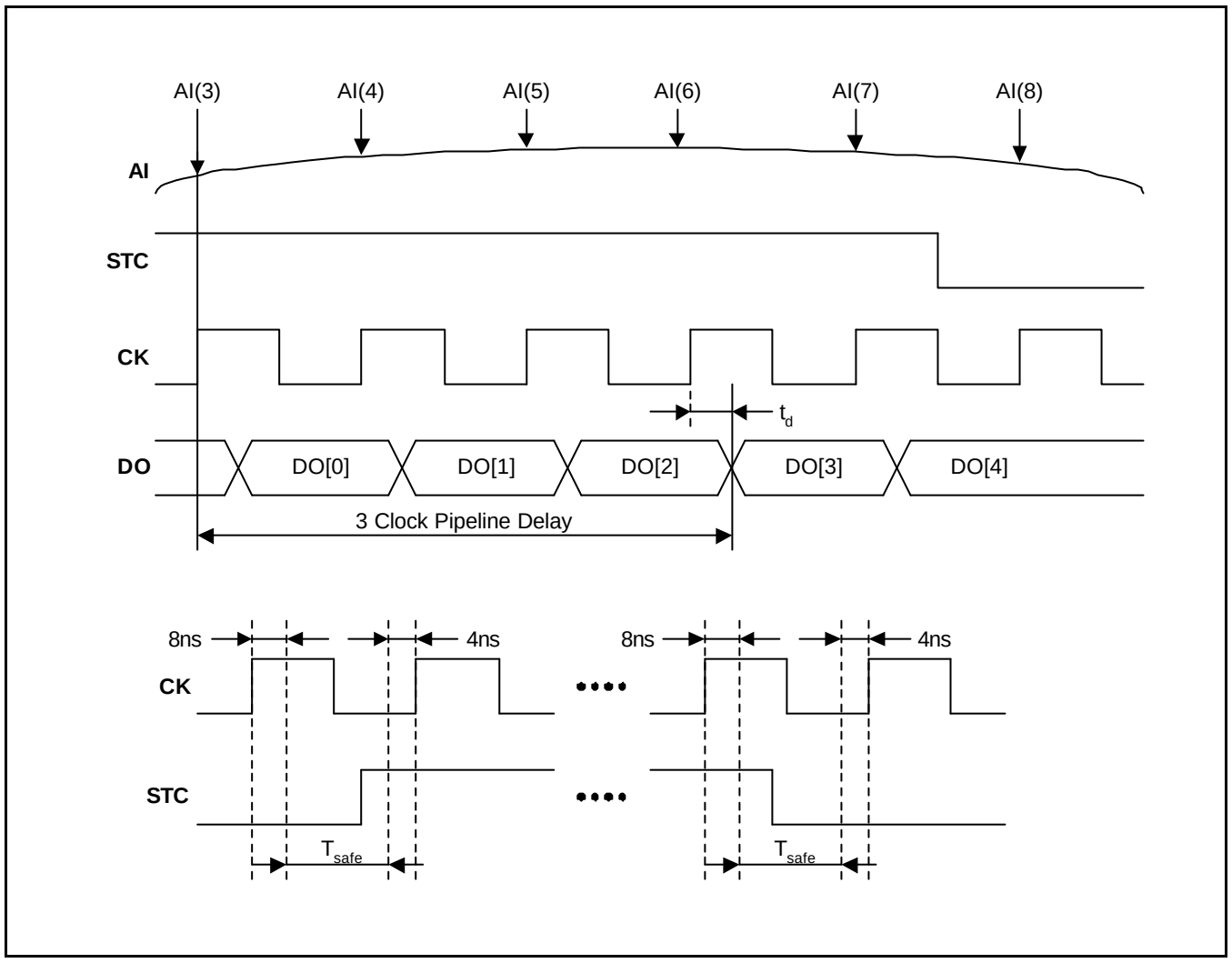
OUTPUT MAPPING TABLE

Index	AIP (V)	AIN (V)	Digital Output
0	1.15 ~ 1.15+1× LSB_D	2.15-1×LSB_D~ 2.15	0000000000
1	1.15+1×LSB_D~1.15+2×LSB_D	2.15-2×LSB_D~ 2.15-1×LSB_D	0000000001
2	1.15+2×LSB_D ~1.15+3×LSB_D	2.15-3×LSB_D~ 2.15-2×LSB_D	0000000010
• • •	• • •	• • •	• • •
511	1.15+511×LSB_D~1.15+512×LSB_D	2.15-512×LSB_D~ 2.15-511×LSB_D	0111111111
512	1.15+512×LSB_D ~1.15+513×LSB_D	2.15-513×LSB_D~ 2.15-512×LSB_D	1000000000
513	1.15+513×LSB_D ~1.15+514×LSB_D	2.15-514×LSB_D~ 2.15-513×LSB_D	1000000001
• • •	• • •	• • •	• • •
1021	1.15+1021×LSB_D ~1.15+1022×LSB_D	2.15-1022×LSB_D~2.15-1021×LSB_D	1111111101
1022	1.15+1022×LSB_D ~1.15+1023×LSB_D	2.15-1023×LSB_D~2.15-1022×LSB_D	1111111110
1023	1.15+1023×LSB_D ~ 2.15	1.25 ~ 2.15-1023×LSB_D	1111111111

NOTES:

1. For Differential Input
   .AIP = RB ~ RT
   .AIN = RT ~ RB
   .1×LSB_D = (RT - RB)/1024 = 0.9765mV
   and for Single Input
   .AIP = (RT + RB)/2 - (RT - RB) ~ (RT + RB)/2 + (RT - RB)
   .AIN = (RT + RB)/2
   .1×LSB_S = 2×(RT - RB)/1024 = 1.9530mV

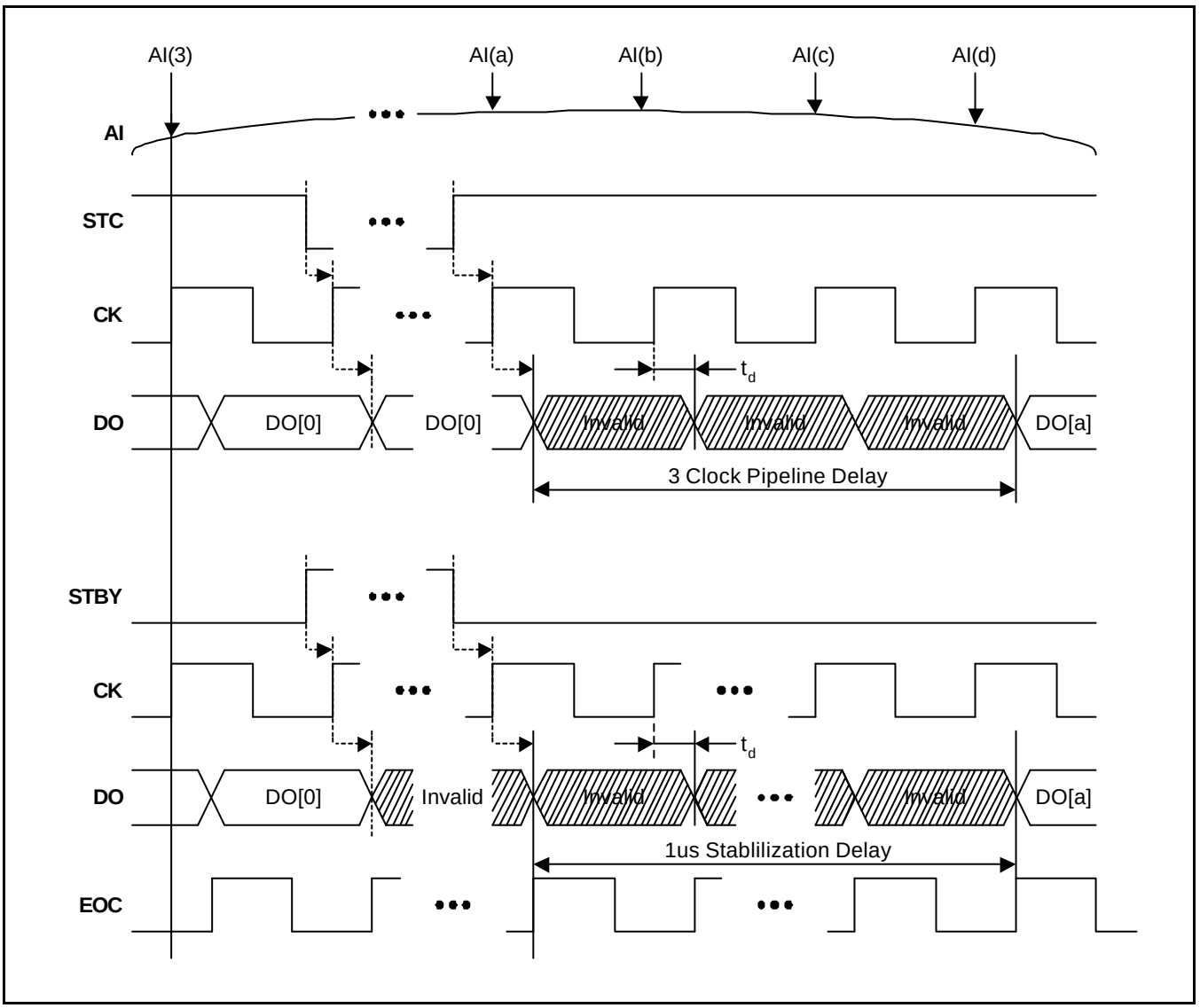
DELAY TIMING DIAGRAM



NOTES:

1. Digital Output Code, DO[9:0], is renewed only when STC (STart-Of-Conversion) is 'HIGH' and the last code during the STC is 'HIGH' will be kept otherwise.
2. During STC is 'HIGH', ADC1298X generates EOC (End-Of-Conversion) and DO[9:0] with the pipeline delay of 3 clock periods from the instant that the counterpart analog input was sampled.
3. The state transition of STC to 'LOW' will be immediately reflected to DO[9:0] and EOC, while the transition to 'HIGH' requires the same delay as the pipeline delay to ensure the validity of DO[9:0] and EOC.
4. The signal transition of STC is valid only in the Tsafe region, so the setup-hold timing constraints must be carefully taken into consideration on STC generation.
5. Because EOC is generated by STC regardless of the state of STBY, EOC will be toggled normally in spite of STBY 'HIGH' if only STC is 'HIGH'. Do not refer to the EOC while STBY is 'HIGH', because it is invalid in actual although it is toggled normaly with STC 'HIGH'.

DELAY TIMING DIAGRAM



NOTES:

1. When STBY goes 'HIGH', the internal circuitry remains active but not operates properly because the current supplied to each internal block is reduced. So although the digital output DO[9:0] seems to be generated normally, it is totally invalid while STBY remains 'HIGH'.
2. When STBY returns to 'LOW', it takes about 1us stabilization time for internal circuitry to stabilize itself and begin to generate vaild outputs. If the current were forced to be zero with STBY 'HIGH', it would take quite longer time than the case we had it small but not zero. That is why we leave some amount of current in low-current mode rather than cutting the current off, and why we call this control signal as 'STBY (STand-BY)' rather than 'PD (Power-Down)'.

FUNCTIONAL DESCRIPTION

1. ADC1298X is a four-stage pipelined A/D Converter comprising a sample-and-hold, two multiflying DAC (MDAC) and four flash ADC each of which yields 4, 3, 3 and 3 bits. The N-bit flash ADC is composed of 2^n latching comparators, and multiplying DAC is composed of N+2 capacitors and a fully-differential amplifier.
2. ADC1298X operates as follows. During the first "Low" cycle of the external clock the analog input data is tracked by the sample-and-holder and sampled at the rising edge of the clock to be converted. The sampled data is fed to the first MDAC and first 4-bit flash ADC which produce 4-bit digital output code corresponding to the sampled analog data. The first MDAC reconstructs the analog voltage corresponding to the first 4-bit flash ADC's digital output, and amplifies, by the gain of 2^3, the residue voltage which is the voltage difference between the recunstructed voltage and the input voltage of the first MDAC. The 3-bit flash ADC, and MDAC of second to fourth stage operate as the same manner with the first stage but that finally these blocks produce 3-bit digital output codes and amplify a residue voltage by a gain of 2^2. The respective digital output codes from each of the flash ADCs are fed to the Digital Correction Logic (DCL) to correct the inter-stage conversion error.
3. ADC1298X has the error correction scheme, which handles the offset error which stems from the mismatch between the first, second, third and fourth flash ADC's comparator.

BLOCK DESCRIPTION

1. SAH

SAH (sample-and-hold) is the circuit which samples the analog input signal and holds the sampled value until the next sampling instant. It is required that the difference between the real analog input signal and the sampled output signal of SAH be as small as it can be to guarantee fidelity of the following 10-bit data conversion process. This SAH consists of fully differential op-amp, switching transistors, and sampling capacitors. The sampling clocks are non-overlapping (Q1, Q2) and sampling capacitance is 1.0pF. SAH uses its own bias circuit to avoid interference from any other blocks and SAH amp is designed to have open-loop dc gain higher than 80dB and phase margin higher than 60 degree. Its input block is designed to be the rail-to-rail architecture using complementary differential pair.

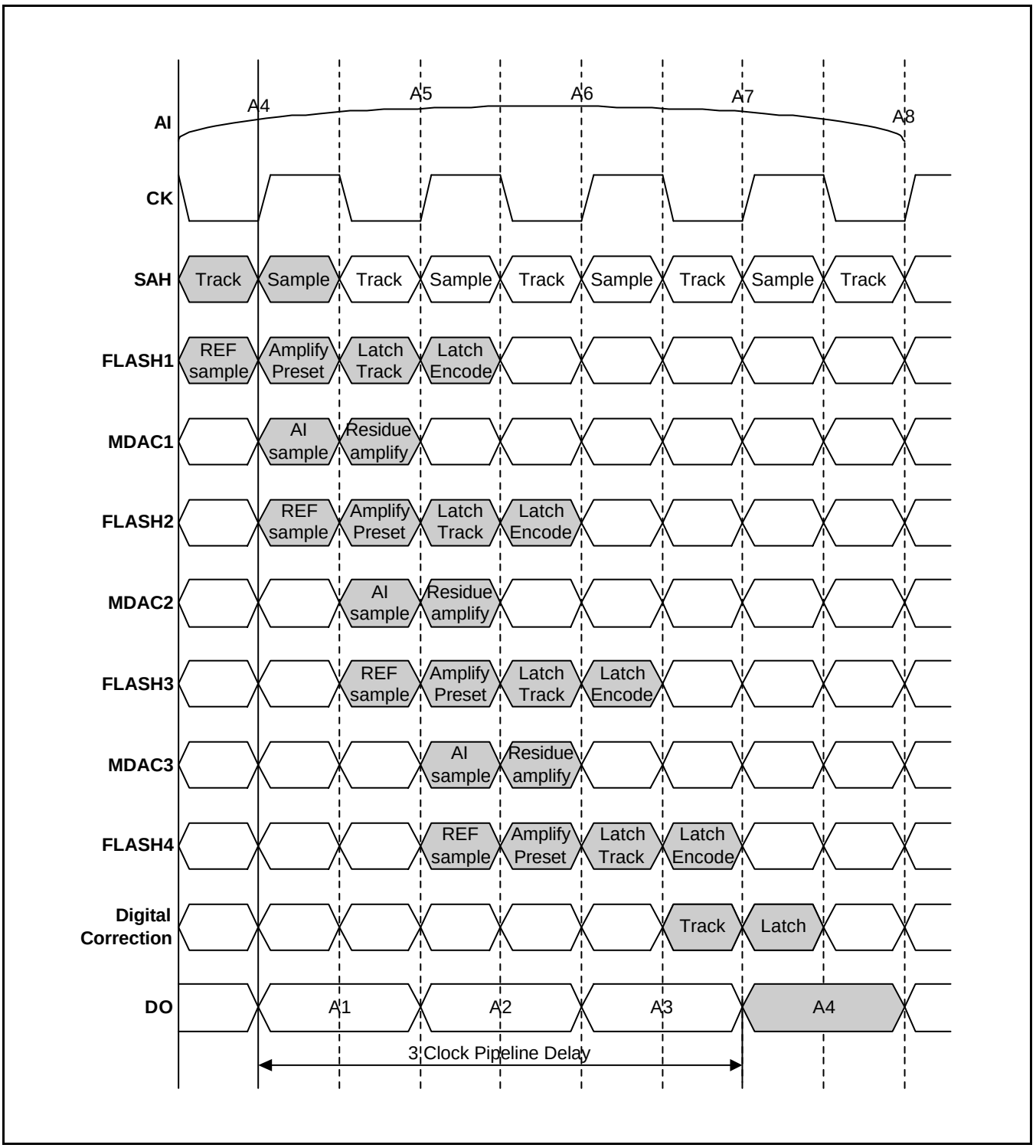
2. FLASH

The flash converter compares analog input signal with reference voltages, and the result are transferred to MDAC and digital correction logic block. The comparators inside have a fully differential structure.

3. MDAC

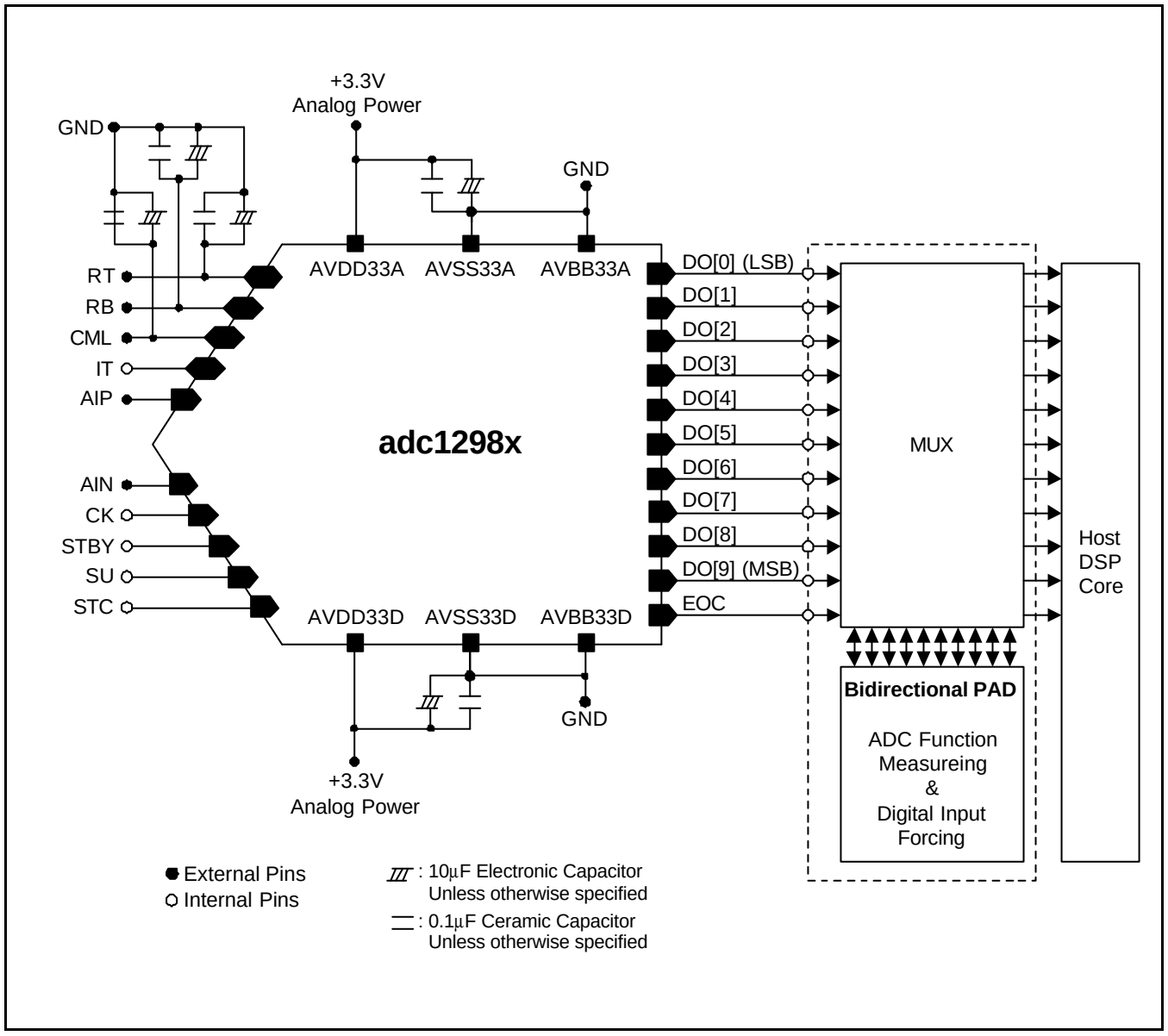
MDAC is the most important block next to SAH and it governs the overall performances of ADC as SAH does. MDAC consists of amp, selection logic and capacitor array. Capacitor array is made up of the sampling capacitors and switches to implement D/A conversion process and predefined gain.

TIMING DIAGRAM



CORE EVALUATION GUIDE

— ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.



USER GUIDE

1. Input Signal Range following Signal Mode

The differential mode input signal is recommend to allow wider dynamic input range and to enhance noise immunity of internal sample-and-holder, although ADC1298X is designed to be able to adopt both the single and the differential mode input.

< Differential Mode Input Range >

Pin	Input Range	Conditions
AIP	RB ~ RT	–
AIN	RT ~ RB	180º phase shifted with respect to AIP

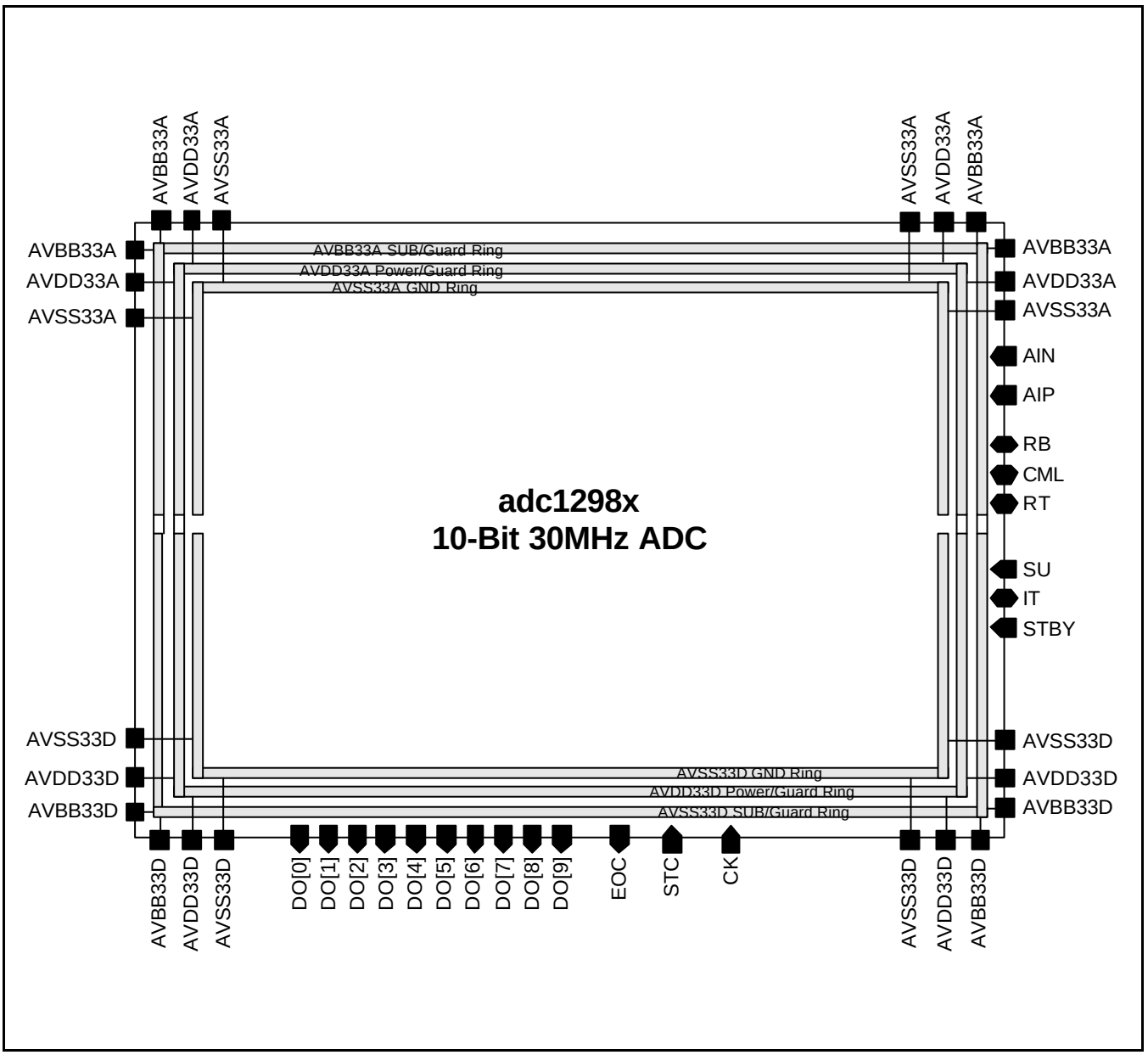
< Single Mode Input Range >

Pin	Input Range	Conditions
AIP	(RT+RB)/2-(RT-RB) ~ (RT+RB)/2+(RT-RB)	–
AIN	(RT + RB)/2	Tied to Clean DC Source (Recommended) Or Internal CML can be used by connecting AIN to CML

2. Input Signal Speed

Normal Input Bandwidth of ADC1298X is in range of 1 ~ 6MHz, which is targeted to the frequency content of the signals in normal video systems. If it is necessary to have the bandwidth of the input signal to ADC1298X near or over nyquist frequency (15MHz, half the clock frequency) to use ADC1298X for the application signals of which to feed to ADC1298X can have signal frequencies higher than 6MHz, contact SEC for the guide on additional performance issues.

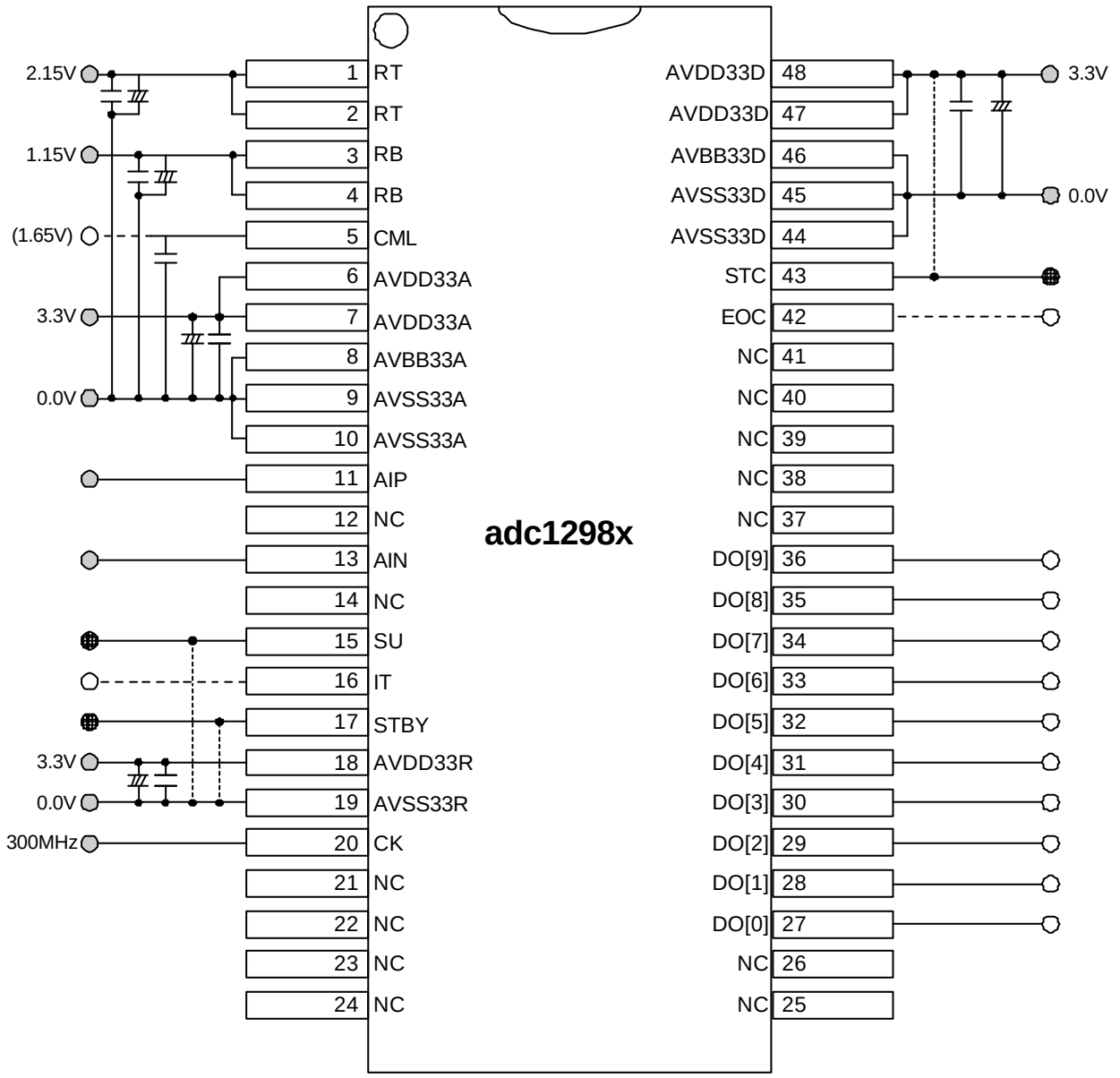
PHANTOM CELL INFORMATION



LAYOUT GUIDE

Port Name	I/O Type	I/O Pad	Layout Guide [Priority]
AIP	AI	phiar50_abb	. Keep the Paths to PADs as Short as Possible. [1] . Overlaps by other Signal Lines, especially by Digital Signal Lines, are not allowed (strong requirement). [1] . Put as many Contacts/Vias as Possible on Contact Area, if Metal Layers are Switched. [-]
AIN	AI	phiar50_abb	. Put as many Contacts/Vias as Possible on Contact Area, if Metal Layers are Switched. [-] . Shield, if Possible. [7]
STBY	DI	phicc_abb	. Keep it from Crossing Analog Signal Line, if possible. [5]
SU	DI	phicc_abb	. Keep it from Crossing Analog Signal Line, if possible. [X]
STC	DI	phicc_abb	. Keep it from Crossing Analog Signal Line, if possible. [X]
CK	DI	phicc_abb	. Keep it from Crossing any Analog Signal Line. (strong requirement) [2]
DO[9:0]	DO	phob8_abb	. Keep it from Crossing Analog Signal Lines, if possible. [4] . Make it not to Run over 1,000um. [6]
EOC	DO	phob8_abb	. Keep it from Crossing any Analog Signal Line. (strong requirement) [2] . Make it not to Run over 1,000um. [6]
RT	AB	phoa_abb	. Keep the Paths to PADs as Short as Possible. [1] . Overlaps by other Signal Lines, especially by Digital Signal Lines, are not allowed. (strong requirement) [1]
RB	AB	phoa_abb	. Put as many Contacts/Vias as Possible on Contact Area, if Metal Layers are Switched. [-]
CML	AB	phoa_abb	. Shield, if Possible. [7]
IT	AB	phiar50_abb	. Leave it Float.
AVDD33A	AP	vdd3t_abb	. Overlaps by Digital Signal Lines are not allowed. (strong requirement) [4] . Keep the Paths to PADs as Short as Possible. [3]
AVSS33A	AG	vss3t_abb	. Put as many Contacts/Vias as Possible on Contact Area, if Metal Layers are Switched. [-]
AVBB33A	AG	vbb3_abb	. Ports exist on 3 sides of Core and internally connected to each other by the power ring. Connect PAD to the Port which is most convenient to Route interconnecting Line. [-]
AVDD33D	DP	vdd3t_abb	. Overlaps by Analog Signal Lines are not allowed. (strong requirement) [2] . Keep the Paths to PADs as Short as Possible. [4]
AVSS33D	DG	vss3t_abb	. Put as many Contacts/Vias as Possible on Contact Area, if Metal Layers are Switched. [-]
AVBB33D	DG	vbb3_abb	. Ports exist on 3 sides of Core and internally connected to each other by the power ring. Connect PAD to the Port which is most convenient to Route interconnecting Line. [-]
. Keep the Phantom Port Width to PAD or Other Core.			

PACKAGE CONFIGURATION



: Actual Input/Output Pin
: Control Input Pin
: Eliminable Input/Output Pin
------- : Default Setting for Control Input Pin