National Semiconductor

ADC12D1800 PRODUCT BRIEF

PRELIMINARY
May 18, 2010

12-Bit, Single 3.6 GSPS ADC

1.0 General Description

The 12-bit, 3.6 GSPS ADC12D1800 is the latest advance in National's Ultra-High-Speed ADC family and builds upon the features, architecture and functionality of the 10-bit GHz family of ADCs.

The ADC12D1800 provides a flexible LVDS interface which has multiple SPI programmable options to facilitate board design and FPGA/ASIC data capture. The LVDS outputs are compatible with IEEE 1596.3-1996 and supports programmable common mode voltage.

The product is packaged in a leaded or lead-free 292-ball thermally enhanced BGA package over the rated industrial temperature range of -40°C to +85°C.

Notice: This document is not a full datasheet. For more information regarding this product or to order samples please contact your local National Semiconductor sales office or visit http://www.national.com/support/dir.html

2.0 Applications

- Wideband Communications
- Data Acquisition Systems
- RADAR/LIDAR
- Set-top Box
- Consumer RF
- Software Defined Radio

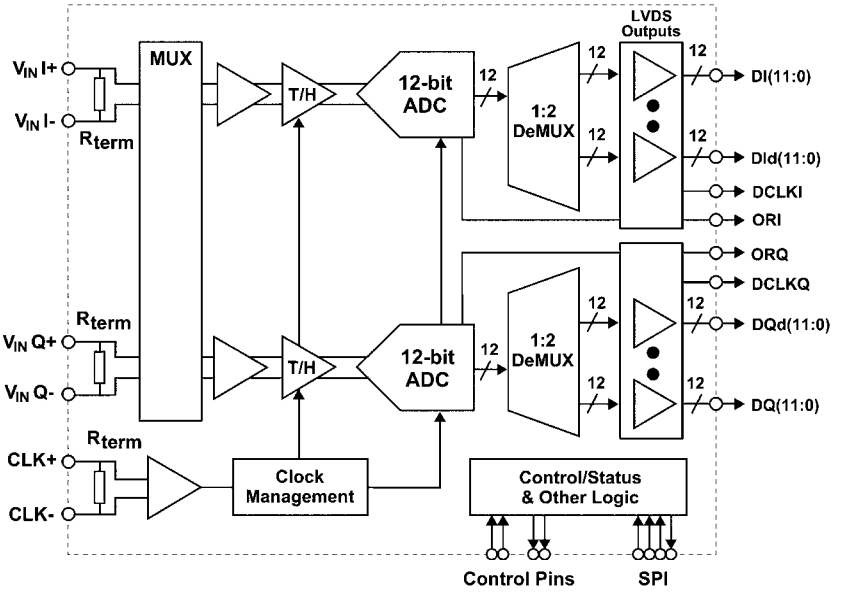
3.0 Features

- Configurable to either 3.6 GSPS interleaved or 1.8 GSPS dual ADC
- Pin-compatible with ADC10D1000/1500 and ADC12D1000/1600
- Internally terminated, buffered, differential analog inputs
- Interleaved timing automatic and manual skew adjust
- Test patterns at output for system debug
- Programmable 15-bit gain and 12-bit plus sign offset
- Programmable t_{AD} adjust feature
- 1:1 non-demuxed or 1:2 demuxed LVDS outputs
- AutoSync feature for multi-chip systems
- Single power supply

4.0 Key Specifications

■ Resolution	12 Bits
Interleaved 3.6 GSPS ADC	
■ Noise Floor	-147 dBm/Hz (typ)
■ IMD3	-61 dBFS (typ)
■ Noise Power Ratio	52 dB (typ)
■ Power	4.1W (typ)
■ Full Power Bandwidth	2.15 GHz (typ)
Dual 1.8 GSPS ADC, Fin = 125MHz	
■ ENOB	9.2 (typ)
■ SNR	57.8 dB (typ)
■ SFDR	67 dBc (typ)
■ Power	4.1W (typ)
■ Full Power Bandwidth	2.8 GHz (typ)

5.0 Block Diagram



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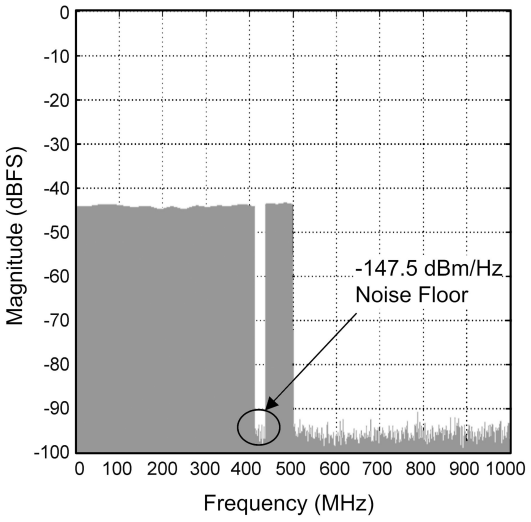
6.0 Wideband Performance



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7.0 Ordering Information

Industrial Temperature Range (-40°C < T_A < +85°C)	NS Package
ADC12D1800CIUT/NOPB	Lead-free 292-Ball BGA Thermally Enhanced Package
ADC12D1800CIUT	Leaded 292-Ball BGA Thermally Enhanced Package
ADC12D1800RB	Reference Board

If Military/Aerospace specified devices are required, please contract the National Semiconductor Sales Office/Distributors for availability and specifications. IBIS models are available at: http://www.national.com/analog/adc/ibis_models.

8.0 Connection Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	V_A	SDO	TPM	NDM	V_A	GND	V_E	GND_E	DId0+	V_DR	DId3+	GND_DR	DId6+	V_DR	DId9+	GND_DR	DId11+	DId11-	GND_DR	A
B	Vbg	GND	ECEb	SDI	CalRun	V_A	GND	GND_E	V_E	DId0-	DId2+	DId3-	DId5+	DId6-	DId8+	DId9-	DId10+	DI0+	DI1+	DI1-	B
C	Rtrim+	Vcmo	Rext+	SCSb	SCLK	V_A	NC	V_E	GND_E	DId1+	DId2-	DId4+	DId5-	DId7+	DId8-	DId10-	DI0-	V_DR	DI2+	DI2-	C
D	DNC	Rtrim-	Rext-	GND	GND	CAL	DNC	V_A	V_A	DId1-	V_DR	DId4-	GND_DR	DId7-	V_DR	GND_DR	V_DR	DI3+	DI4+	DI4-	D
E	V_A	Tdiode+	DNC	GND													GND_DR	DI3-	DI5+	DI5-	E
F	V_A	GND_TC	Tdiode-	DNC													GND_DR	DI6+	DI6-	GND_DR	F
G	V_TC	GND_TC	V_TC	V_TC													DI7+	DI7-	DI8+	DI8-	G
H	VinI+	V_TC	GND_TC	V_A				GND	GND	GND	GND	GND	GND				DI9+	DI9-	DI10+	DI10-	H
J	VinI-	GND_TC	V_TC	VbiasI				GND	GND	GND	GND	GND	GND				V_DR	DI11+	DI11-	V_DR	J
K	GND	VbiasI	V_TC	GND_TC				GND	GND	GND	GND	GND	GND				ORI+	ORI-	DCLKI+	DCLKI-	K
L	GND	VbiasQ	V_TC	GND_TC				GND	GND	GND	GND	GND	GND				ORQ+	ORQ-	DCLKQ+	DCLKQ-	L
M	VinQ-	GND_TC	V_TC	VbiasQ				GND	GND	GND	GND	GND	GND				GND_DR	DQ11+	DQ11-	GND_DR	M
N	VinQ+	V_TC	GND_TC	V_A				GND	GND	GND	GND	GND	GND				DQ9+	DQ9-	DQ10+	DQ10-	N
P	V_TC	GND_TC	V_TC	V_TC													DQ7+	DQ7-	DQ8+	DQ8-	P
R	V_A	GND_TC	V_TC	V_TC													V_DR	DQ6+	DQ6-	V_DR	R
T	V_A	GND_TC	GND_TC	GND													V_DR	DQ3-	DQ5+	DQ5-	T
U	GND_TC	CLK+	PDI	GND	GND	RCOut1-	DNC	V_A	V_A	DQd1-	V_DR	DQd4-	GND_DR	DQd7-	V_DR	V_DR	GND_DR	DQ3+	DQ4+	DQ4-	U
V	CLK-	DCLK _RST+	PDQ	CalDly	DES	RCOut2+	RCOut2-	V_E	GND_E	DQd1+	DQd2-	DQd4+	DQd5-	DQd7+	DQd8-	DQd10-	DQ0-	GND_DR	DQ2+	DQ2-	V
W	DCLK _RST-	GND	DNC	DDRPh	RCLK-	V_A	GND	GND_E	V_E	DQd0-	DQd2+	DQd3-	DQd5+	DQd6-	DQd8+	DQd9-	DQd10+	DQ0+	DQ1+	DQ1-	W
Y	GND	V_A	FSR	RCLK+	RCOut1+	V_A	GND	V_E	GND_E	DQd0+	V_DR	DQd3+	GND_DR	DQd6+	V_DR	DQd9+	GND_DR	DQd11+	DQd11-	GND_DR	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

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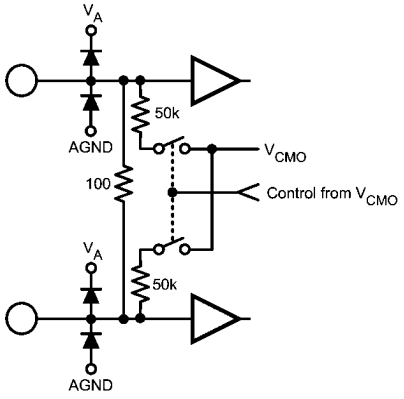
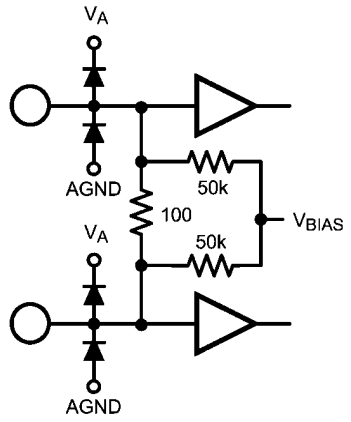
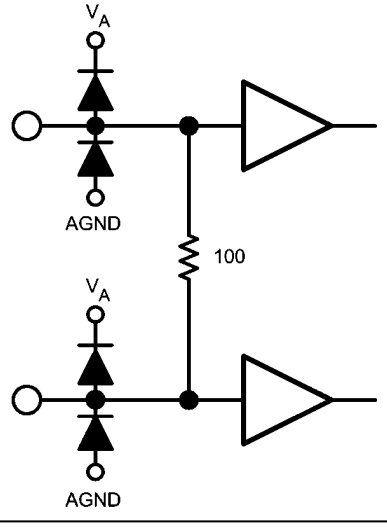
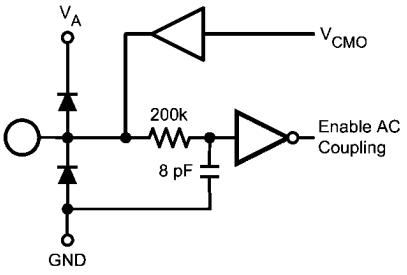
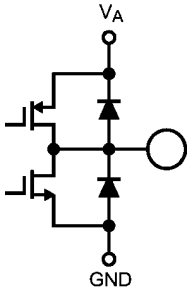
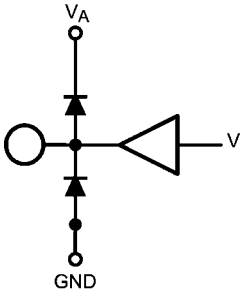
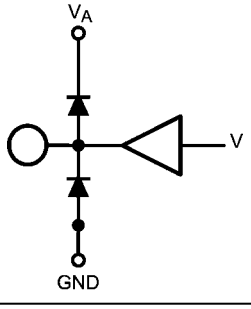
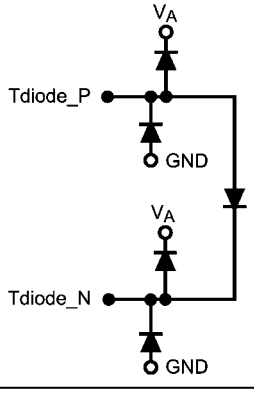
FIGURE 1. ADC12D1800 Connection Diagram

The center ground pins are for thermal dissipation and must be soldered to a ground plane to ensure rated performance.

9.0 Ball Descriptions and Equivalent Circuits

TABLE 1. Analog Front-End and Clock Balls

Ball No.	Name	Equivalent Circuit	Description
H1/J1 N1/M1	VinI+/- VinQ+/-		Differential signal I- and Q-inputs. In the Non-Dual Edge Sampling (Non-DES) Mode, each I- and Q-input is sampled and converted by its respective channel with each positive transition of the CLK input. In Non-ECM (Non-Extended Control Mode) and DES Mode, both channels sample the I-input. In Extended Control Mode (ECM), the Q-input may optionally be selected for conversion in DES Mode by the DEQ Bit (Addr: 0**h**, Bit 6). Each I- and Q-channel input has an internal common mode bias that is disabled when DC-coupled Mode is selected. Both inputs must be either AC- or DC-coupled. The coupling mode is selected by the V_{CMO} Pin. In Non-ECM, the full-scale range of these inputs is determined by the FSR Pin; both I- and Q-channels have the same full-scale input range. In ECM, the full-scale input range of the I- and Q-channel inputs may be independently set via the Control Register (Addr: 3**h** and Addr: B**h**). Note that the high and low full-scale input range setting in Non-ECM corresponds to the mid and minimum full-scale input range in ECM. The input offset may also be adjusted in ECM.
U2/V1	CLK+/-		Differential Converter Sampling Clock. In the Non-DES Mode, the analog inputs are sampled on the positive transitions of this clock signal. In the DES Mode, the selected input is sampled on both transitions of this clock. This clock must be AC-coupled.
V2/W1	DCLK_RST+/-		Differential DCLK Reset. A positive pulse on this input is used to reset the DCLKI and DCLKQ outputs of two or more ADC12D1800s in order to synchronize them with other ADC12D1800s in the system. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized. The pulse applied here must meet timing relationships with respect to the CLK input. Although supported, this feature has been superseded by AutoSync.

Ball No.	Name	Equivalent Circuit	Description
C2	V_{CMO}		Common Mode Voltage Output or Signal Coupling Select. If AC-coupled operation at the analog inputs is desired, this pin should be held at logic-low level. This pin is capable of sourcing/ sinking up to 100 µA. For DC-coupled operation, this pin should be left floating or terminated into high-impedance. In DC-coupled Mode, this pin provides an output voltage which is the optimal common-mode voltage for the input signal and should be used to set the common-mode voltage of the driving buffer.
B1	V_{BG}		Bandgap Voltage Output or LVDS Common-mode Voltage Select. This pin provides a buffered version of the bandgap output voltage and is capable of sourcing/sinking 100 uA and driving a load of up to 80 pF. Alternately, this pin may be used to select the LVDS digital output common-mode voltage. If tied to logic-high, the 1.2V LVDS common-mode voltage is selected; 0.8V is the default.
C3/D3	Rext+/-		External Reference Resistor terminals. A 3.3 kΩ ±0.1% resistor should be connected between Rext+/-. The Rext resistor is used as a reference to trim internal circuits which affect the linearity of the converter; the value and precision of this resistor should not be compromised.
C1/D2	Rtrim+/-		Input Termination Trim Resistor terminals. A 3.3 kΩ ±0.1% resistor should be connected between Rtrim+/-. The Rtrim resistor is used to establish the calibrated 100Ω input impedance of VinI, VinQ and CLK. These impedances may be fine tuned by varying the value of the resistor by a corresponding percentage; however, the tuning range and performance is not guaranteed for such an alternate value.
E2/F3	Tdiode+/-		Temperature Sensor Diode Positive (Anode) and Negative (Cathode) Terminals. This set of pins is used for die temperature measurements. It has not been fully characterized.

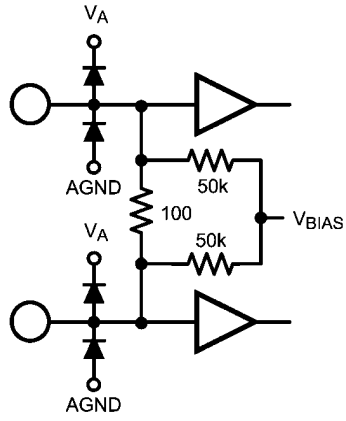
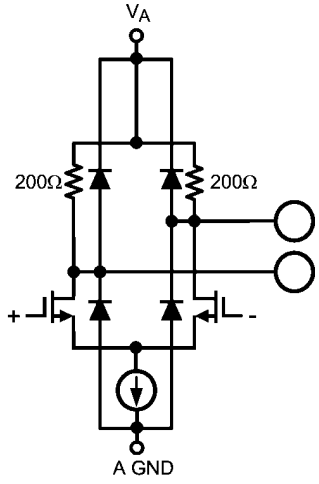
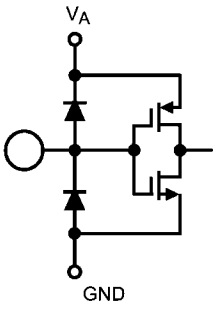
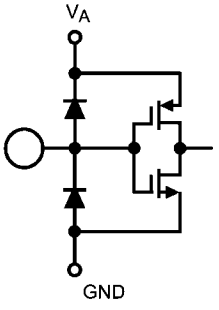
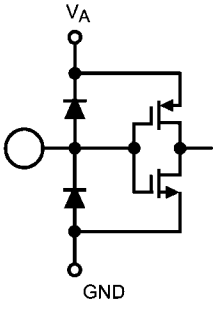
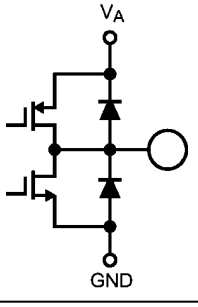
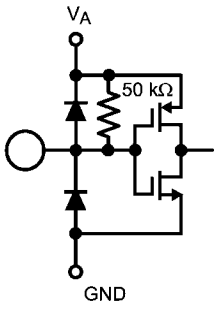
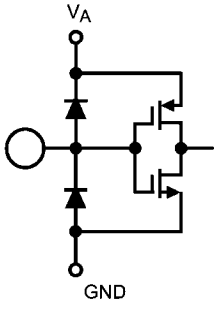
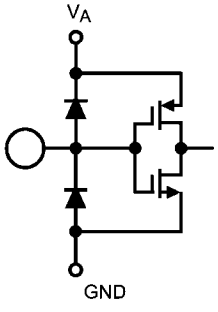
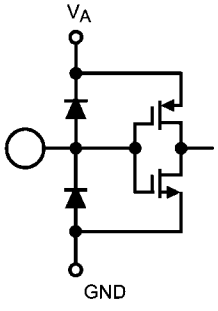
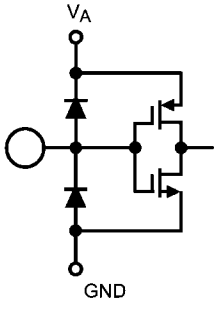
Ball No.	Name	Equivalent Circuit	Description
Y4/W5	RCLK+/-		Reference Clock Input. When the AutoSync feature is active, and the ADC12D1800 is in Slave Mode, the internal divided clocks are synchronized with respect to this input clock. The delay on this clock may be adjusted when synchronizing multiple ADCs. This feature is available in ECM via Control Register (Addr: E**h**).
Y5/U6 V6/V7	RCOut1+/- RCOut2+/-		Reference Clock Output 1 and 2. These signals provide a reference clock at a rate of CLK/4, when enabled, independently of whether the ADC is in Master or Slave Mode. They are used to drive the RCLK of another ADC12D1800, to enable automatic synchronization for multiple ADCs (AutoSync feature). The impedance of each trace from RCOut1 and RCOut2 to the RCLK of another ADC12D1800 should be 100Ω differential. Having two clock outputs allows the auto-synchronization to propagate as a binary tree. Use the DOC Bit (Addr: E**h**, Bit 1) to enable/ disable this feature; default is disabled.

TABLE 2. Control and Status Balls

Ball No.	Name	Equivalent Circuit	Description
V5	DES		Dual Edge Sampling (DES) Mode select. In the Non-Extended Control Mode (Non-ECM), when this input is set to logic-high, the DES Mode of operation is selected, meaning that the VinI input is sampled by both channels in a time-interleaved manner. The VinQ input is ignored. When this input is set to logic-low, the device is in Non-DES Mode, i.e. the I- and Q-channels operate independently. In the Extended Control Mode (ECM), this input is ignored and DES Mode selection is controlled through the Control Register by the DES Bit (Addr: 0**h**, Bit 7); default is Non-DES Mode operation.
V4	CalDly		Calibration Delay select. By setting this input logic-high or logic-low, the user can select the device to wait a longer or shorter amount of time, respectively, before the automatic power-on self-calibration is initiated. This feature is pin-controlled only and is always active during ECM and Non-ECM.
D6	CAL		Calibration cycle initiate. The user can command the device to execute a self-calibration cycle by holding this input high a minimum of t_{CAL_H} after having held it low a minimum of t_{CAL_L}. If this input is held high at the time of power-on, the automatic power-on calibration cycle is inhibited until this input is cycled low-then-high. This pin is active in both ECM and Non-ECM. In ECM, this pin is logically OR'd with the CAL Bit (Addr: 0**h**, Bit 15) in the Control Register. Therefore, both pin and bit must be set low and then either can be set high to execute an on-command calibration.
B5	CalRun		Calibration Running indication. This output is logic-high while the calibration sequence is executing. This output is logic-low otherwise.

Ball No.	Name	Equivalent Circuit	Description
U3 V3	PDI PDQ		Power Down I- and Q-channel. Setting either input to logic-high powers down the respective I- or Q-channel. Setting either input to logic-low brings the respective I- or Q-channel to a operational state after a finite time delay. This pin is active in both ECM and Non-ECM. In ECM, each Pin is logically OR'd with its respective Bit. Therefore, either this pin or the PDI and PDQ Bit in the Control Register can be used to power-down the I- and Q-channel (Addr: 0**h**, Bit 11 and Bit 10), respectively.
A4	TPM		Test Pattern Mode select. With this input at logic-high, the device continuously outputs a fixed, repetitive test pattern at the digital outputs. In the ECM, this input is ignored and the Test Pattern Mode can only be activated through the Control Register by the TPM Bit (Addr: 0**h**, Bit 12).
A5	NDM		Non-Demuxed Mode select. Setting this input to logic-high causes the digital output bus to be in the 1:1 Non-Demuxed Mode. Setting this input to logic-low causes the digital output bus to be in the 1:2 Demuxed Mode. This feature is pin-controlled only and remains active during ECM and Non-ECM.
Y3	FSR		Full-Scale input Range select. In Non-ECM, when this input is set to logic-low or logic-high, the full-scale differential input range for both I- and Q-channel inputs is set to the lower or higher FSR value, respectively. In the ECM, this input is ignored and the full-scale range of the I- and Q-channel inputs is independently determined by the setting of Addr: 3**h** and Addr: B**h**, respectively. Note that the high (lower) FSR value in Non-ECM corresponds to the mid (min) available selection in ECM; the FSR range in ECM is greater.
W4	DDRPh		DDR Phase select. This input, when logic-low, selects the 0° Data-to-DCLK phase relationship. When logic-high, it selects the 90° Data-to-DCLK phase relationship, i.e. the DCLK transition indicates the middle of the valid data outputs. This pin only has an effect when the chip is in 1:2 Demuxed Mode, i.e. the NDM pin is set to logic-low. In ECM, this input is ignored and the DDR phase is selected through the Control Register by the DPS Bit (Addr: 0**h**, Bit 14); the default is 0° Mode.

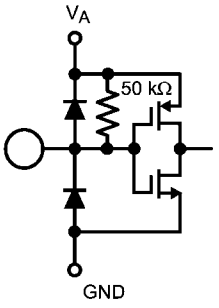
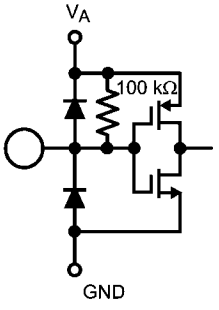
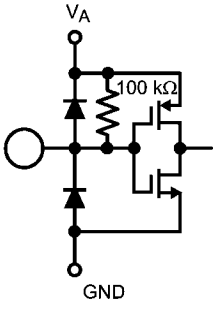
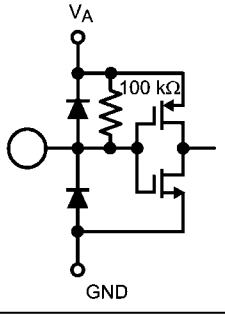
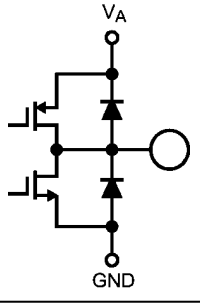
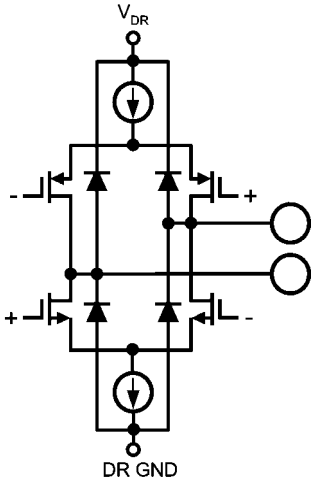
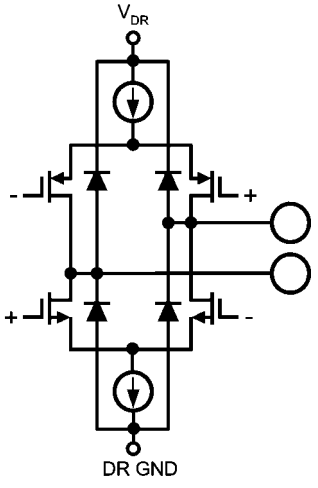
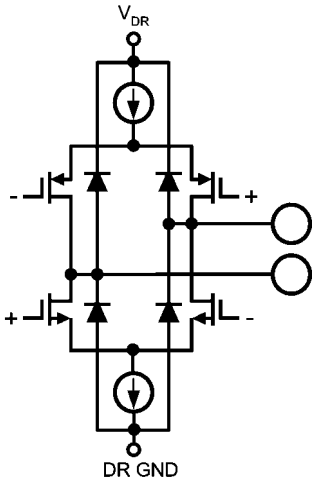
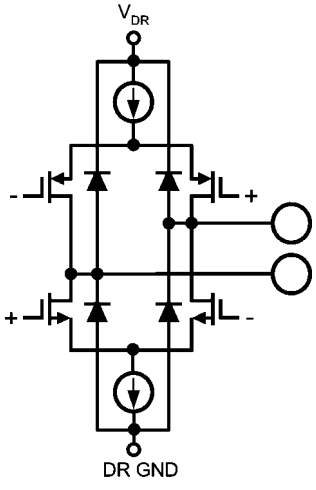
Ball No.	Name	Equivalent Circuit	Description
B3	$\overline{ECE}$		Extended Control Enable bar. Extended feature control through the SPI interface is enabled when this signal is asserted (logic-low). In this case, most of the direct control pins have no effect. When this signal is de-asserted (logic-high), the SPI interface is disabled, all SPI registers are reset to their default values, and all available settings are controlled via the control pins.
C4	$\overline{SCS}$		Serial Chip Select bar. In ECM, when this signal is asserted (logic-low), SCLK is used to clock in serial data which is present on SDI and to source serial data on SDO. When this signal is de-asserted (logic-high), SDI is ignored and SDO is in tri-stated.
C5	SCLK		Serial Clock. In ECM, serial data is shifted into and out of the device synchronously to this clock signal. This clock may be disabled and held logic-low, as long as timing specifications are not violated when the clock is enabled or disabled.
B4	SDI		Serial Data-In. In ECM, serial data is shifted into the device on this pin while $\overline{SCS}$ signal is asserted (logic-low).
A3	SDO		Serial Data-Out. In ECM, serial data is shifted out of the device on this pin while $\overline{SCS}$ signal is asserted (logic-low). This output is tri-stated when $\overline{SCS}$ is de-asserted.
D1, D7, E3, F4, W3, U7	DNC	NONE	Do Not Connect. These pins are used for internal purposes and should not be connected, i.e. left floating. Do not ground.
C7	NC	NONE	Not Connected. This pin is not bonded and may be left floating or connected to any potential.

TABLE 3. Power and Ground Balls

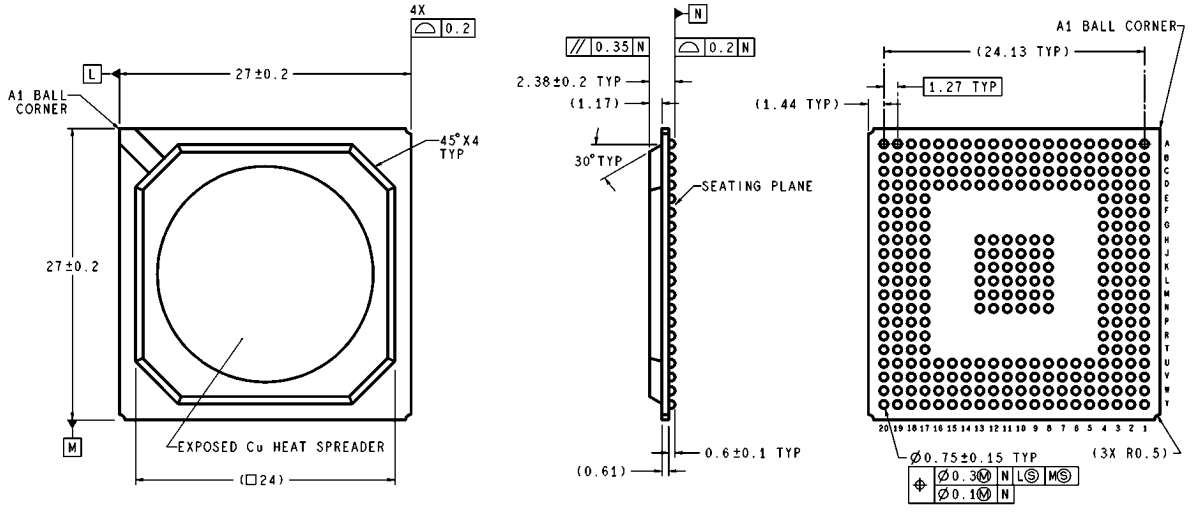
Ball No.	Name	Equivalent Circuit	Description
A2, A6, B6, C6, D8, D9, E1, F1, H4, N4, R1, T1, U8, U9, W6, Y2, Y6	V_A	NONE	Power Supply for the Analog circuitry. This supply is tied to the ESD ring. Therefore, it must be powered up before or with any other supply.
G1, G3, G4, H2, J3, K3, L3, M3, N2, P1, P3, P4, R3, R4	V_{TC}	NONE	Power Supply for the Track-and-Hold and Clock circuitry.
A11, A15, C18, D11, D15, D17, J17, J20, R17, R20, T17, U11, U15, U16, Y11, Y15	V_{DR}	NONE	Power Supply for the Output Drivers.
A8, B9, C8, V8, W9, Y8	V_E	NONE	Power Supply for the Digital Encoder.
J4, K2	VbiasI	NONE	Bias Voltage I-channel. This is an externally decoupled bias voltage for the I-channel. Each pin should individually be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.
L2, M4	VbiasQ	NONE	Bias Voltage Q-channel. This is an externally decoupled bias voltage for the Q-channel. Each pin should individually be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.
A1, A7, B2, B7, D4, D5, E4, K1, L1, T4, U4, U5, W2, W7, Y1, Y7, H8:N13	GND	NONE	Ground Return for the Analog circuitry.
F2, G2, H3, J2, K4, L4, M2, N3, P2, R2, T2, T3, U1	GND_{TC}	NONE	Ground Return for the Track-and-Hold and Clock circuitry.
A13, A17, A20, D13, D16, E17, F17, F20, M17, M20, U13, U17, V18, Y13, Y17, Y20	GND_{DR}	NONE	Ground Return for the Output Drivers.
A9, B8, C9, V9, W8, Y9	GND_E	NONE	Ground Return for the Digital Encoder.

TABLE 4. High-Speed Digital Outputs

Ball No.	Name	Equivalent Circuit	Description
K19/K20 L19/L20	DCLKI+/- DCLKQ+/-		Data Clock Output for the I- and Q-channel data bus. These differential clock outputs are used to latch the output data and, if used, should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver. Delayed and non-delayed data outputs are supplied synchronously to this signal. In 1:2 Demux Mode or Non-Demux Mode, this signal is at ¼ or ½ the sampling clock rate, respectively. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized.
K17/K18 L17/L18	ORI+/- ORQ+/-		Out-of-Range Output for the I- and Q-channel. This differential output is asserted logic-high while the over- or under-range condition exists, i.e. the differential signal at each respective analog input exceeds the full-scale value. Each OR result refers to the current Data, with which it is clocked out. If used, each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.

Ball No.	Name	Equivalent Circuit	Description
J18/J19	DI11+/-		I- and Q-channel Digital Data Outputs. In Non-Demux Mode, this LVDS data is transmitted at the sampling clock rate. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the delayed data, i.e. the other ½ of the data which was sampled one clock cycle earlier. Compared with the DId and DQd outputs, these outputs represent the later time samples. If used, each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.
H19/H20	DI10+/-		
H17/H18	DI9+/-		
G19/G20	DI8+/-		
G17/G18	DI7+/-		
F18/F19	DI6+/-		
E19/E20	DI5+/-		
D19/D20	DI4+/-		
D18/E18	DI3+/-		
C19/C20	DI2+/-		
B19/B20	DI1+/-		
B18/C17	DI0+/-		
.	.		
M18/M19	DQ11+/-		
N19/N20	DQ10+/-		
N17/N18	DQ9+/-		
P19/P20	DQ8+/-		
P17/P18	DQ7+/-		
R18/R19	DQ6+/-		
T19/T20	DQ5+/-		
U19/U20	DQ4+/-		
U18/T18	DQ3+/-		
V19/V20	DQ2+/-		
W19/W20	DQ1+/-		
W18/V17	DQ0+/-		
A18/A19	DId11+/-		Delayed I- and Q-channel Digital Data Outputs. In Non-Demux Mode, these outputs are tri-stated. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the non-delayed data, i.e. the other ½ of the data which was sampled one clock cycle later. Compared with the DI and DQ outputs, these outputs represent the earlier time samples. If used, each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.
B17/C16	DId10+/-		
A16/B16	DId9+/-		
B15/C15	DId8+/-		
C14/D14	DId7+/-		
A14/B14	DId6+/-		
B13/C13	DId5+/-		
C12/D12	DId4+/-		
A12/B12	DId3+/-		
B11/C11	DId2+/-		
C10/D10	DId1+/-		
A10/B10	DId0+/-		
.	.		
Y18/Y19	DQd11+/-		
W17/V16	DQd10+/-		
Y16/W16	DQd9+/-		
W15/V15	DQd8+/-		
V14/U14	DQd7+/-		
Y14/W14	DQd6+/-		
W13/V13	DQd5+/-		
V12/U12	DQd4+/-		
Y12/W12	DQd3+/-		
W11/V11	DQd2+/-		
V10/U10	DQd1+/-		
Y10/W10	DQd0+/-		

10.0 Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

UFH292A (Rev A)

NOTES: UNLESS OTHERWISE SPECIFIED
REFERENCE JEDEC REGISTRATION MS-034, VARIATION BAL-2.

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Notes

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