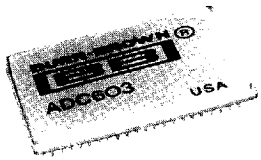
BURR - BROWN®



ADC603

12-Bit 10MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SPURIOUS-FREE DYNAMIC RANGE
- SAMPLE RATE: DC to 10MHz
- HIGH SIGNAL/NOISE RATIO: 68.2dB
- HIGH SINAD RATIO: 66dB
- LOW HARMONIC DISTORTION: –69.6dBc
- LOW INTERMOD. DISTORTION: –77.7dBc
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- 46-PIN DIP PACKAGE
- 0°C TO +70°C AND –55°C TO +100°C

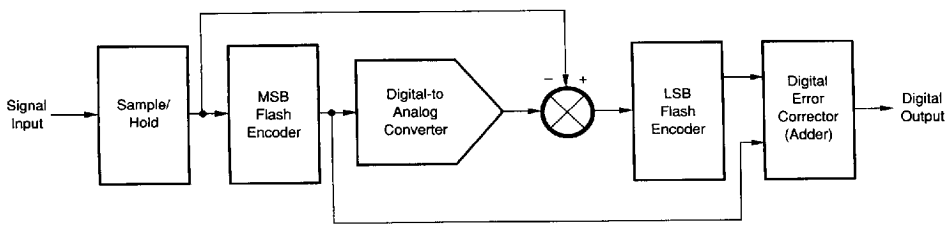
APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- RADAR SIGNAL ANALYSIS
- TRANSIENT SIGNAL RECORDING
- FFT SPECTRUM ANALYSIS
- HIGH-SPEED DATA ACQUISITION
- IR IMAGING SYSTEMS
- DIGITAL RECEIVERS
- SIGINT, ECM, AND EW SYSTEMS
- DIGITAL OSCILLOSCOPES

DESCRIPTION

The ADC603 is an high performance analog-to-digital converter capable of digitizing signals at any rate from DC to 10 megasamples per second. Outstanding spurious-free dynamic range has been achieved by minimizing noise and distortion.

The ADC603 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a 46-pin hybrid DIP package. Logic is TTL. Two temperature ranges are available: 0°C to +70°C (JH, KH) and –55°C to +100°C, environmentally screened (SHQ).



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 10MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603JH MIN	ADC603JH TYP	ADC603JH MAX	ADC603KH MIN	ADC603KH TYP	ADC603KH MAX	UNITS
RESOLUTION				12			12	Bits
INPUTS								
ANALOG								
Input Range	Full Scale	–1.25		+1.25	*		*	V
Input Impedance			1.5			*		MΩ
Input Capacitance			5			*		pF
DIGITAL								
Logic Family				TTL Compatible				
Convert Command	Start Conversion			Positive Edge				
Pulse Width	t = Conversion Period	10		t – 20	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.2	1		±0.1	0.8	%FSR[1]
Input Offset	DC		±0.2	0.75		*	0.5	%FSR
Integral Linearity Error	f = 200Hz		0.75			0.5	1	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all Codes		0.3			0.25	0.5	LSB
	99.7% of all Codes		0.4			0.3	0.65	LSB
	100% of all Codes		0.5	1		0.4	0.75	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.03			*	±0.07	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.04			*	±0.07	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004			*	±0.03	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.01			*	±0.03	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
Pipeline Delay	Logic Selectable			1, 2 or 3 Convert Command Periods				
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all Codes		0.3			*		LSB
	99.7% of all Codes		0.75			0.5		LSB
	100% of all Codes		1	1.25		0.6	0.9	LSB
Spurious Free Dynamic Range								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	63	72		66	74		dB
Total Harmonic Distortion[2](THD)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		–68	–61		–69	–64	dBc[3]
f = 100kHz			–70	–65		–72	–68	dBc
Two-Tone Intermodulation Distortion[2][4]								
f = 2.2MHz (–6.5dB)	f_S = 8.006MHz		–75	–67		–7	–71	dBc
f = 2.5MHz (–6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	60	65		62	66		dB
f = 100kHz (–0.5dB)		64	67		66	68.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	63	67		66	68		dB
f = 100kHz (–0.5dB)		66	68		67	70		dB
Aperture Delay Time			–5			*	+9	ns
Aperture Jitter			9			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		70		50	*		MHz
Full Power	0dB Input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale Input		80			*	140	ns
OUTPUTS								
Logic Family				TTL Compatible				
Logic Coding	Logic Selectable			Two's Complement or Inverted Two's Complement				
Logic Levels	Logic LO, I_{OL} = –3.2mA	0	+0.3	+0.8	0	+0.3	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	+2.4	+3.5	+5	V
EOC Delay Time	Data Out to DV	5	35		5	35		ns
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		37	100		37	100	ns
Data Valid Pulse Width		20	45	60	20	45	60	ns
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	+14.25	+15	+15.75	V
$-V_{CC}$		–14.25	–15	–15.75	–14.25	–15	–15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	+4.75	+5	+5.25	V
$-V_{DD2}$		–4.95	–5.2	–5.46	–4.95	–5.2	–5.46	V
Supply Currents: $+I_{CC}$			+60			+60	+80	mA
$-I_{CC}$			–60			–60	–80	mA
$+I_{DD1}$			+280			+280	+330	mA
$-I_{DD2}$			–565			–565	–630	mA
Power Consumption	Operating		6.1			6.1		W

SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 15-minute warmup, and $T_C = T_{MIN}$ to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603JH MIN	ADC603JH TYP	ADC603JH MAX	ADC603KH MIN	ADC603KH TYP	ADC603KH MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE}	0		+70	*		*	°C
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.4	1.5		*	1	%FSR
Input Offset	DC		±0.4	1		*	0.5	%FSR
Integral Linear Error	f = 200Hz		0.75			0.6	1.25	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all Codes		0.4			0.3	0.6	LSB
	99.7% of all Codes		0.5			0.4	0.75	LSB
	100% of all Codes		0.75			0.6	1	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.04			*	±0.08	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.05			*	±0.08	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004			*	±0.05	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.02			*	±0.05	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all Codes		0.5			0.4		LSB
	99.7% of all Codes		1			0.6		LSB
	100% of all Codes		1.25	1.5		0.7	1	LSB
Spurious Free Dynamic Range[5]	f = 5MHz (–0.5dB)	60	65		65	72		dB
Total Harmonic Distortion[2]								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		–67	–58		–69	–62	dBc
f = 100kHz			–69	–62		–69.5	–67	dBc
Two-Tone Intermodulation Distortion								
f = 2.2MHz (–6.5dB)	f_S = 8.006MHz		–72	–64		–74.5	–68	dBc
f = 2.5MHz (–6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	57	65		61	65.5		dB
f = 100kHz (–0.5dB)		62	66		64	66.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	60	67		64	68		dB
f = 100kHz (–0.5dB)		64	68		66	69.5		dB
Aperture Delay Time			–6			*	+10	ns
Aperture Jitter			10			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		70		50	*		MHz
Full Power	0dB Input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale Input		80			*		ns
OUTPUTS								
Logic Levels	Logic LO, I_{OL} = –3.2mA	0	+0.3	+0.8	*	*	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	*	*	*	V
EOC Delay Time	Data Out to DV	5	35		*	*		ns
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		42	100		*	*	ns
Data Valid Pulse Width		20	45	60	*	*	*	ns
POWER SUPPLY REQUIREMENTS								
Supply Currents: $+I_{CC}$	Operating		+65			*	+80	mA
$-I_{CC}$			–61			*	–80	mA
$+I_{DD1}$ [6]			+285			*	+333	mA
$-I_{DD2}$ [7]			–570			*	–630	mA
Power Consumption	Operating		6.1			*		W

* Same specifications as ADC603JH.

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with tested and guaranteed distortion specifications are available on special order—inquire. (3) dBC = level referred to carrier-input signal = 0dB); F = input frequency; F_S = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. (5) SFDR tested at temperature for K grade only. (6) Pins 3 and 30 (analog) typically draw 80% of the total +5V current. Pin 21 (digital) typically draws 20%. (7) Pin 6 (analog) typically draws 45% of the total –5.2V current. Pin 31 (digital) typically draws 55%.

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SPECIFICATIONS

ELECTRICAL

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 15-minute warmup F_S = 10MHz (–55°C to +85°C), F_S = 8MHz (+85°C to +100°C).

PARAMETER	CONDITIONS	ADC603SHQ MIN	ADC603SHQ TYP	ADC603SHQ MAX	UNITS
TEMPERATURE RANGE[4]	T_{CASE}	–55		+100	C°
RESOLUTION				12	Bits
ANALOG					
Input Range		–1.25		+1.25	V
Input Resistance		1.5			MΩ
Input Capacitance		5			pF
DIGITAL					
Logic Family			TTL Compatible		
Convert Command	Start Conversion		Positive Edge		
Pulse Width	t = conversion period	10		20	ns
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error	DC			1.0	%FSR[1]
Input Offset	DC			1.0	%FSR
Integral Nonlinearity	f = 100kHz		0.75		LSB
Differential Nonlinearity	f = 100KHz, all codes		0.6	1.0	LSB
No Missing Codes			Guaranteed		
Power Supply Rejection	$\Delta + V_{CC}$ = ±10%	–0.1		0.1	%FSR%
	$\Delta - V_{CC}$ = ±10%	–0.1		0.1	%FSR%
	$\Delta + V_{DD}$ = ±10%	–0.05		0.05	%FSR%
	$\Delta - V_{DD}$ = ±10%	–0.05		0.05	%FSR%
CONVERSION CHARACTERISTICS					
Sample Rate	–55°C ≤ T_C ≤ +85°C	DC		10M	Samples/s
	+85°C ≤ T_C ≤ +100°C	DC		8M	Samples/s
DYNAMIC CHARACTERISTICS					
Differential Nonlinearity	f = 4.9MHz: All Codes		0.6	1.0	LSB
Spurious Free Dynamic Range	f = 5.0MHz (–0.5dB)	65	72		dBc
Total Harmonic Distortion[2]	f = 5.0MHz (–0.5dB)		–68	–63	dBc
	f = 100kHz (–0.5dB)		–73	–68	dBc
2-Tone Intermodulation Distortion[3]					
f_1 = 2.2MHz (–6.5dB)			–74	–70	
f_2 = 2.3MHz (–6.5dB)					dBc
Signal-to-Noise and Distortion	f = 5.0MHz (–0.5dB)	63	65		dB
(SINAD ratio)	f = 100kHz (–0.5dB)	67	69		dB
Signal-to-Noise Ratio (SNR)	f = 5.0MHz (–0.5dB)	65	68		dB
	f = 100kHz (–0.5dB)	66	69		dB
Aperture Delay Time				10	ns
Aperture Jitter				10	ps rms
Analog Input Bandwidth (–3dB)					
Small Signal	–20dB Input		70		MHz
Full Power	0dB Input		40		MHz
Overload Recovery Time	2 x Full Scale Input			140	ns
OUTPUTS					
Logic Family			TTL Compatible		
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement		
Logic Levels	Logic LO, I_{OL} = –3.2mA	0	+0.3	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	V
EOC Delay Time	Data Out to DV	5	35		ns
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		42	100	ns
Data Valid Pulse Width		20	45	60	ns
POWER SUPPLY REQUIREMENTS					
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	V
$-V_{CC}$		–14.25	–15	–15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	V
$-V_{DD2}$		–4.95	–5.2	–5.46	V
Supply Currents: $+I_{CC}$	Operating		+60	+80	mA
$-I_{CC}$			–60	–80	mA
$+I_{DD1}$			+280	+333	mA
$-I_{DD2}$			–565	–630	mA
Power Consumption	Operating		6.1		W

NOTE: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) dBc = level referred to carrier-input signal = 0dB; f = input frequency; F_S = sampling frequency. (3) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. (4) Temperature is specified as –55°C ambient, +100°C case.

PIN ASSIGNMENTS

1	Common (Case)	46	Common (Analog)
2	NC	45	Analog Signal In
3	$+V_{DD1}$ (+5V) Analog	44	$+V_{CC}$ (+15V) Analog
4	S/H Out	43	$-V_{CC}$ (–15V) Analog
5	A/D In	42	NC
6	$-V_{DD2}$ (–5.2V) Analog	41	NC
7	NC	40	NC
8	NC	39	DNC
9	Bit 1(MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	$+V_{CC}$ (+15V) Analog
14	Bit 6	33	$-V_{CC}$ (–15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	$-V_{DD2}$ (–5.2V) Digital
17	Bit 9	30	$+V_{DD1}$ (+5V) Analog
18	Bit 10	29	1 Pipeline Delay Select
19	Bit 11	28	0 Pipeline Delay Select
20	Bit 12 (LSB)	27	Output Logic Invert
21	$+V_{DD1}$ (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	Tri-State $\overline{\text{ENABLE}}$
23	Common (Digital)	24	Convert Command In

ORDERING INFORMATION

ADC603 ( ) H Q

Basic Model Number

Performance Grade Code
- J, K: 0°C to +70°C Case Temperature
- S: –55°C to +100°C Case Temperature

Package Code
- H: Metal and Ceramic

Environmental Screening Option

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±16.5V
$+V_{DD1}$	+7V
$\pm V_{DD2}$	–7V
Analog Input	±5V
Logic Input	–0.5V to $+V_{DD1}$
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C

Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION[1]

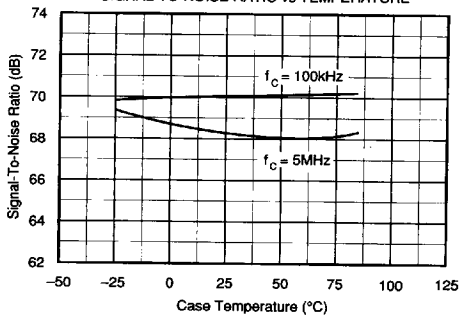
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC603JH	Metal and Ceramic	234
ADC603KH	Metal and Ceramic	234
ADC603SHQ	Metal and Ceramic	234

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

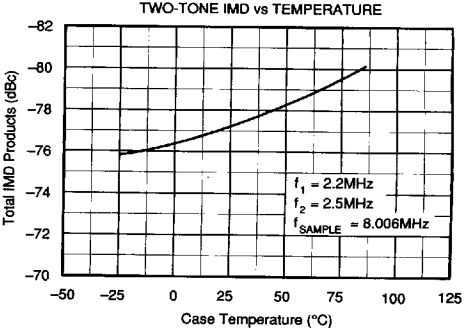
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$= ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S= 50Ω, 15-minute warmup, and T_C = +25°C, unless otherwise noted. All plots are 4096 point FFTs.

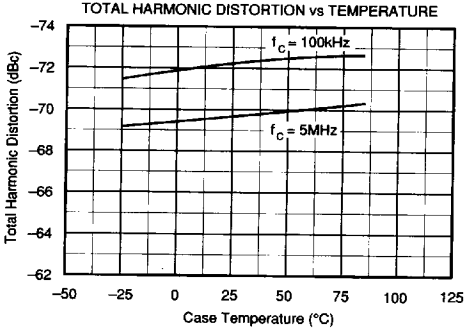
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



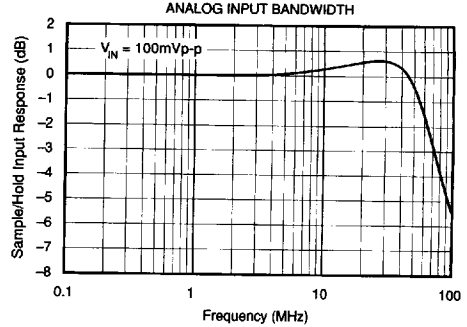
TWO-TONE IMD vs TEMPERATURE



TOTAL HARMONIC DISTORTION vs TEMPERATURE



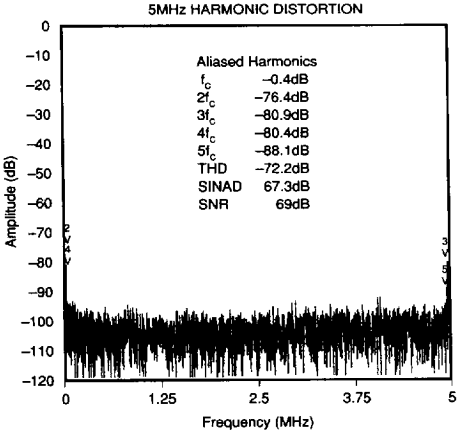
ANALOG INPUT BANDWIDTH



TYPICAL PERFORMANCE CURVES (CONT)

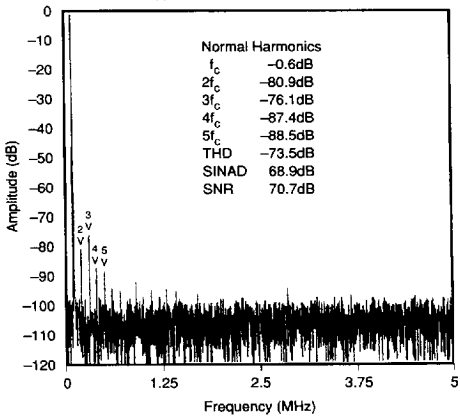
$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, R_S = 50Ω, 10MHz sample rate, 15-minute warmup, and T_C = +25°C, unless otherwise noted. All plots are 4096-point FFTs.

5MHz HARMONIC DISTORTION



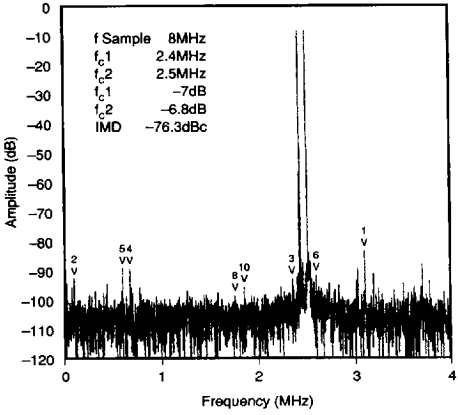
NOTE: Sample rate = 9.99 MHz; even harmonics folded to left edge and odd harmonics folded to right edge. Any non-harmonically related spurious products show clearly in the center.

100kHz HARMONIC DISTORTION



NOTE: Sample rate = 9.99 MHz; harmonics appear in normal order.

TWO-TONE INTERMODULATION DISTORTION



NOTE: Sample rate = 8MHz; highest IMD product is cursor number 1: f1 +f2. The second-order −76.3dBc product determines the wideband spurious-free dynamic range of this example. For RF applications third-order IMD products such as those at cursors 3 and 6 are the limiting spurs. Under these conditions spurious-free dynamic range is limited by 2f2+f1 to 84.3dBc.

Sample rates of 10MHz show similar results.

TWO-TONE INTERMODULATION DISTORTION PRODUCTS

CURSOR	IMD	FREQUENCY	dB
1	2nd order : f1 + f2	3.086395621579MHz	−83.1
2	2nd order : f2 − f1	0.080140734949MHz	−91.4
3	3rd order : 2f1 − f2	2.339718530102MHz	−92.4
4	3rd order : 2f1 + f2	0.666536356529MHz	−88.4
5	3rd order : 2f2 − f1	0.586395621579MHz	−88.2
6	3rd order : 2f2 + f1	2.580140734949MHz	−91.1
7	4th order : 3f1 − f2	3.246677091478MHz	−109
8	4th order : 3f1 + f2	1.753322908522MHz	−100
9	4th order : 2f2 − 2f1	0.130281469898MHz	−114.8
10	4th order : 2f2 + 2f1	1.833463643471MHz	−95
11	4th order : 3f2 − f1	2.926114151681MHz	−115.4
12	4th order : 3f2 + f1	1.913604378421MHz	−98.2

NOTE: IMD products in this table are refered to full-scale (0dB). To refer IMD to carrier, subtract the larger of f_c1 or f_c2. In this example, IMD referred to carrier will be 6.8dB higher (worse) than the full-scale value shown.

THEORY OF OPERATION

The ADC603 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: sample/hold amplifier, MSB flash encoder, DAC and error amplifier, LSB flash encoder, digital error corrector, and timing circuits. The ADC603 uses hybrid technology with laser-trimmed integrated circuits mounted in a multilayer ceramic package to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 25ns. The low-bias-current output buffer is then required to settle to only the resolution (7 bits) of the first (MSB) flash encoder in 25ns, while an additional 60ns is allowed for settling to the resolution (12 bits) of the second (LSB) flash encoder. Sample/hold droop appears as only an offset error and does not effect linearity.

Both the MSB and the LSB flash encoder (ADC) function are performed by multiplexing one high-speed 7-bit resolution converter formed by parallel-connecting two 6-bit flash ADCs. The DAC voltage reference is also used to generate reference voltages for the MSB and LSB encoder to compensate drift errors. Buffering and scaling amplifiers are laser-trimmed to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 7-bit resolution monolithic DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome resistors and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 35ns.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling two-input amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, the active input is switched off to blank the amplifier input from the beginning of the S/H acquisition time to the end of the MSB encoder update time.

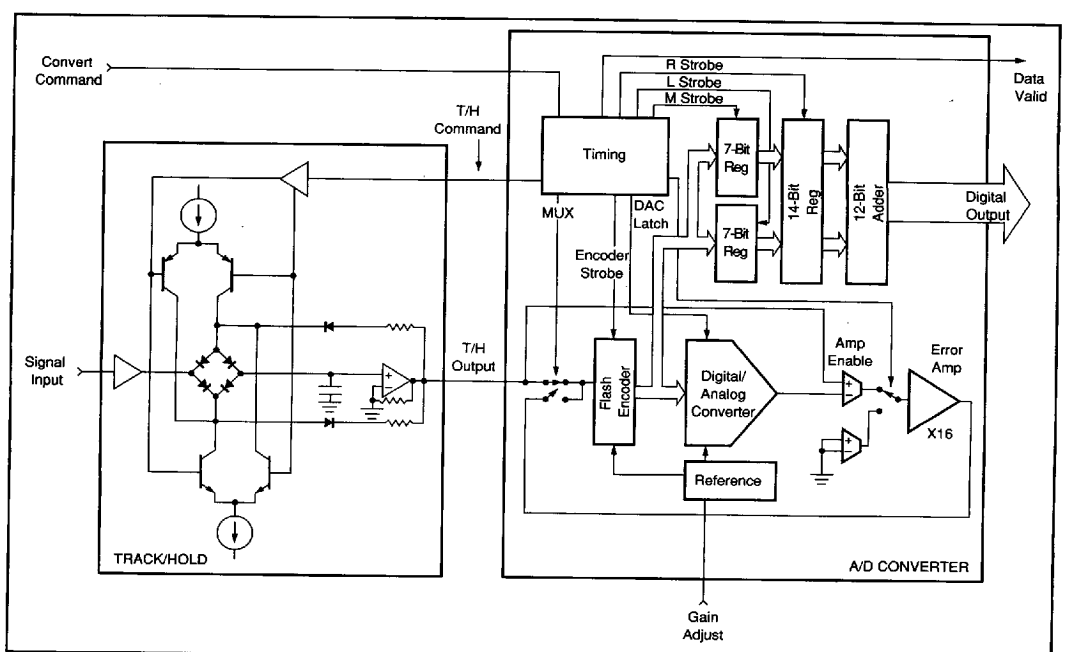


FIGURE 1. ADC603 Block Diagram—A Two-Step Subranging Architecture.

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADC603. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated to allow triggering by pulses from as narrow as 10ns to as wide as 80% duty cycle.

The ADC603 timing technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus a fixed 67ns ADC conversion time. ADC603 conversion rates are therefore possible somewhat above the 10MHz specification, but S/H acquisition time is sacrificed and accuracy is rapidly degraded. Converters with guaranteed operation at 10.24MHz sample rate are available on special order.

The output of the MSB and LSB encoders are read into separate 7-bit latches. The latched MSB data, along with the latched LSB data, is then read into a 14-bit latch after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. These latches eliminate any critical timing problems that could result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry is to assemble the 7-bit words from the two flash encoders into a 12-bit output word. A data valid (DV) pulse is also generated which is used to indicate when output data can be latched into an external register. This DV pulse is delayed 6ns after the output data has settled to allow sufficient set-up time for an external TTL data latch. A high-speed latch such as a 74F174 is recommended.

The 14-bit register output is then sent to a 12-bit adder where the final data output word is created. The MSB data forms the most significant seven bits of a 12-bit word, with the last five bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits forms the other input to the adder, with the first five bits being assigned zeros. As two 12-bit words are being added, the output of the adder could exceed 12 bits in range; however, the final data output is only a 12-bit word, so a means of detecting an overrange is included to prevent reading erroneous data. The converter data output is forced to all ones for a full-scale input or overrange. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±1.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADC603 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: total harmonic distortion (THD), signal-to-noise ratio (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), and intermodulation distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 2. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This was used to generate the typical FFT performance curves shown on page 5.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To

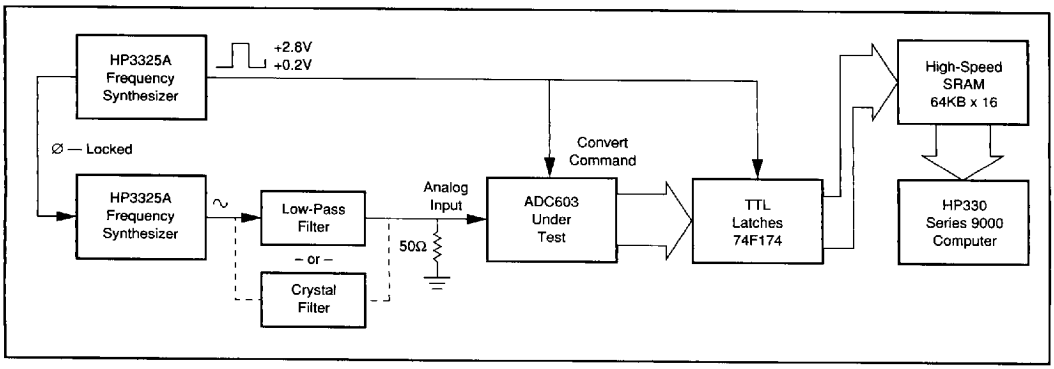


FIGURE 2. Block Diagram of FFT Test for THD, SNR, and SINAD.

assure that the majority of codes are exercised in the ADC603 (12 bits), a 4096-point FFT is taken. If the data storage RAM is limited, a smaller FFT may be taken if a sufficient number of samples are averaged (i.e., a 10-sample average of 512-point FFTs).

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion[2] Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 9 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first 9 harmonics)}}{\text{Sinewave Signal Power}}$$

4. Intermodulation Distortion (IMD):

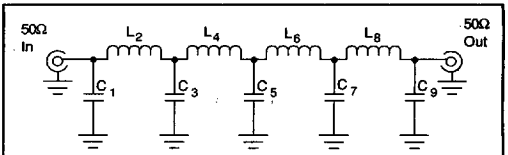
$$10 \log \frac{\text{Highest IMD Product Power (to 5th order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced[3] to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

APPLICATION TIPS

Attention to test set-up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6dB to prevent "hard limiting" on peaks.
3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 4) will eliminate harmonics from the test signal generator.
4. Test signal generators must have exceptional noise performance (better than –155dBC/Hz) to achieve accurate SNR measurements.[4] Good generators together with fifth-order elliptical bandpass filters are recommended for



9th Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2x cutoff frequency = 90dB.

Cutoff frequency = –3dB frequency; to convert cutoff frequency to –0.5dB frequency, multiply all LC values by 0.98997.

CUTOFF FREQ. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_2 (µH)	L_4 (µH)	L_6 (µH)	L_8 (µH)
5	1134.6	1729.2	1765.6	1729.2	1134.6	2.056	2.216	2.216	2.056
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45

FIGURE 4. Ninth-Order Harmonic Filter.

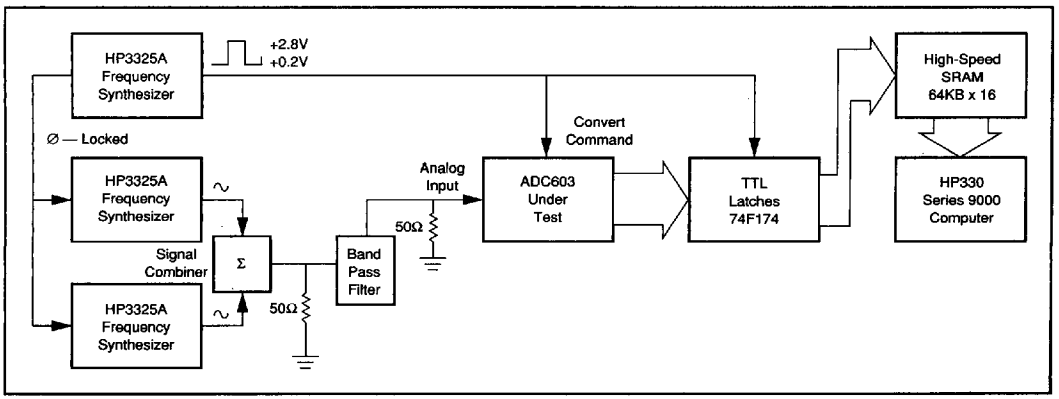


FIGURE 3. Block Diagram of FFT Test for Two-Tone IMD.

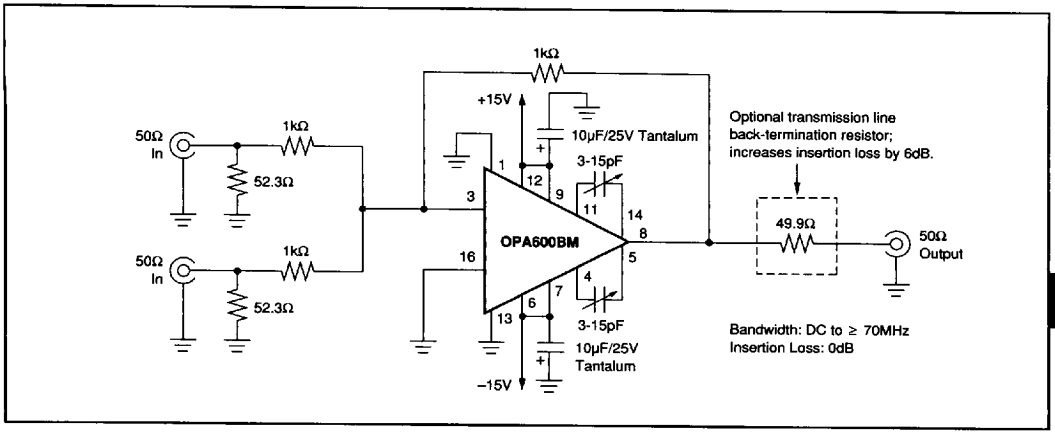


FIGURE 5. Active Signal Combiner.

SNR tests. Narrow-bandwidth crystal filters can also be used to filter generator broadband noise, but they should be carefully tested for operation at high levels.

5. The analog input of the ADC603 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω), or it should be driven by a low output impedance buffer such as an OPA642/643. Short leads are necessary to prevent digital noise pickup.
6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance. Short leads are necessary to preserve fast TTL rise times.
7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. An active summing amplifier using an OPA600 is shown in Figure 5. This circuit will provide excellent performance from DC to 5MHz with harmonic and intermodulation distortion products typically better than –70dBC. A passive (hybrid transformer) signal combiner can also be used (Figure 6) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be ≈45dB between signal generators and its input-output insertion loss will be ≈6dB. Distortion will be better than –85dBC for the powdered-iron core specified.
8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies. A minimum four-sample Blackman-Harris window function is recommended.[1]
9. Digital data must be latched into an external TTL 12-bit register by the Data Valid output pulse or by using the convert command pulse (Figures 11, 12, 13, and 14). Latches should be mounted on PC boards in very close proximity to the ADC603. Avoid long leads.

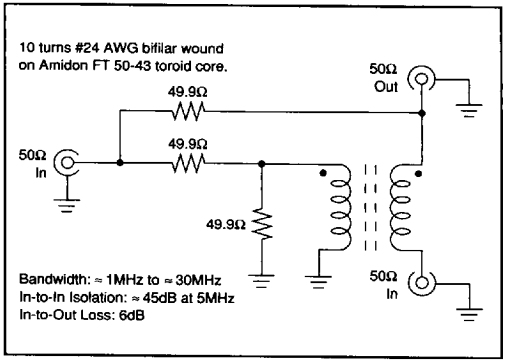


FIGURE 6. Passive Signal Combiner.

10. Do not overload the data output logic. These outputs are designed to drive 2 TTL loads. Do not connect ADC603 data output pins directly to a noisy digital bus; use external 3-state logic for noise immunity.
11. A well-designed, clean PC board layout will assure proper operation and clean spectral response.[5, 6] Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (2oz-foil) ground planes can give excellent results, if carefully designed.
12. Prototyping "plug-boards" or wire-wrap boards will not be satisfactory.
13. Floating inputs can eliminate ground-loop noise. A simple common-mode choke (balun) shown in Figure 7 and 8, or a differential amplifier (Figure 9 and 10) can reduce analog input noise.

14. Connect analog and digital ground pins of the ADC603 directly to the ground plane. In our experience, connecting these pins to a common ground plane gives the best results. Analog and digital power supply commons should be tied together at the ground plane. Adding power supply and ground-return filtering[7] is optional and may improve noise rejection.

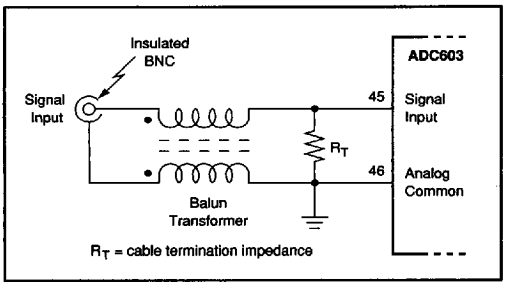


FIGURE 7. Floating-Input Balun Transformer.

NOTES:

1. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", Fredric J. Harris. *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
2. SINAD test includes harmonics whereas SNR does not include these important spurious products.
3. If IMD is referenced to peak envelope power, distortion will be of 6dB better.
4. "Test Report: FFT Characterization of Burr-Brown ADC600K", Signal Conversion Ltd., Swansea, Wales, U.K.
5. *MECL System Design Handbook*, 3rd Edition, Motorola Corp.
6. Motorola MECL, Motorola Corp.
7. Murata-Erie BNX002-01.

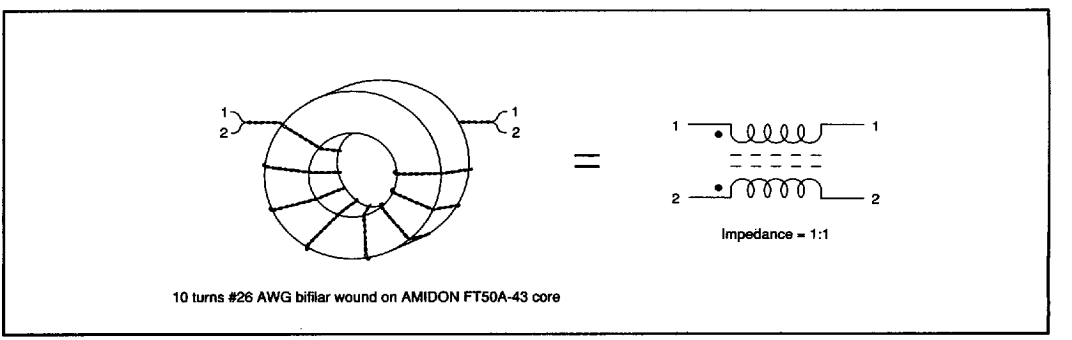


FIGURE 8. Balun Transformer Windings.

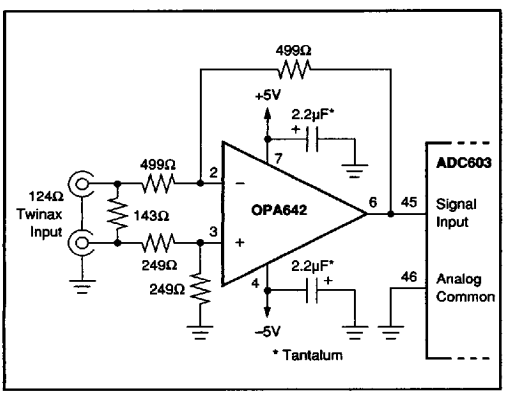


FIGURE 9. Differential Input Buffer Amplifier (Gain = –1V/V).

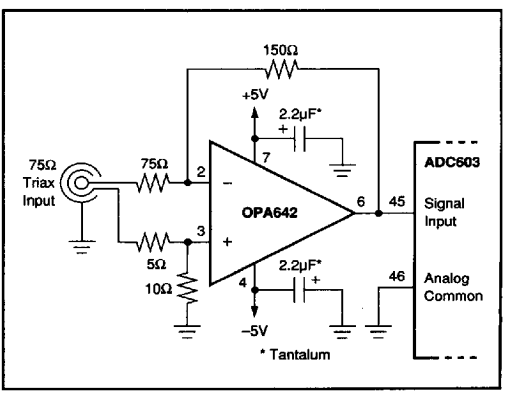


FIGURE 10. Differential Input Buffer Amplifier (Gain = –2V/V).

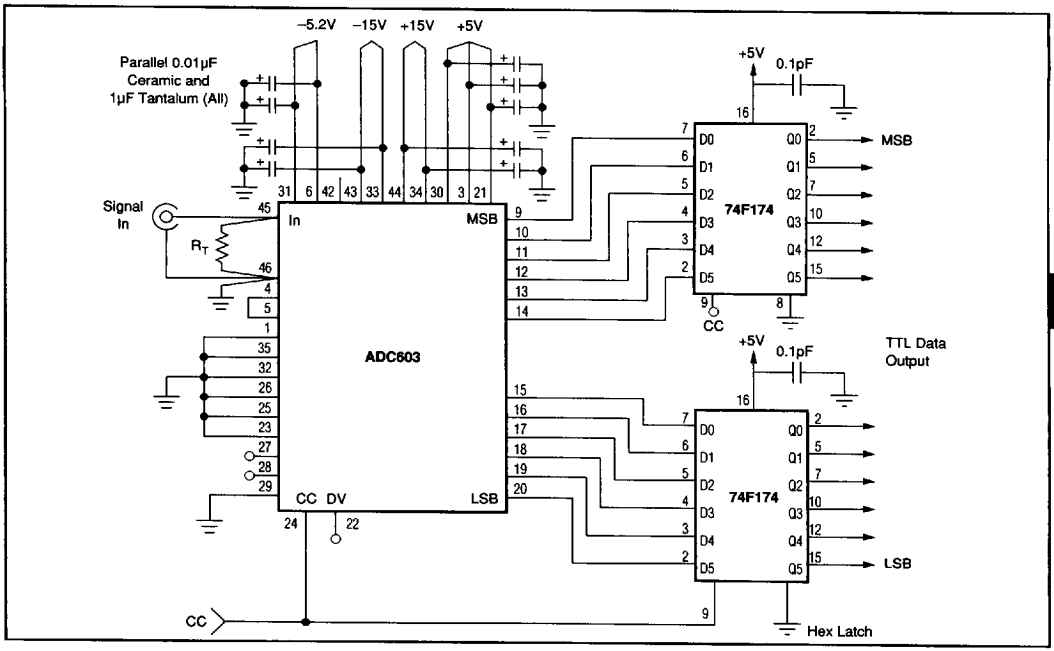


FIGURE 11. Interface Circuit—Digital Output Strobed by Convert Command. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane (recommended circuit).

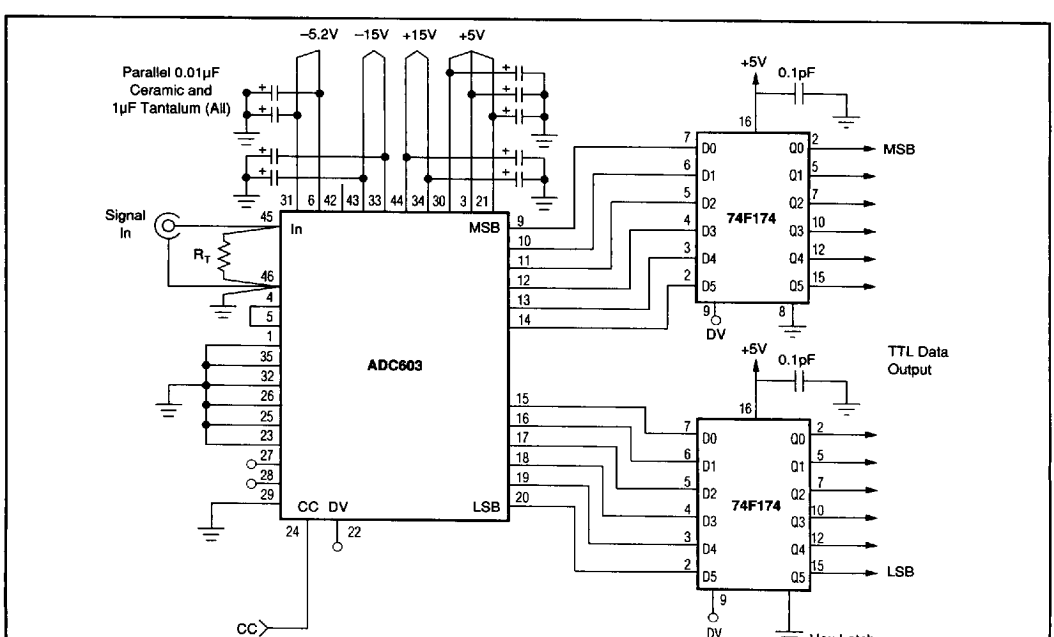
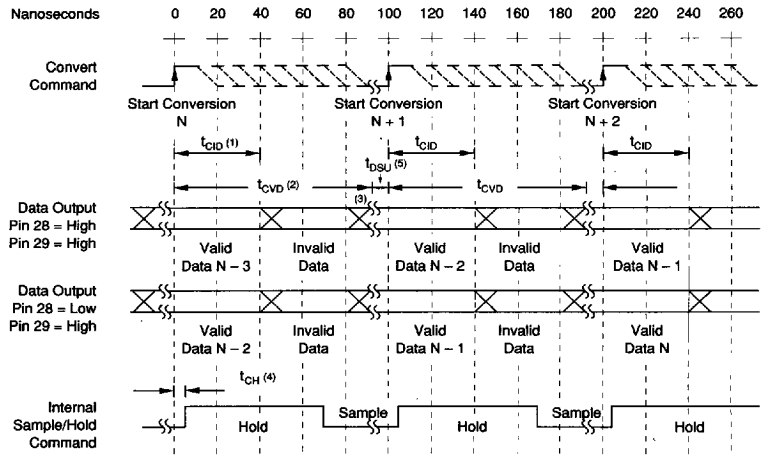


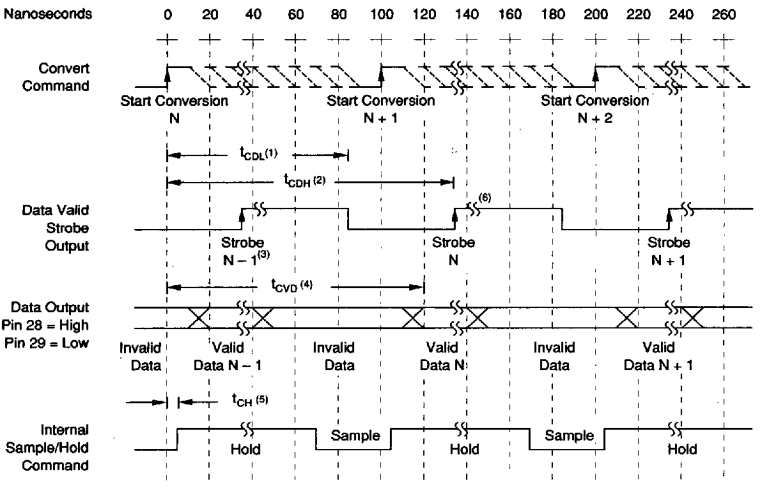
FIGURE 12. Interface Circuit—Digital Output Strobed by Data Valid Pulse. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane.



NOTES: (1) t_{CID} = Delay time from Convert Command to Invalid Data. Typical value = 40ns. Independent of conversion rate. (2) t_{CVD} = Delay time from Convert Command to Valid Data. Typical value = 93ns. Independent of conversion rate. (3) The ⊠ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (4) t_{CH} = Delay time from Convert Command to the internal hold. Typical value = 6ns. Independent of conversion rate. (5) t_{DSU} = data set-up time. This depends on conversion rate and may be calculated by:

$$t_{DSU} = \frac{1}{f_{SAMPLE}} - t_{CVD}$$

FIGURE 13. Convert Command Strobe Timing.



NOTES: (1) t_{CDL} = Delay time from Convert Command to the falling edge of Data Valid Strobe. Typical value = 85ns. Independent of conversion rate. (2) t_{CDH} = Delay time from Convert Command to the rising edge of Data Valid Strobe. Typical value = 135ns. Independent of conversion rate. (3) If Conversion "N" is the first conversion, then there is no Strobe N-1, and the Data Valid Strobe Signal will simply be high until t_{CDL} after the first Convert Command. (4) t_{CVD} = delay time from Convert Command to Valid Data. Typical value = 120ns. Independent of conversion rate. (5) t_{CH} = Delay time from Convert Command to Internal Hold Command. Typical value = 6ns. Independent of conversion rate. (6) The ⊠ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates.

FIGURE 14. Data Valid Strobe Timing.

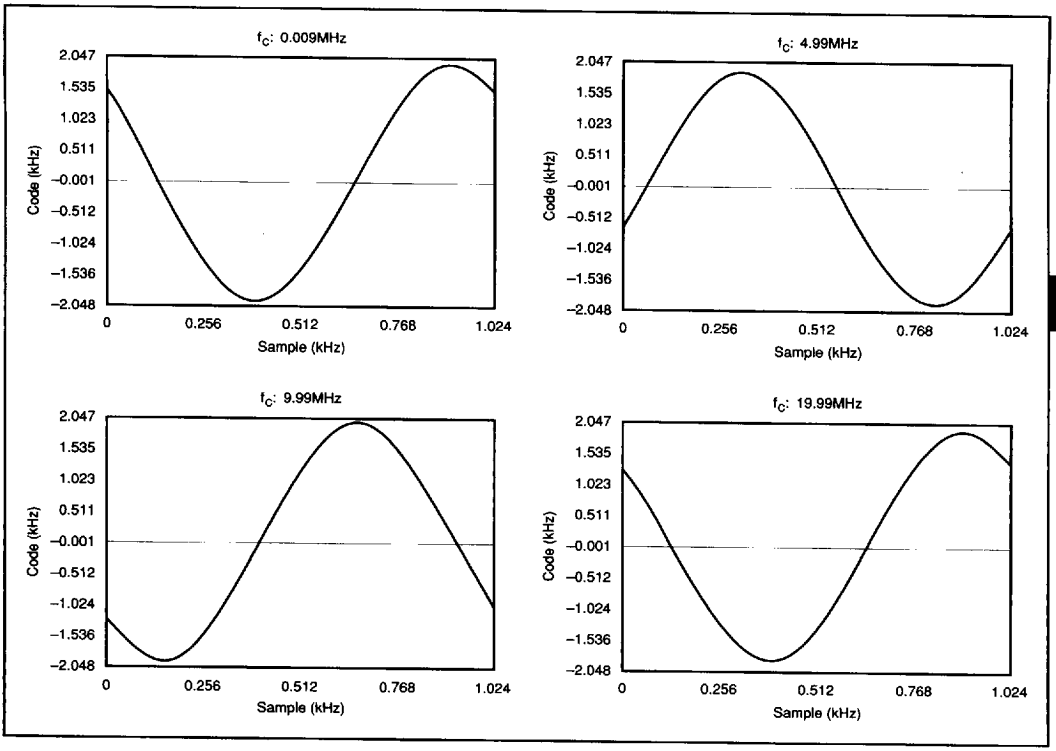


FIGURE 15. Digitized Sine Waves (f_S = 10MHz).

DIGITIZING INPUT WAVEFORMS

The response of the ADC603 is illustrated by the digitized waveforms of Figure 15. The 4.99MHz sine wave near the Nyquist limit is virtually identical to much lower frequency sine wave input. The under-sampled 19.999MHz sine wave illustrates the ADC603's excellent analog input full-power bandwidth.

HISTOGRAM TESTING

Histogram testing is used to test differential nonlinearity of the ADC603. This system's block diagram (the same for FFT testing and waveform digitizing) is shown in Figure 2 and histogram test results for a typical converter are shown in Figure 16. Note that low-frequency differential nonlinearity is 1/2LSB and it shows virtually no degradation near the Nyquist limit of 5MHz; there are no missing codes present and the peak nonlinearity does not exceed 1LSB. Histogram testing is a useful performance indicator as the width of all codes can be determined.

SPECTRUM ANALYZER TESTING

A beat-frequency technique (Figure 17) can be used to view digitized waveforms on an oscilloscope and, with care, this technique can also be used for testing high-speed ADC dynamic characteristics with an analog spectrum analyzer.

In this method a test signal is digitized by the ADC603 and the output digital data is latched into an external latch by the converter Data Valid output pulse driving a divide-by-N counter. The buffered ECL/TTL level translator latch drives a 12-bit video-speed DAC which reconstructs the digital signal back into an analog replica of the ADC603 input. This analog signal, including distortion products and noise resulting from digitization, can then be viewed on an ordinary analog RF spectrum analyzer.

It is important to realize that the distortion and noise measured by this technique include not only that from the ADC603, but also from the entire analog-to-analog test system. Nonlinearity of the reconstruction circuit must be very low to measure a high performance ADC, and this places severe requirements on the ADC, deglitcher, and buffer amplifiers.

Using a high-speed video DAC600 in the analog reconstruction circuit allows excellent test circuit linearity to be achieved. Clocking the DAC (demodulating) at f_C/N allows a longer DAC settling time and keeps linearity high in the digital-to-

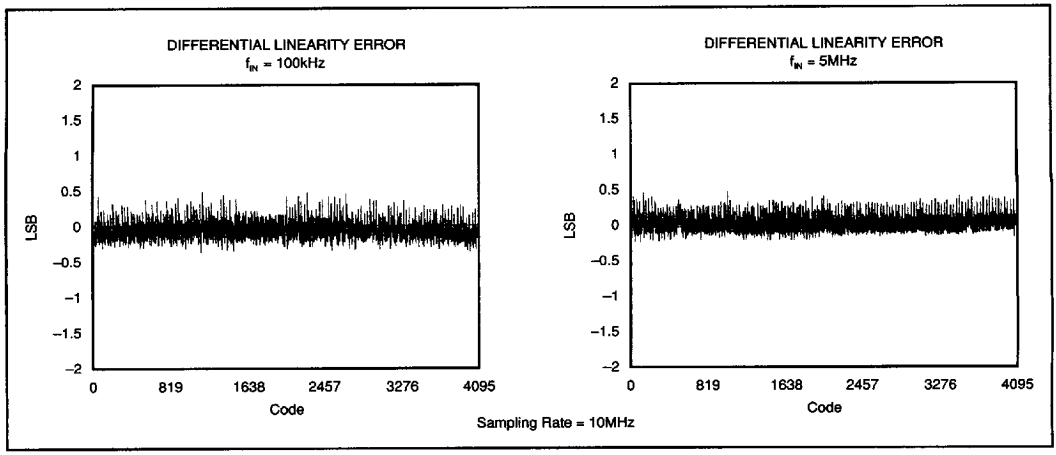


FIGURE 16. 100kHz and 5MHz Differential Linearity.

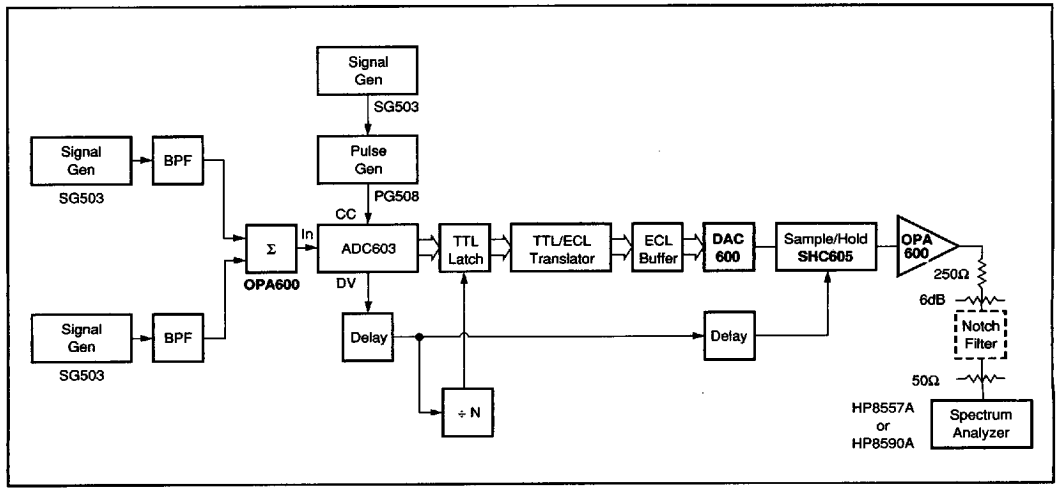


FIGURE 17. Analog-to-Analog Spectral Analysis by Beat-Frequency Techniques.

analog portion of the test circuit. Spectrum analyzer dynamic range can be a limiting factor in this method. To increase dynamic range, a sharp notch filter can be used to attenuate the high-level fundamental frequency. Attenuating the high-level fundamental signal allows the analog spectrum analyzer to be used on a more sensitive range without generating distortion products within its front end.

Note that even though the signal is demodulated at a frequency of sample rate/N, the distortion products still maintain a correct frequency relationship to the fundamental. While this analog technique can give good performance, it cannot exclude some distortion products unavoidably generated within the analog reconstruction portion of the test system. For this reason, the digital FFT technique is capable of more accurate high-speed analog/digital converter dynamic performance measurements and is the preferred method of testing high-performance A/D converters.

TIMING

The ADC603 generates all necessary timing signals internally. There are two methods for reading output data, offering three selectable levels of data pipeline delay as described below.

Convert Command Timing Option (pin 29 = HI)

With this option, the Convert Command signal is used both for initiating a new conversion and for reading valid data

from a previous conversion. This method is most useful in synchronous systems where data samples are taken continuously.

See Figure 13 for timing relationships.

Pin 28 is used to control the amount of pipeline delay. If pin 28 is held LO, then output data "N – 2" will be valid on the rising edge of Convert Command "N." If pin 28 is held HI, then output data "N – 3" will be valid on the rising edge of Convert Command "N." These timing relationships are valid at any conversion rate up to 10MHz. At rates approaching 10MHz, however, the data setup time before the rising Convert Command edge may become as short as 6ns. Therefore, the use of high-speed TTL latches such as the 74F174 hex flip-flop is recommended to capture the data. If slower latches must be used, then the setup time can effectively be improved by adding several nanoseconds of delay between the Convert Command and the latch clock signal.

Data Valid Timing Option (pin 29 = LO)

With this option, data from conversion "N" becomes valid after a fixed delay from the rising edge of Convert Command "N." The delay is approximately 135ns, at which time the Data Valid strobe signal will rise. This signal may be connected directly to the clock input of the user's data latch.

See Figure 18 for timing relationships. Pin 28 must be left HI at all times when using the Data Valid timing option.

The advantages of this method are that no subsequent conversions are required in order to read the data, and the data is available as soon as possible after the start of conversion. Therefore, the Data Valid option is most useful in systems where the ADC may be operated asynchronously, or where the very first data latch output after power-up must represent a valid conversion. Note that because the delay is fixed at approximately 135ns independent of conversion rate, the Data Valid pulse will overlap into the next conversion at rates above 7.4MHz. This does not preclude proper operation at any rate up to 10MHz.

DATA OUTPUT

Output logic inversion can be accomplished by programming pin 27. Binary Two's Complement or Inverted Binary Two's Complement output data formats are available (Table II).

The ADC603 output logic is TTL compatible. The tri-state output is controlled by $\overline{\text{ENABLE}}$ pin 25. For normal operation, pin 25 will be tied LO. A logic HI on pin 25 will switch the ouput data register to a high-impedance state (Figure 20). Output OFF leakage current I_{OZL} and I_{OZH} will be less than 50µA over the converter's specified operating temperature range. Tri-state output should be isolated from noisy digital bus lines, since the noise can couple back through the OFF data register and create noise in the ADC.

PIN NUMBER	DATA LATCHED BY CONVERT COMMAND		DATA LATCHED BY DATA VALID STROBE
	N–3	N–2	N–1
28	HI	LO	HI
29	HI	HI	LO

TABLE I. Pipeline Delay Selection Logic.

DIGITAL INPUTS

Logic inputs are TTL compatible. Open inputs will assume a HI logic state; unused inputs may be allowed to float or they may be tied to an appropriate TTL logic level.

NOTES:

1. *FAST™ Applications Handbook*, 1987. Fairchild Semiconductor Corp.
2. *Fairchild Advanced CMOS Technology*, Technology Seminar Notes, 1985.
3. "Impedance Matching Tweaks Advance CMOS IC Testing", Gerald C. Cox, *Electronic Design*, April, 1987.
4. "Grounding for Electromagnetic Compatibility", Jerry H. Boogar, *Design News*, 23 February, 1987.

OFFSET AND GAIN ADJUSTMENT

The ADC603 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed to zero with external potentiometers (Figure 23). Trim range is typically 2%; large offsets and gain changes should be made elsewhere in the system. Using an input buffer amplifier allows a convenient point for injecting large offset voltages and making wide gain adjustments.

If offset and gain trim is not used, pins 36 and 37 should be left unconnected.

INPUT VOLTAGE (Exact Center of Code)	DIGITAL DATA OUTPUT LOGIC CODING	
	Binary Two's Complement (BTC) Pin 27 = LO	Inverted Binary Two's Complement (BTC) Pin 27 = HI
	MSB LSB	MSB LSB
+FS (+1.25V)	011111111111*	100000000000*
+FS – 1LSB (+1.2494V)	011111111111	100000000000
+FS – 2LSB (+1.2488V)	011111111110	100000000001
+3/4FS (+0.9375V)	011000000000	100111111111
+1/2FS (+0.625V)	010000000000	101111111111
+1/4FS (+0.3125V)	001000000000	110111111111
+1LSB (+610µV)	000000000001	111111111110
Bipolar Zero (0V)	000000000000	111111111111
–1LSB (–610µV)	111111111111	000000000000
–1/4FS (–0.3125V)	111000000000	000111111111
–1/2FS (+0.625V)	110000000000	001111111111
–3/4FS (–0.9375V)	101000000000	010111111111
–(FS – 1LSB) (–1.2494V)	100000000001	011111111110
–FS (–1.25V)	100000000000	011111111111

* Indicates overrange condition.

TABLE II. Digital Data Output Logic Coding.

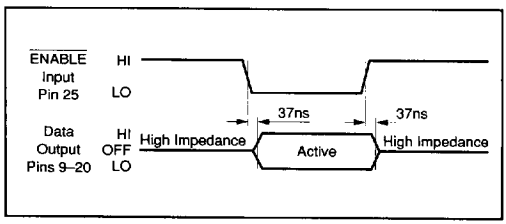


FIGURE 22. Digital Data Tri-State Output.

THERMAL REQUIREMENTS

The ADC603 is tested and specified over a temperature range of 0°C to +70°C (J, K grade) and –55°C to +100°C (S grade). The converters are tested in a forced-air environment with a 10 SCFM air flow. With a small heat sink (Figure 24) the ADC603 can be operated in a normal convection ambient-air environment if submodule case temperature does not exceed the upper limit of its specification.(1)

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient temperatures. Thermal resistance of the ADC603 package is: θ_{JC} = 4.8°C/W, measured to the underside of the case.

NOTES:

1. "Maximizing Heat Transfer from PCBs", *Machine Design*, March 26, 1987, Jeilong Chung.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device —it cannot be improved by testing. However, environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels.

Burr-Brown offers environmentally screened versions of our standard military temperature range products, designed to provide enhanced reliability at moderate cost. The screening illustrated in Table III is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

SCREEN	MIL-STD-883 METHOD, CONDITION	SCREENING LEVEL
Internal Visual	2017	Visual requirements only (par 3.1 through 3.1.8)
Electrical Test	Burr-Brown Test Procedure	
High Temperature Storage (Stabilization Bake)	1008	24hr, +100°C
Temperature Cycling	1010	10 cycles, –55°C to –125°C
Constant Acceleration	2001, A	2000G; Y Axis Only
Burn-In	1015, D	160hr, +125°C T_J, No PDA
Hermeticity, Gross Leak	1014, C	Bubble Test Only, Preconditioning Omitted
Final Electrical	Burr-Brown Test Procedure	
External Visual	2009	

TABLE III. Optional Screening Flow for ADC603SHQ.

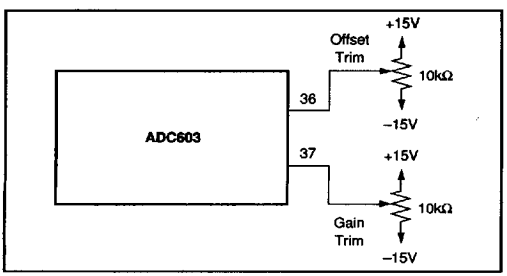


FIGURE 19. Optional Gain and Offset Trim.

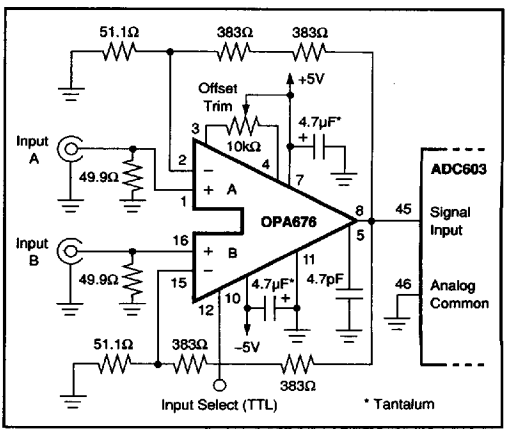


FIGURE 21. A Multiplexed-Input Buffer Amplifier (Gain = +16V/V).

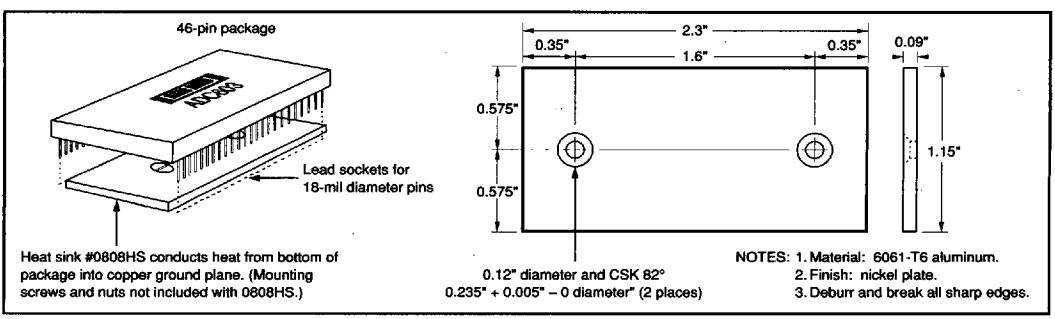


FIGURE 20. Heat Sink Transfers Heat from the DIP Package into a Copper Ground Plane.